Joint ICTP-IAEA School on Zynq-7000 SoC and its Applications for Nuclear and Related Instrumentation

Zynq Architecture
7-Series FPGA Architecture

Cristian Sisterna
Universidad Nacional de San Juan
Argentina

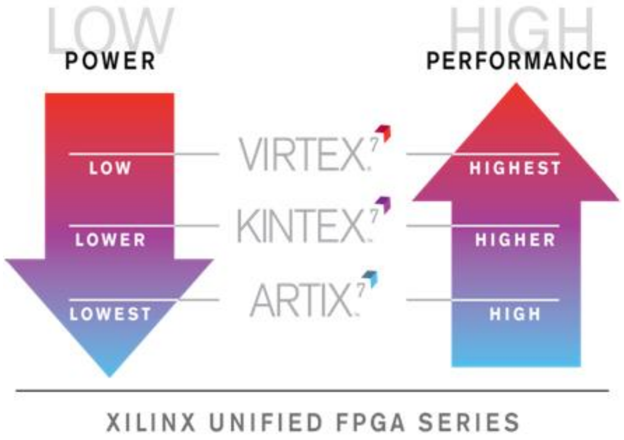
7-Series FPGA Architecture

7-Series FPGA Families

Maximum Capability	ARTIX 7	KINTEX 7	VIRTEX 7	ZYNQ
	Lowest Power and Cost	Industry's Best Price/Performance	Industry's Highest System Performance	Extensible Processing Platform
Logic Cells	20K – 355K	70K – 480K	285K – 2,000K	30K – 350K
Block RAM	12 Mb	34 Mb	65 Mb	240KB – 2180KB
DSP Slices	40 – 700	240 – 1,920	700 – 3,960	80 – 900
Peak DSP Perf.	504 GMACS	2,450 GMACs	5,053 GMACS	1080 GMACS
Transceivers	4	32	88	16
Transceiver Performance	3.75Gbps	6.6Gbps and 12.5Gbps	12.5Gbps, 13.1Gbps and 28Gbps	6.6Gbps and 12.5Gbps
Memory Performance	1066Mbps	1866Mbps	1866Mbps	1333Mbps
I/O Pins	450	500	1,200	372
I/O Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below

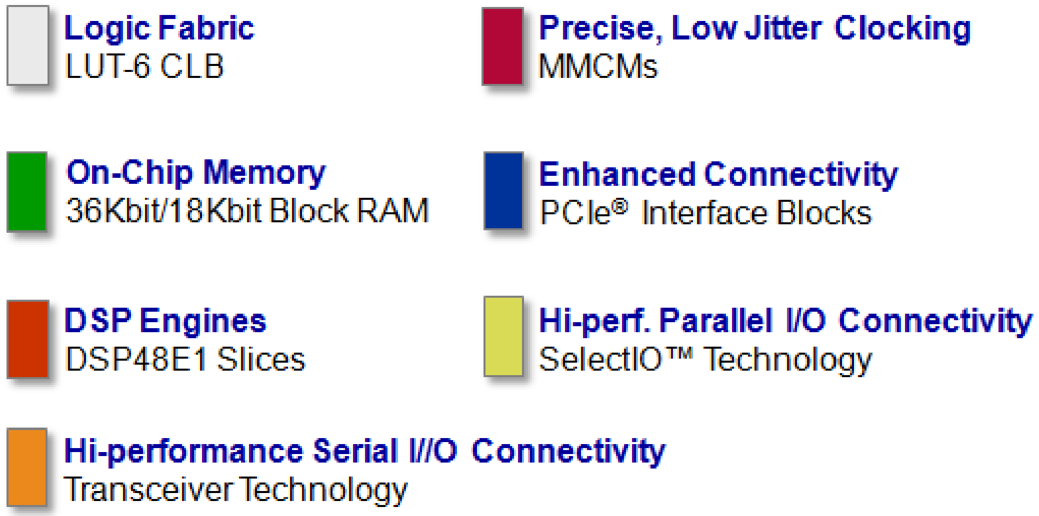
7-Series Cost, Power and Performance

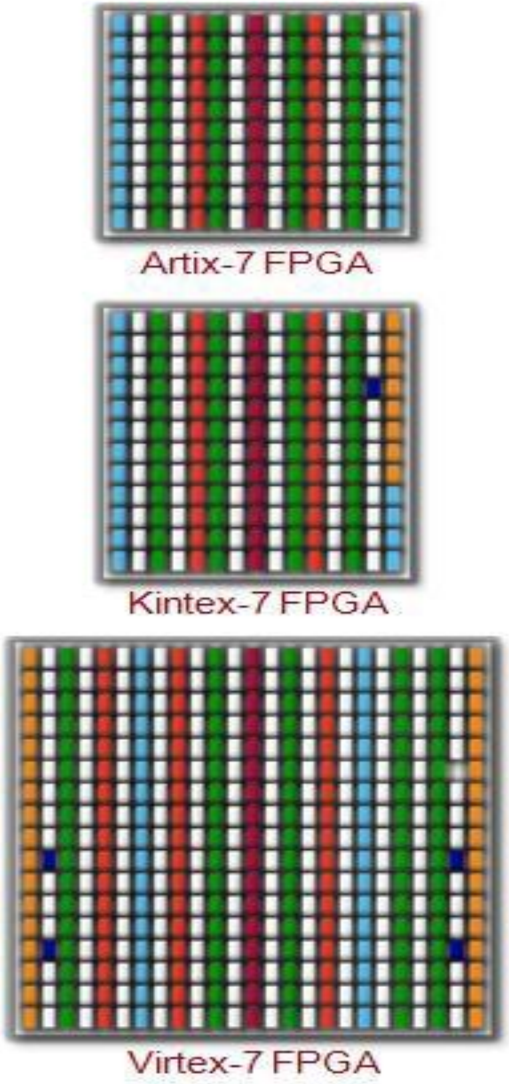
- The different families in the 7-series provide solutions to address the different price/performance/power requirements of the FPGA market
  - **Artix™-7** family: Lowest price and power for high volume and consumer applications
    - Battery powered devices, automotive, commercial digital cameras
  - **Kintex™-7** family: Best price/performance
    - Wireless and wired communication, medical, broadcast
  - **Virtex-7** family: Highest performance and capacity
    - High-end wired communication, test and measurement, advanced RADAR, high-performance computing



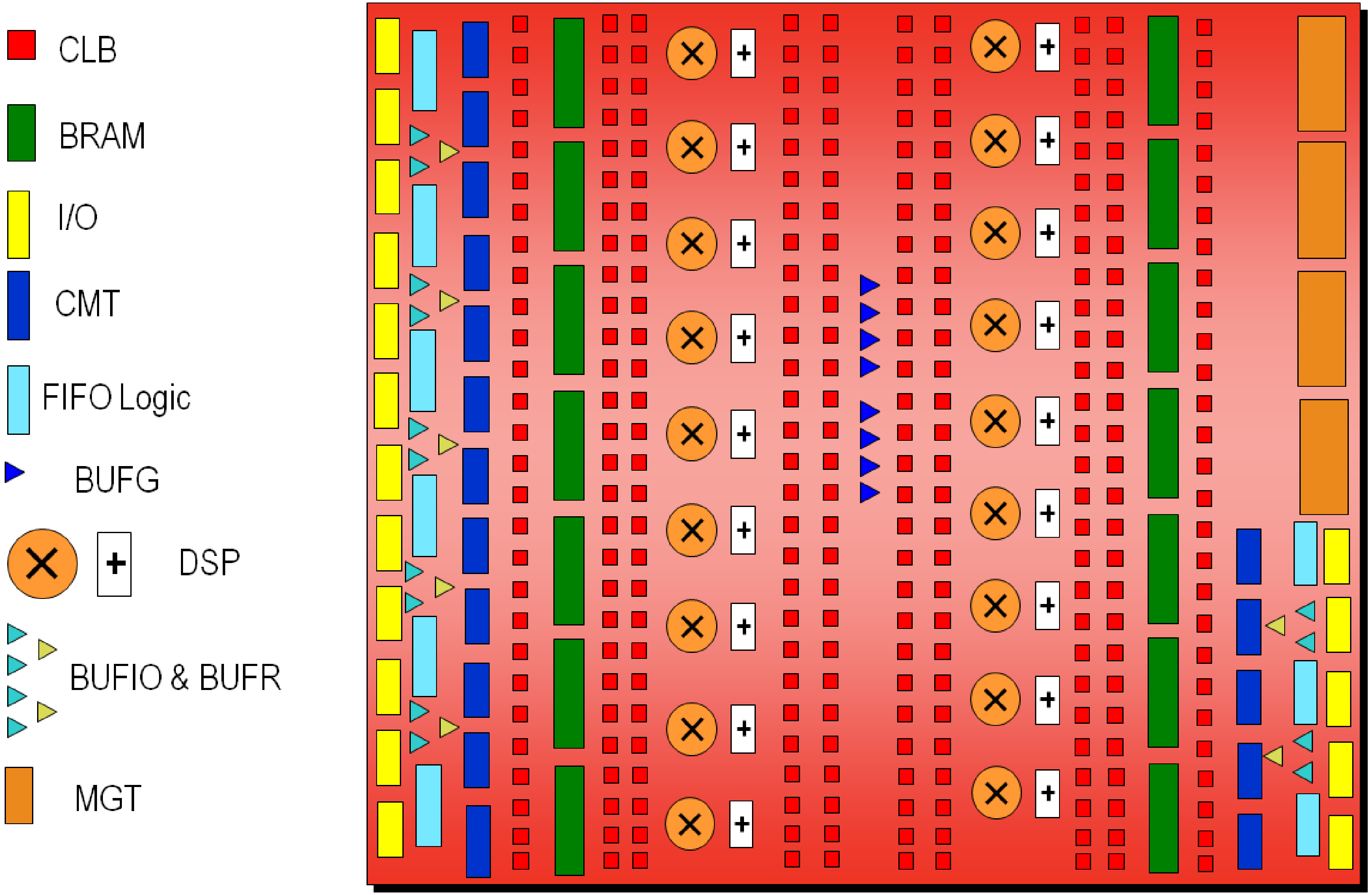
7-Series Architecture – Common Elements

- Common elements enable easy IP reuse for quick design portability across all 7-series families
  - Design scalability from low-cost to high-performance
  - Expanded eco-system support
  - Quickest time to market



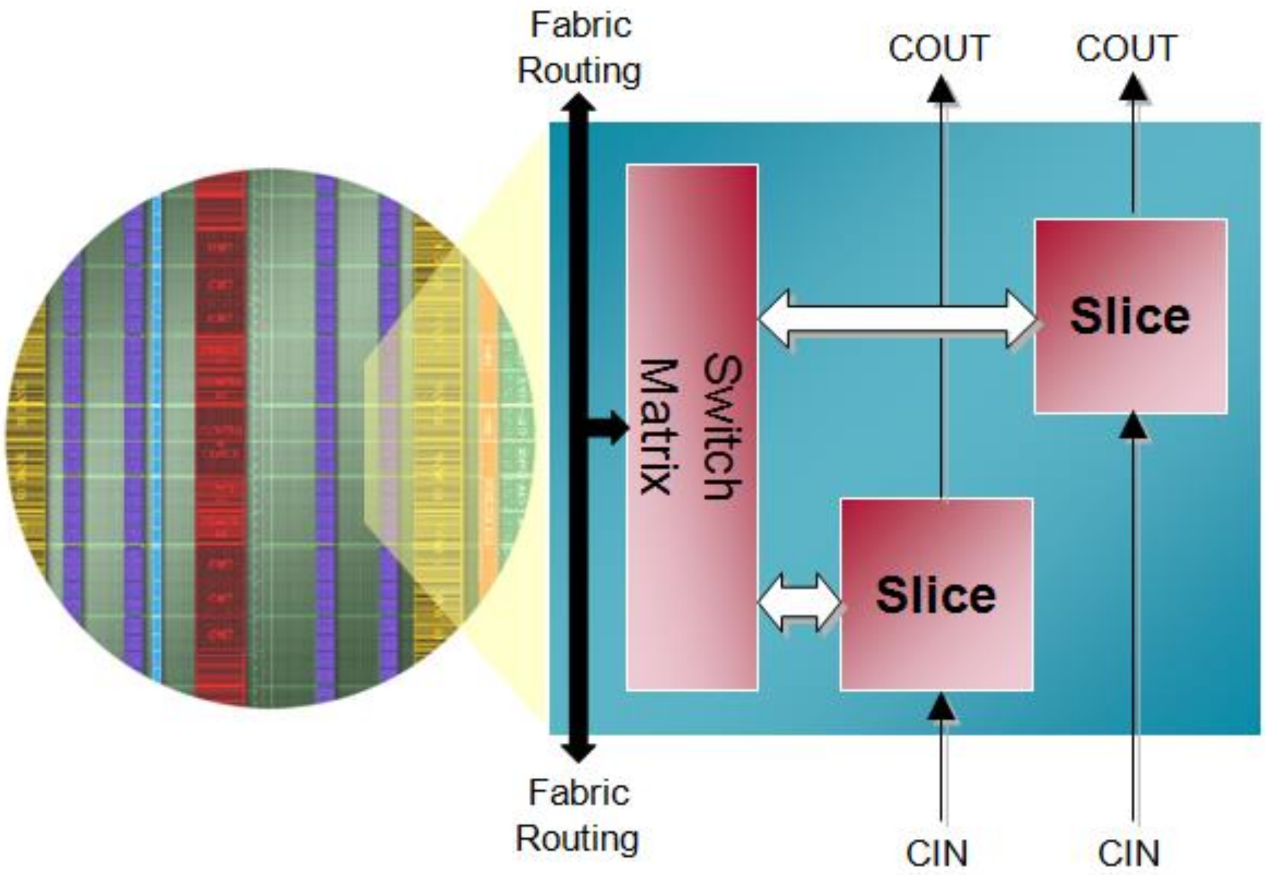


Example of 7-Series Architecture: Artix-7



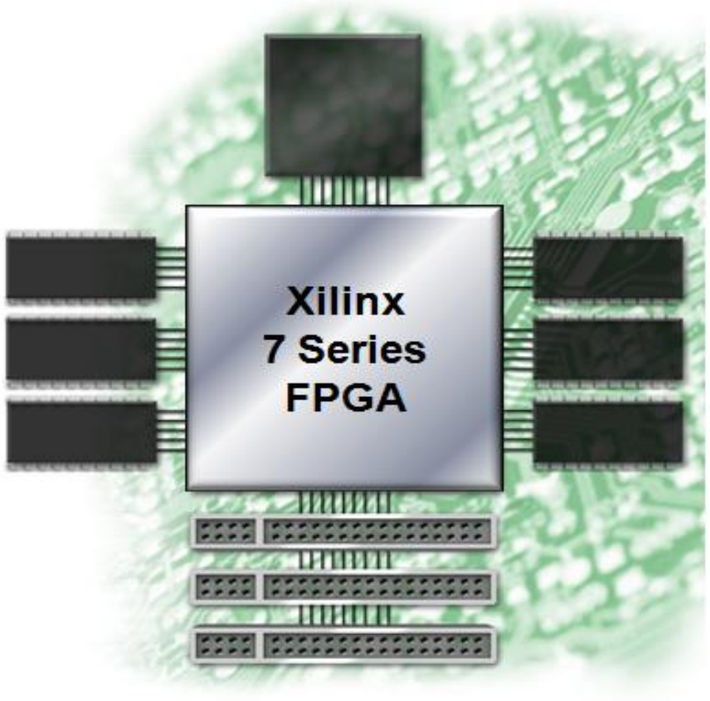
Logic Resources

- Primary resource for design
  - Combinatorial functions
  - Flip-flops
- CLB contains two slices
- Connected to switch matrix for routing to other FPGA resources
  - Carry chain runs vertically in a column from one slice to the one above



7-Series FPGA Inputs/Outputs

- Wide range of voltages
  - 1.2V to 3.3V operation
- Many different I/O standards
  - Single ended and differential
  - Referenced inputs
  - 3-state support
- Very high performance
  - Up to 1600 Mbps LVDS
  - Up to 1866 Mbps single-ended for DDR3
- Easy interfacing to standard memories
  - Hardware support for QDRII+ and DDR3
- Digitally controlled impedance
- Low power



Input/Output Types

- Two different types of I/O in 7-series FPGAs
  - **High Range (HR)**
    - Supports I/O standards with Vcco voltages up to 3.3V
  - **High Performance (HP)**
    - Supports I/O standards with Vcco voltages up to 1.8V ***only***
    - Designed for the highest performance
    - Has ODELAY and DCI capability

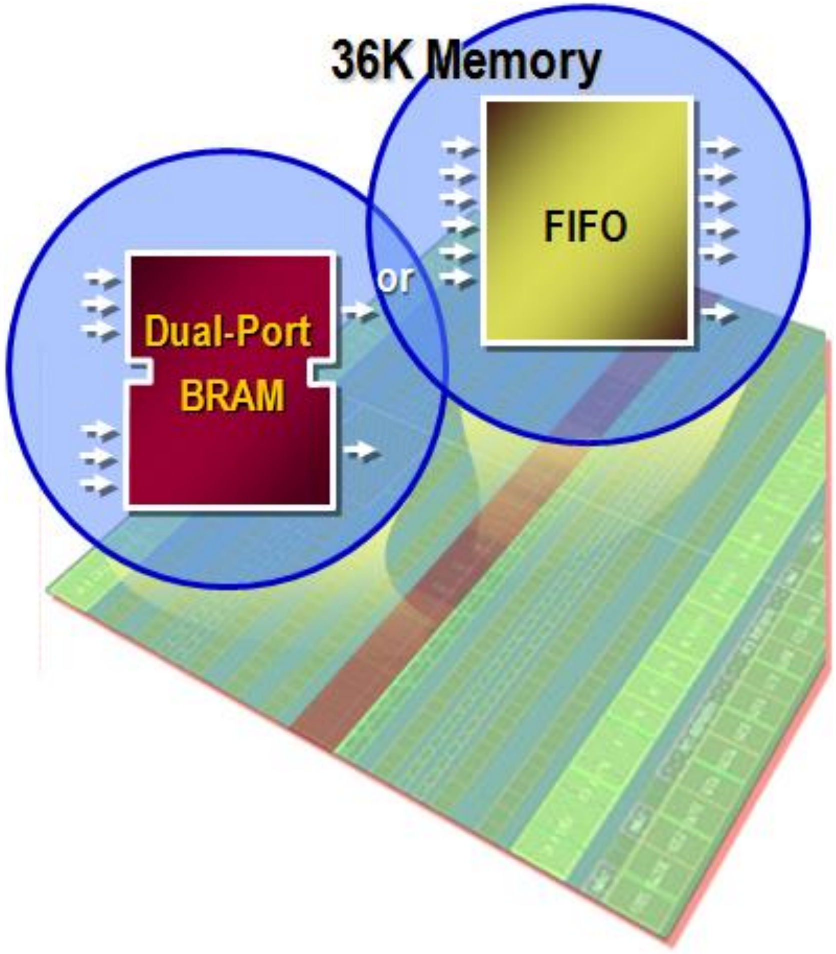
I/O Type	Artix-7 Family	Kintex-7 Family	Virtex-7 Family	Virtex-7 XT/HT/ Family
High Range	All	Most Some		
High Performance		Some	Most	All

Most Common I/O Supported

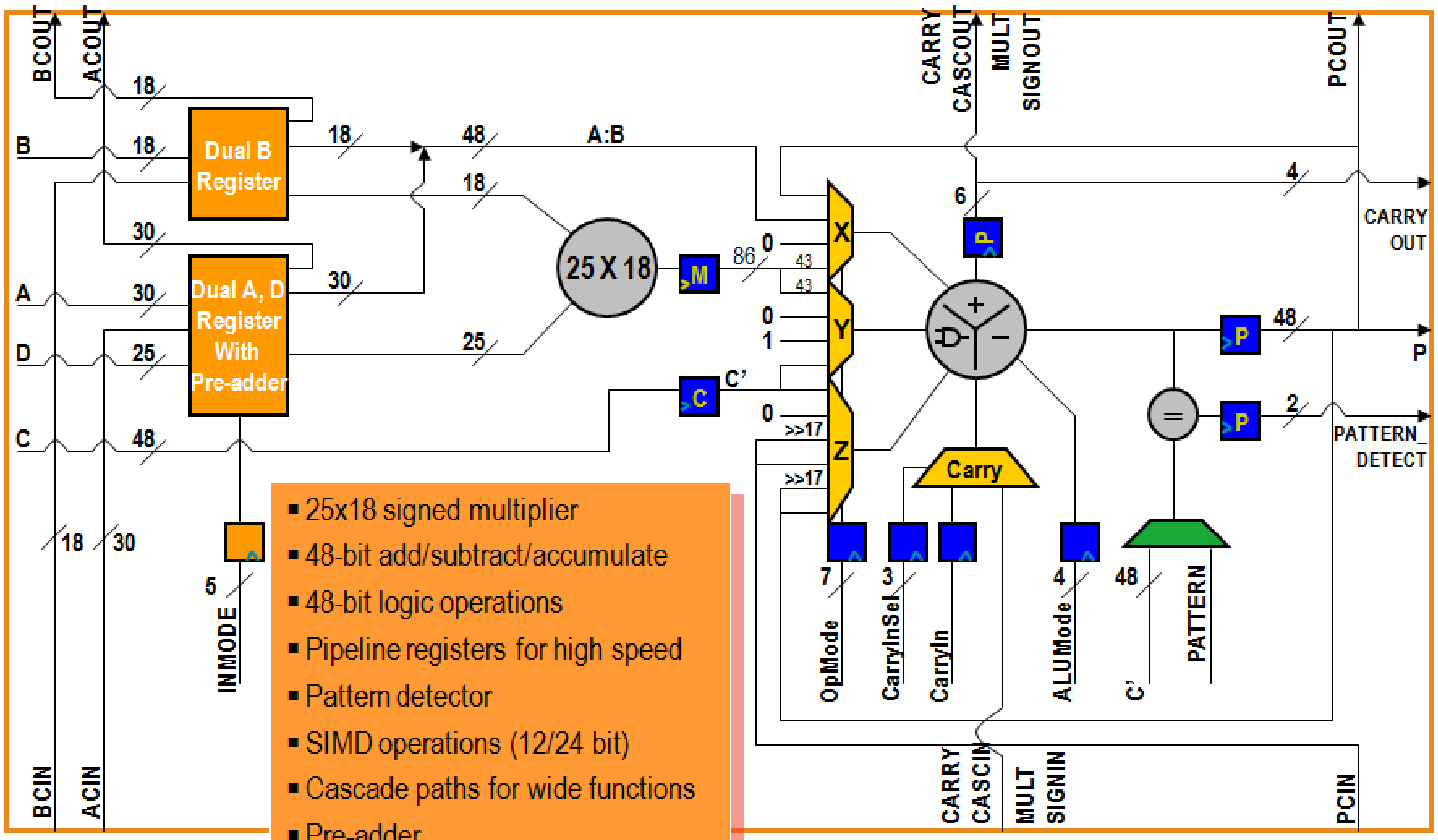
Feature	HP I/O Bank	HR I/O Bank
3.3 V I/O Standard	N/A	Supported
2.5 V I/O Standard	N/A	Supported
1.8 V I/O Standard	Supported	Supported
1.5 V I/O Standard	Supported	Supported
1.35 V I/O Standard	Supported	Supported
1.2 V I/O Standard	Supported	Supported
LVDS	Supported	Supported
Digital Controlled Impedance	Supported	N/A
Internal Vref	Supported	Supported
Internal Diff. Termination	Supported	Supported
IDELAY	Supported	Supported
ODELAY	Supported	N/A
ISERDES	Supported	Supported
OSERDES	Supported	Supported

7-Series Block RAM and FIFO

- All members of the 7-series families have the same Block RAM/FIFO
- Fully synchronous operation
  - All operations are synchronous; all outputs are latched
- Optional internal pipeline register for higher frequency operation
- Two independent ports access common data
  - Individual address, clock, write enable, clock enable
  - Independent data widths for each port
- Multiple configuration options
  - True dual-port, simple dual-port, single-port
- Integrated control for fast and efficient FIFOs



7- Series DSP48E1 Slice



- 25x18 signed multiplier
- 48-bit add/subtract/accumulate
- 48-bit logic operations
- Pipeline registers for high speed
- Pattern detector
- SIMD operations (12/24 bit)
- Cascade paths for wide functions
- Pre-adder

XADC and Analog Mixed Signals (AMS)

- XADC is a high quality and flexible analog interface new to the 7-series
  - Dual 12-bit 1Msps ADCs, on-chip sensors, 17 flexible analog inputs, and track & holds with programmable signal conditioning
  - 1V input range (unipolar, bipolar and differential)
  - 12-bit resolution conversion
  - Built in digital gain and offset calibration
  - On-chip thermal and Voltage sensors
  - Sample rate of 1 MSPS
- Analog Mixed Signal (AMS)
  - Using the FPGA programmable logic to customize the XADC and replace other external analog functions; for example, linearization, calibration, filtering, and DC balancing to improve data conversion resolution

Zynq Architecture

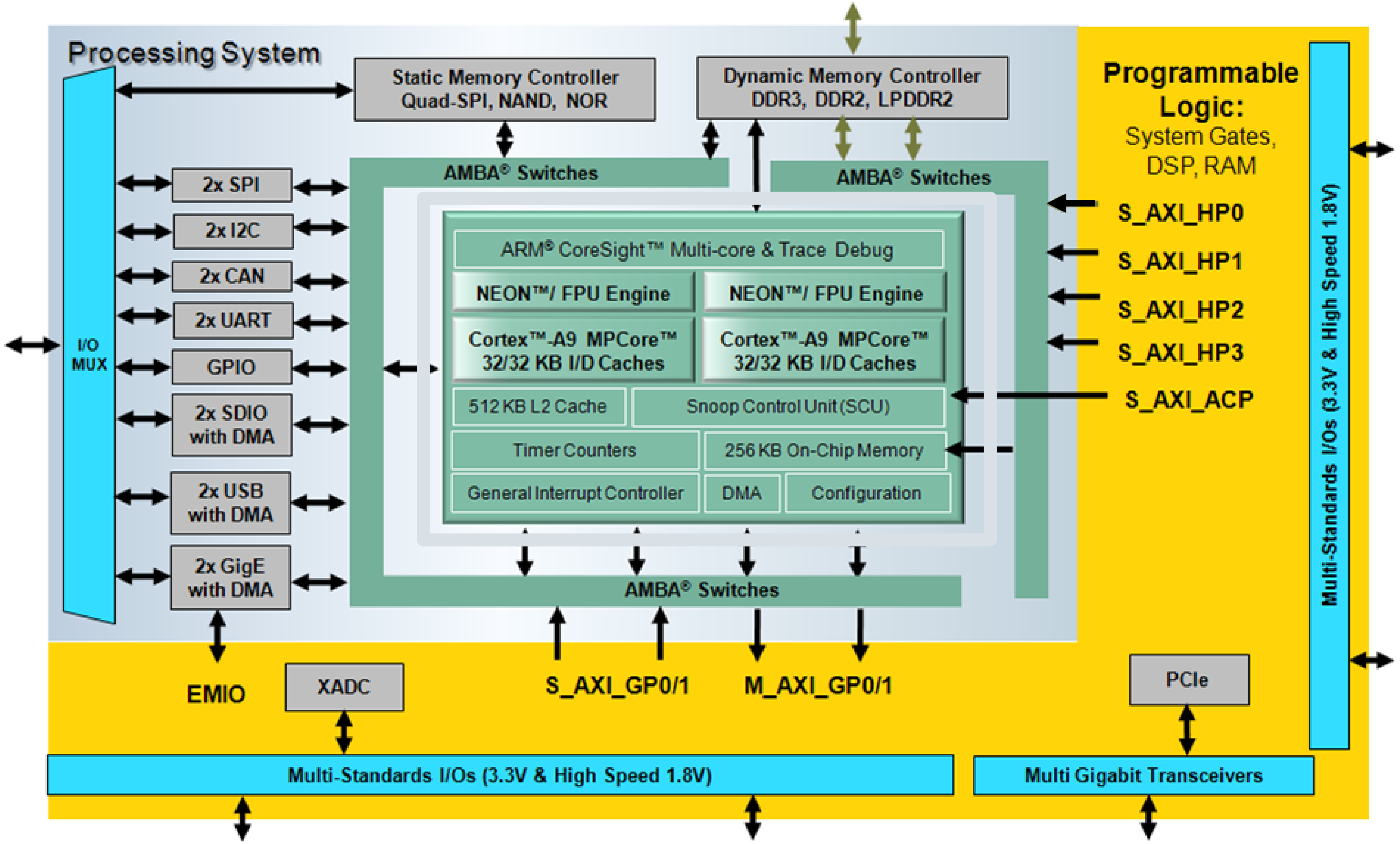
Zynq-7000 Main Features

- **Complete ARM®-based processing system**
  - Application Processor Unit (APU)
    - Dual ARM Cortex™-A9 processors
    - Caches and support blocks
  - Fully integrated memory controllers
  - I/O peripherals
- **Tightly integrated programmable logic**
  - Used to extend the processing system
  - Scalable density and performance
- **Flexible array of I/O**
  - Wide range of external multi-standard I/O
  - High-performance integrated serial transceivers
  - Analog-to-digital converter inputs

ARM Processor Architecture

- **ARM Cortex-A9 processor implements the ARMv7-A architecture**
  - ARMv7 is the ARM Instruction Set Architecture (ISA)
    - Thumb instructions: 16 bits; Thumb-2 instructions: 32 bits
    - NEON: ARM's Single Instruction Multiple Data (SIMD) instructions
  - ARMv7-A: Application set that includes support for a Memory Management Unit (MMU)
  - ARMv7-R: Real-time set that includes support for a Memory Protection Unit (MPU)
  - ARMv7-M: Microcontroller set that is the smallest set
- **ARM Advanced Microcontroller Bus Architecture (AMBA®) protocol**
  - AXI3: Third-generation ARM interface
  - AXI4: Adding to the existing AXI definition (extended bursts, subsets)
- **Cortex is the new family of processors**
  - ARM family is older generation; Cortex is current; MMUs in Cortex processors and MPUs in ARM

Zynq SoC Block Diagram



PS Main Components

- **Application processing unit (APU)**
- **I/O peripherals (IOP)**
  - Multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
- **Memory interfaces**
- **PS interconnect**
- **DMA**
- **Timers**
  - Public and private
- **General interrupt controller (GIC)**
- **On-chip memory (OCM): RAM**
- **Debug controller: CoreSight**

PL Main Components

- Configurable logic blocks (CLB)
  - 6-input look-up tables (LUTs)
  - Memory capability within the LUT
  - Register and shift register functionality
- 36 Kb BRAM
- DSP48E1 Slice
- Clock management
- Configurable I/Os
- High Speed Serial Transceivers
- Integrated interface for PCI Express

Zynq	FPGA Based Fabric
7z010, 7z015, 7z020	Artix
7z030, 7z035, 7z045, 7z100	Kintex

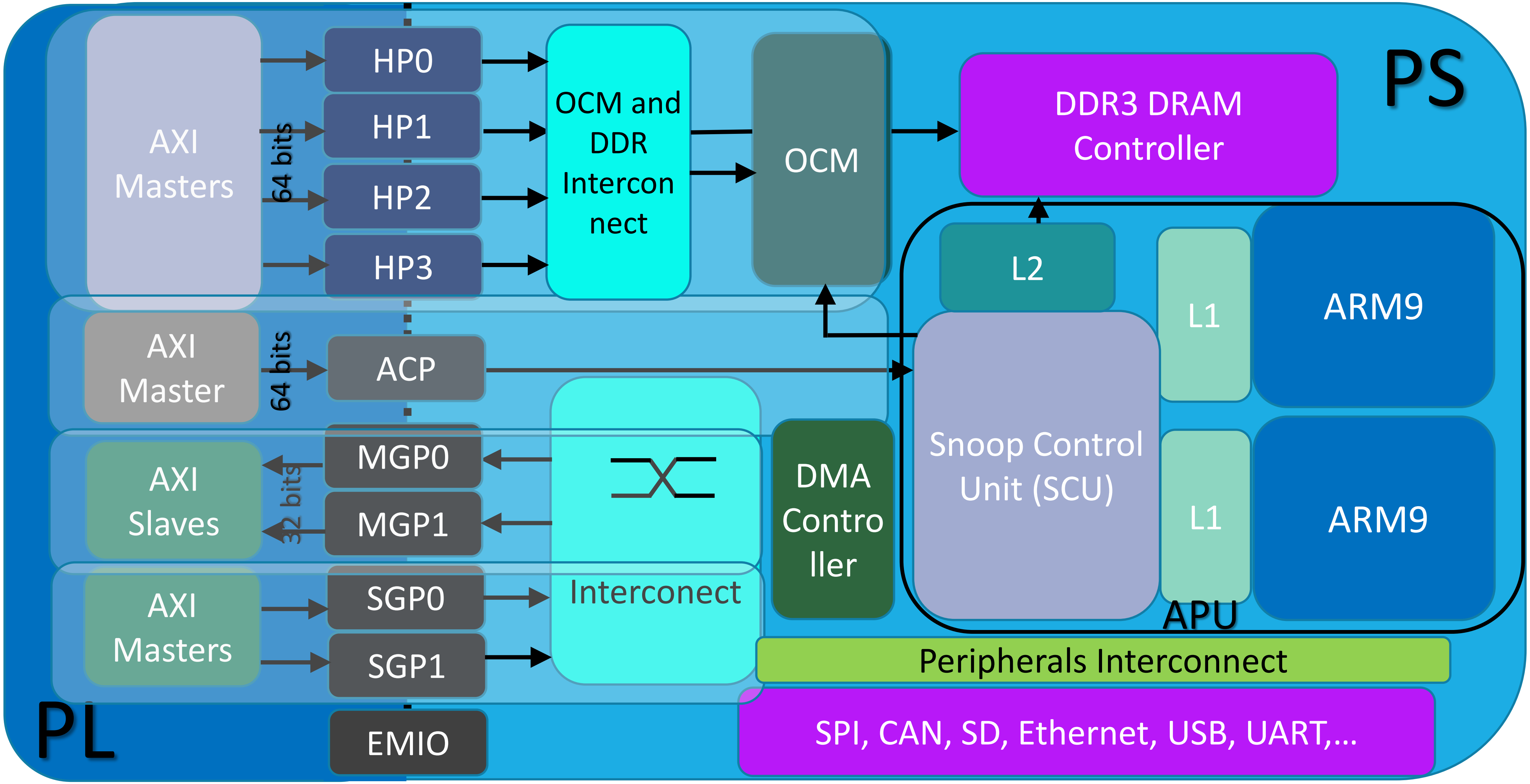
PS-PL Interface

- **AXI high-performance slave ports (HP0-HP3)**
  - Configurable 32-bit or 64-bit data width
  - Access to OCM and DDR only
  - Conversion to processing system clock domain
  - AXI FIFO Interface (AFI) are FIFOs (1KB) to smooth large data transfers
- **AXI general-purpose ports (GP0-GP1)**
  - Two masters from PS to PL
  - Two slaves from PL to PS
  - 32-bit data width
  - Conversation and sync to processing system clock domain

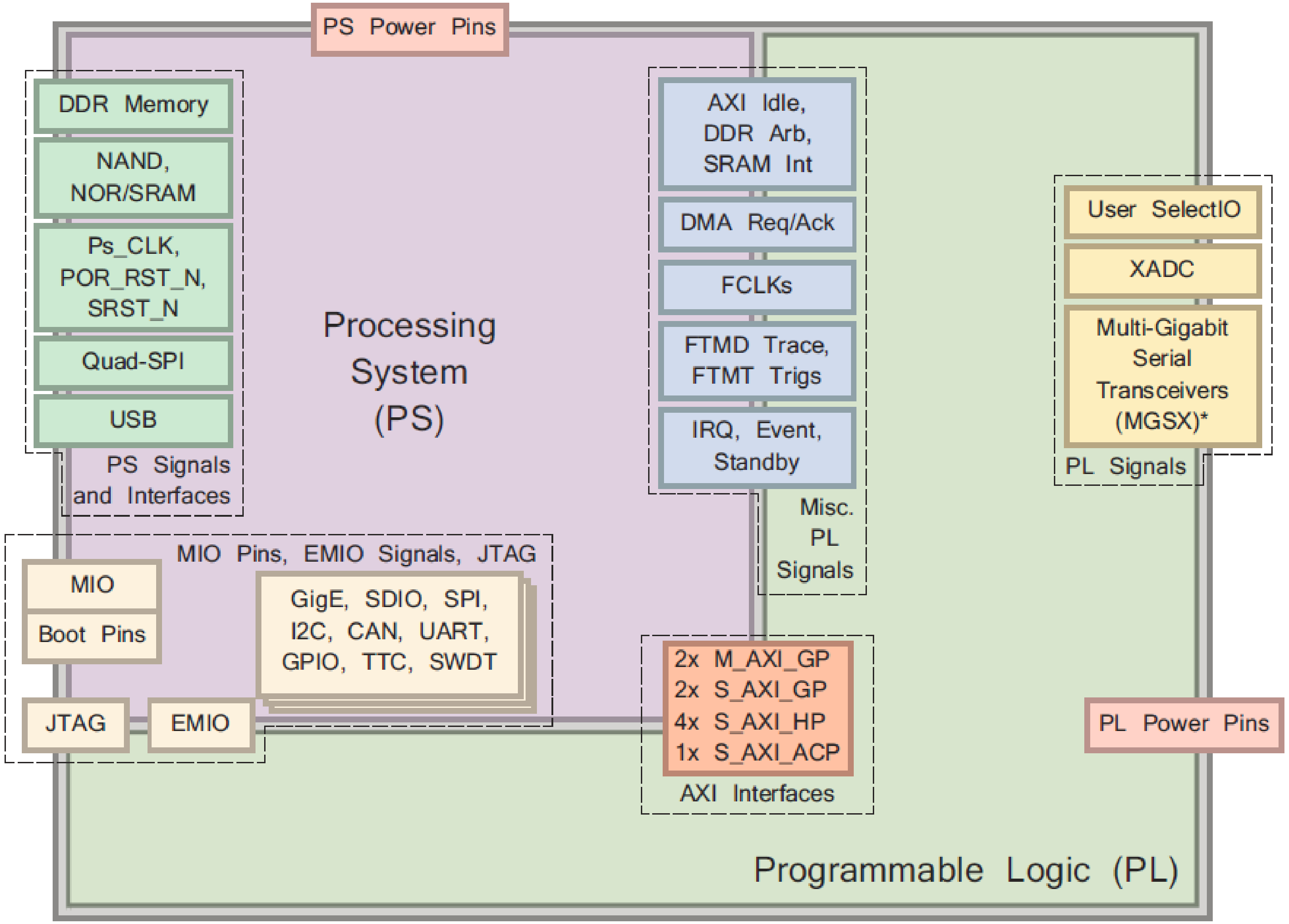
PS-PL Interface

- **One 64-bit accelerator coherence port (ACP) AXI slave interface to CPU memory**
- **DMA, interrupts, events signals**
  - Processor event bus for signaling event information to the CPU
  - PL peripheral IP interrupts to the PS general interrupt controller (GIC)
  - Four DMA channel RDY/ACK signals
- **Extended multiplexed I/O (EMIO) allows PS peripheral ports access to PL logic and device I/O pins**
- **Clock and resets**
  - Four PS clock outputs to the PL with enable control
  - Four PS reset outputs to the PL
- **Configuration and miscellaneous**

Zynq Architecture



PS-PL Interface



*Zynq 7z030, 7x045 & 7z100 only

PS-PL AXI Interfaces

Interface Name	Interface Description	Master	Slave
M_AXI_GP0	General Purpose (AXI_GP)	PS	PL
M_AXI_GP1		PS	PL
S_AXI_GPO	General Purpose (AXI_GP)	PL	PS
S_AXI_GP1		PL	PS
S_AXI_ACP	Accelerator Coherence Port	PL	PS
S_AXI_HP0	High Performance Ports (AXI_HP)with read/write FIFOs and two dedicated memory ports on DDR controller and a path to the OCM	PL	PS
S_AXI_HP1		PL	PS
S_AXI_HP2		PL	PS
S_AXI_HP3		PL	PS

PS-PL Interface Performance

Method	Benefits	Drawbacks	Usage	Performance
PL AXI-HP DMA	• Highest throughput • Multiple interfaces • Command/Data FIFO	• OC/DDR access only • Complex PL Master design	• HP DMA for large datasets	1.200 MB/s (per interface)
PL AXI-ACP DMA	• - Highest throughput - Lowest latency - Optional cache coherency	• Large burst might cause cache trashing • Shares CPU interconnect bandwidth • Complex PL Master design	• HP DMA for smaller coherent datasets • Medium granularity CPU offload	1.200 MB/s
PL AXI-GP DMA	• Medium throughput	• More complex PL Master design	• PL to PS control functions • PS I/O Peripheral access	600 MB/s
CPU Programmed I/O	• Simple Sw • Least PL resources • Simple PL Slave	• Lowest throughput	• Control functions	< 25 MB/s

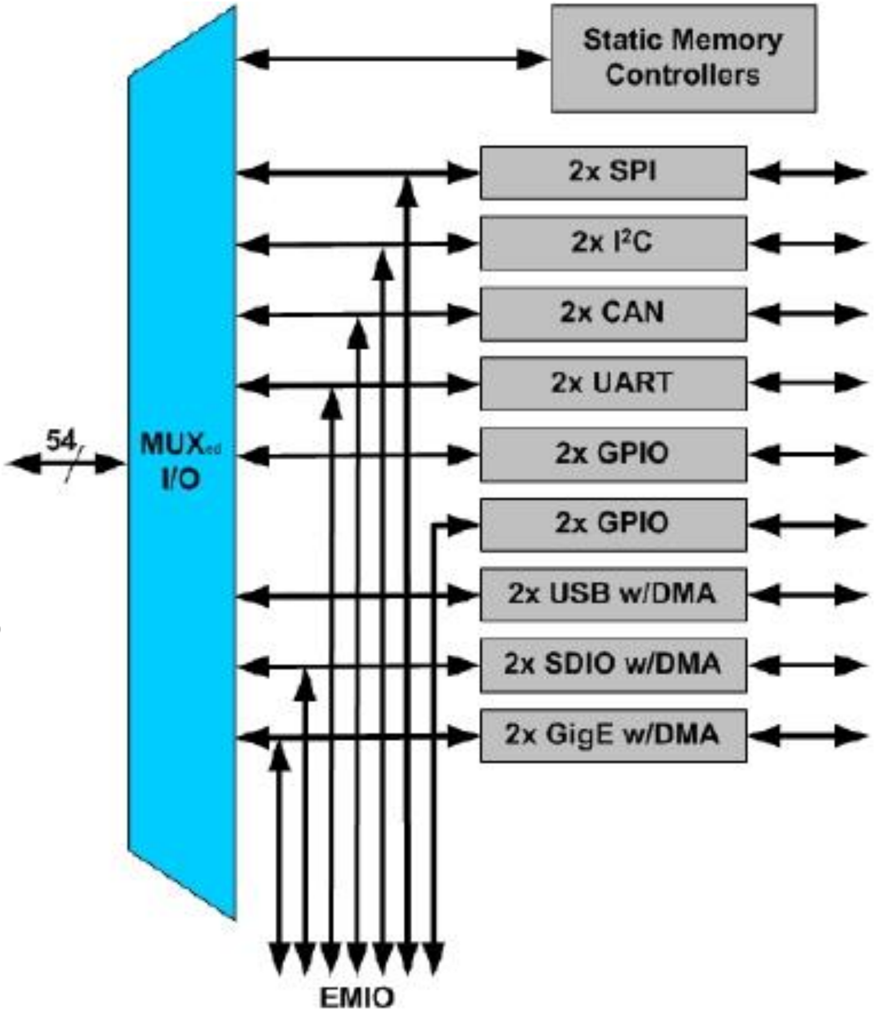
PS-PL Miscellaneous Signals

- PL Clocks and Resets
- PL Interrupts to PS
- IOP Interrupts to PL
- Events
- Idle AXI, DDR, ARB, SRAM Interrupt
- DMA Controller
- EMIO Signals

PS Peripherals and Connections

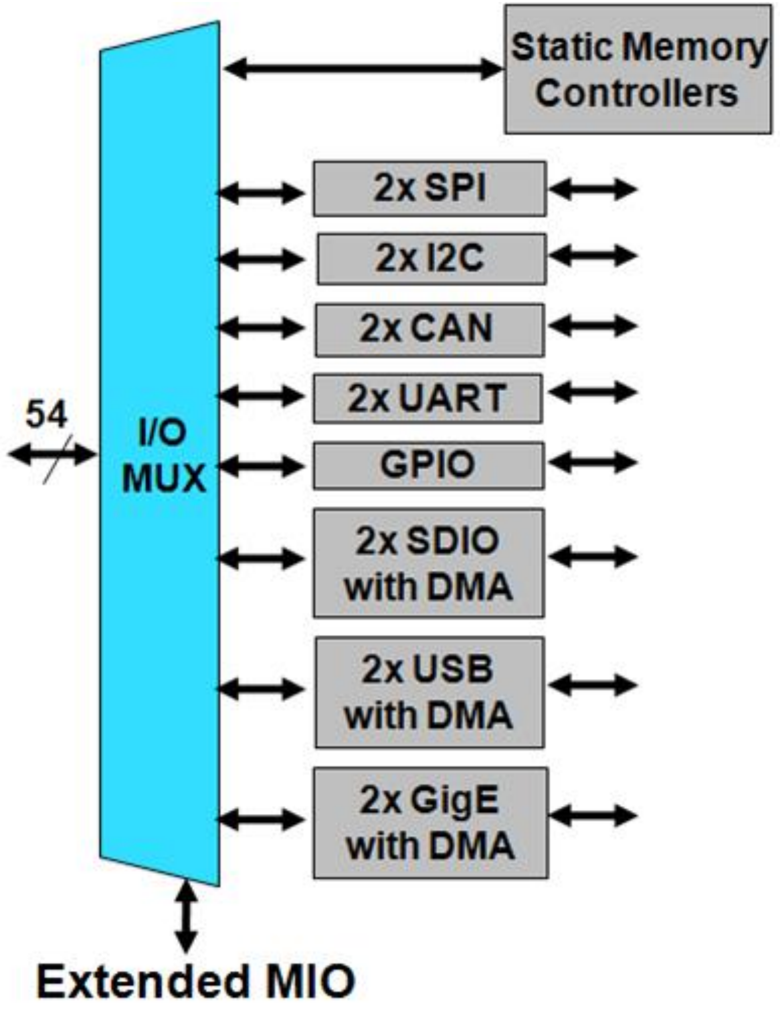
Zynq Architecture – Build-In Devices

- Two USB 2.0 OTG/device/host
- Two tri-mode gigabit Ethernet (10/100/1000)
- Two SD/SDIO interfaces
  - Memory, I/O, and combo cards
- Two CAN 2.0Bs, SPIs, I2Cs, UARTs
- Four GPIO 32-bit blocks
  - 54 available through MIO; other 64 available through EMIO

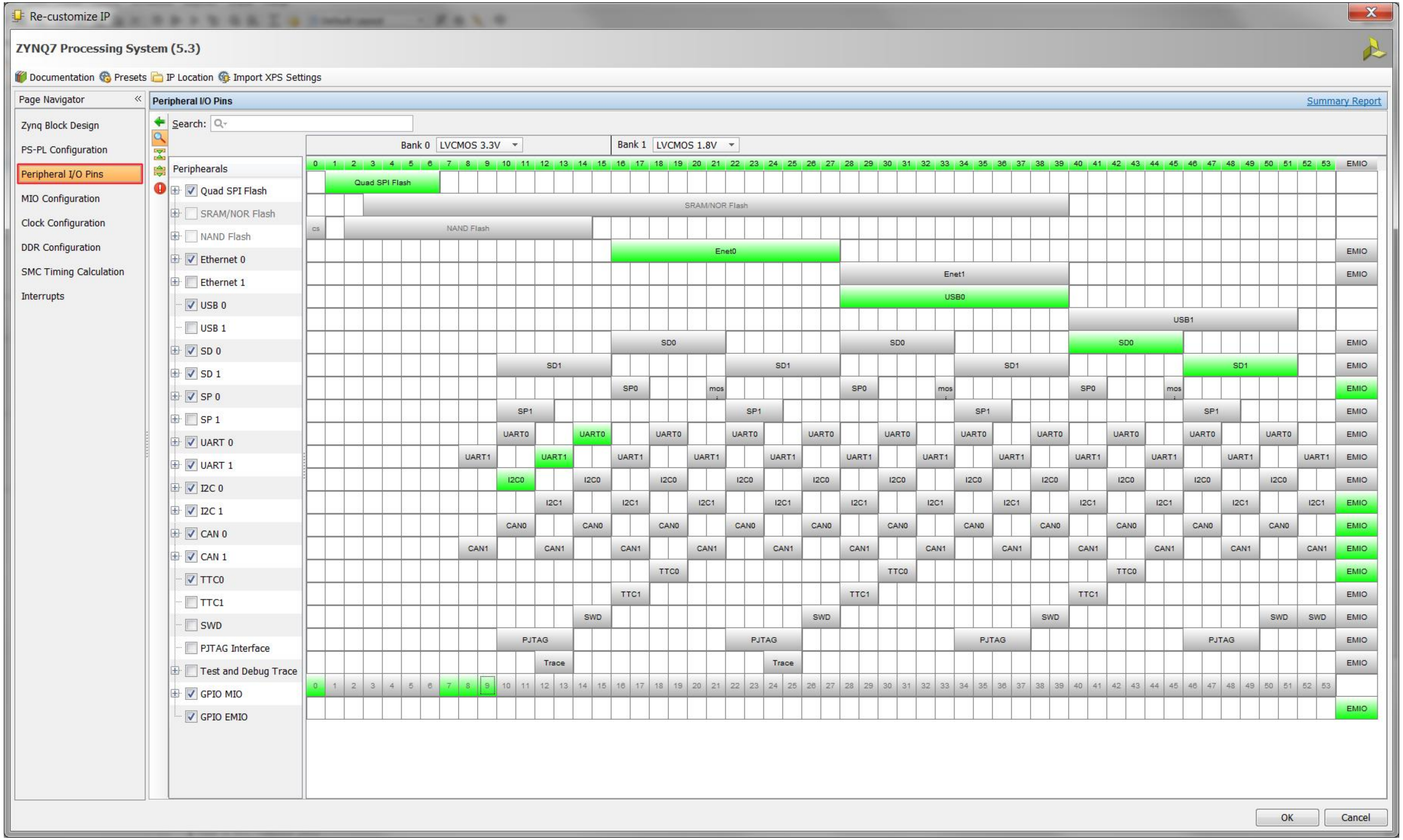


Multiplexed I/O – Internal / External

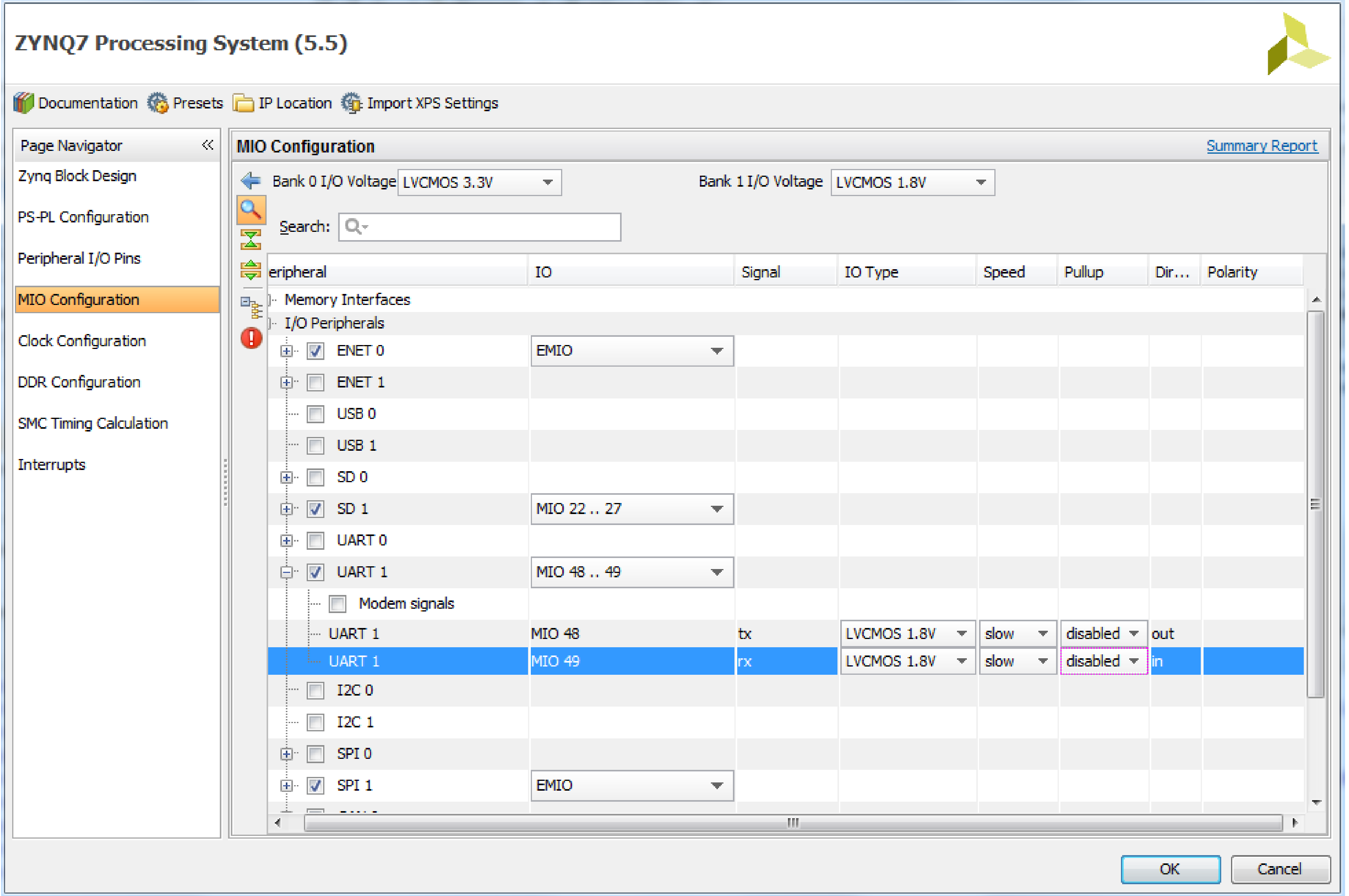
- **Multiplexed input/output (MIO)**
  - Multiplexed output of peripheral and static memories
  - Two I/O banks; each selectable: 1.8V, 2.5V, or 3.3V
  - Configured using configuration
  - Dedicated pins are used
    - User constraints (LOC) should not be present
      - The BitGen process will throw errors if LOC constraints are present
- **Extended MIO**
  - Enables use of the SelectIO™ interface with PS peripherals
  - User constraints must be present for the signals brought out to the SelectIO pins
    - The BitGen process will throw errors if LOC constraints are not present



Multiplexed I/O - EMIO



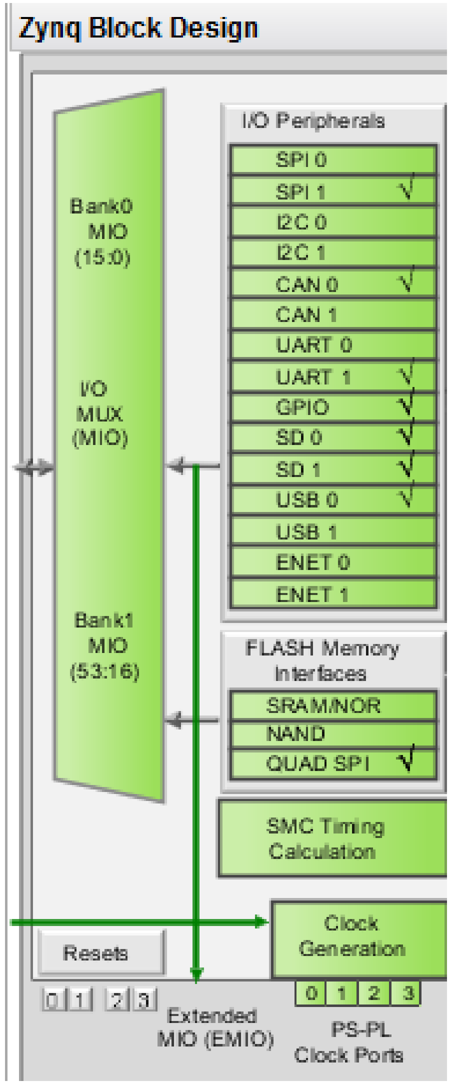
MIO Port Configuration



Extended Multiplexed I/O (EMIO)

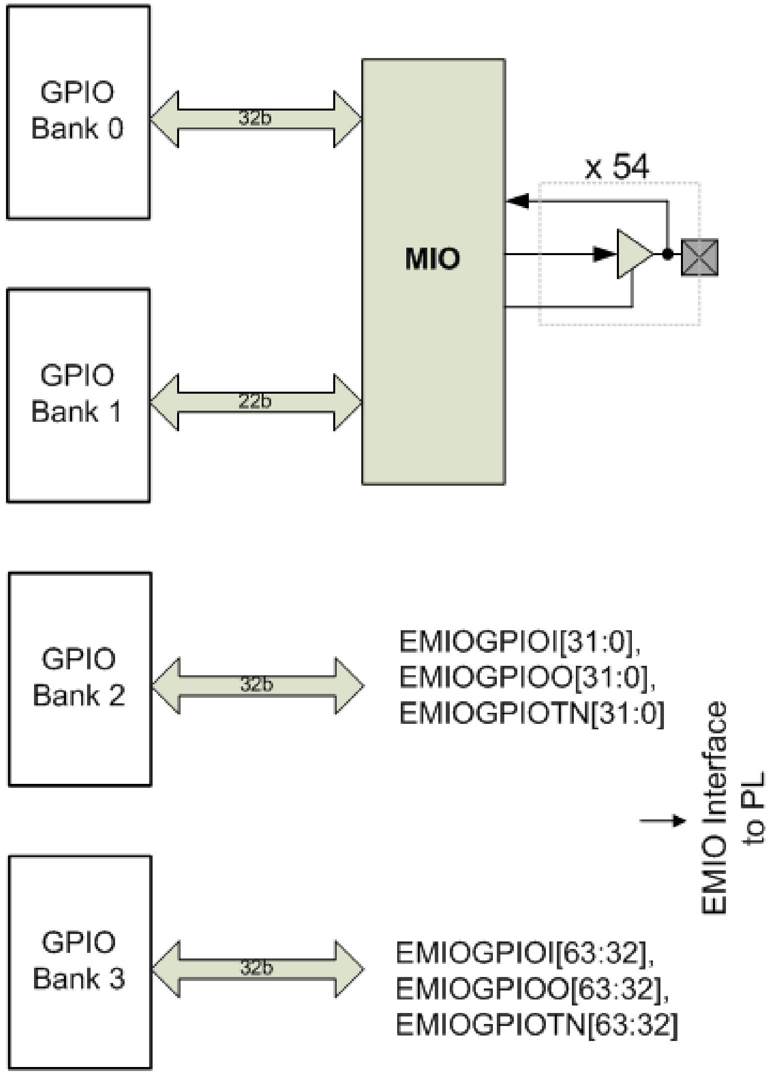
Extended interface to PS I/O peripheral ports

- EMIO: Peripheral port to PL
- Alternative to using MIO
- Mandatory for some peripheral ports
- Facilitates
  - Connection to peripheral in programmable logic
  - Use of general I/O pins to supplement MIO pin usage
  - Allows additional signals for many of the peripherals
  - Alleviates competition for MIO pin usage



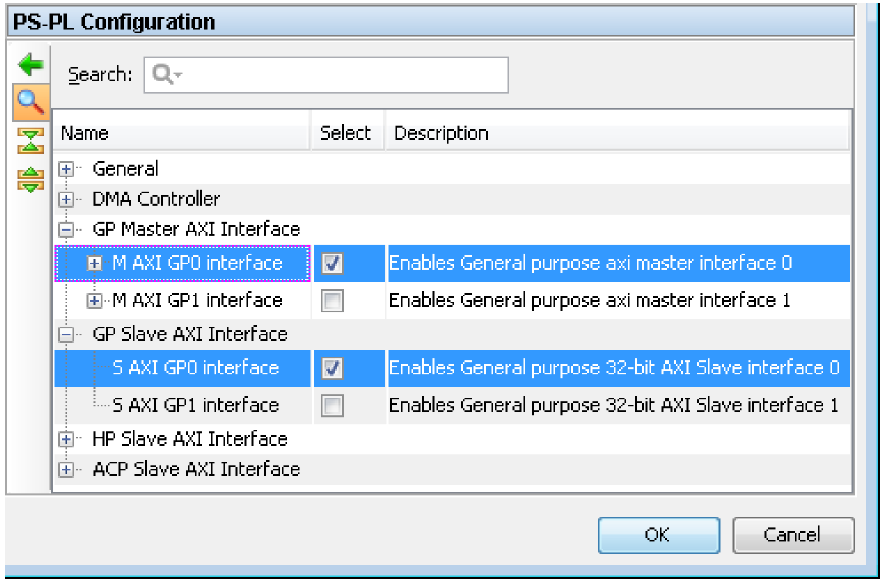
General Purpose I/O Blocks in PS

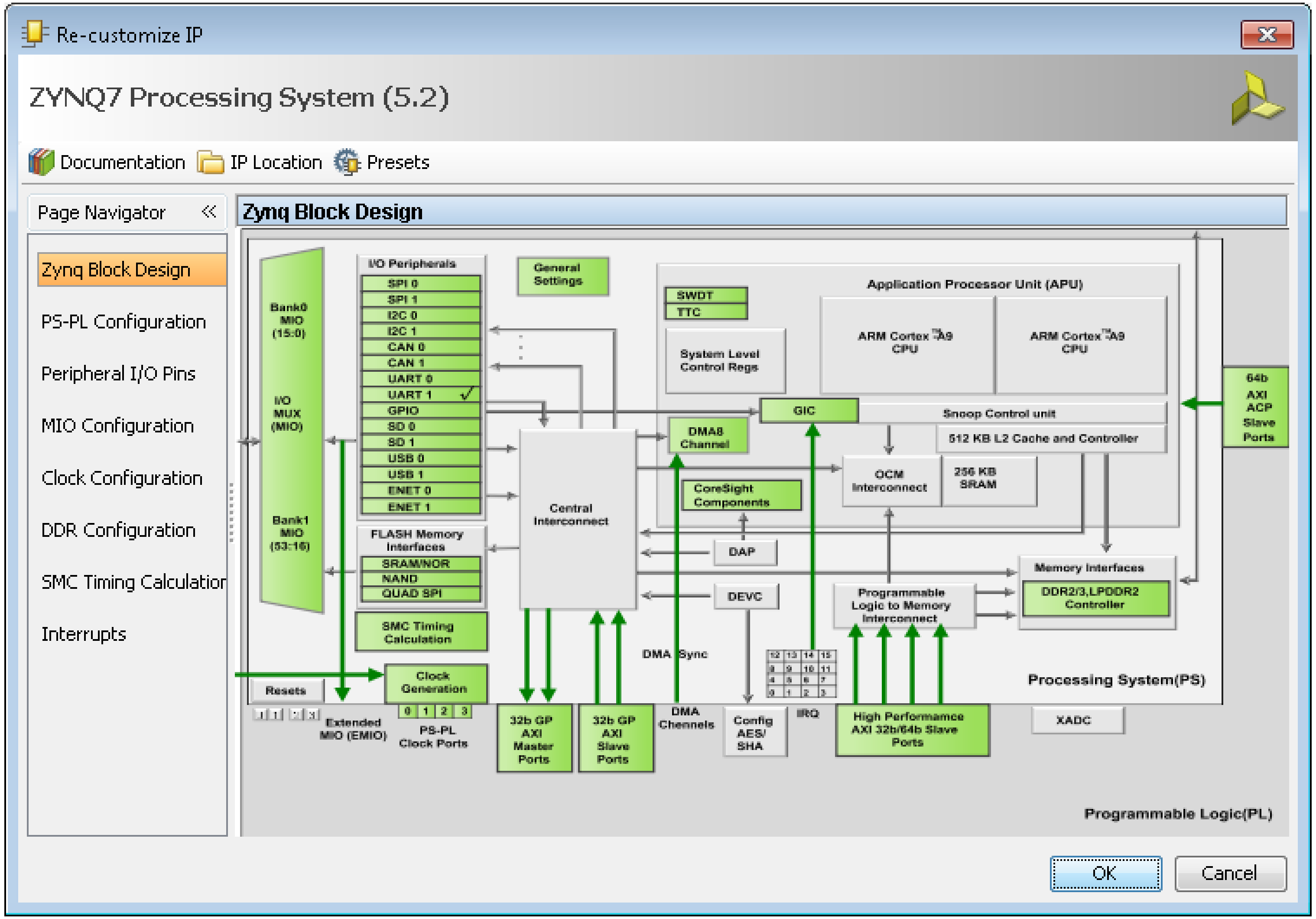
- **GPIO blocks**
  - Four separate banks of 32 GPIO bits each
    - Two banks connect to the 54 MIO pins
      - 32 bits and 22 bits, respectively
    - Two banks connect to EMIO (64 bits)
  - Each GPIO bit can be dynamically programmed as input or output
  - Reset values independently configurable for each bit
  - Programmable interrupt generation for each bit
    - One interrupt generated per GPIO bank



GP0/1 Ports Configuration for PS-PL Interface

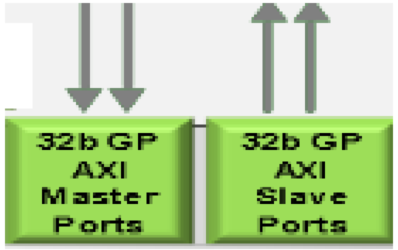
- Click on the menu or green GP Blocks to configure





GP 0/1 Ports

- By default, GP Slave and Master ports are disabled



- Enable GP Master and/or Slave ports depending on whether a slave or a master peripheral is going to be added in PL
- axi_interconnect block is required to connect IP to a port with different protocols
  - Automatically convert Protocols
  - Can be automatically added when using Block Automation in IPI

‘C’ Divers Support for GP 0/1

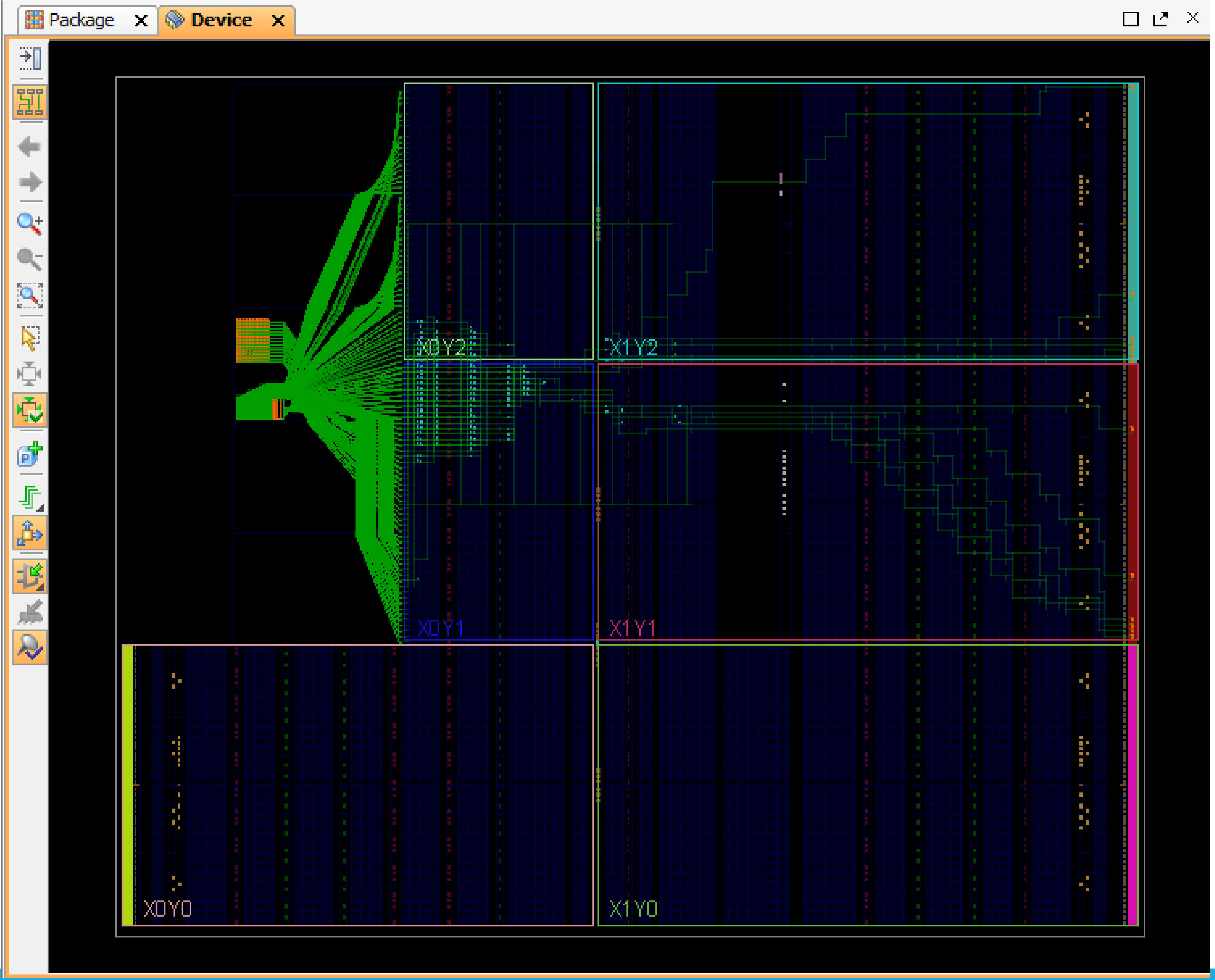
- **Include files needed**
  - `xgpiops.h, xgpiops_hw.h` (for low-level functions)
- **Initialize GPIO device driver**
  - ConfigPtr = `XGpioPs_LookupConfig(GPIO_DEVICE_ID);`
  - Status = `XGpioPs_CfgInitialize(&Gpio, ConfigPtr, ConfigPtr->BaseAddr);`
- **Configure and use GPIO device for output**
  - `XGpioPs_SetDirectionPin(&Gpio, OUTPUT_PIN, 1);`
  - `XGpioPs_SetOutputEnablePin(&Gpio, OUTPUT_PIN, 1);`
  - `XGpioPs_WritePin(&Gpio, OUTPUT_PIN, 0x0);`
- **Configure and use GPIO device for input**
  - `XGpioPs_SetDirectionPin(&Gpio, INPUT_PIN, 0x0);`
  - `*DataRead = XGpioPs_ReadPin(&Gpio, INPUT_PIN);`

Other Driver Support for GP 0/1

- **Interrupts setup**
  - `XGpioPs_SetIntrType (InstancePtr, Bank, IntrType, IntrPolarity, IntrOnAny);`
  - `XGpioPs_SetCallbackHandler (InstancePtr, CallBackRef, FuncPtr);`
  - `XGpioPs_IntrEnable (InstancePtr, Bank, Mask);`
- **Interrupts processing**
  - `XGpioPs_IntrGetStatus (InstancePtr, Bank);`
  - `XGpioPs_IntrGetStatusPin (InstancePtr, Pin);`
  - `XGpioPs_IntrClear (InstancePtr, Bank, Mask);`
- **Of course, there are more functions than the listed here**

Zynq – Package View

Zynq – Internal Device View



Apendix

IO Peripherals

I2C

- I^2C bus specification version 2
- Programmable to use normal (7-bit) or extended (10-bit) addressing
- Programmable rates: fast mode (400 kbit/s) , standard (10 0kbits/s), and low (10 kbits/s)
  - Rates higher than 400 kbits/sec are not supported
- Programmable as either a master or slave interface
- Capable of clock synchronization and bus arbitration
- Fully programmable slave response address
- Reversible FIFO operation supported
- 16-byte buffer size
- Slave monitor mode when set up as master
- I^2C bus hold for slow host service
- Slave timeout detection with programmable period
- Transfer status interrupts and flags

CAN

- Up to 24-MHz CAN_REF clock as system clock
- 64 message-deep receiver and transmitter buffer
- Full CAN 2.0B compliant; conforms to ISO 11898-1
- Maximum baud rate of 1 Mb/s
- Four message filters required for buffer mode
- Listen-only mode for test and debug
- External PHY I/O
- “Wake-on-message”
- Time-stamping for receive messages
- TX and RX FIFO watermarking
- Exception: no power-down mode

SD-SDIO

- Support for version 2.0 of SD Specification
- Full-speed (4 MB/s) and low-speed (2 MB/s) support
  - Low-speed clock (400 KHz) used until bandwidth negotiated
- 1-bit and 4-bit data interface support
- Host mode support only
- Built-in DMA controller
- Full-speed clock (0-50 MHz) with maximum throughput at 25 MB/s
- 1 KB data FIFO interface
- Support for MMC 3.31 card at 52 MHz
- Support for memory, I/O, and combo cards
- Support for power control modes and interrupts

SPI

- Master or slave SPI mode
- Four wire bus: MOSI, MISO, SCK, nSS
- Supports up to three slave select lines
- Supports multi-master environment
- Identifies an error condition if more than one master detected
- Software can poll for status or function as interrupt-driven device
- Programmable interrupt generation
- 50-MHz maximum external SPI clock rate
- Selectable master clock reference
- Integrated 128-byte deep read and write FIFOs
- Full-duplex operation offers simultaneous receive and transmit

UART

- Two UARTs
- Programmable baud rate generator
- 64-byte receive and transmit FIFOs
- 6, 7, or 8 data bits and 1, 1.5, or 2 stop bits
- Odd, even, space, mark, or no parity with parity, framing, and overrun error detection
- "Line break" generation and detection
- Normal, automatic echo, local loopback, and remote loopback channel modes
- Interrupts generation
- Support 8 Mb/s maximum baud rate with additional reference clock or up to 1.5 Mb/s with a 100-MHz peripheral bus clock
- Modem control signals: CTS, RTS, DSR, DTR, RI, and DCD (through EMIO)
- Simple UART: only two pins (TX and RX through MIO)

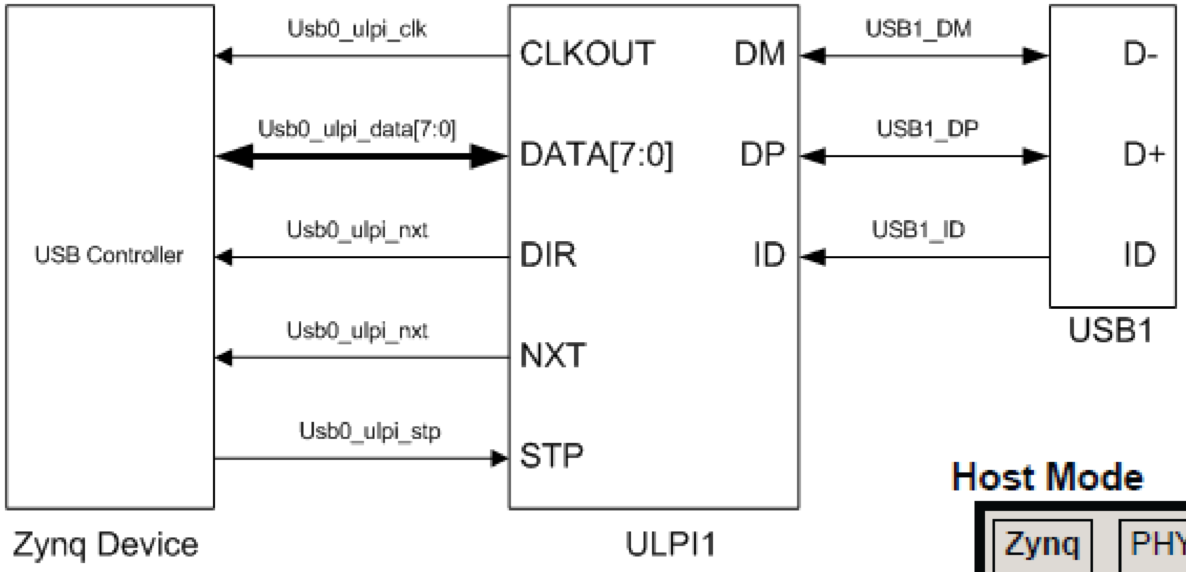
USB

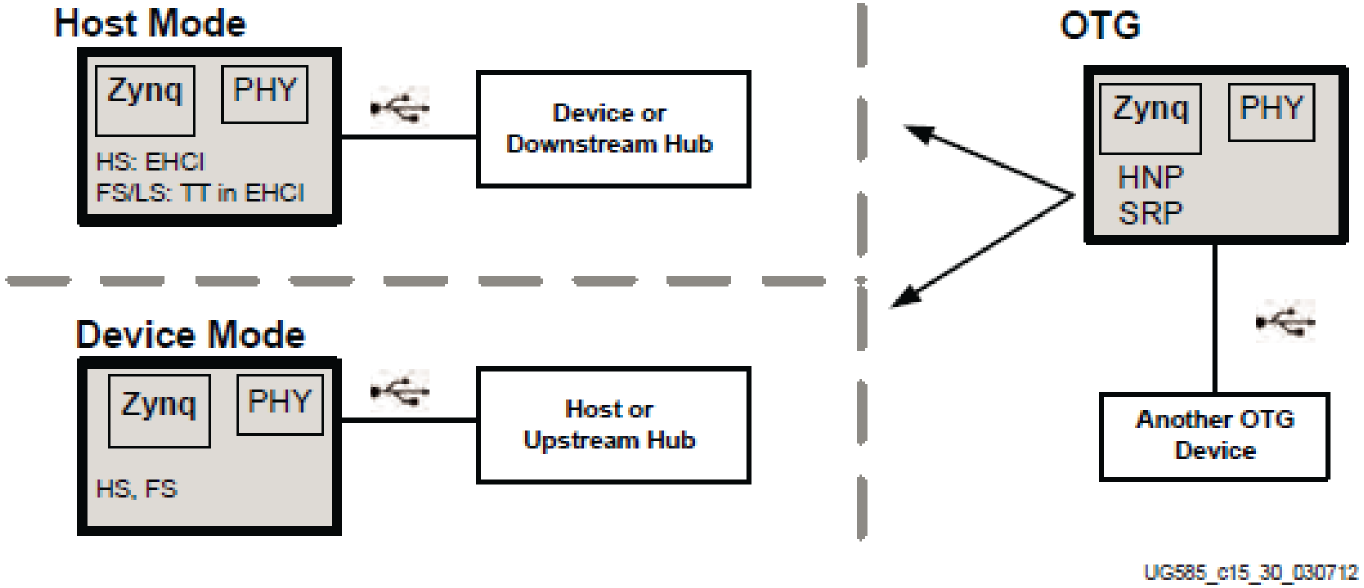
- Two USB 2.0 hardened IP peripherals per Zynq device
  - Each independently controlled and configured
- Supported interfaces
  - High-speed USB 2.0: 480 Mbit/s
  - Full-speed USB 1.1: 12 Mbit/s
  - Low-speed USB 1.0: 1.5 Mbit/s
  - Communication starts at USB 2.0 speed and drops until sync is achieved
- Each block can be configured as host, device, or on-the-go (OTG)
- 8-bit ULPI interface
- All four transfer types supported: isochronous, interrupt, bulk, and control
- Supports up to 12 endpoints per USB block in the Zynq device
  - Running in host mode
- Source-code drivers

USB 2.0 OTG

- Control and configuration registers for each USB block
- Software-ready with standalone and OS linux source-code delivered drivers
- EHCI compliant host registers
- USB host controller registers and data structures compliant to Intel EHCI specifications
- Internal DMA
- Must use the MIO pins

USB 2.0 Usage Example

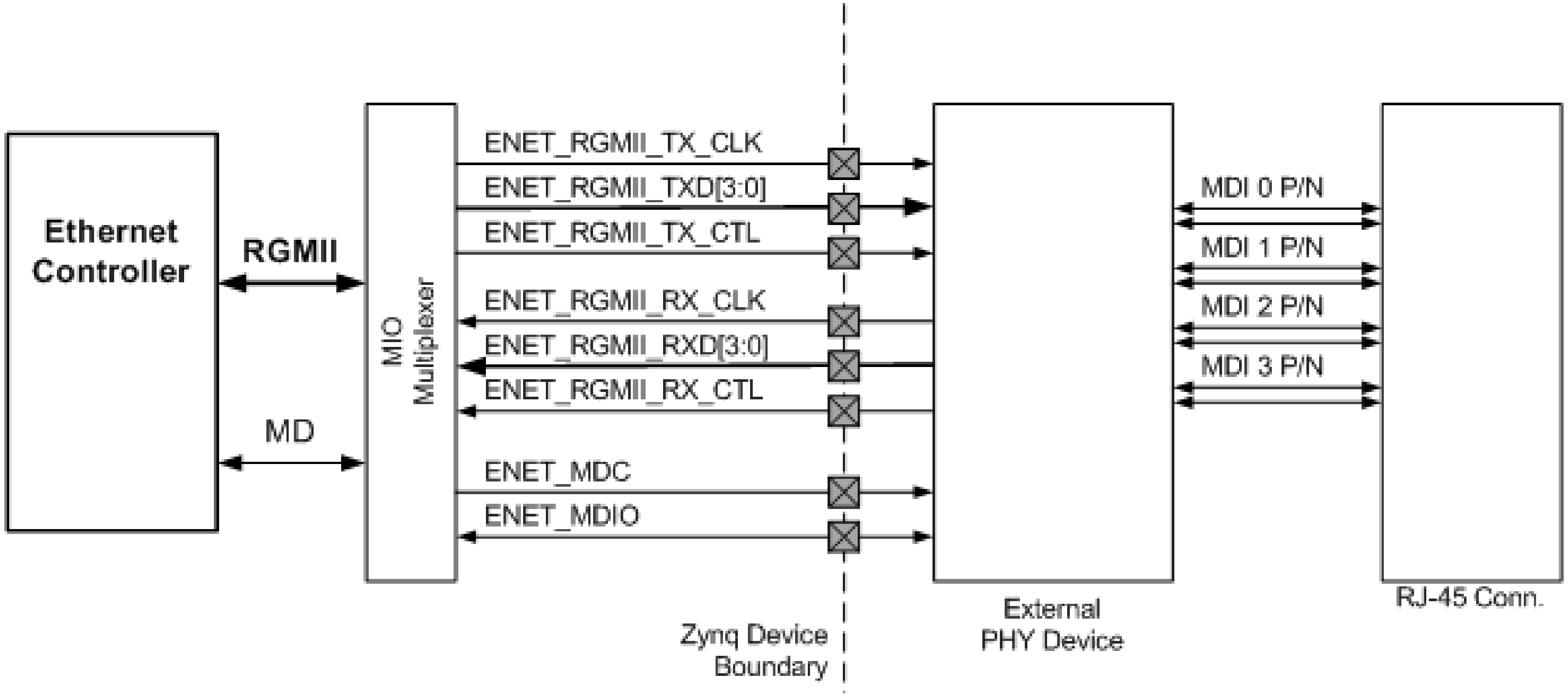




Gigabit Ethernet Controller

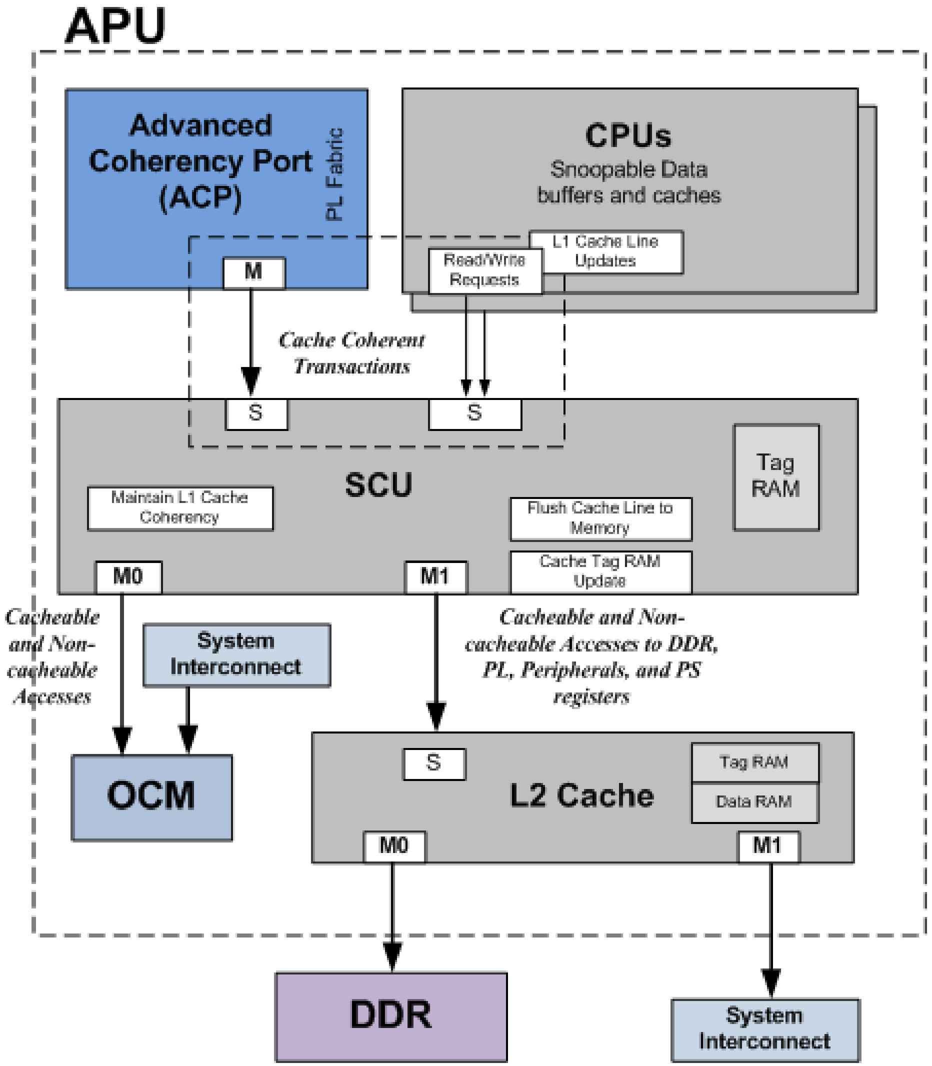
- Tri-mode Ethernet MAC (10/100/1G) with native GMII interface
- IEEE1588 rev 2.0
  - Time stamp support
  - 1 us resolution
- IEEE802.3
- RGMII v2.0 (HSTL) interface to MIO pins
  - Need MIO set at 1.8V to support RGMII speed
  - Need to use large bank of MIO pins for two Ethernets
- MII/GMII/SGMII/RGMII ver1.3 (LVCMOS) and ver2.0 (HSTL) interface available through EMIO (programmable logic I/O)
- TX/RX checksum offload for TCP and UDP
- Internal DMA and wake on LAN

Gigabit Ethernet Controller



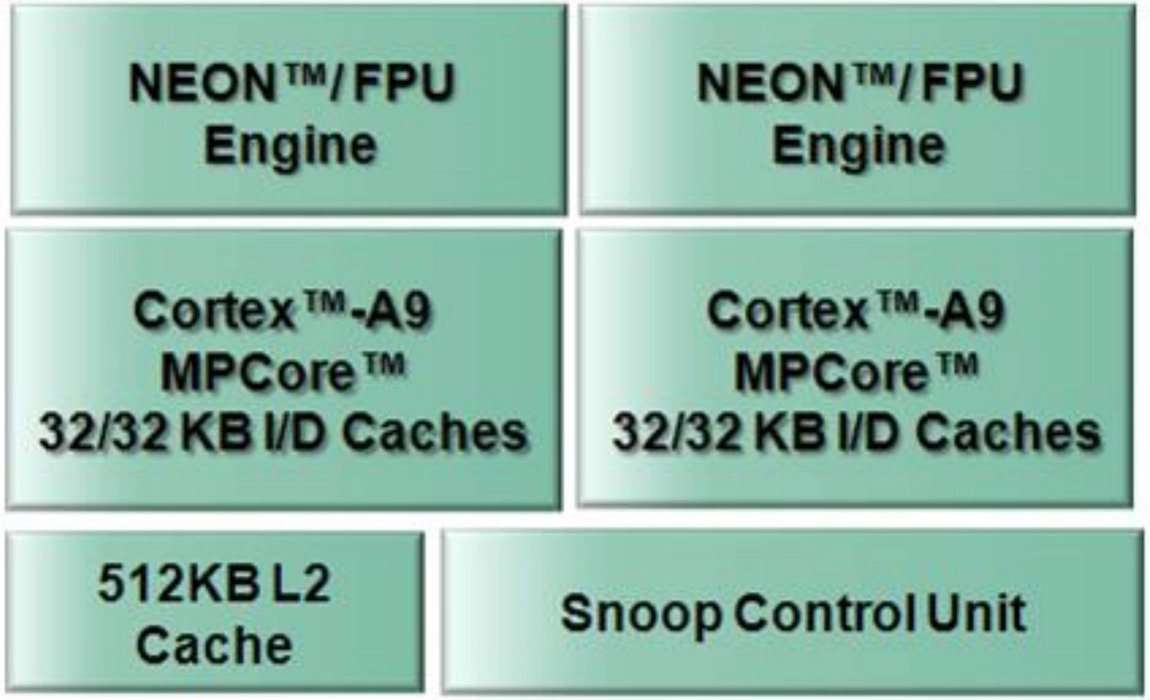
Application Processor Unit (APU)

APU


APU
Advanced Coherency Port (ACP)
PL Fabric
M
CPUs
Snoopable Data buffers and caches
L1 Cache Line Updates
Read/Write Requests
Cache Coherent Transactions
S
S
SCU
Tag RAM
Maintain L1 Cache Coherency
Flush Cache Line to Memory
Cache Tag RAM Update
M0
M1
Cacheable and Non-cacheable Accesses
System Interconnect
Cacheable and Non-cacheable Accesses to DDR, PL, Peripherals, and PS registers
OCM
S
L2 Cache
Tag RAM
Data RAM
M0
M1
DDR
System Interconnect

APU Components

- Dual ARM® Cortex™-A9 MPCore with NEON extensions
  - Up to 800-MHz operation
  - 2.5 DMIPS/MHz per core
  - Separate 32KB instruction and data caches
- Snoop Control Unit (SCU)
  - L1 cache snoop control
    - Accelerator coherency port
- Level 2 cache and controller
  - Shared 512 KB cache with parity



APU Sub-Components

- General interrupt controller (GIC)
- On-chip memory (OCM): RAM and boot ROM
- Central DMA (eight channels)
- Device configuration (DEVCFG)
- Private watchdog timer and timer for each CPU
- System watchdog and triple timer counters shared between CPUs
- ARM CoreSight debug technology

APU Address Map

- All registers for both CPUs are grouped into two contiguous 4KB pages
  - Accessed through a dedicated internal bus
- Fixed at 0xF8F0_0000 with a register block size of 8 KB
  - Each CPU uses an offset into this base address

0x0000-0x00FC	SCU registers
0x0100-0x01FF	Interrupt controller interface
0x0200-0x02FF	Global timer
0x0600-0x06FF	Private timers and watchdog timers
0x1000-0x1FFF	Interrupt distributor

NEON Main Features

- NEON is the ARM codename for the vector processing unit
  - Provides multimedia and signal processing support
- FPU is the floating-point unit extension to NEON
  - Both NEON and FPU share a single set of registers
- NEON technology is a wide single instruction, multiple data (SIMD) parallel and co-processing architecture
  - 32 registers, 64-bits wide (dual view as 16 registers, 128-bits wide)
  - Data types can be: signed/unsigned 8-bit, 16-bit, 32-bit, 64-bit, or 32-bit float

L1 Cache Features

- Separate instruction and data caches for each processor
- Caches are four-way, set associative and are write-back
- Non-lockable
- Eight words cache length
- On a cache miss, critical word first filling of the cache is performed followed by the next word in sequence

L2 Cache Features

- 512K bytes of RAM built into the SCU
  - Latency of 25 CPU cycles
  - Unified instruction and data cache
- Fixed, 256-bit (32 words) cache line size
- Support for per-master way lockdown between multiple CPUs
- Eight-way, set associative
- Two AXI interfaces
  - One to DDR controller
  - One to programmable logic master (to peripherals)

On-Chip Memory (OCM)

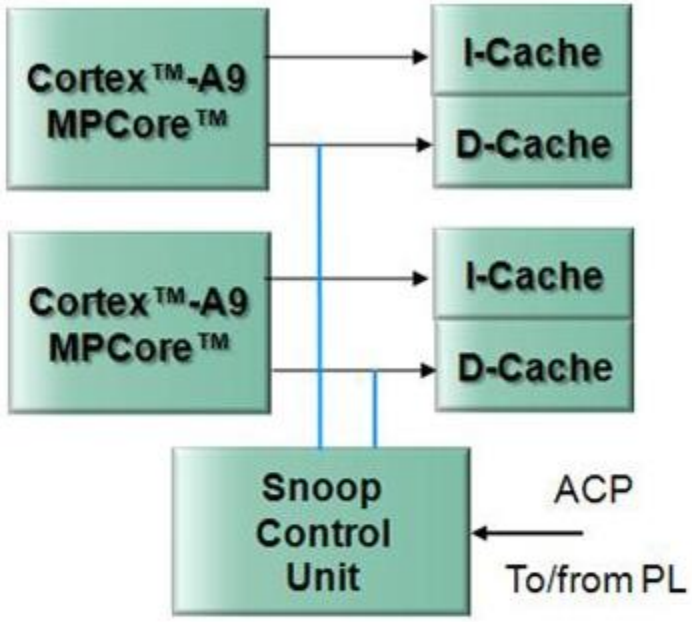
- The on-chip memory (OCM) module contains 256 KB of RAM and 128 KB of ROM (BootROM).
- It supports two 64-bit AXI slave interface ports, one dedicated for CPU/ACP access via the APU snoop control unit (SCU), and the other shared by all other bus masters within the processing system (PS) and programmable logic (PL).
- The BootROM memory is used exclusively by the boot process and is not visible to the user.

Snoop Control Unit (SCU)

- Shares and arbitrates functions between the two processor cores
  - Data cache coherency between the processors
  - Initiates L2 AXI memory access
  - Arbitrates between the processors requesting L2 accesses
  - Manages ACP accesses
  - A second master port with programmable address filtering between OCM and L2 memory support

Cache Coherency Using SCU

- High-performance, cache-to-cache transfers
- Snoop each CPU and cache each interface independently
- Coherency protocol is MESI
  - M: Cache line has been modified
  - E: Cache line is held exclusively
  - S: Cache line is shared with another CPU
  - I: Cache line is invalidated
- Uses Accelerator Coherence Port (ACP) to allow coherency to be extended to PL



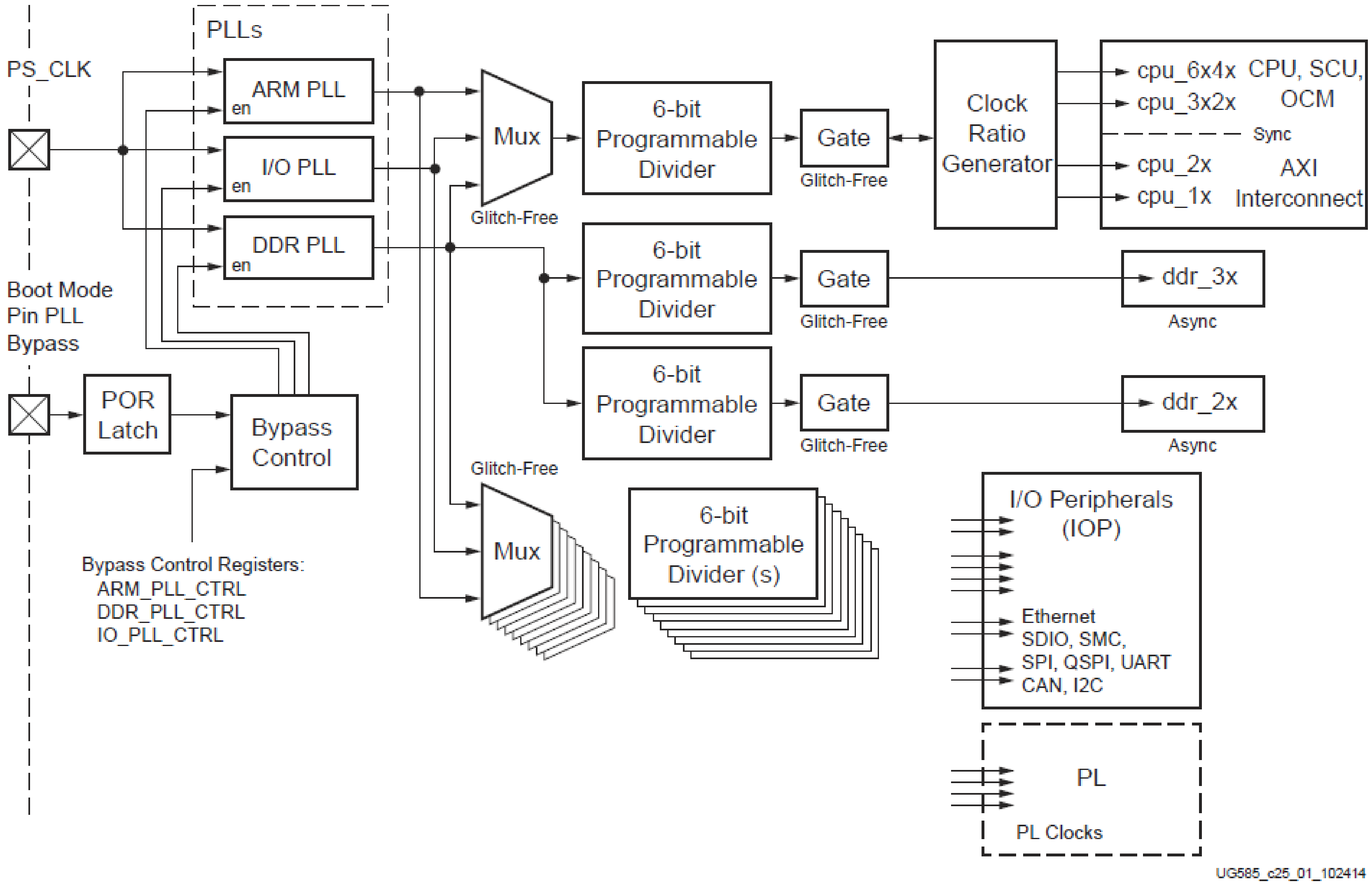
System Level Control Register (SLCR)

- A set of of special registers in the APU used to configure the PS
  - Power and clock management
  - Reset control
  - MIO/EMIO management
- Accessible through software
  - Standalone BSP support

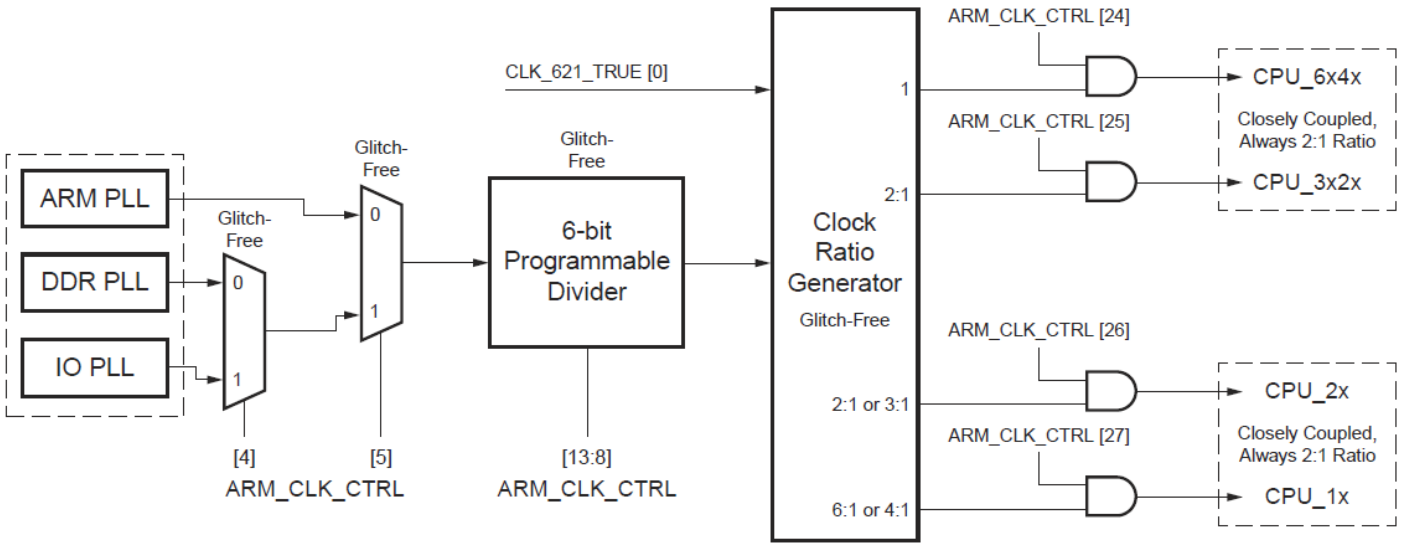
SLCR Categories	
System clock and reset control/status registers	TrustZone control register
APU control registers	SoC debug control registers
DMA initialization registers	MIO/IOP control/status registers
DDR control registers	Miscellaneous control registers
PL reset registers	RAM and ROM control registers

Zynq Clocks

System Clocks

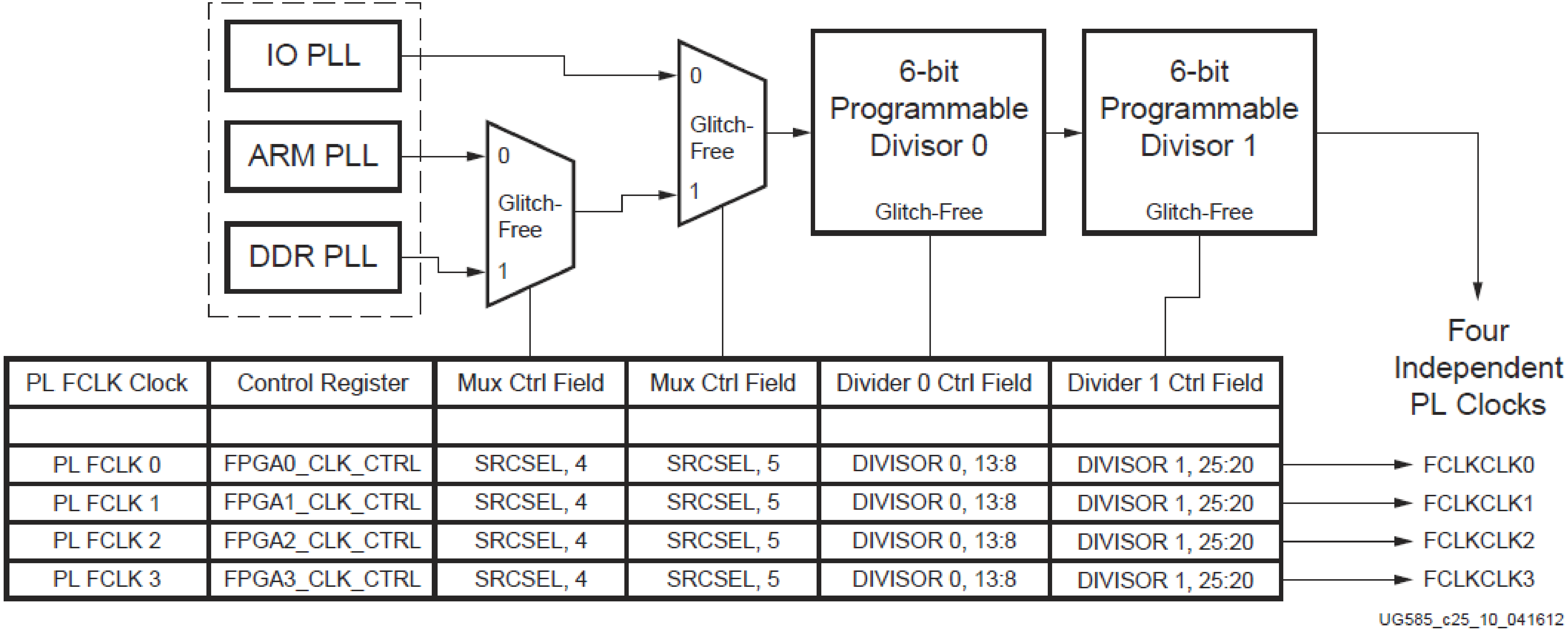


CPU Clock



CPU Clock	6:2:1	4:2:1	Clock Domain Modules
CPU_6x4x	800 MHz (6 times faster than CPU_1x)	600 MHz (4 times faster than CPU_1x)	CPU clock freq, SCU, OCM arbitrer, NEON and L2 Cache
CPU_3x2x	400 MHz (3 times faster than CPU_1x)	300 MHz (2 times faster than CPU_1x)	APU Timers
CPU_2x	266MHz (2 times faster than CPU_1x)	300 MHz (2 times faster than CPU_1x)	IOP, central interconnect, master interconeect, slave interconnect and OCM RAM
CPU_1x	133 MHz	150 MHz	IOP, AHB and APB interface busses

PL Clocks



PL FCLK Clock	Control Register	Mux Ctrl Field	Mux Ctrl Field	Divider 0 Ctrl Field	Divider 1 Ctrl Field	
PL FCLK 0	FPGA0_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	FCLKCLK0
PL FCLK 1	FPGA1_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	FCLKCLK1
PL FCLK 2	FPGA2_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	FCLKCLK2
PL FCLK 3	FPGA3_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	FCLKCLK3