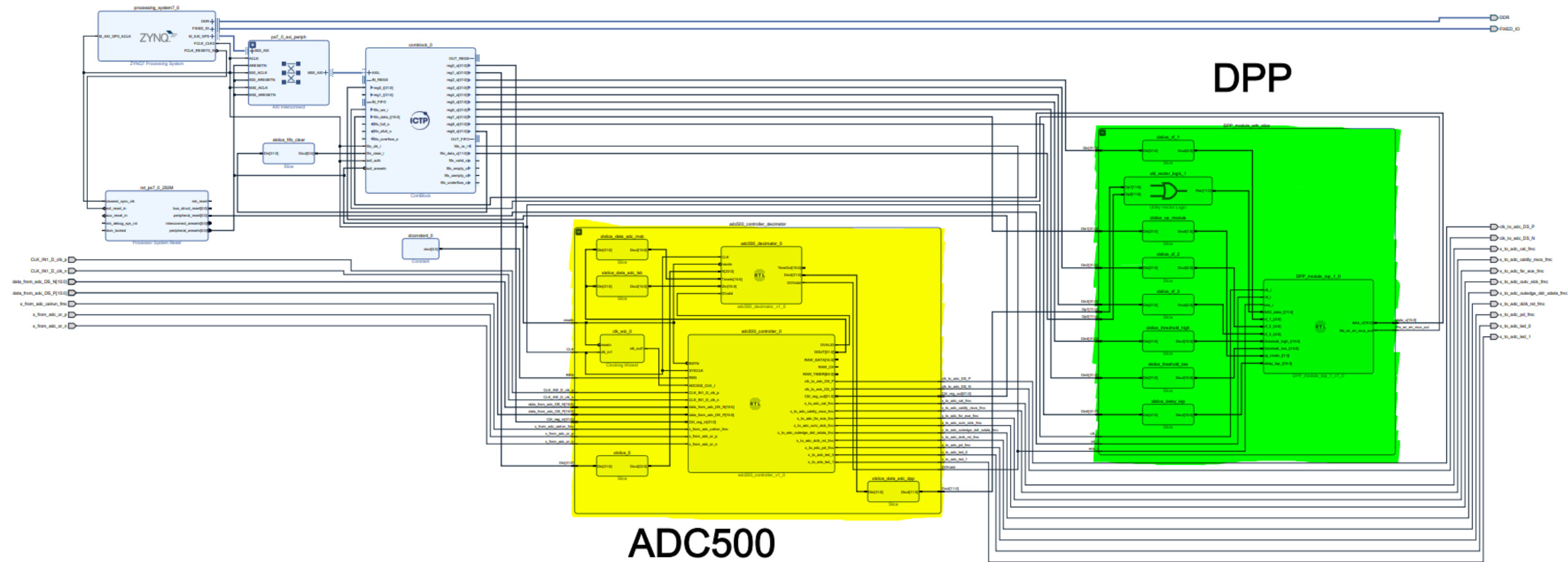


Maynor Ballina



Final Project implementation

Joint ICTP-IAEA School on FPGA-based SoC and its Applications for Nuclear and Related Instrumentation

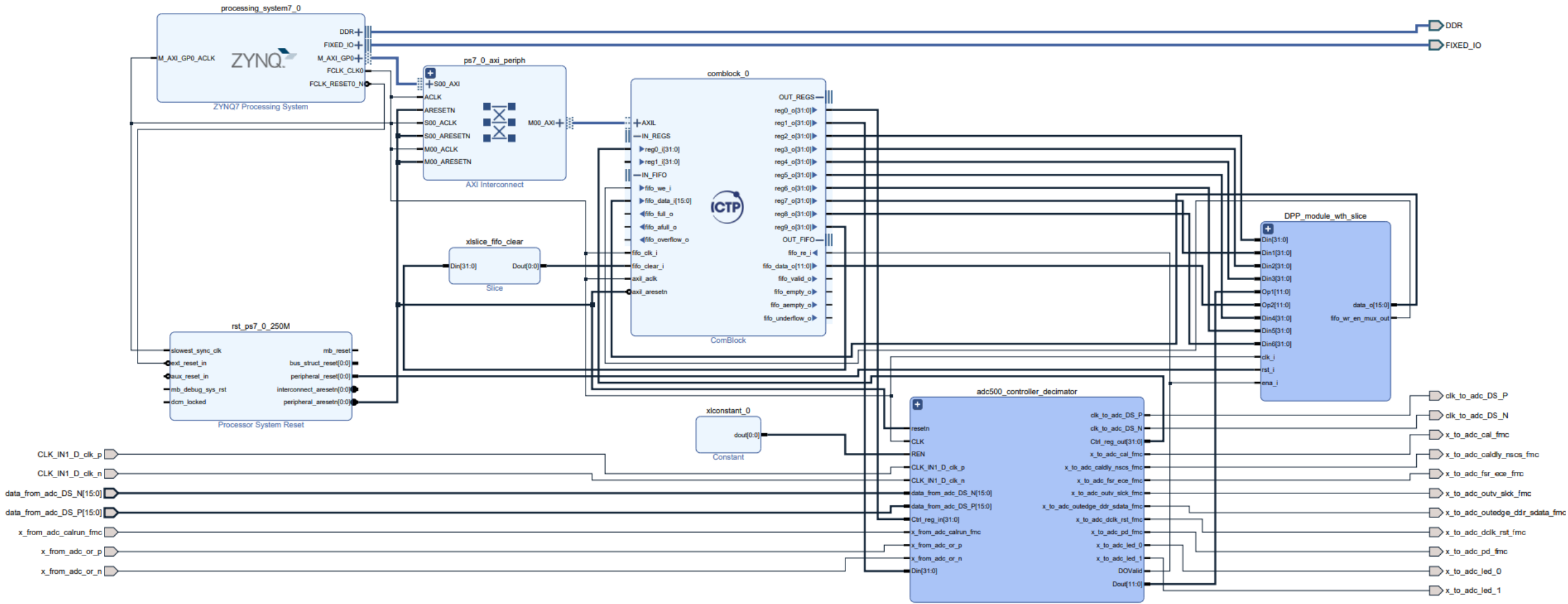


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Final Project implementation

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Difficulties and challenges

I was not very clear about the functionality of certain pins of some blocks

✓ *VHDL files.*

Missing some signal connections

✓ *Documentation provided.*

Misconceptions of functionality

✓ *Help from faculty members and fellow participants*

Time, personal activities, internet connection

✓ *Recorded talks, connection to the lab computers at any time, contact information of faculty members*

TO DO:

- Perfect understanding of all the topics.
- Signals for debugging via UDMA
- Use comblock for the manage of the signals obtained from two SIPMs

**Teachers of high academic level
and experience**



**Diverse topics on
lab activities:**

Digital Pulse Processor



**Meet researchers
working on
something similar**



ADC 500, UDMA, DPP

Digital Pulse Processing for X Ray Spectroscopy



**By applying what I have learned in my
project, it will facilitate its implementation**

**My research and the activities:
Detection of vertical muons with water Cherenkov detectors**

Thank you so much

Despite the difficulty due to the covid 19 pandemic, the activities turned out perfect, thanks for the effort made by the organizers

