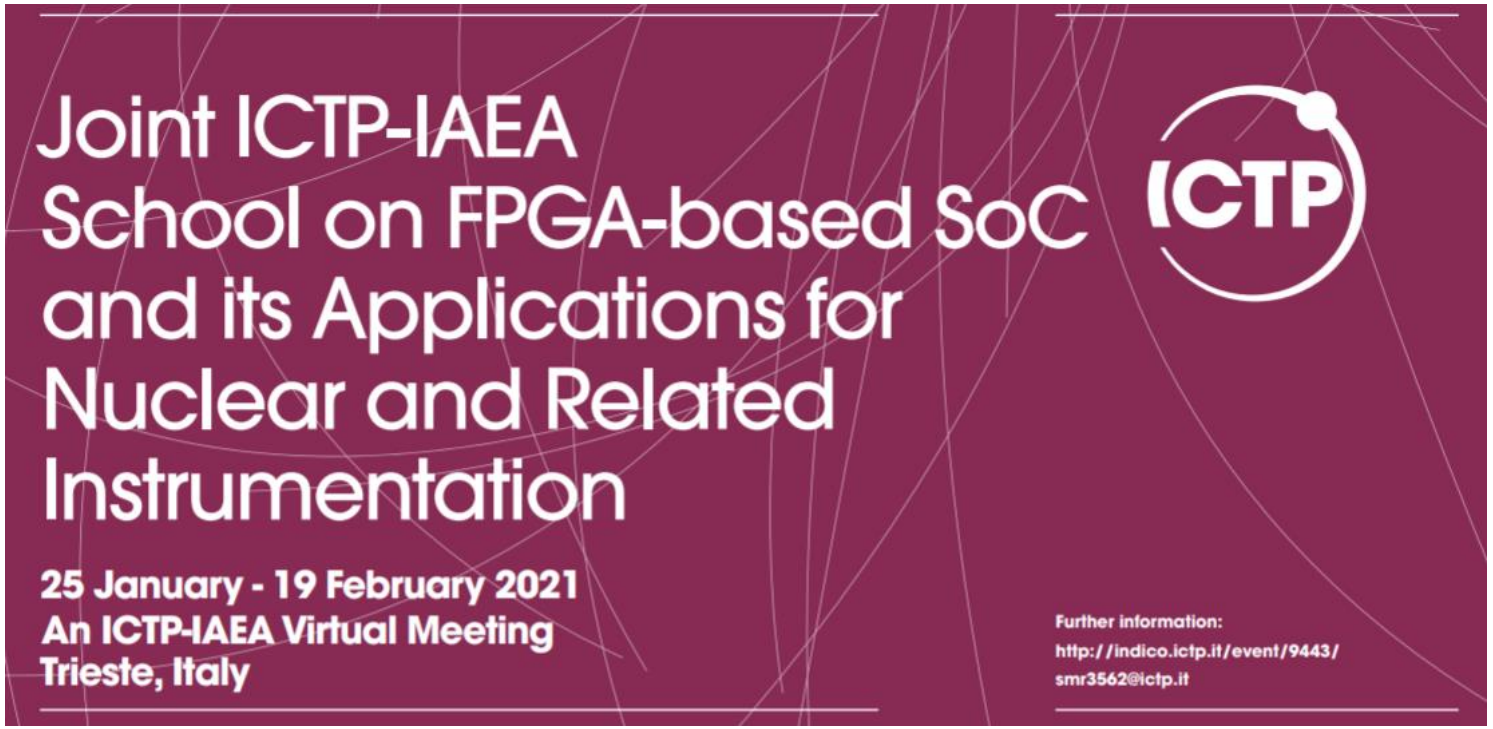


Personal reflection on the workshop

Rajiv Bishwokarma

#include "**before_workshop**.h"

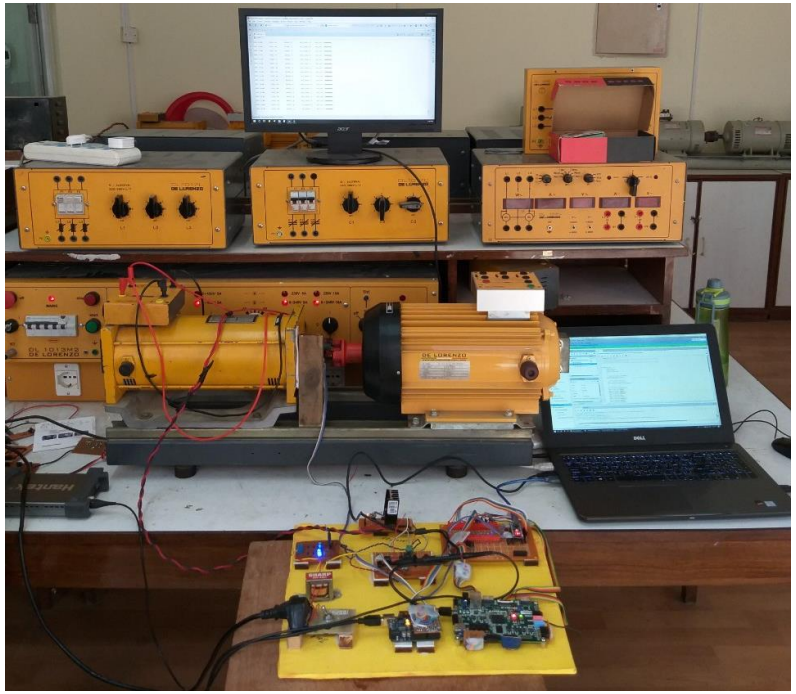
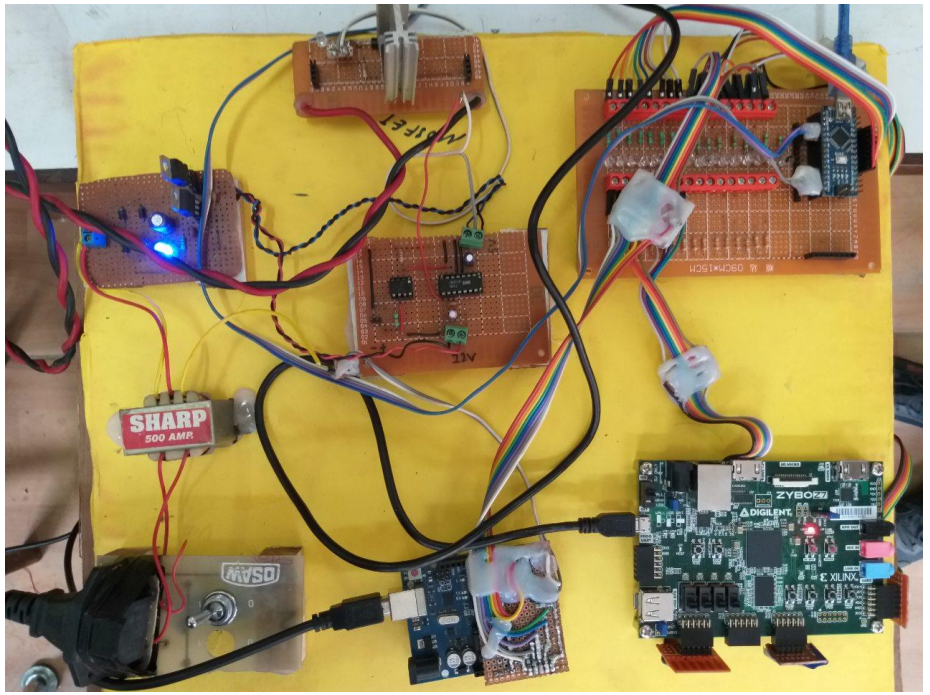


Fig. 1 (a) Complete experimental setup



(b) Controller System

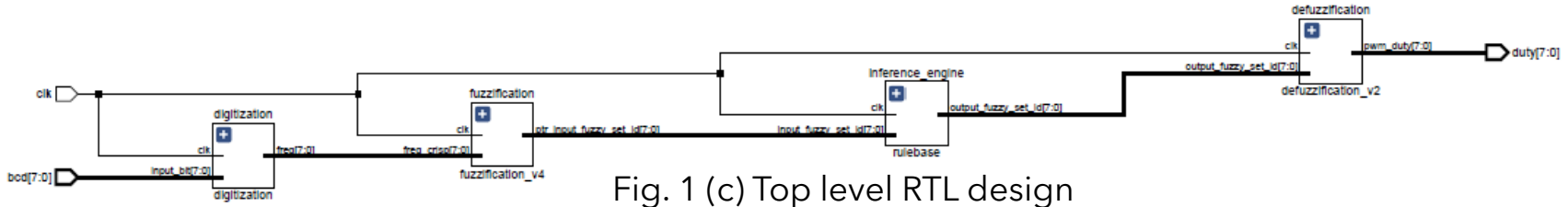


Fig. 1 (c) Top level RTL design

- FPGA-based Fuzzy Controller for Synchronous Generator Frequency Control
- Verilog, C

BUT

- No VHDL
- No SoC
- No Zynq PS
- No MicroBlaze
- No UART
- No Interrupts
- No ZedBoard
- No DMA
- No AXI
- No Block Design

```
int main()
{
    for (int day=1; day < 30; day++)
        start_ICTP_IAEA_workshop();
}
```

xil_printf("**Hello World!**");

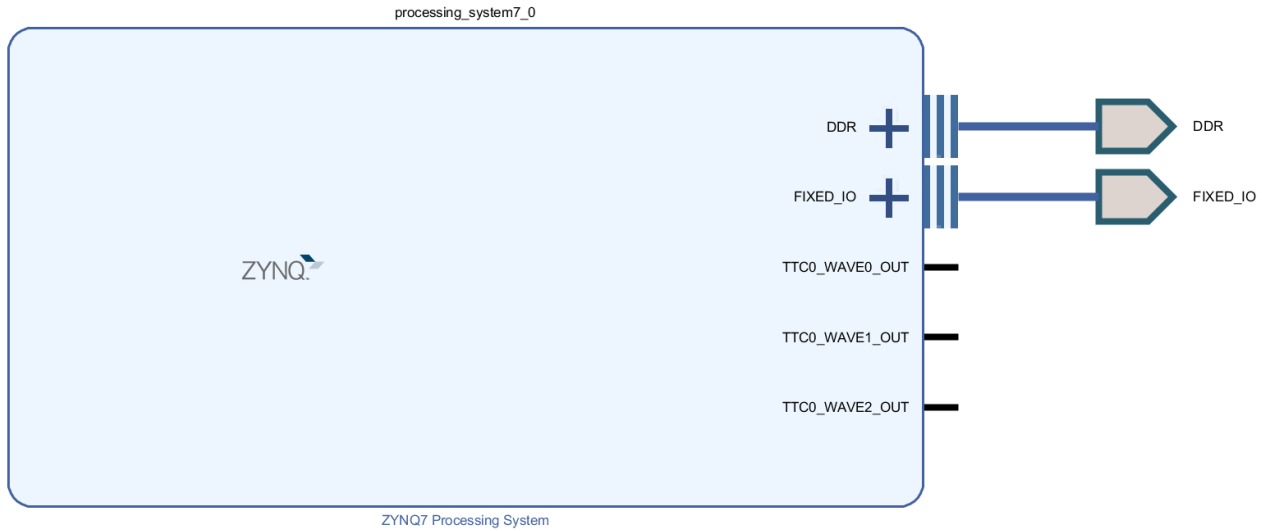


Fig. 2 (a) Zynq PS block for UART

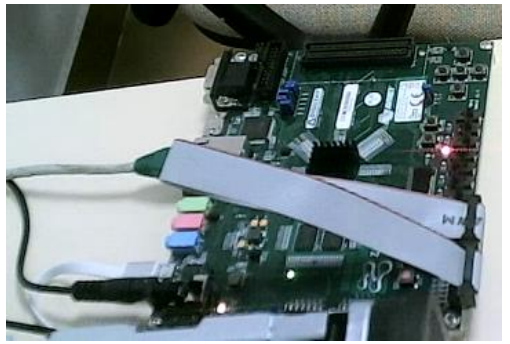


Fig. 2 (b) ZedBoard used for UART

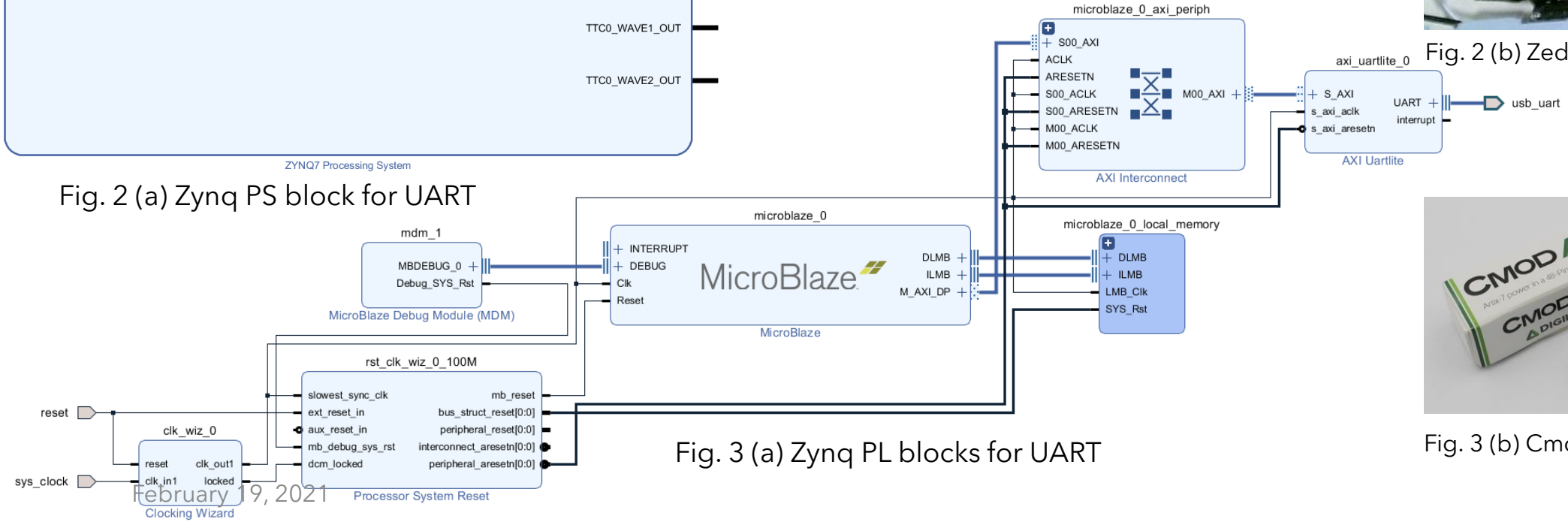


Fig. 3 (a) Zynq PL blocks for UART

Fig. 3 (b) Cmod A7 used for UART

cbWrite(XPAR_COMBLOCK_0_AXIL_BASEADDR, CB_IFIFO_CONTROL, 1)

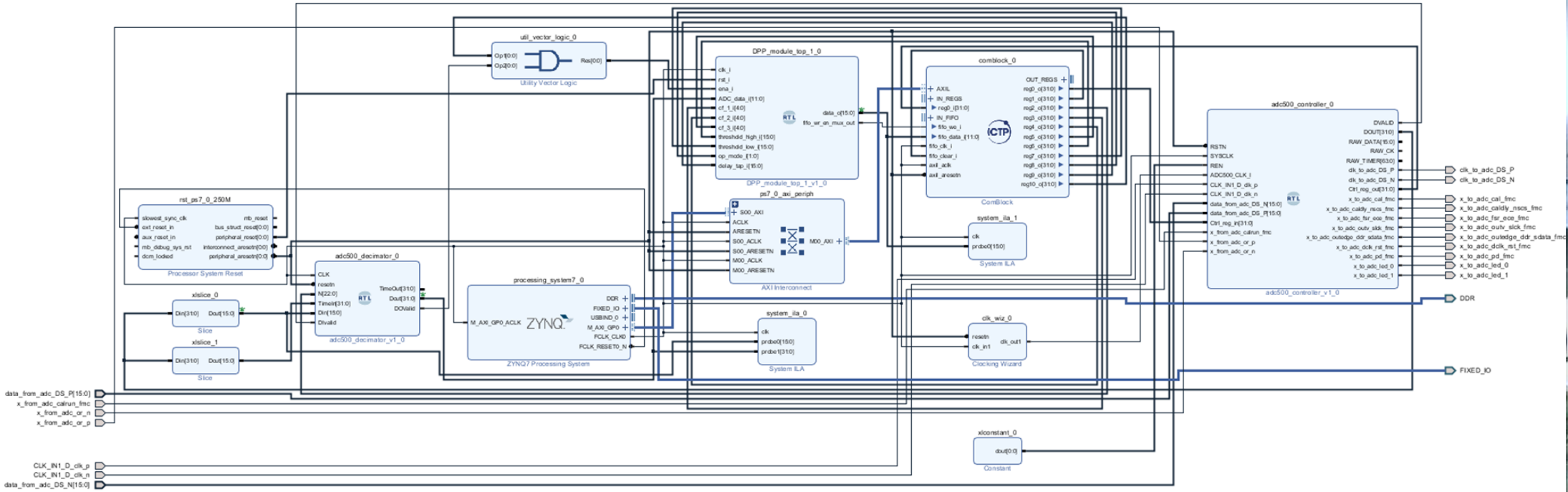


Fig. 4 (a) Complete design for pulse detection system

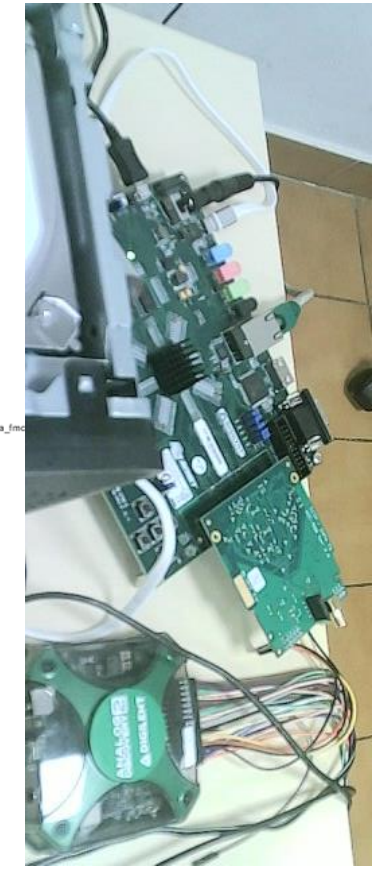


Fig. 4 (b) Board setup for pulse detection system

```
start_ICTP_IAEA_workshop()
{
        learn_great_things();
        meet_amazing_people();
}
```

x_write_mem mind_buff 0x37

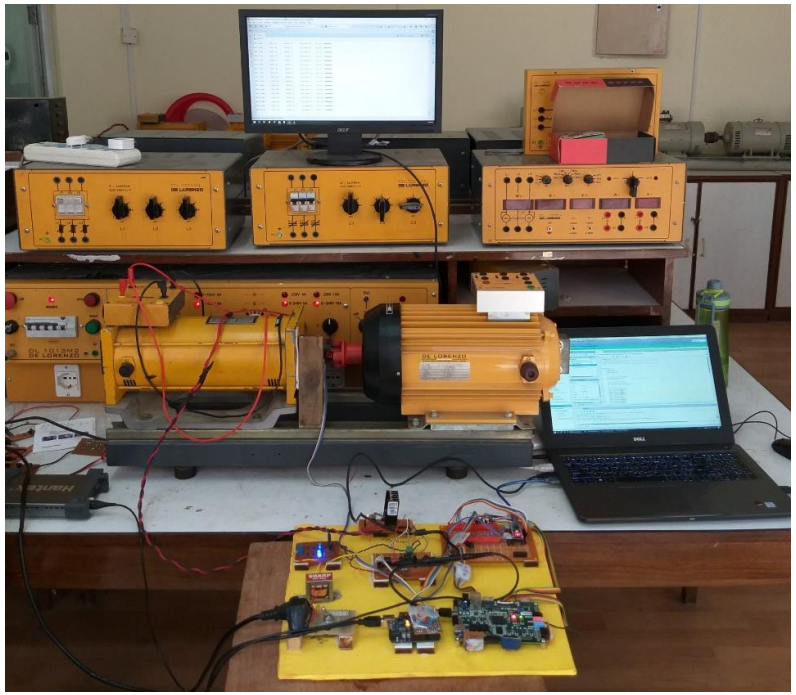
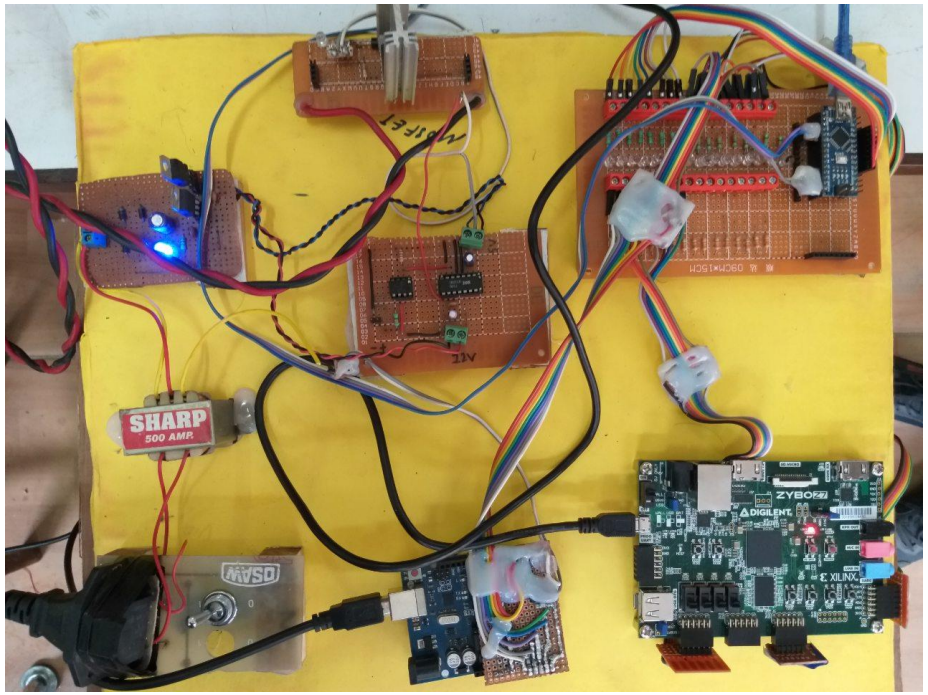


Fig. 1 (a) Complete experimental setup



(b) Controller System

1. Yes VHDL
2. Yes SoC
3. Yes Zynq PS
4. Yes MicroBlaze
5. Yes UART
6. Yes Interrupts
7. Yes ZedBoard
8. Yes DMA
9. Yes AXI
10. Yes Block Design

0x37 = (hex) (1 + 2+ .. + 10)

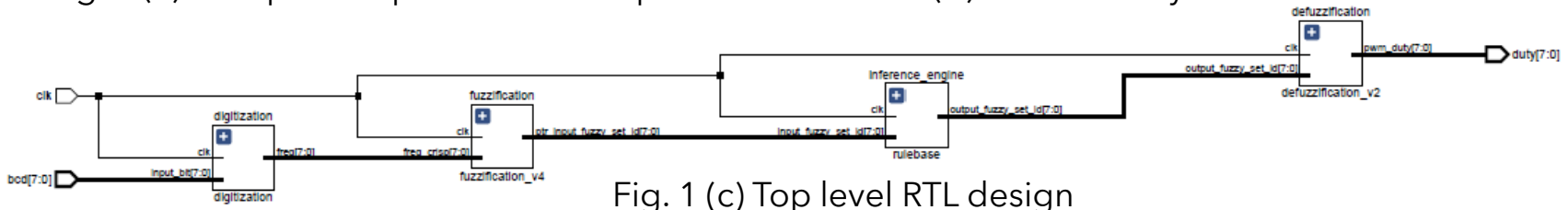


Fig. 1 (c) Top level RTL design

from __future__ import work_plans

1. DAQ for Particle Detectors (L1 Trigger Systems in ATLAS and LHCb)
2. High Level Synthesis For Machine Learning (HLS4ML)
3. RISC-V SoC

All great things must come to an end.

xil_printf("Thank You");
return 0;

linkedin.com/in/rajivbishwokarma