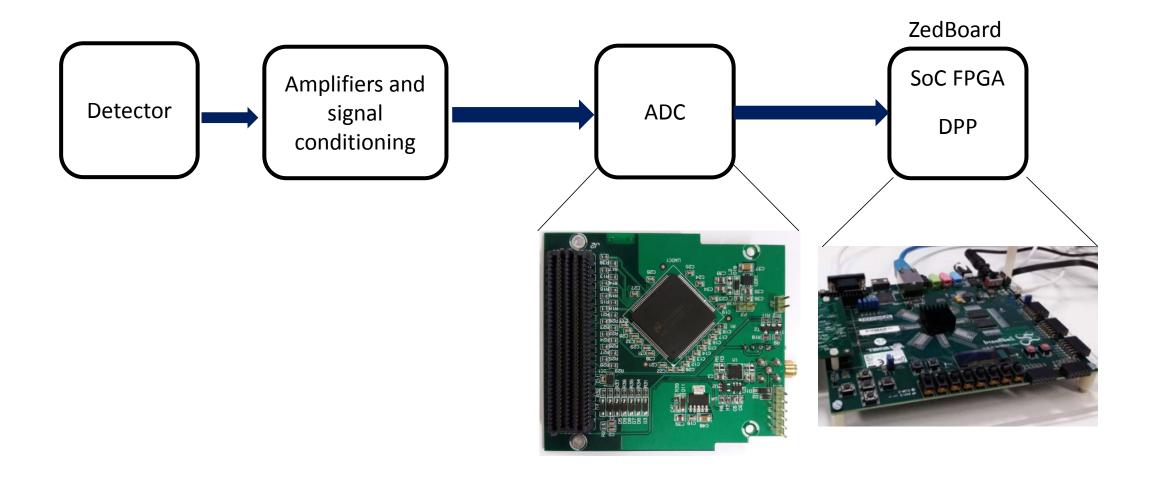
Digital Pulse Processor based on SoC-FPGA for Particle Detectors

ICTP guided Project

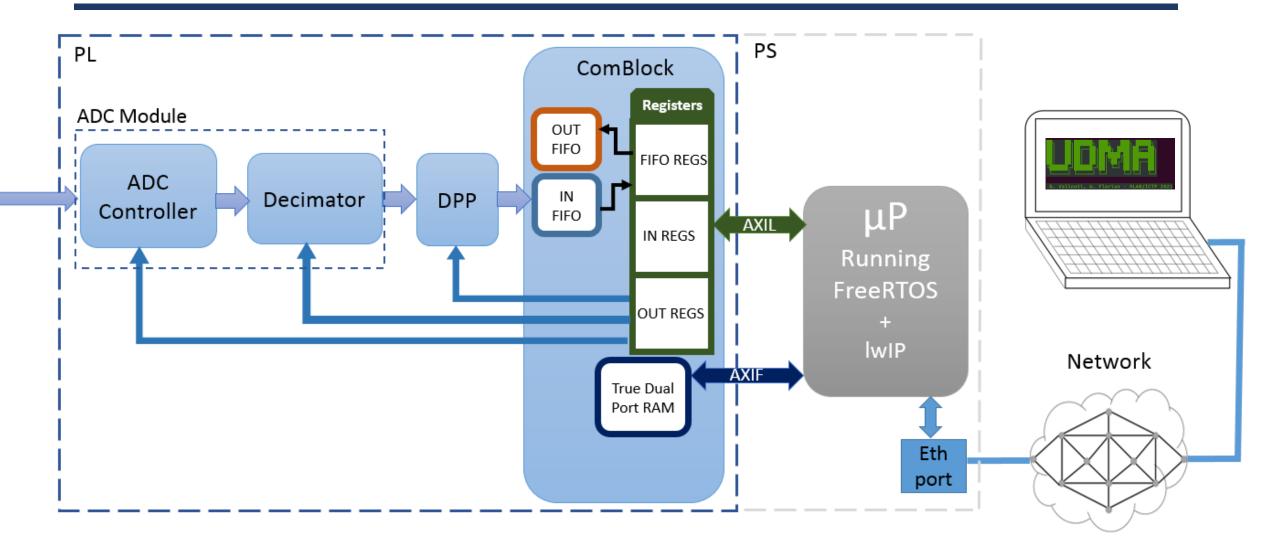
Joint ICTP-IAEA School on FPGA-based SoC and its Applications for Nuclear and Related Instrumentation

> Oscar Olaya 19/02/2021

General project structure

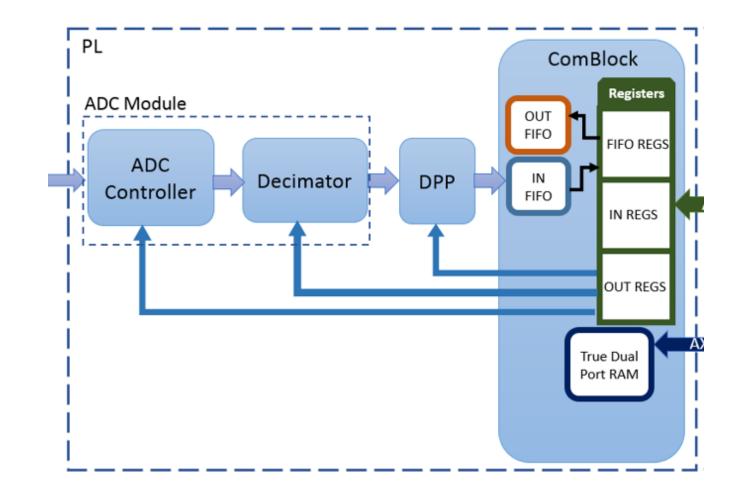


General project structure



Configuration registers

- Configuration registers:
 - ADC Module:
 - ADC control registers
 - ADC decimator
 - DPP Module:
 - FIR coefficients
 - Thresholds
 - Operation mode
 - DPP enable
 - ComBlock FIFO clear



Light weight IP – IwIP:

"IwIP is a small independent implementation of the TCP/IP protocol suite. The focus of the IwIP TCP/IP implementation is to reduce the RAM usage while still having a full scale TCP. This making IwIP suitable for use in embedded systems with tens of kilobytes of free RAM and room for around 40 kilobytes of code ROM."

Taken from:

https://www.nongnu.org/lwip/2 1 x/index.html

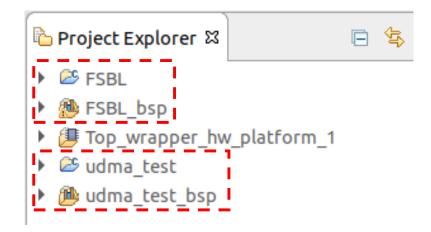
ARM μP FreeRTOS **WIP**

"First Stage Bootloader (FSBL) for Zynq. The FSBL configures the FPGA with HW bit stream (if it exists) and loads the Operating System (OS) Image or Standalone (SA) Image..."

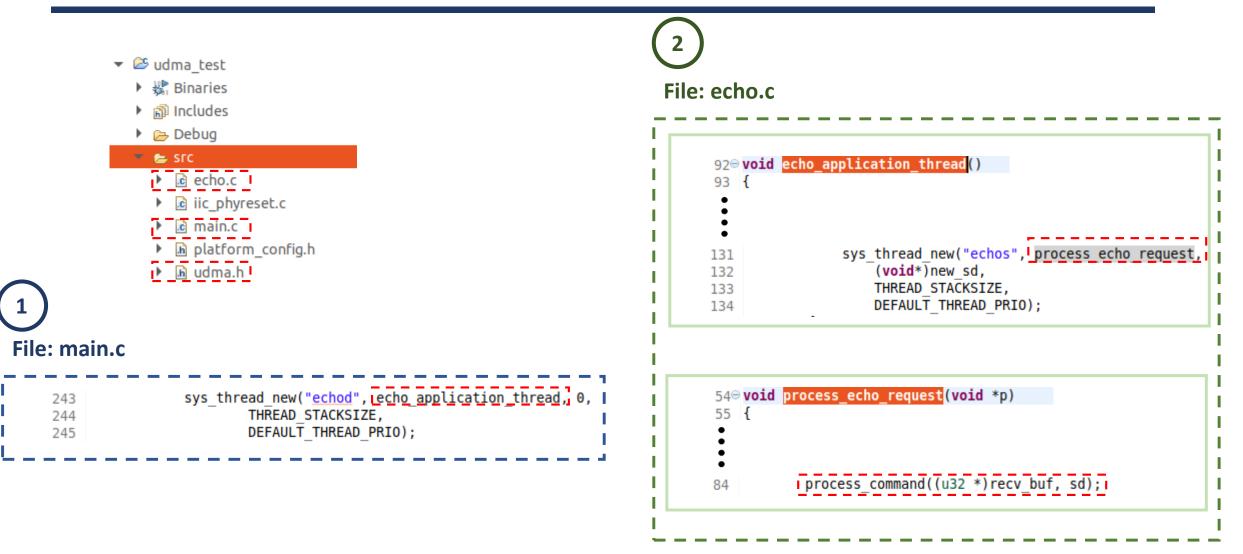
Taken from template description.

"The FreeRTOS IwIP Echo Server application provides a simple demonstration of how to use the light-weight IP stack (IwIP) with FreeRTOS... The server listens for input at port 7 and simply echoes back whatever data is sent to the port"

Taken from template description.



SDK – Application project



SDK – Application project

udma.h

149⊖ static inline void process_command (u32 *recv_buf, int sd) {		
150	u32 send buf[BUFF SIZE];	
151	<pre>send_buf[0]= 0; // always error unless a successful operation</pre>	
152	u32 pack_type = recv_buf[0];	
153	if(logging)	
154	<pre>xil_printf("\n Packet type:\t %d\n",pack_type);</pre>	xparameters.h
155	u32 o = 0;	Aparametersin
156	<pre>switch(pack_type){</pre>	35 #define XPAR COMBLOCK 0 AXIL BASEADDR 0x43C00000
157	case READ_REG:	
158	if(logging)	
159	xil_printf("Register:\t %u \n", recv_buf[1]);	
160	if (XPAR_COMBLOCK 0 REGS_IN_ENA) {	
161	<pre>send buf[1] = cbRead(XPAR_COMBLOCK 0 AXIL_BASEADDR, recv_buf[1]);</pre>	──→ comblock.h
162	send_buf[0] = 1;	
163	if(logging)	
164	xil_printf("READ VALUE:\t %u \n", send_buf[1]);	72 [©] static inline u32 cbRead (UINTPTR baseaddr, u32 reg) {
165	write(sd, send_buf, 2 * 4);	
166	} else	<pre>73 return *(volatile u32 *)(baseaddr + reg*4);</pre>
167	write(sd, send_buf, 4);	
168	break;	· · · · · · · · · · · · · · · · · · ·
169	case READ_RAM:	
170	if(logging)	

UDMA

Configure registers:

- ComBlock FIFO clear
- DPP Module:
 - FIR coefficients
 - Thresholds
 - Operation mode
 - DPP enable
- ADC Module:
 - ADC decimator
 - ADC control registers

Possibility of generating scripts that allow creating different configuration templates for the system.



edit

help macro

B. Valinoti, W. Florian - MLAB/ICTP 2021 his CLI application is the first edition of the UDMA on Cmd2. Use -h or --hel RVI CLI >: help Documented commands (use 'help -v' for verbose/'help <topic>' for details): Board communication _____ connect log udma Comblock Read _____ x_read_fifo x_read_mem x_read_ram x_read_reg Comblock Write ================== x_write_fifo x_write_mem x_write_ram x_write_reg Uncategorized ______ alias exit history py run pyscript set shortcuts

shell

quit run_script

Experience

- SoC FPGAs design flow
- Working with Xilinx tools
- Working with Git and Vivado
- Nuclear and related instrumentation
- A lot more...

Thank you!