ICTP-INFN Microprocessor Laboratory

ICTP-KNUST REGIONAL MICROELECTRONICS WORKSHOP ON FPGA AND VHDL FOR RESEARCH AND TRAINING IN AFRICA

25 July – 5 August 2005

Kumasi – Ghana

The Abdus Salam International Centre for Theoretical Physics (ICTP), Trieste, Italy and the Kwame Nkrumah University of Science and Technology (KNUST) will jointly organize the above mentioned course, to be held at KNUST, Kumasi, Ghana, from 25 July – 5 August 2005. The Course will be directed by Professor Francis K. Allotey (IMS), Dr. Andres Cicuttin (ICTP) and Dr. Nizar Abdallah (Actel Corp.).

Summary

The proposed Workshop is intended as a training activity in Microelectronics, to introduce engineers, physicists and computer scientists from Africa to the State-of-Art design methodologies of Programmable Logic Devices (PLDs). Emphasis will be placed on Field Programmable Gate Arrays (FPGAs) using a Hardware Description Language, VHDL, as cost effective solution for research and training in microelectronics. FPGAs are extensively reconfigurable and the NRE (Non Recurring Engineering) cost is very low. They are easy to design and to implement compared to Application Specific Integrated Circuits (ASICs). The laboratory exercises will focus on hands-on experimentation with FPGA evaluation boards and corresponding design software, which has been kindly donated by Actel Corp. (www.actel.com), a supplier of programmable logic solutions, including field-programmable gate arrays (FPGAs) based on antifuse and flash technologies. The Workshop contains a ground-up introduction to top-down digital design methodology using VHDL, a hardware description language. The course includes hands-on laboratory work to which 60-75 % of the time is allocated.

Purpose of the Workshop

The aim of the workshop will be to train engineers, physicists and computer scientists in Africa in the latest microelectronics design methodology and to promote research and human capacity development in design of microelectronic systems and devices.

Programmable Logic Devices (PLDs) have been growing dramatically in size, complexity and sophistication during the last few years. They are increasingly attracting the attention of many experimental physicists, electronic engineers and computing scientists due to several factors such as virtually unlimited re-configurability, fast design time, low cost design tools, extreme versatility and performance, etc. They are in fact cost-effective solutions for advanced designs in many areas such as: Telecommunications, Data Acquisition, Scientific Instrumentation, Digital Signal Processing, Reconfigurable Computing, etc…

The necessary Know-How to take full advantage of these devices implies knowing the State-of-Art methodologies and modern EDA tools along with some hands-on design experience to grasp the real possibilities and limitations.

Topics to be covered **will include:**

- **FPGA**: Technologies, Architectures, Design Methodology and Design Flow
- **VHDL**: Modeling and Simulation, VHDL for Synthesis
- **Digital Signal Processing** (DSP) : Fourier Theory, Sampling Theory, Digital filters
- **Digital System Design**
- **Reuse methodology for System-on-a-Chip Designs**
- **Hands-on Laboratory Exercises**: VHDL Modeling, Simulation and FPGA Design

Scientists and students **from African countries only** that are members of the UN, UNESCO or IAEA can attend the Course. The main purpose of the Centre is to help research workers from developing countries through a program of training activities within a framework of international cooperation. As the Course will be conducted in English, participants should have an adequate working knowledge of that language. A basic knowledge of digital electronics is also required.

As a rule, travel and subsistence expenses of the participants should be borne by the home institution. Every effort should be made by candidates to secure support for their fare (or at least half-fare). However, limited funds are available for some participants, who are nationals of, and working in, a developing country, and who are not more than 45 years old. Such support is available only for those who attend the entire activity. There is no registration fee.

All participants are required to take part in all aspects of this activity for its entire duration

The **Application Form** obtainable from the ICTP WWW server: http://agenda.ictp.trieste.it/agenda/current/fullAgenda.php?ida=a04224 (which will be constantly up-dated) or from the activity Secretariat. **It** should be completed and returned before **15 April 2005** to:

2005 WORKSHOP ON FPGA AND VHDL FOR RESEARCH AND TRAINING IN AFRICA
(smr1691) (c/o Ms. S. Tanaskovic)
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Sponsored by Actel® INNOVATIVE programmable logic solutions

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HEAD OF LABORATORY EXERCISES

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THE DEADLINE
for requesting participation:

15 April 2005