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**ICTP-INFN Advanced Tranining Course on
FPGA and VHDL for Hardware Simulation and Synthesis
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Packaging Test Practices

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These lecture notes are intended only for distribution to participants

Packaging, testing and (good design practices)

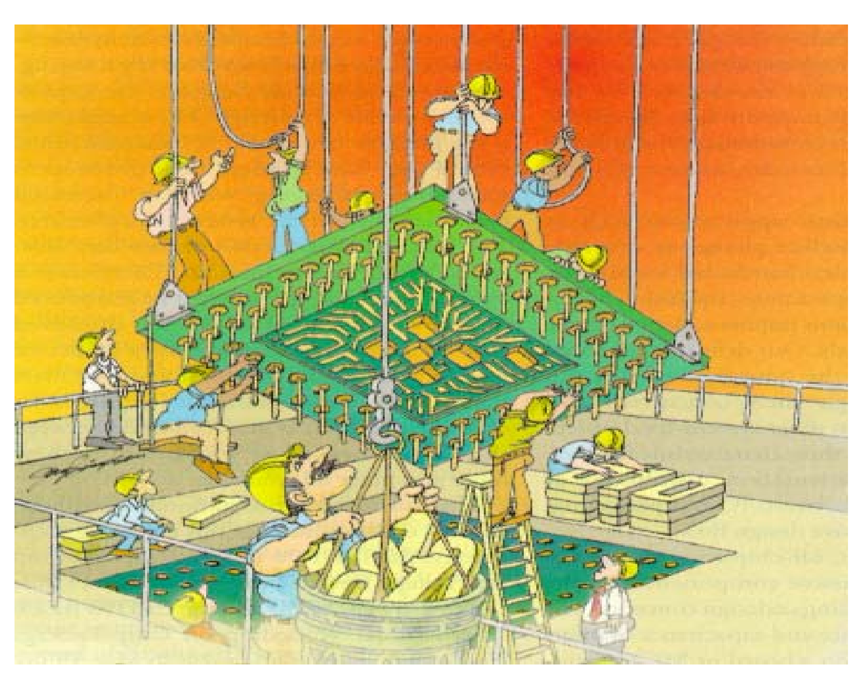
Jorgen Christiansen

Packaging, Testing and good design practices

- Package types
- Cooling
- I/O signals
- How to test IC's
- What not to do: design practices (if time allows)

Requirements to package

- Protect circuit from external environment
- Protect circuit during production of PCB
- Mechanical interface to PCB
- Interface for production testing
- Good signal transfer between chip and PCB
- Good power supply to IC
- Cooling
- Small
- Cheap

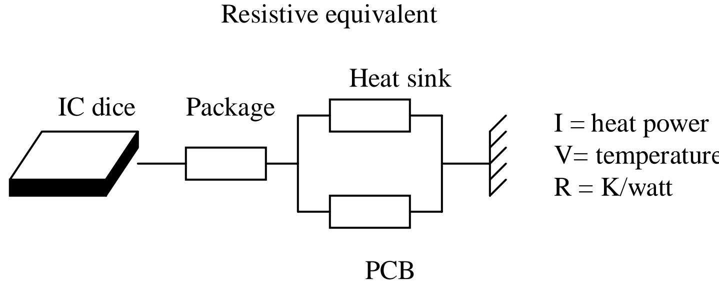


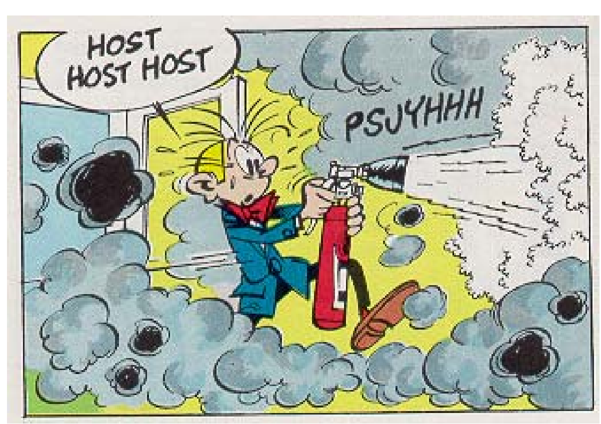
Materials

- Ceramic
  - Good heat conductivity
  - Hermetic
  - Expensive (often more expensive than chip itself !)
- Metal (has been used internally in IBM)
  - Good heat conductivity
  - Hermetic
  - Electrical conductive (must be mixed with other material)
- Plastic
  - Cheap
  - Poor heat conductivity
    Can be improved by incorporating metallic heat plate.

Cooling

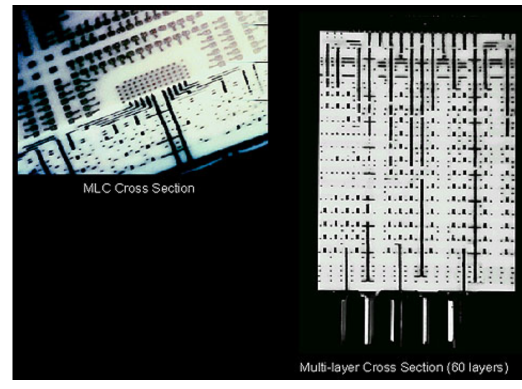
- Package must transport heat from IC to environment
- Heat removed from package by:
  - Air: Natural air flow, Forced air flow improved by mounting heat sink
  - PCB: Transported to PCB by package pins
  - Liquid: Used in large mainframe computers



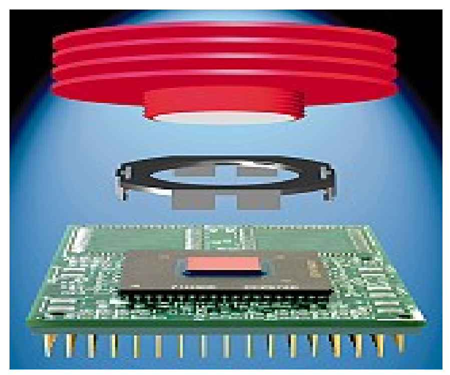


- Package types:
  - Below 1 watt: Plastic
  - Below 5 watt: Standard ceramic
  - Up to 30 watt: Special

60 layers MCM substrate

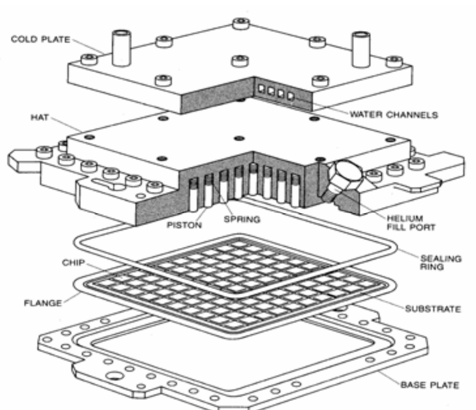


Passive heat sink



Active heat sink

Water cooled mainframe computer



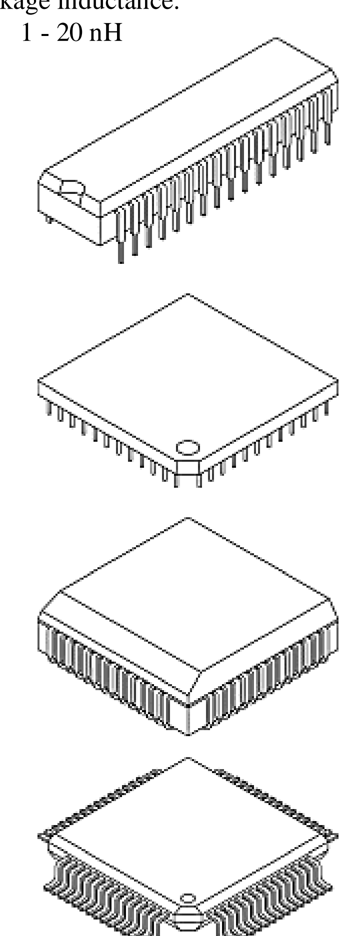
Chip mounting

- Pin through hole
  - Pins traversing PCB
  - Easy manual mounting
  - Problem passing signals between pins on PCB (All layers)
  - Limited density
- Surface Mount Devices (SMD)
  - Small footprint on surface of PCB
  - Special machines required for mounting
  - No blocking of wires on lower PCB layers
  - High density

Traditional packages

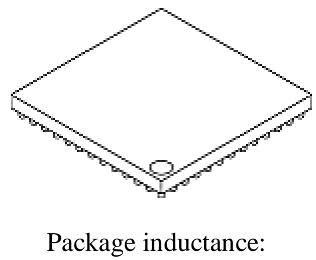
- DIL (Dual In Line)
  - Low pin count
  - Large
- PGA (Pin Grid Array)
  - High pin count (up to 400)
  - Previously used for most CPU's
- PLCC (Plastic leaded chip carrier
  - Limited pin count (max 84)
  - Large
  - Cheap
  - SMD
- QFP (Quarter Flat pack)
  - High pin count (up to 300)
  - small
  - Cheap
  - SMD

Package inductance:
1 - 20 nH



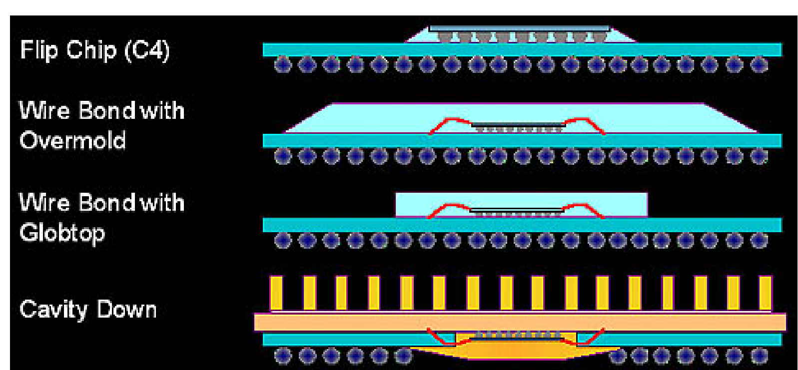
Modern package types

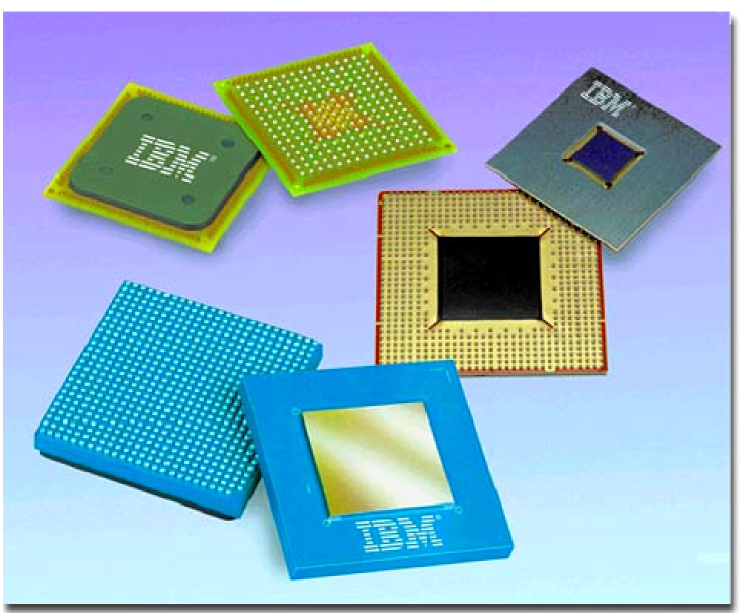
- BGA (Ball Grid Array)
  - Small solder balls to connect to board
  - small
  - High pin count
  - Cheap
  - Low inductance



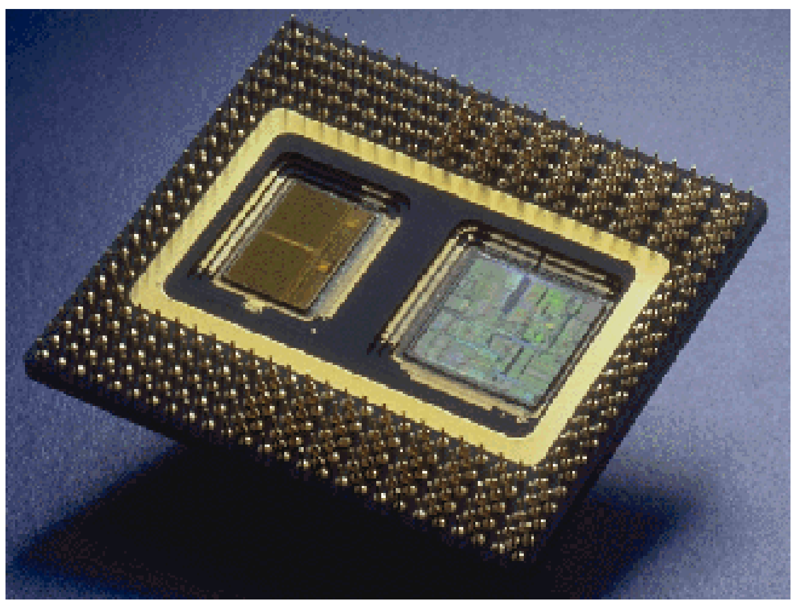
Package inductance:
1 - 5 nH

- CSP (Chip scale Packaging)
  - Similar to BGA
  - Very small packages





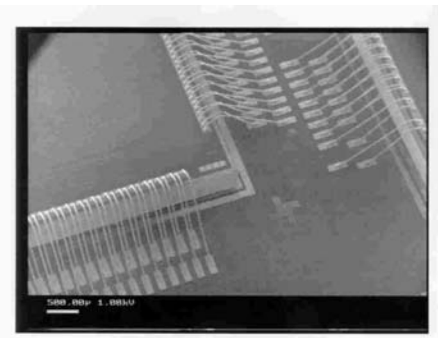
- MCP (Multi Chip Package)
  - Mixing of several technologies in same component
  - Yield improvement by making two chips instead of one

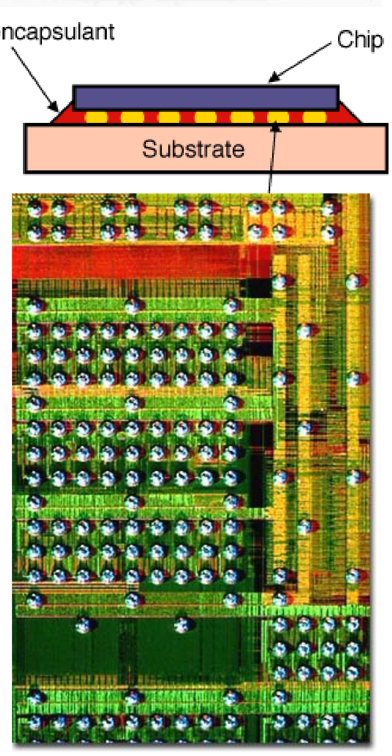


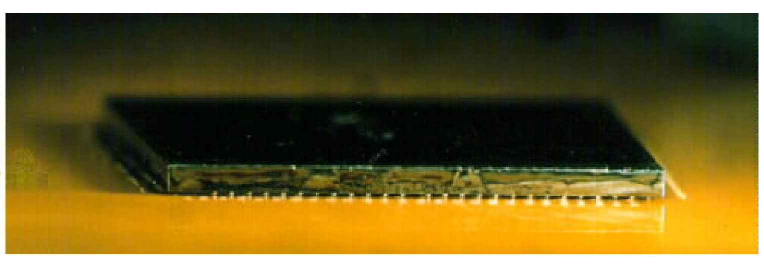
P6: processor + second level cache

Chip to package connection

- Wire bonding
  - Only periphery of chip available for IO connections
  - Mechanical bonding of one pin at a time (sequential)
  - Cooling from back of chip
  - High inductance (~1nH)
- Flip-chip
  - Whole chip area available for IO connections
  - Automatic alignment
  - One step process (parallel)
  - Cooling via balls (front) and back if required
  - Thermal matching between chip and substrate required
  - Low inductance (~0.1nH)

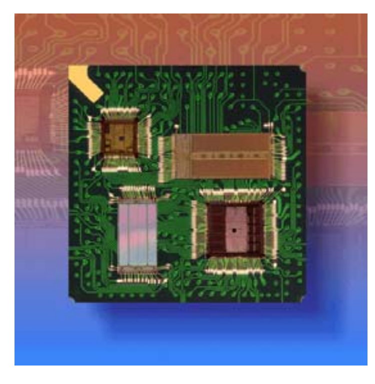
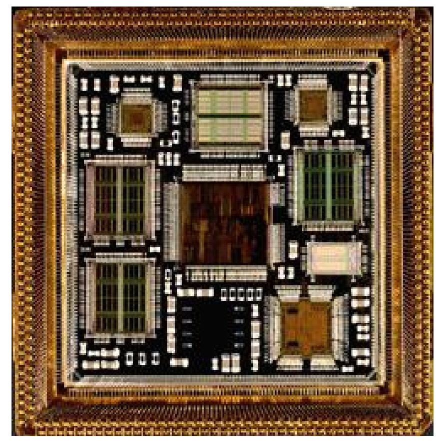
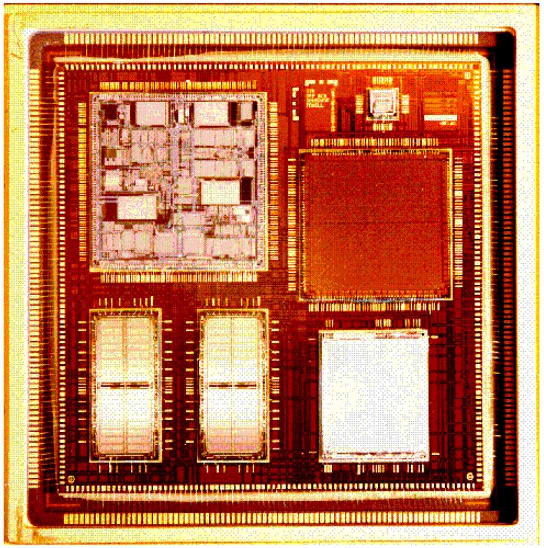




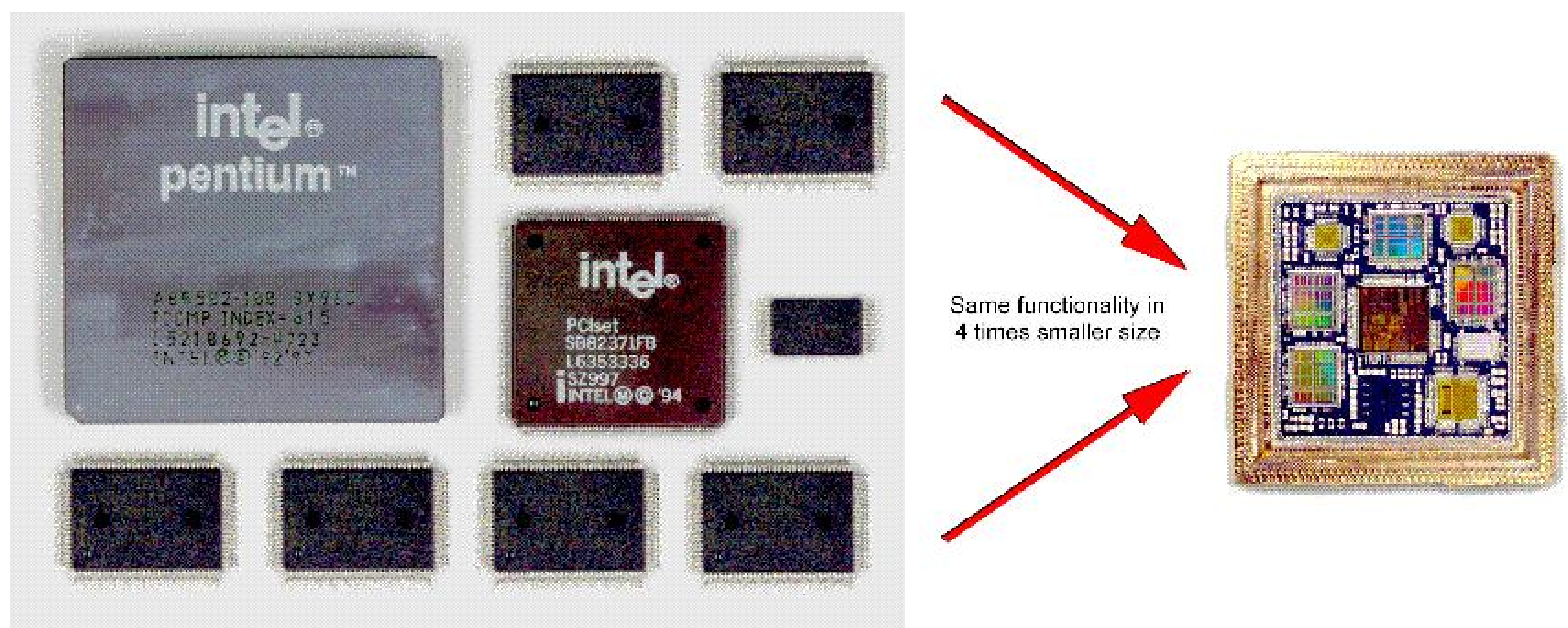


Multiple Chip Module (MCM)

- Increase integration level of system (smaller size)
- Decrease loading of external signals > higher performance
- No packaging of individual chips
- Problems with known good die:
  - Single chip fault coverage: 95%
  - MCM yield with 10 chips: $(0.95)^{10} = 60\%$
- Problems with cooling
- Expensive (OK for military)
- No commercial success

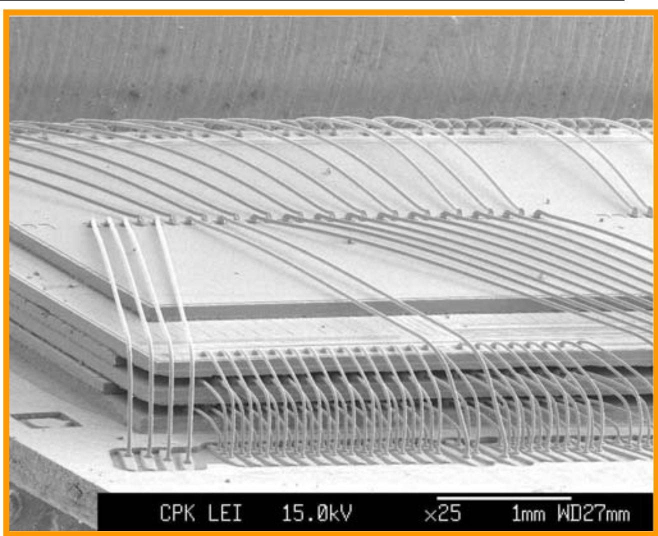
Complete PC in MCM

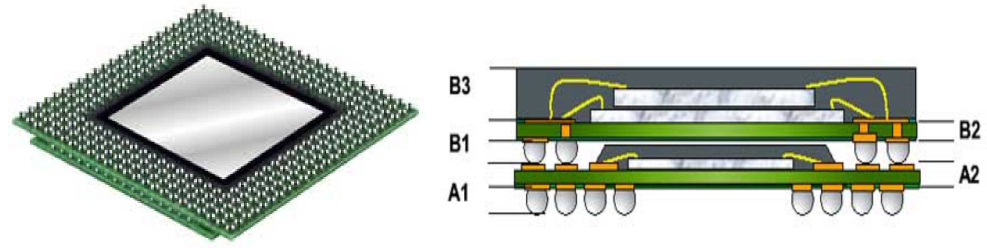


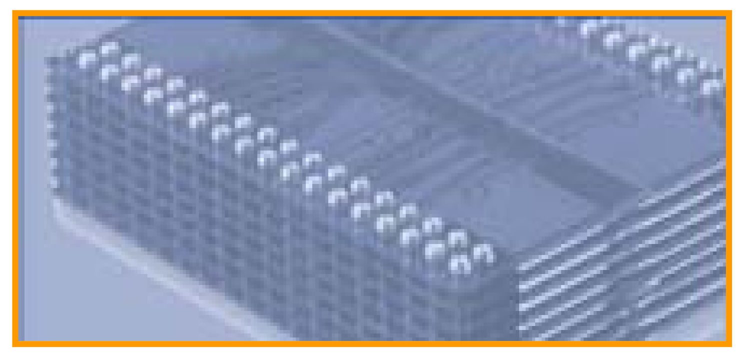
- Now they put all this into a single chip (SOC)

Chip stacking

- Gluing bare chips on top of each other within a package
  - Where it makes sense to put many chips of same kind in very small volume
  - Each chip must have limited power dissipation.
  - Limited pin count per chip or common bus
  - Memories: DRAM, FLASH

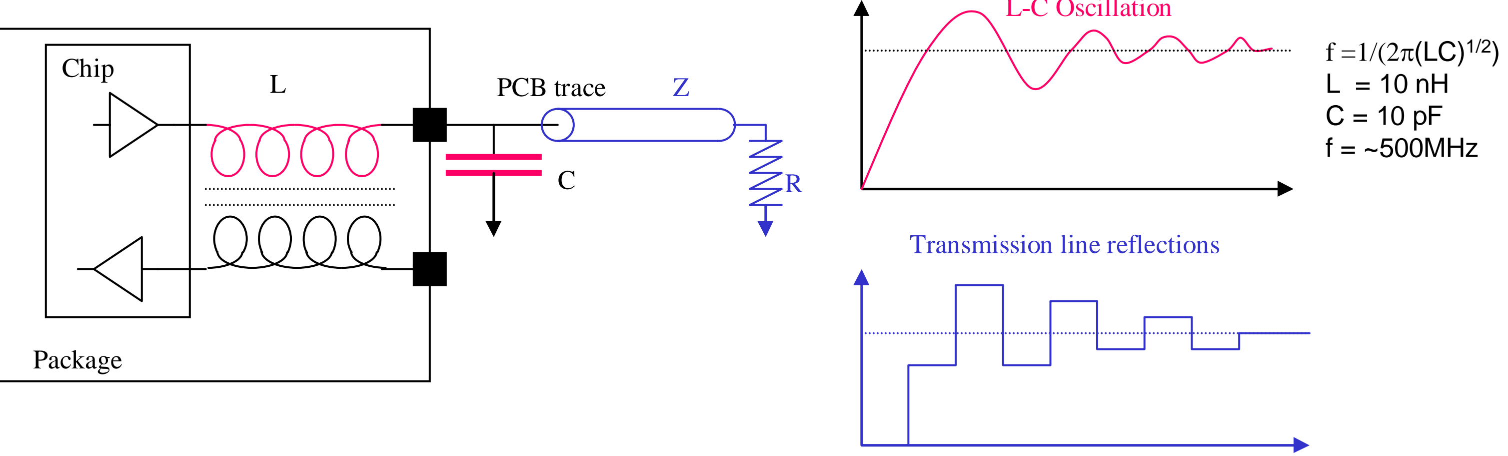






Signal Interface

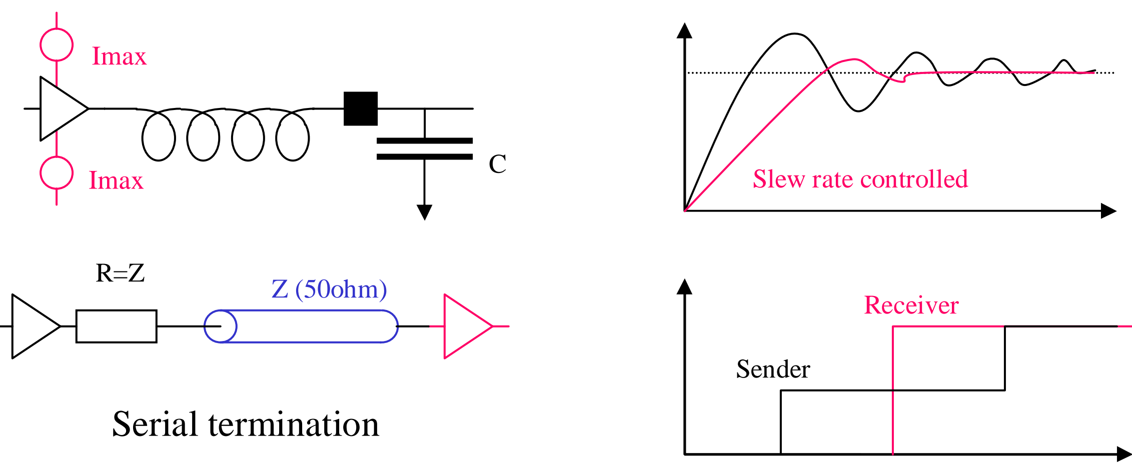
- Transfer of IC signals to PCB
  - Package inductance.
  - PCB wire capacitance.
  - L - C resonator circuit generating oscillations.
  - Transmission line effects may generate reflections
  - Cross-talk via mutual inductance



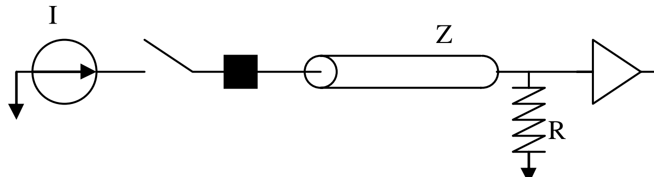
$f = 1/(2\pi(LC)^{1/2})$
L = 10 nH
C = 10 pF
f = ~500MHz

IO signals

- Direct voltage mode
  - Simple driver (Large CMOS inverter)
  - TTL, CMOS, LV-TTL, etc. Problems when Vdd of IC's change.
  - Large current peaks during transitions resulting in large oscillations
- Slew rated controlled
  - Limiting output current during transitions
  - Reduced oscillations
  - (Reduced speed)
- Serial termination
  - Driver must have same impedance as transmission line (or external resistor)
  - Only good for point to point

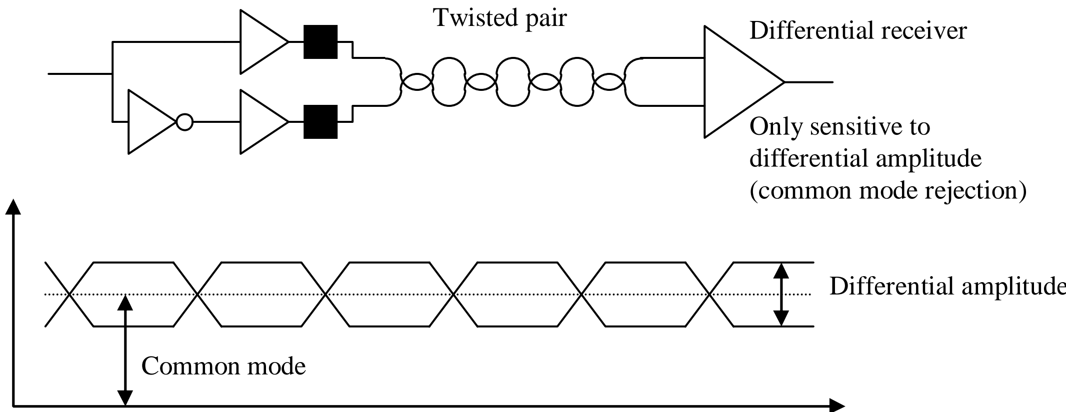


- Current mode
  - Switch current instead of voltage
  - Reduced current surge in power supply of driver
  - Reduced oscillations
  - External resistor to translate into voltage or
    Low impedance measuring current directly
  - Very good to drive transmission lines (similar to ECL)

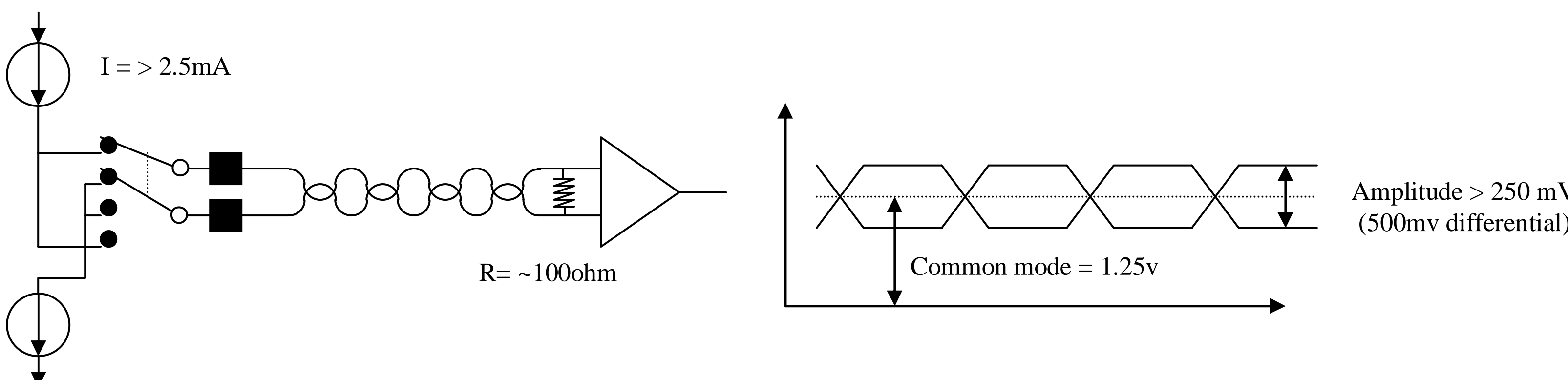


Parallel termination at the end

- Differential
  - Switch two opposite signals: signal and signal inverted
  - Good for twisted pairs
    - Prevents pickup from external noise sources
  - Common mode of signal can be rejected
  - Two pins per signal required
  - High speed

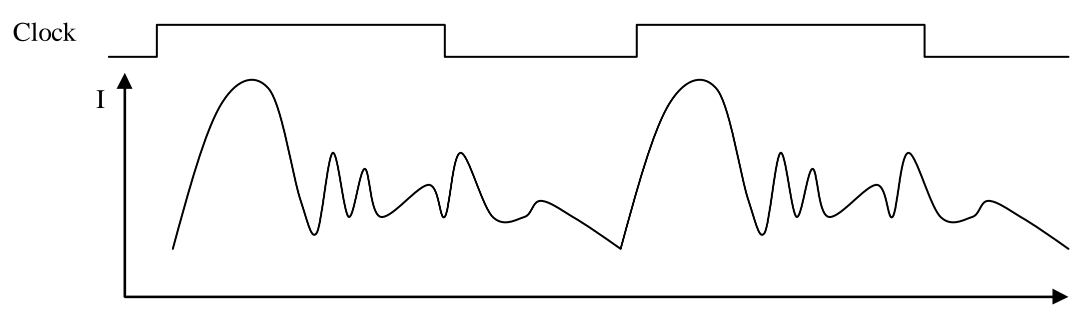


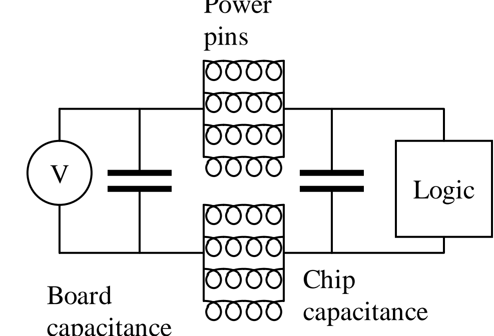
- LVDS (Low Voltage swing Differential signaling)
  - High speed (up to 250 MHz or higher)
  - Low voltage (independent of Vdd of different technologies)
  - Differential (twisted pairs)
  - Current mode
  - Terminated with same impedance as cable
  - Constant current in driver power supply (low noise)



Power supply

- Power supply current to synchronous circuits strongly correlated to clock
- Large current surges when normal CMOS output drivers change state
- Inductance in power supply lines in package.
- 10% - 50% of IC pins dedicated to power to ensure on-chip power with low voltage drop and acceptable noise.
- Modern High end microprocessors needs tens of amperes at a voltage of 1 – 2 volt !.
- IC packages with special power-ground planes and decoupling capacitors
- Decoupling capacitors on chip





Testing: Cost of finding failing chip

LEVEL	FAILURE MECHANISM	PRICE	
Specification	Functionality, Performance Testability, reliability Interoperability	1$	
Design	——— " ———	1000$	100 $
Prototype	Verification, Qualification, Production margins	100.000$	GOLD
Wafer	Yield, speed, noise, gain	1$	
Chip	Cutting, bonding	10$	
(MCM) Module	Soldering, ESD	100$	100 $
(Sub) System	Cables, connectors	1000$	100 $
At customer	Reliability of components, vibrations, corrosion, radiation, high voltage	10.000$	GOLD

Design verification testing

(price per design)

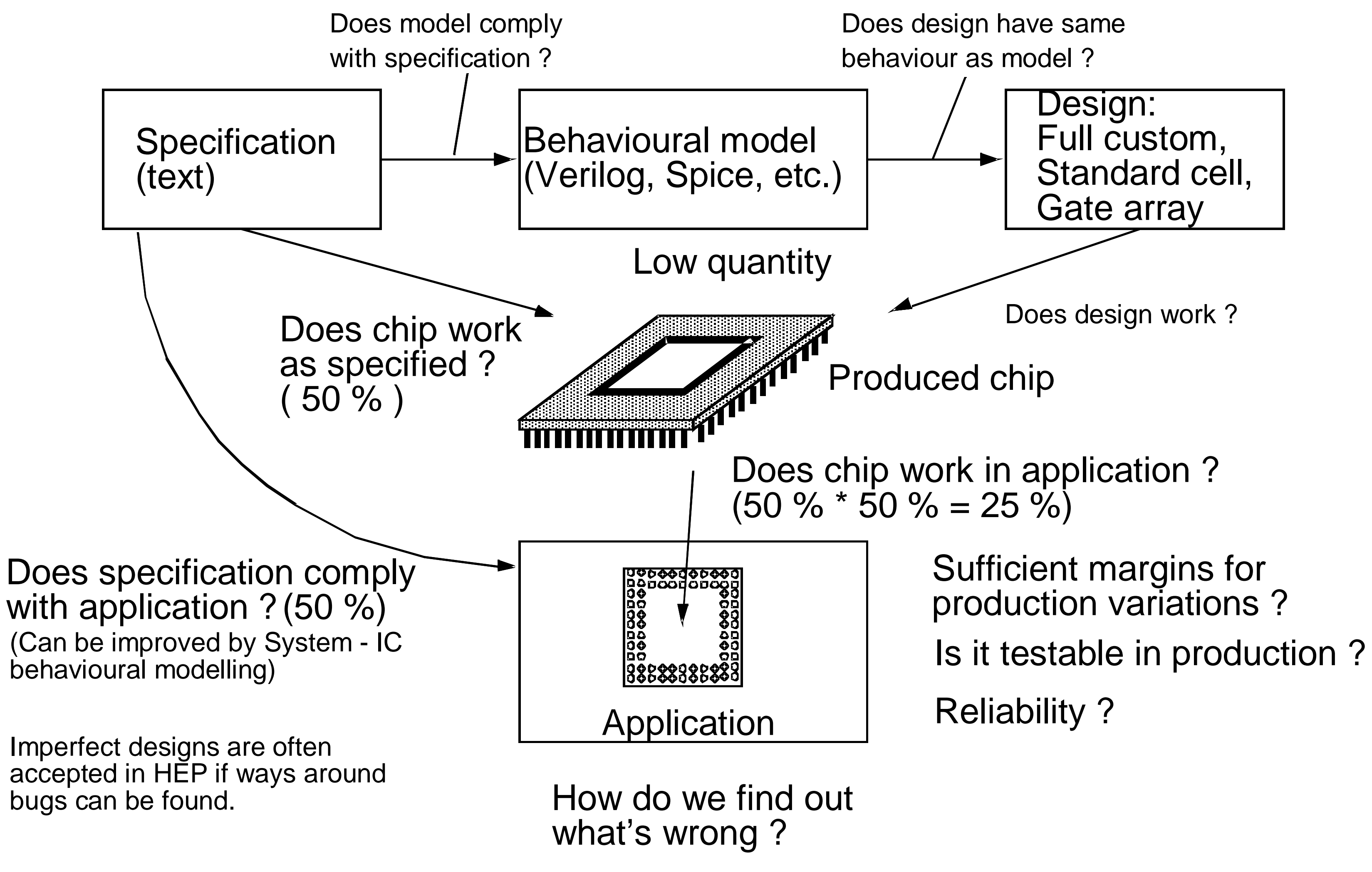
100K$ - ? $
(if not sufficient design verification performed)

Production testing

(price per chip)

Design verification testing

(10- 50% of total development costs)



Production testing

(Production test pattern development 5 - 25 % of development costs)
(Production test 20 - 50% of final chip cost)

Wafer

Bare die

Packaged

MCM

Burn-in ?

Functional test:
fault coverage,
stuck at 0/1

Internal speed test:
clocking speed

Margins ? (noise, measurement accuracy, etc.)

Temperature ?.
Supply voltage ?
External loads ?

External speed test:
setup time,
hold time,
delay

I/O level test:
output levels,
input thresholds

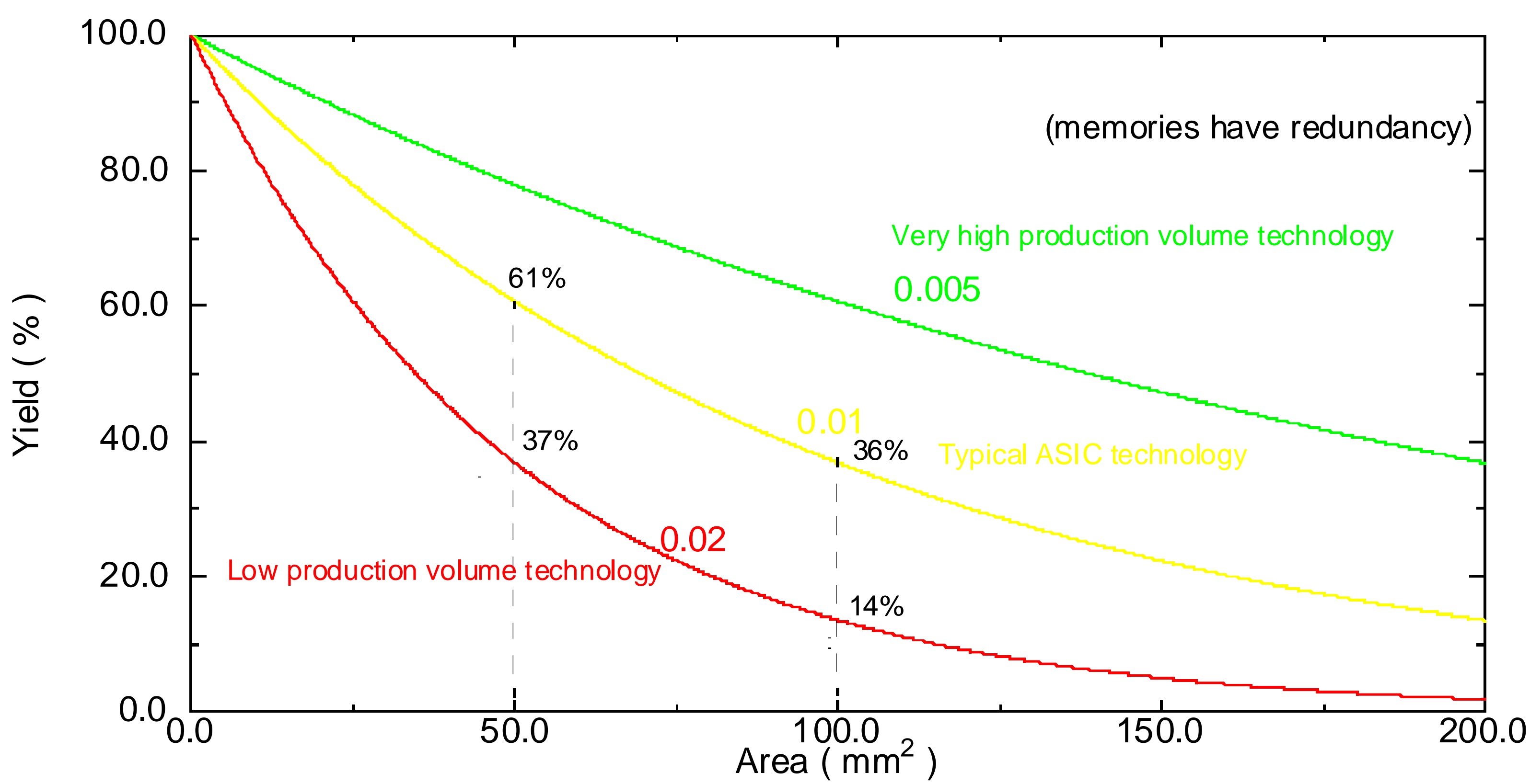
Analog parameters:
gain, noise,
time constants,
precision, etc.

Monitoring of radiation resistance (destructive test)

Production yield

Yield is calculated from defects per mm^2 (= exp(- A * D))

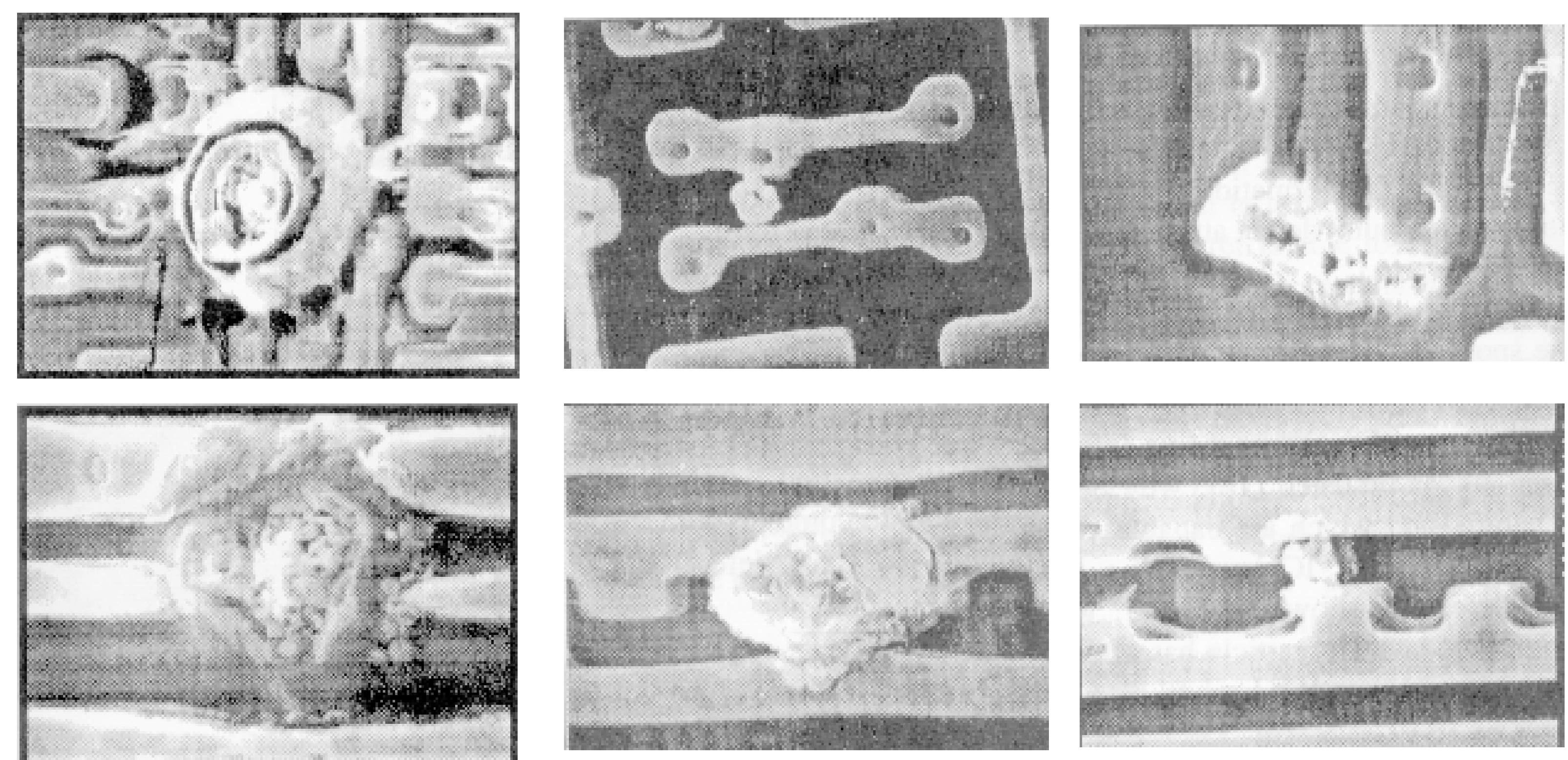
Typical defect density is of the order of 0.005 - 0.02 defects/mm^2



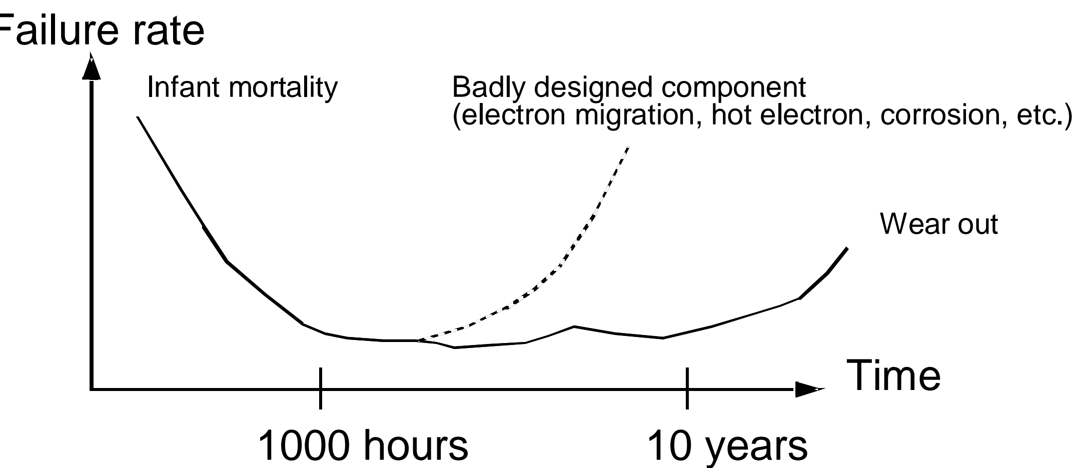
Price of 100 mm^2 chip compared to 50 mm^2 chip: 100 mm^2/50 mm^2 x 0.61/0.37 = 3.4 (D=0.01)

100 mm^2/50 mm^2 x 0.36/0.14 = **5.3** (D= 0.02)

Typical IC faults



Reliability of integrated circuits



Failing parts within first 1000 hours: 0.1 - 1 % (type, package, etc.)

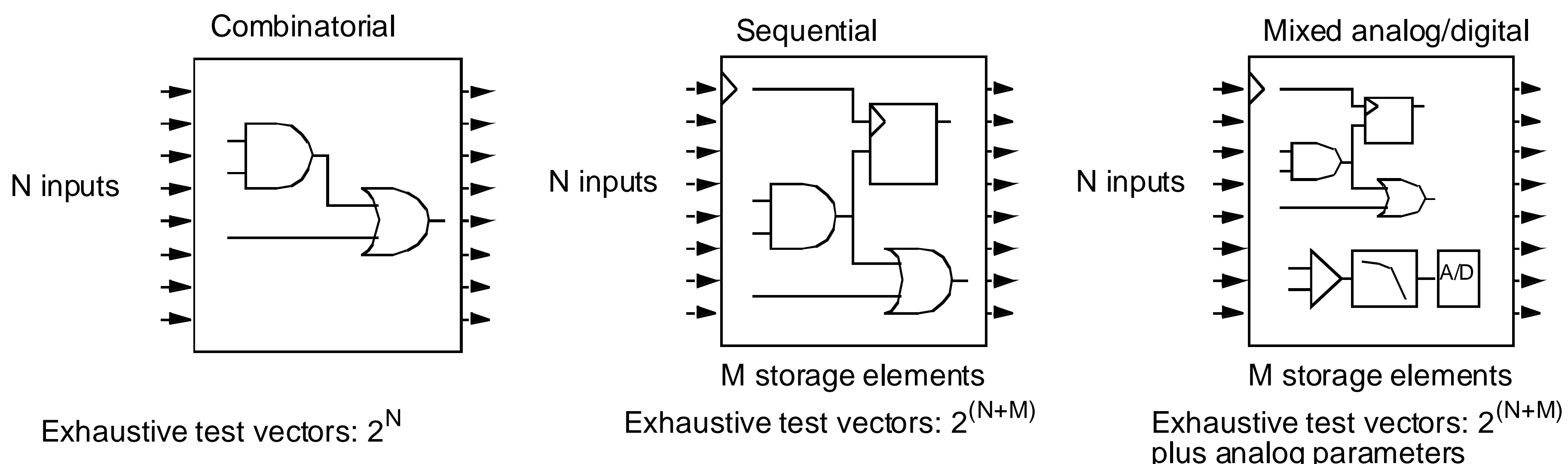
Burn-in testing : Heating up chips to 125 deg. accelerates 1000 hours period to approx. 24 hours.

Static: power supply connected.
Dynamic: Power + stimulation patterns.
Functional test: Power + stimulation patterns + test.

Temperature cycling: Continuous temperature cycling of chips to provoke temperature gradient induced faults. (Non matching thermal expansion coefficients).

Electrical stress: Operation at elevated supply voltage

What to test



100 Mhz tester:
N=32 ; test time = 40 seconds.
N=64 ; test time = 6.000 years

Knowledge about topology of circuit must be used to reduce number of test vectors so they can be generated by tester (tester memory: 10K - 10M).

Analog and digital stimuli must be generated from a tightly synchronised system.

Basic testing terms

CONTROLABILITY: The ease of controlling the state of a node in the circuit.

OBSERVABILITY: The ease of observing the state of a node in the circuit

Example: 4 bit counter with clear

Control of q3:

Set low: perform clear = 1 vector

Set high : perform clear + count to 1000B = 9 vectors

clr q3 q2 q1 q0

Testing a node in a circuit

A: Apply sequence of test vectors to circuit which sets node to demanded state.

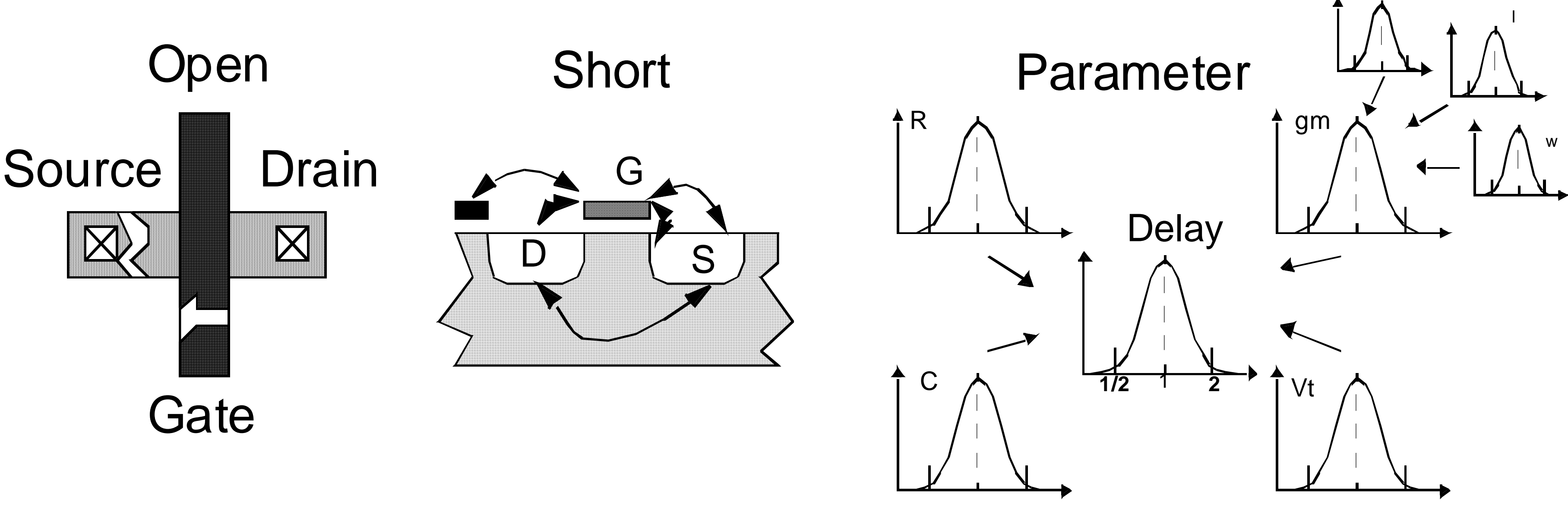
B: Apply sequence of test vectors to circuit which enables state of node to be observed.

C: The observing test vector sequence must not change state of node.

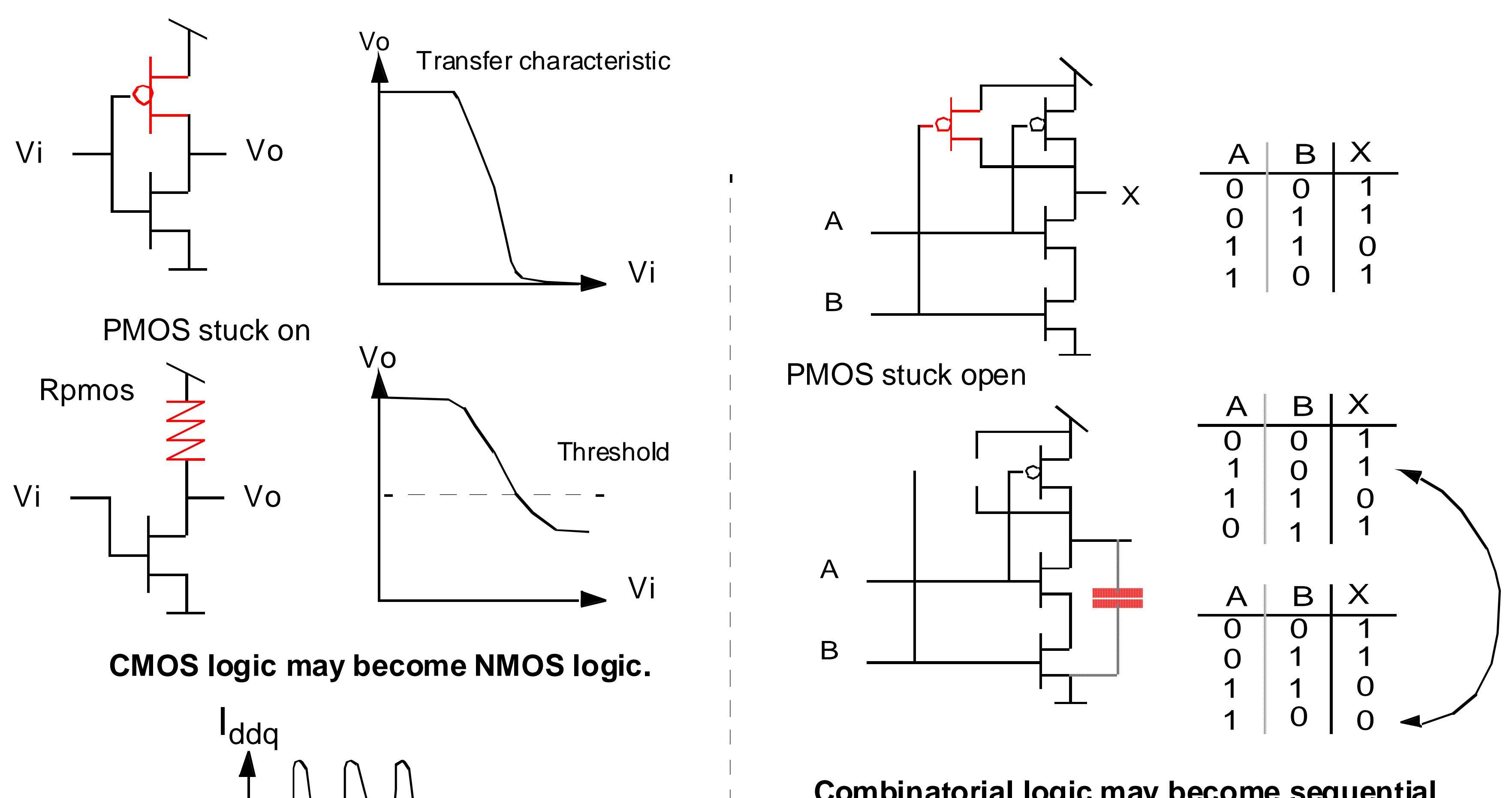
Fault models

Fault types: Functional.
Timing.

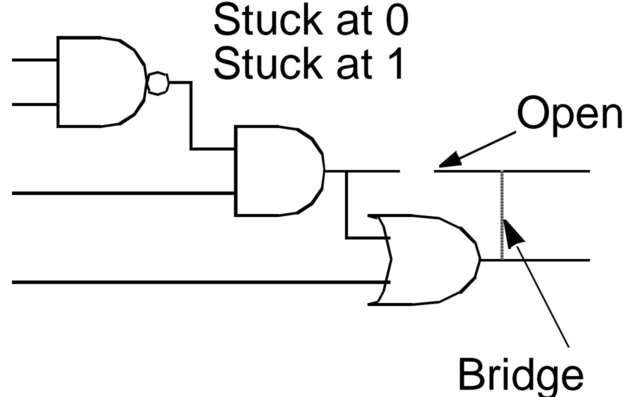
Abstraction level: Transistor. (layout)
Gate. (netlist)
Macro (functional blocks).



Problematic faults at transistor level



Gate level (stuck at 0/1model)

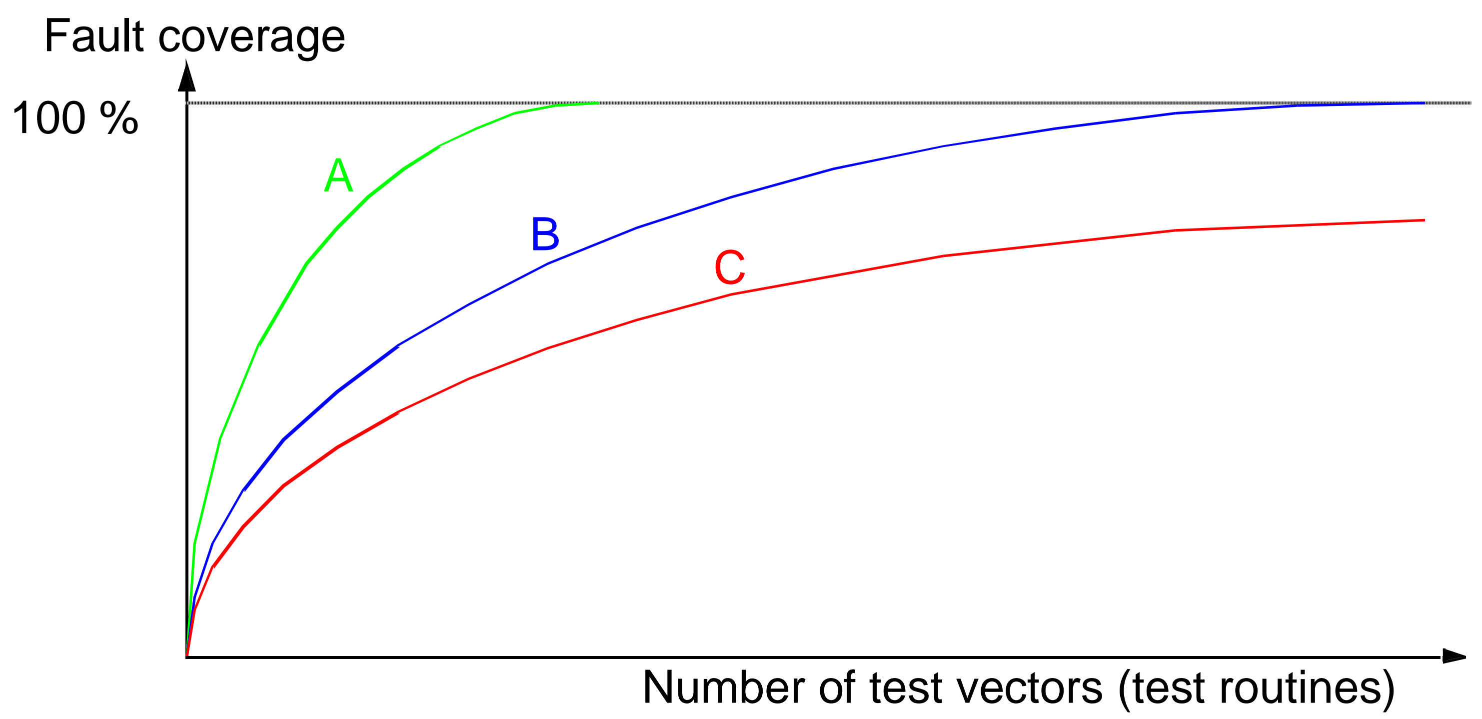


The gate level stuck at 0/1 is the dominantly used fault model for VLSI circuits, because of its simplicity.

Fault coverage calculated by fault simulation are always calculated using the stuck at 0/1 model. Other more complicated fault models are to compute intensive for VLSI designs.

$$\text{Fault coverage} = \frac{\text{Number of faults detected by test pattern}}{\text{Total number of possible stuck at faults in circuit}}$$

Testability



A: Design made with testability in mind. (~1 test vector per gate)

B: Design made without testability in mind but good fault coverage obtained by large effort in making test vectors.

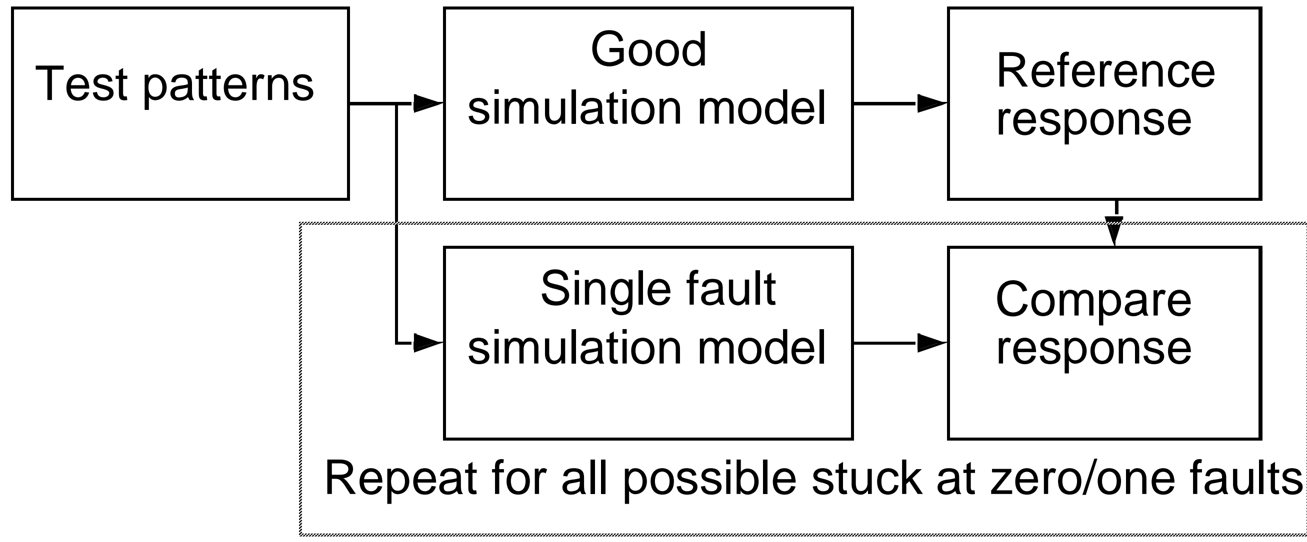
C: Design very difficult to test even using large effort in test vector generation.

Generation of test patterns

- Test vectors made by test engineer based on functional description and schematics. Proprietary test vector languages used to drive tester. (over the wall)
- Test vectors made by design engineer on CAE system. Subset of test patterns may be taken from design verification simulations.
- Generated by Automatic Test Pattern Generators (ATPG). Requires internal scan path
- Pseudo random generated test patterns.
- Fault simulation calculates fault coverage.

Fault simulation

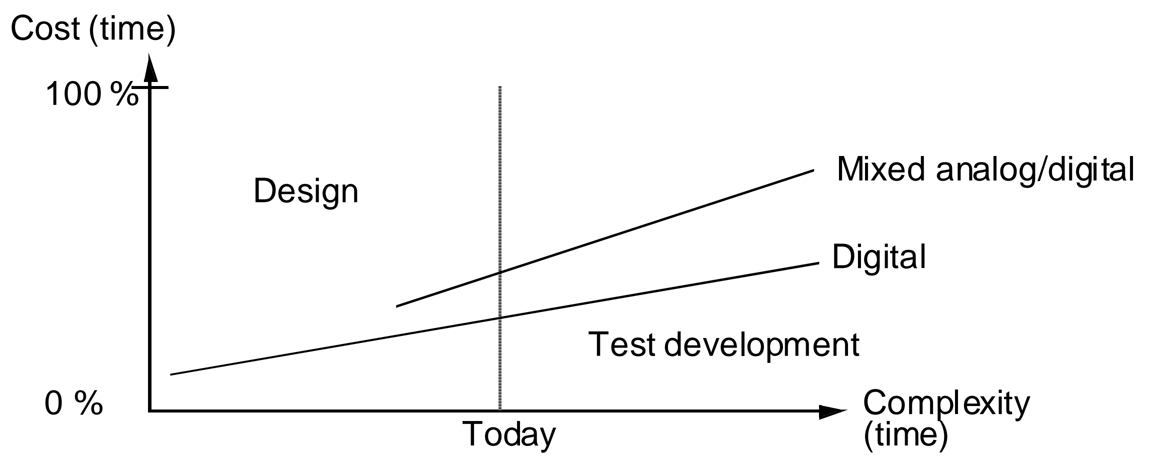
Fault coverage found by fault simulations



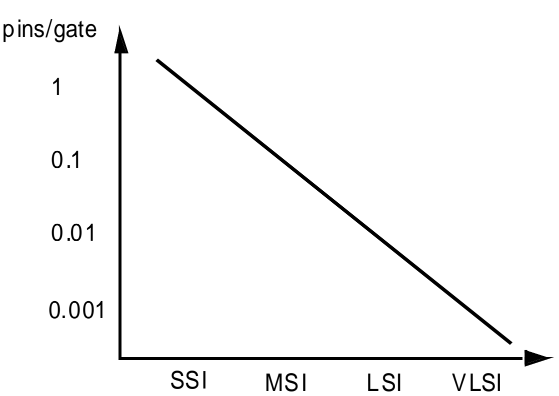
Requires long simulation times !.

Toggle test (counts how many times each node has changed) can be used to get a first impression of fault coverage.

Test development with increased complexity



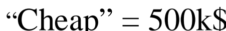
Testability is decreasing drastically with increased integration level

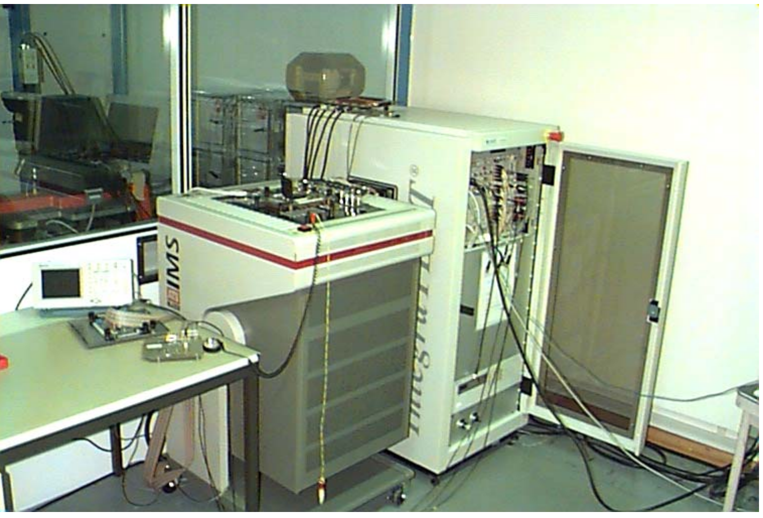


IC testers

High speed high pin count VLSI testers are very expensive and complicated machines. (500 k$ - 10 M$).

Vector speed: 100 - 1000MHz,
Vector depth: 32k - 1G
Time resolution: 100ps - 10ps
Pin count: 100 - 1024



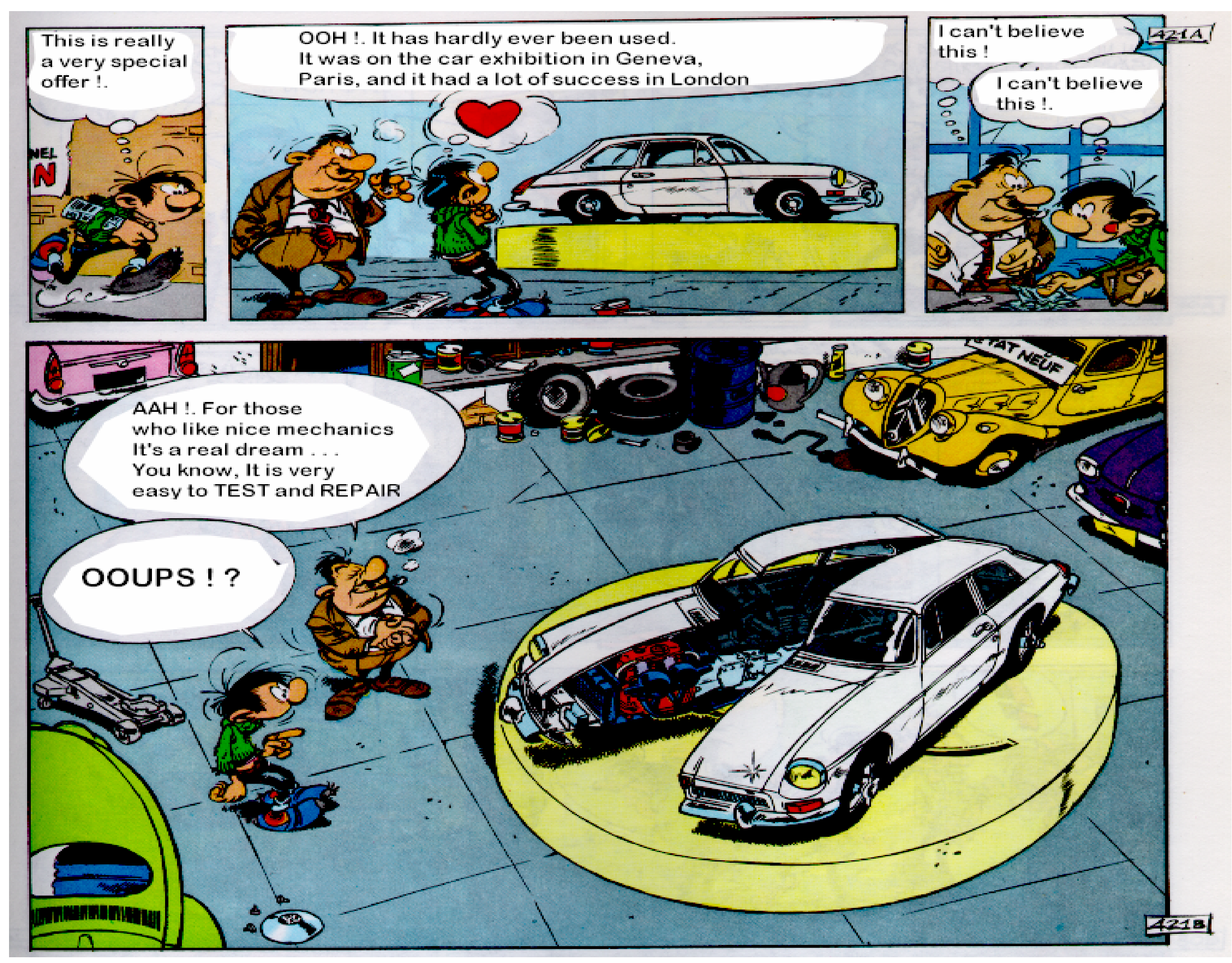


+ Measurements of DC characteristics

No standard Mixed signal tester exists (mixed signal tests are always special)

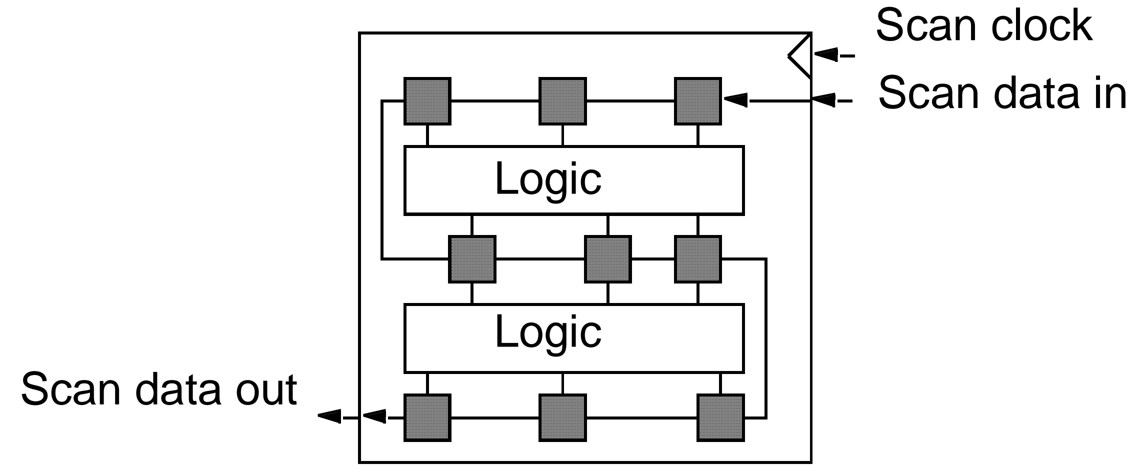
Testers must be faster than current IC technology !.

Scan Path testing



Scan path testing

Improving controllability/observability by enabling all storage nodes to be controlled/observed via serial scan path.



Test principle:

1: Enable scan mode and scan in control data.
2: Disable scan mode and clock chip one cycle.
3: Enable scan mode and scan out observing data.

Generation of test vectors: With the high controllability/observability the test vectors can be generated automatically with a ATPG program.

JTAG standard

IEEE 1149 standard.

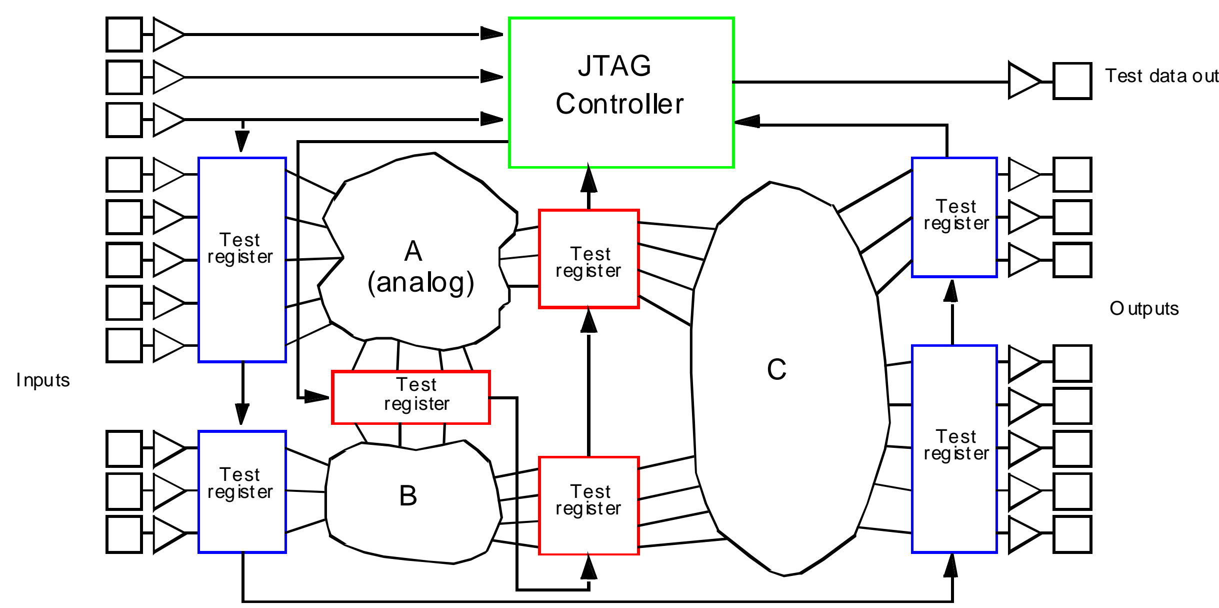
Boundary scan to test interconnect between chips.

Internal scan to test chip.

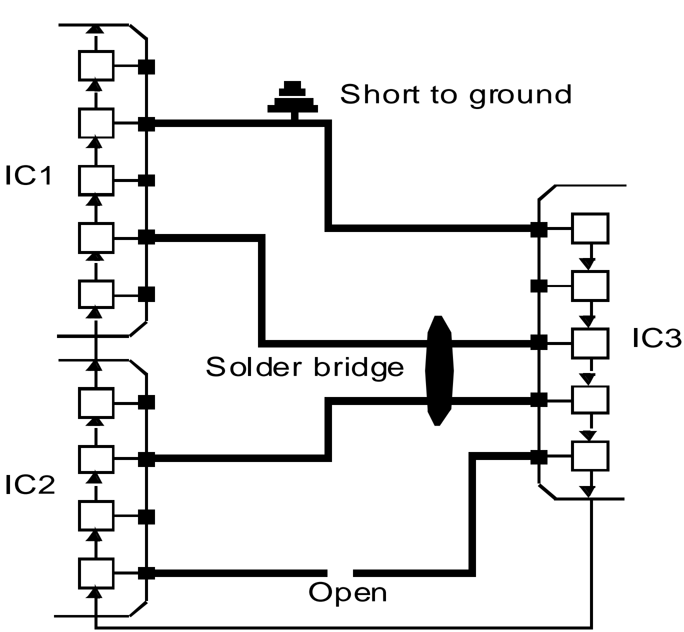
Control and status of built in self test.

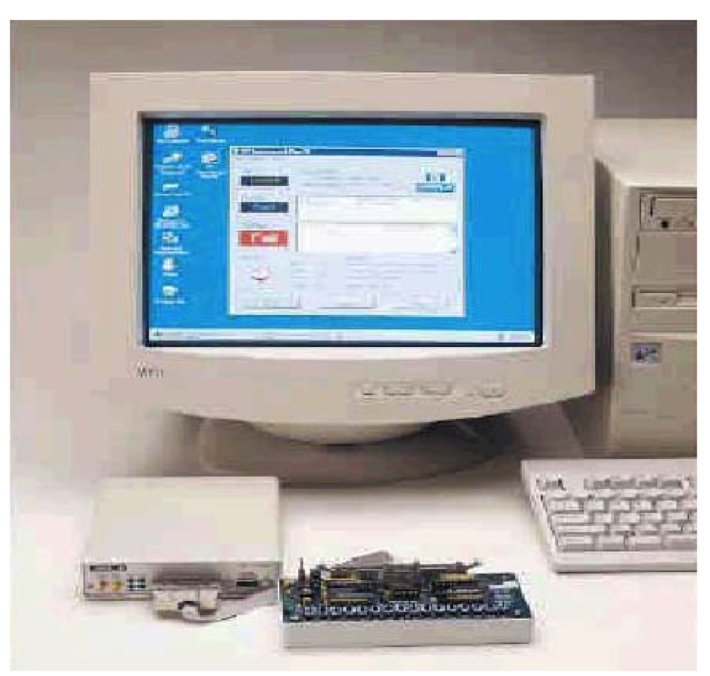
Chip ID

Many commercial chips with JTAG standard implemented:
 Processors, FPGA, etc.



- Boundary scan enables test of digital board connections.
  - (automatic test generation from netlist of board)
- JTAG ID enables verification of correct component type.
- Enables access to internal test features in components.
- Testing can be also be performed in-situ.
- Small and “cheap” test system required.
- Many commercial IC’s now have JTAG (Processors, FPGA’s, etc.)

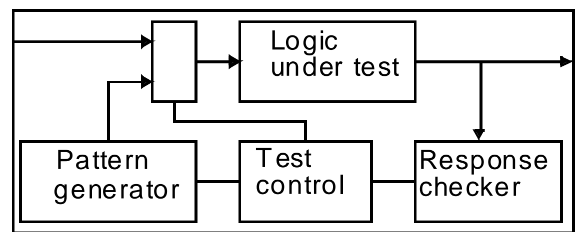




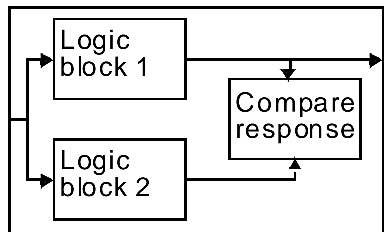
Built In Self Test (BIST)

Different schemes of built in (self) test

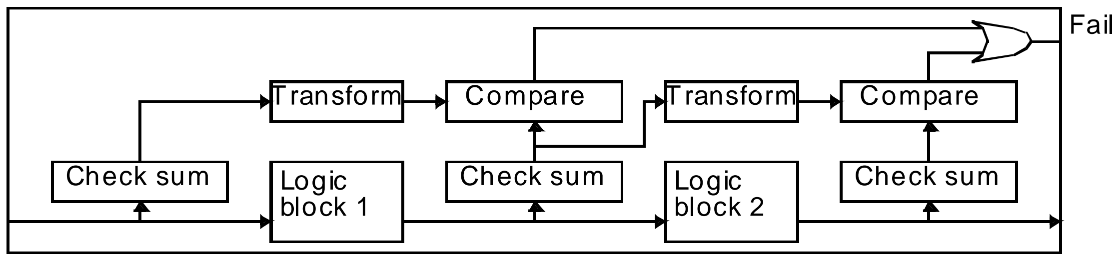
Include test pattern generator and response check on chip



Make self checking during operation by duplicating all functions



Generate local check sums and check with transformation of previous check sum



Hardware overhead !!

All commercial high end IC have extensive built in test features, but they are not documented for normal users as they do not need to know for normal use and it is a part of the "secrets" of how to produce high quality ICs

Good design practices
(If time allows)

Purpose of good design practices

- Improve chance of chip working first time
- Reduce (total) design time
- Reduce development cost
- Improved reliability
- Improved production yield.
- Follow vendor rules to get standard guarantees.
- Some performance reduction may have to be accepted
- (Be smart but not to smart)

Choice of technology

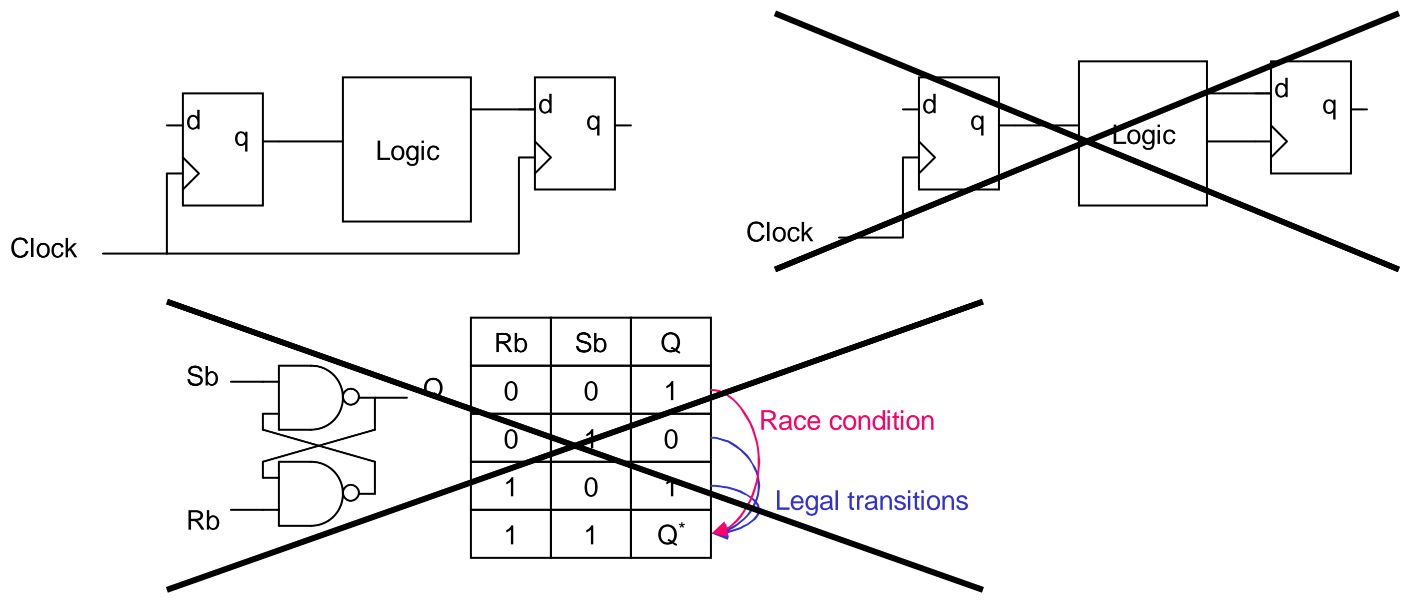
- Performance (speed, complexity)
- Design tools : Synthesis, P&R, etc.
  - Cost of required tools
  - Support for tools from which CAE tool supplier
- Libraries (gates, adders, RAM, ROM, PLL's, PCI, ADC, etc.)
- Development costs
  - Full engineering run: NRE (several hundred thousand dollars)
  - Multi Project Wafer (MPW)
- Life time of technology
  - Modern CMOS only have a life time of ~5 years
- Production
  - Price as function of volume
  - Production testing

Well planned design hierarchy

- The hierarchy of a design is the base for the whole design process.
  - Define logical functional blocks
  - Minimize connections between branches of hierarchy
  - Keep in mind that Hierarchy is going to be used for synthesis, simulation, Place & route, testing, etc.
- Define architecture in a top-down approach
- Evaluate implementation and performance of critical blocks to determine if architecture must be changed.

Synchronous design

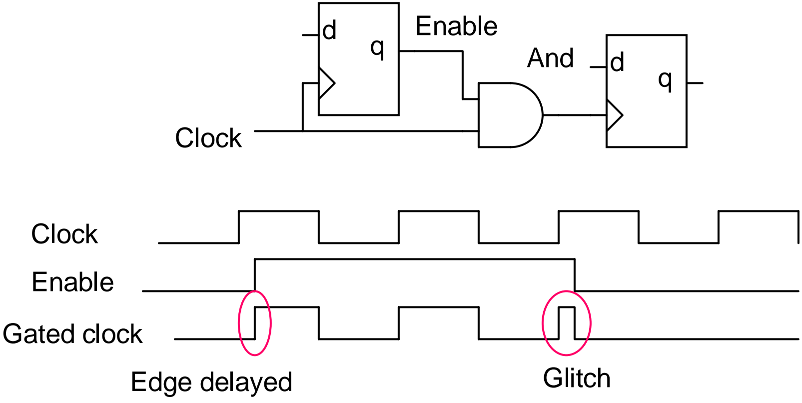
- All flip-flops clocked with same clock.
- Only use clocked flip-flops
  - no RS latches, cross coupled gates, J-K flip-flops, etc.
- No asynchronous state machines
- No self-timed circuits



Rb	Sb	Q
0	0	1
0	1	0
1	0	1
1	1	Q*

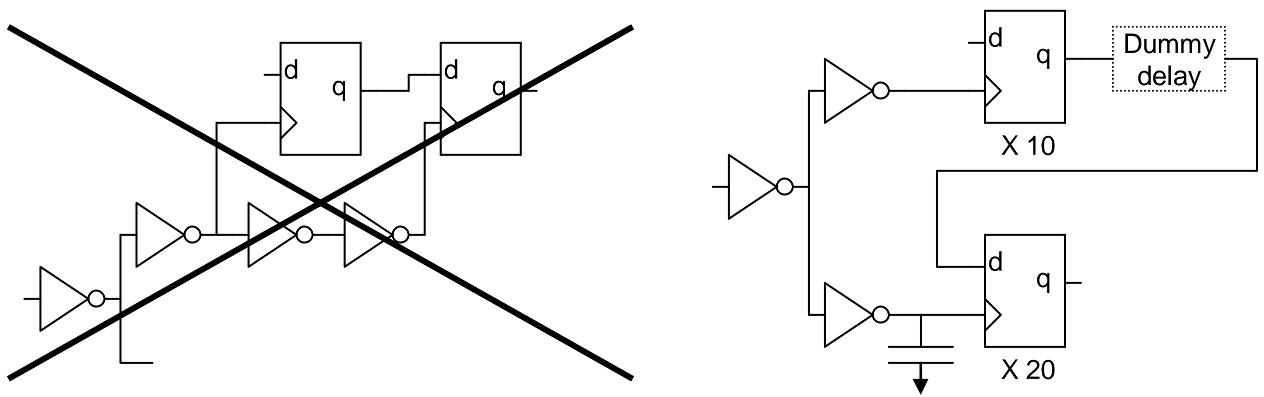
Clock gating

- Clock gating has the potential of significant power savings disabling clocks to functions not active.
- Clock gating introduces a significant risk of malfunctions caused by glitches when enabling/disabling clock



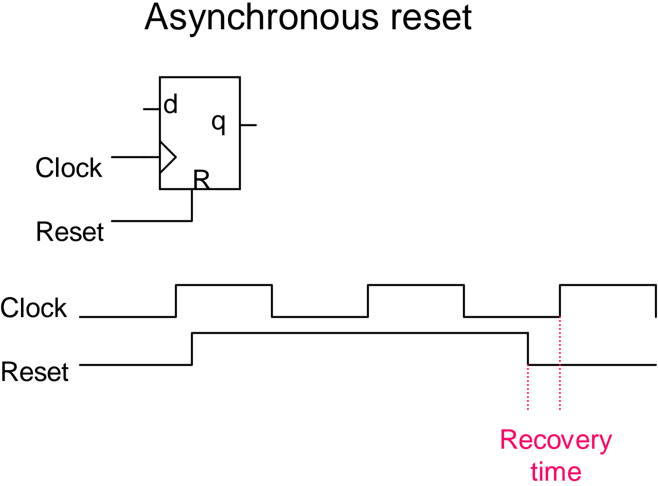
Clock distribution

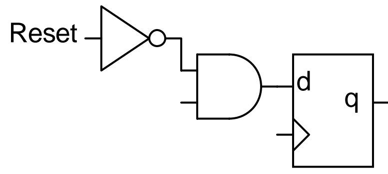
- Even in synchronous designs, race conditions can occur if clock not properly distributed
  - Flip-flops have set-up and hold time restrictions
  - Clocks may not arrive at same time to different flip-flops.
  - Especially critical for shift registers where no logic delays exists between neighbor flip-flops.
  - Clock distribution must be very - very carefully designed and dummy logic may be needed between flip-flops.



Resets

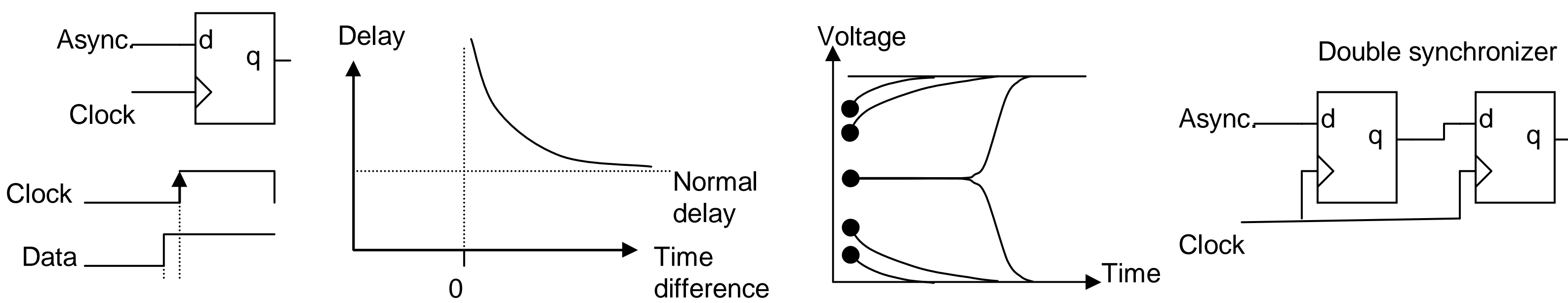
- Asynchronous resets must still be synchronized to clock to insure correct start when reset released
- Synchronous reset made by simple gating of input





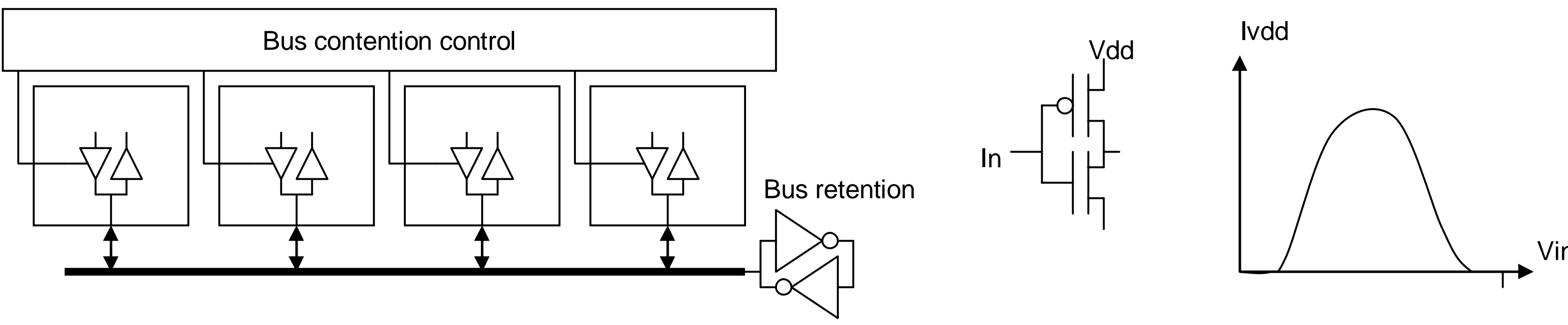
Interface to asynchronous world

- It is in many applications necessary to interface to circuits not running with the same clock.
  - Natural signals are asynchronous
  - Signals between different systems
  - Many chips today uses special internal clocks (e.g.. X 2)
- Asynchronous signals must be synchronized
  - Synchronizers are sensitive to meta-stability
  - Use double or triple synchronizers



On-chip data busses

- Data busses are often required to exchange data between many functional units.
  - Insure that only one driver actively driving bus
    - Also before chip have been properly initialized
    - Bus drivers are often power full and a bus contention may be destructive.
  - Insure that bus is never left in a tri-state state.
    - A floating bus may result in significant short circuit currents in receivers
      - Always have one source driving the bus
      - Use special bus retention generators.



Mixed signal designs

- Extreme care must be taken in mixed analog - digital integrated circuits to limit coupling to the sensitive analog part.
  - Separate power supplies for analog and digital
    - Best powering scheme for sensitive mixed signal designs depends strongly on used technology:
      - High conductive substrate
      - Low conductive substrate
      - Silicon on Insulator (SOI)
  - Guard ring connected to ground around analog blocks
    Efficiency of this depends a lot on substrate type.
  - Separate test of analog and digital (scan path)
  - Use differential analog circuits to reject common mode noise
    - If not using differential analog one is most likely in trouble
  - Be careful with digital outputs which may inject noise into analog part (use if possible differential outputs)
- Difficult but can be done

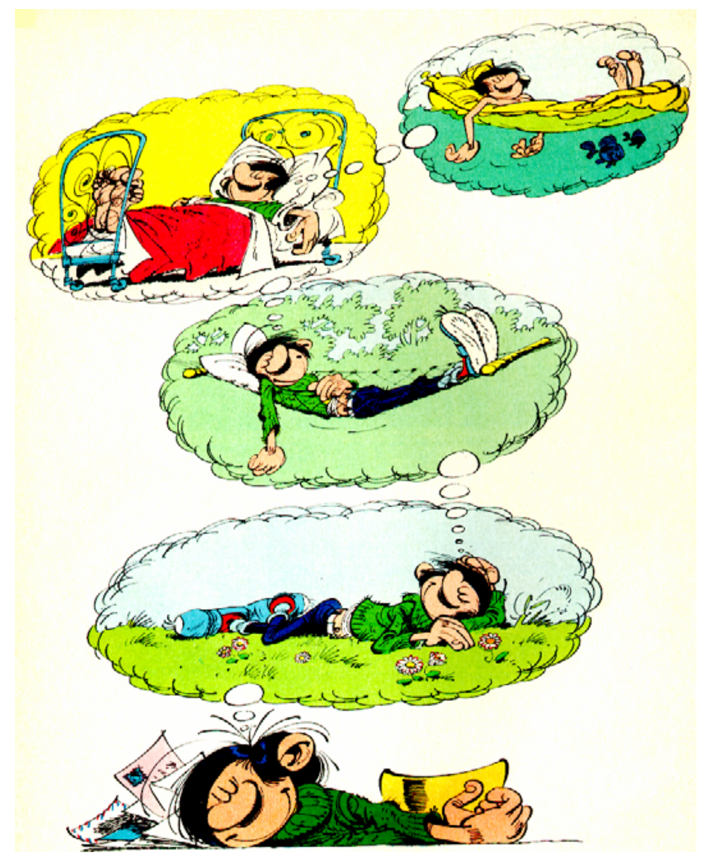
Simulation

- Simulation is the most important tool to Ensure correct behavior of IC.
  - Circuit must be simulated in all possible operating modes
  - Digital simulator output should not only be checked by looking at waveforms
  - Circuit must be simulated under all process and operating conditions (corner parameters)
    - Best case: -20 deg. , good process, Vdd + 10% x ~0.5
    - Typical: 20 deg., typical process, Vdd x 1.0
    - Worst case: 100 deg., bad process, Vdd - 10% x ~2.0
    - Worst N - best P: NMOS bad process, PMOS good process (analog)
    - Best N - worst P: NMOS good process, PMOS bad process (analog)
    - Plus many other combinations of different device parameters (which combination is the worst for my circuit ?)
- IC designers spend most of their time simulating and writing simulation environments.

Testing

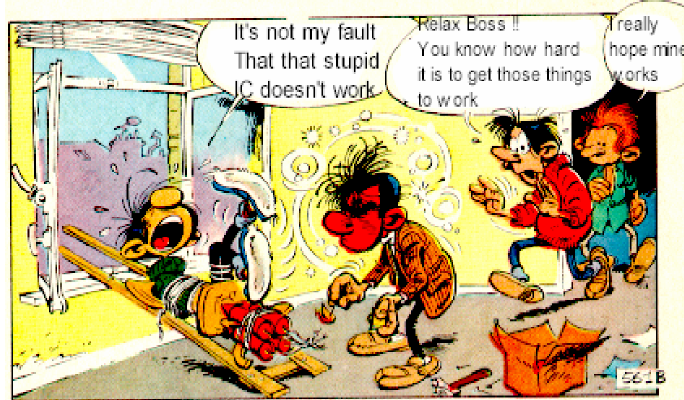
- One can “never” put to much test facilities in chips.
- Put scan path where ever possible.
- Have special test outputs which can be used for monitoring of critical circuits.
- Put internal test pads on special tricky analog circuits.
- If in doubt about critical parameters of design make it programmable if possible.
- Do not forget about production testing.
- Do not make a redesign before problems with current version well understood.
- Most designs needs some kind of redesign.

If you make IC design like this



You may end up like this

Or like this



When something is wrong it is very hard to find the exact cause of the problem.
Design changes are expensive and introduces significant delays