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Future Trends

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These lecture notes are intended only for distribution to participants

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Future trends
Where is all this leading ?

Figures and pictures “stolen” from multiple web sites, conference papers and from my CERN colleagues (Allesandro Marchioro)

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SIA CMOS Roadmap (from 1997, old)

	1997	**1999**	**2001**	**2003**	**2006**	**2009**	**2012**
Technology							
Technology	.25 µm	.18 µm	.15 µm	.13 µm	**100 nm**	70 nm	50 nm
Gate Delay Metric *CV/I* (7)	16-17 ps	12-13 ps	10-12 ps	9-10 ps	7 ps	4-5 ps	3-4 ps
Overall Characteristics							
Logic transistor density	3.7 M/cm^2	6.2 M/cm^2	10 M/cm^2	18 M/cm^2	39 M/cm^2	84 M/cm^2	180 M/cm^2
DRAM size	256M	1G	1G	4G	16G	64G	256G
DRAM IC size	170 mm^2	240 mm^2	270 mm^2	340 mm^2	480 mm^2	670 mm^2	950 mm^2
MPU chip size	300 mm^2	340 mm^2	385 mm^2	430 mm^2	520 mm^2	620 mm^2	750 mm^2
MPU pin count	800	1000	1200	1500	2000	2600	3600
MPU clock frequency	750 MHz	1.2 GHz	1.4 GHz	1.6 GHz	**2.0 GHz**	2.5 GHz	3 GHz
ASIC clock frequency	300 MHz	500 MHz	600 MHz	700 MHz	900 MHz	1.2GHz	1.5GHz
Power supply voltage	1.8-2.5V	1.5-1.8V	1.2-1.5V	1.2-1.5V	.9-1.2V	.6-.9V	.5-.6V
MPU high power	70 W	90 W	110 W	130 W	160 W	170 W	175 W
MPU low power	1.2W	1.4W	1.7W	2W	2.4W	2.8W	3.3W

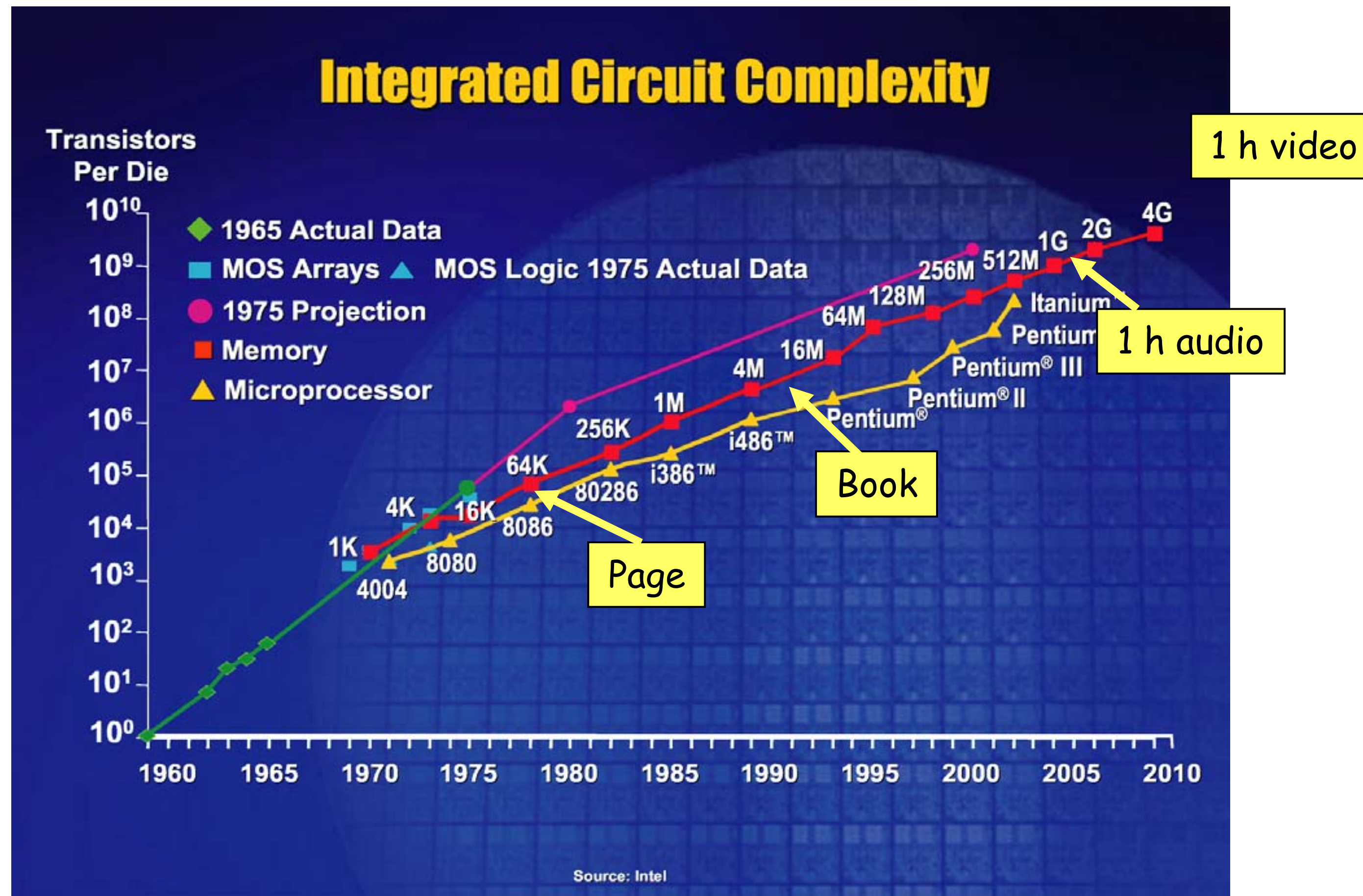
Notice that the predictions made in 97 (considered to be quite aggressive at that time) has been overtaken.
We today have MPU’s at 3 GHz in 65nm technology available in the local supermarket

SIA CMOS Roadmap (from 2004)

	2004	2007	2010	2013	2016
Technology Node [nm]	90	65	45	32	22
Transistor count [Mtr]			1500	3092	6184
Transistor Density [Mtr/cm2]	77	154	309	617	1235
Chip Size [mm^2]	140				280
Clock freq [GHz]	3		15		53
Vdd	1.2	1.1	1.0	0.9	0.7
Signal IO Pads	512	1024	1024	1024	1024
Power Pads	1024				2048

The current tendency in micro-processors is NOT to increase clock frequency but to have multiple cores per chip to get maximum CPU power at lowest power.
Solving cooling problems.
Low power for mobile applications.
Handling multi GHz across large chips very difficult (and wire delays increasing)
Large CPU's getting too complicated (multi core: "just copy and past", but communication complicated)
Now we just need software that can effectively use multi core CPU's

Moore’s law

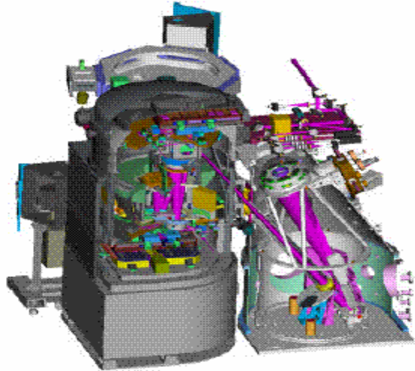


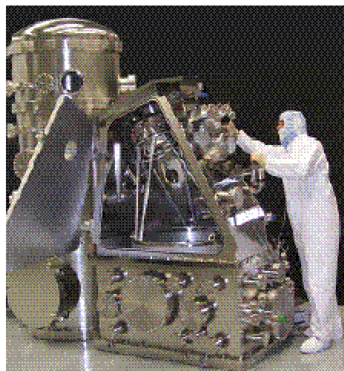
We are now at the level of 1 billion transistors per chip !.

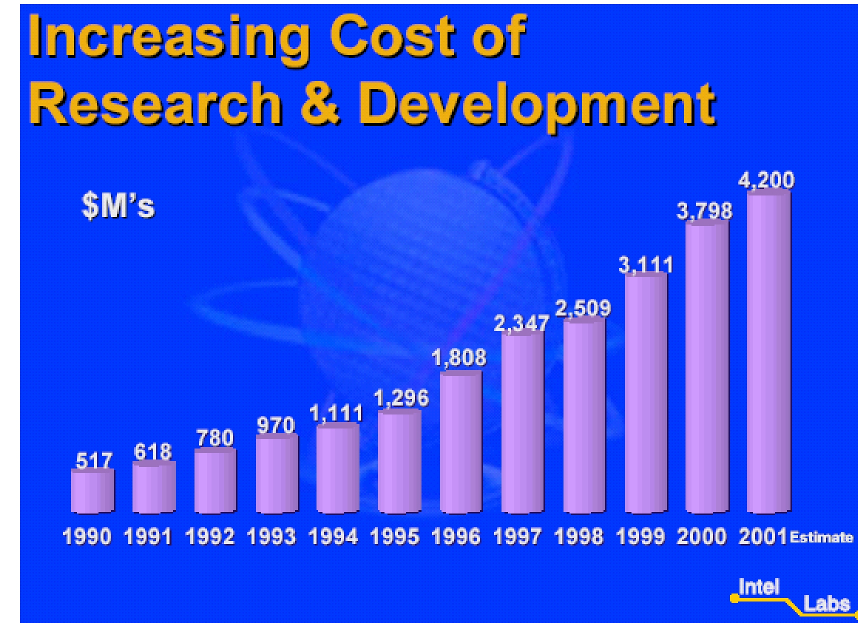
How to have so many transistors used in an effective manner
Verification, production test, power dissipation , etc.

Technology

- Developing new technologies are increasingly expensive
  - Significant changes in fabrication needed for deep sub-micro:
    - Deep UV lithography with reflective optics or E-beam or X-ray

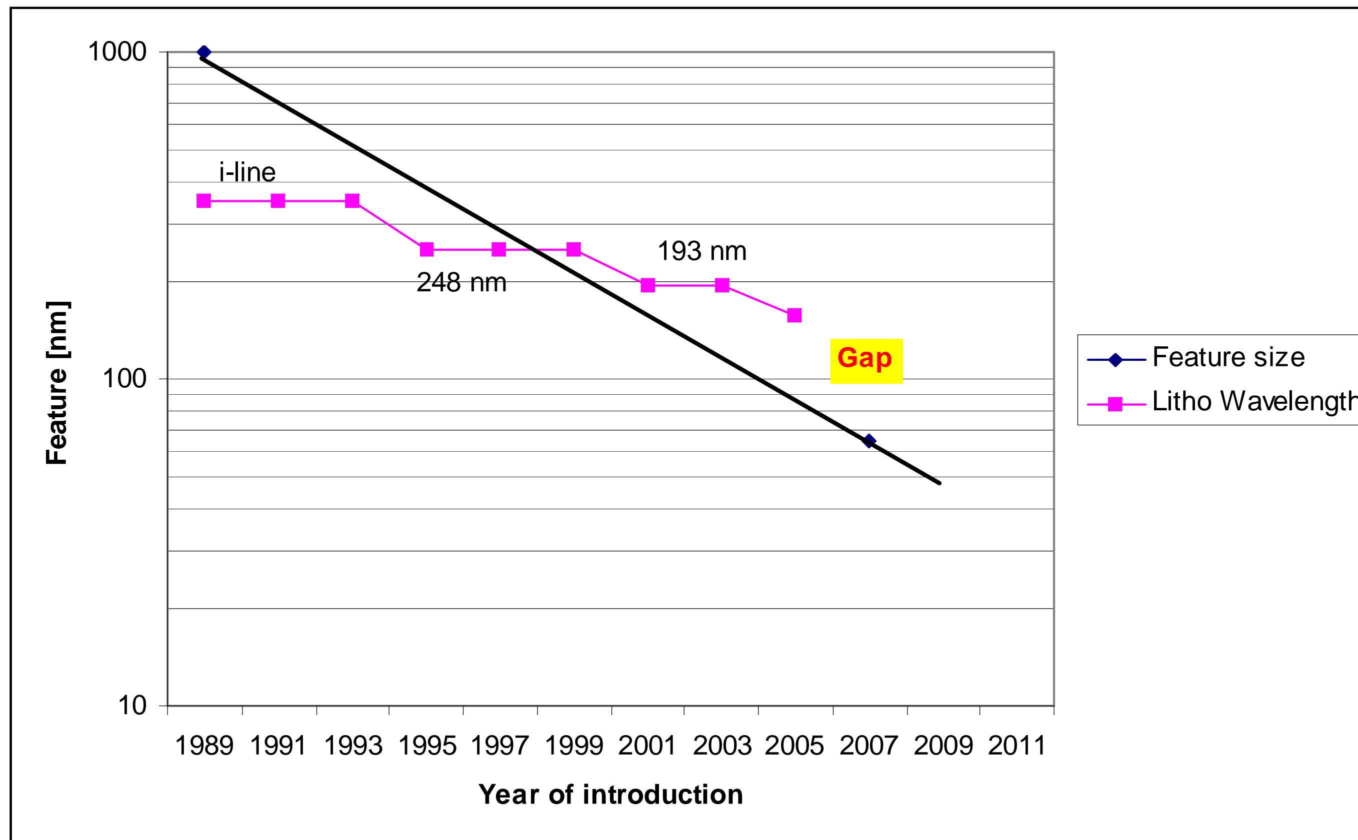






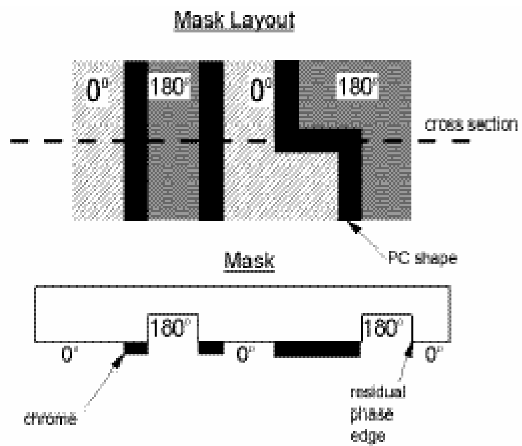
- Large companies forced to make strategic alliances to finance development of new technologies
    - IBM, Infinion, UMC
    - ST, Phillips, Motorola
    - IMEC: Infinion, Intel, Samsung, ST
    - Others

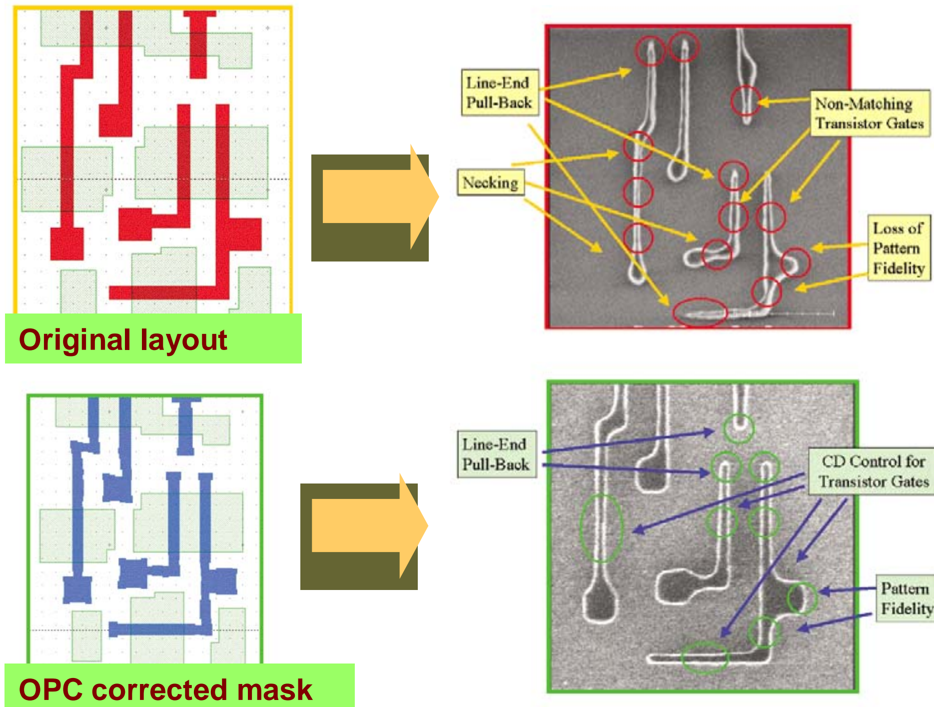
Lithographic wavelength



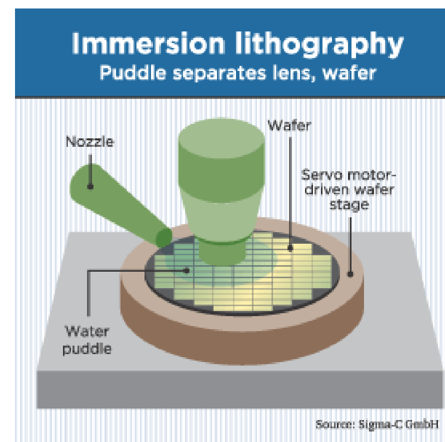
Tricks to use "old" equipment

- Phase shifting masks and pre-correct masks
  - Extensively used



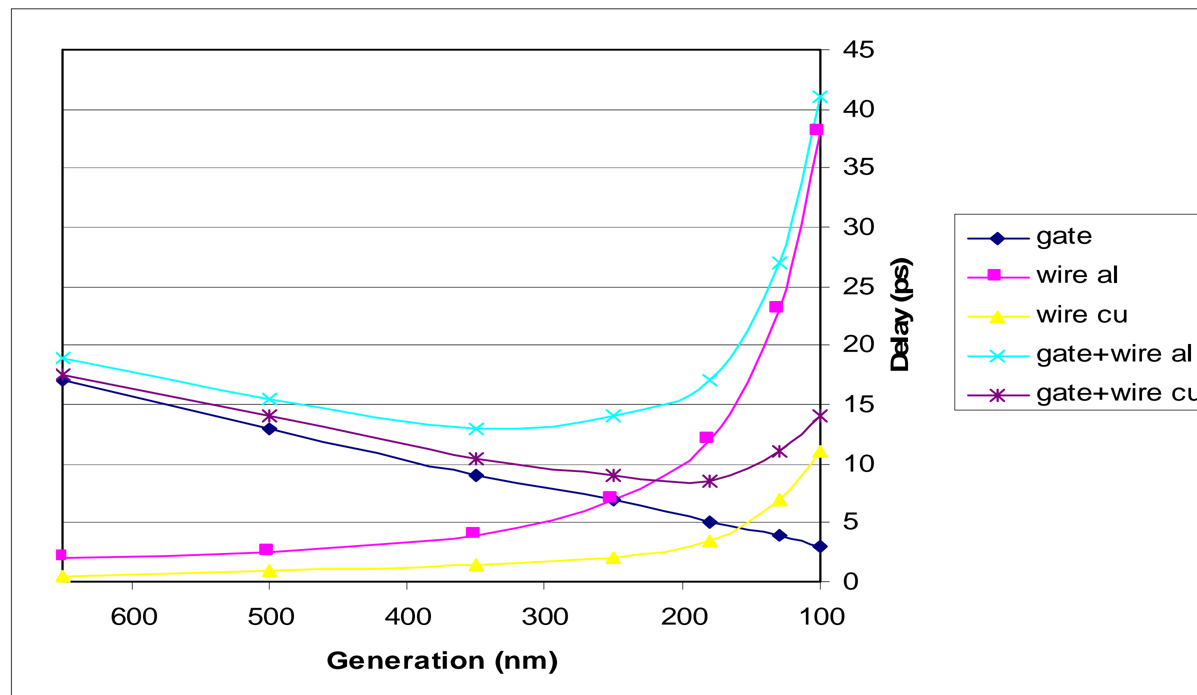


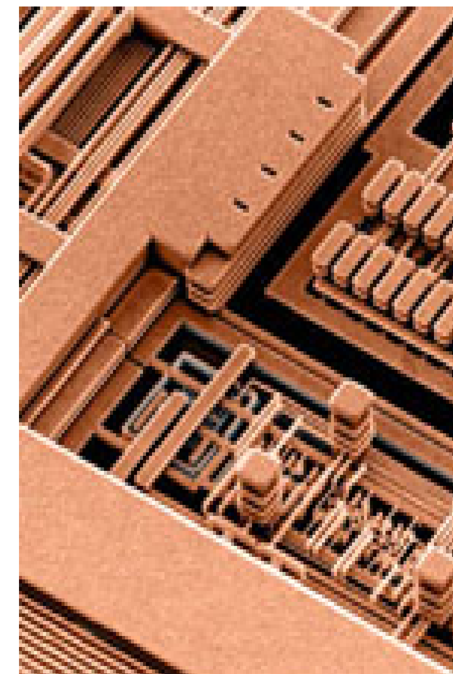
- Immersion lithography
  - The wavelength is slightly smaller and the effective aperture of the projection lens is improved



Gate and wire delay

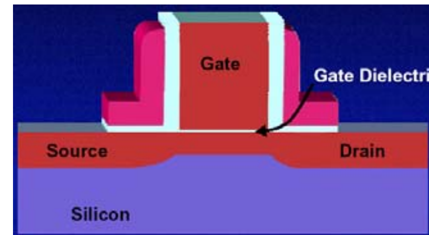
- Gate delay decreases
- Wire delay increases
- Copper wires required to take advantage of decreased gate delay
- Place and route critical

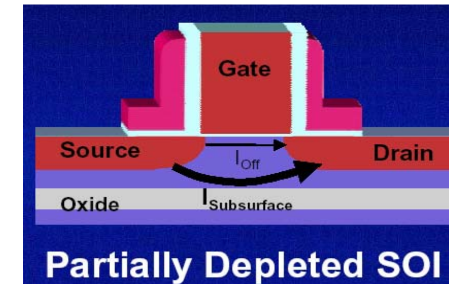


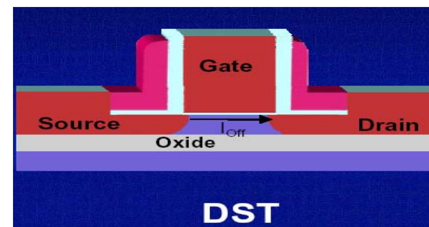


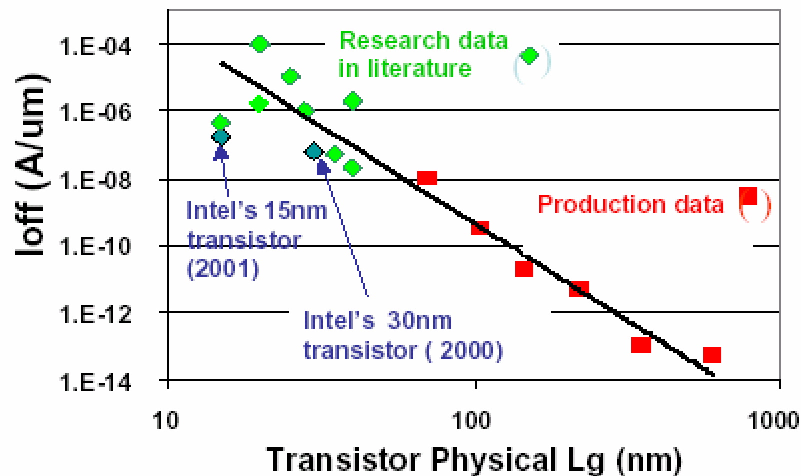
CMOS technology changes

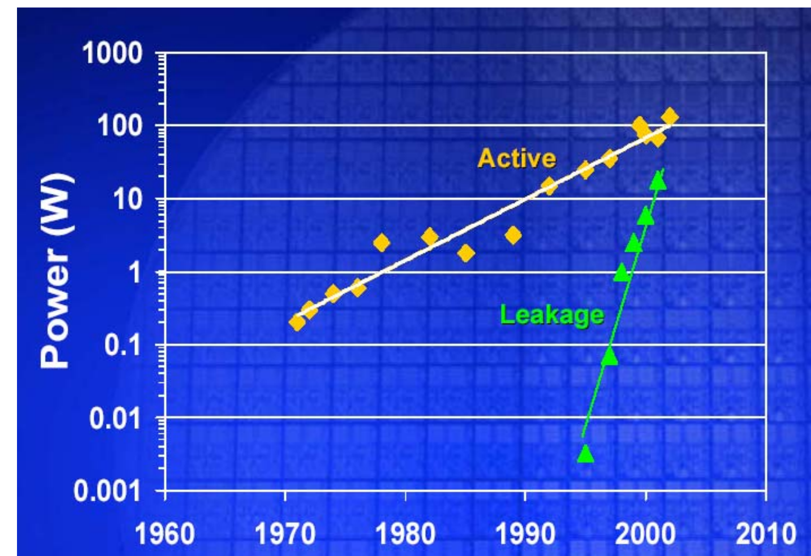
- Ever decreasing device sizes (higher integration and faster)
  - When will it all end ?
- Decreasing power supply voltage
  - Leakage becoming significant part of power consumption
- Use of Silicon on insulator
  - Better control of channel
  - Reduced sub-threshold leakage
  - Reduced capacitances
- New gate isolation materials (High K) to reduce gate leakage.



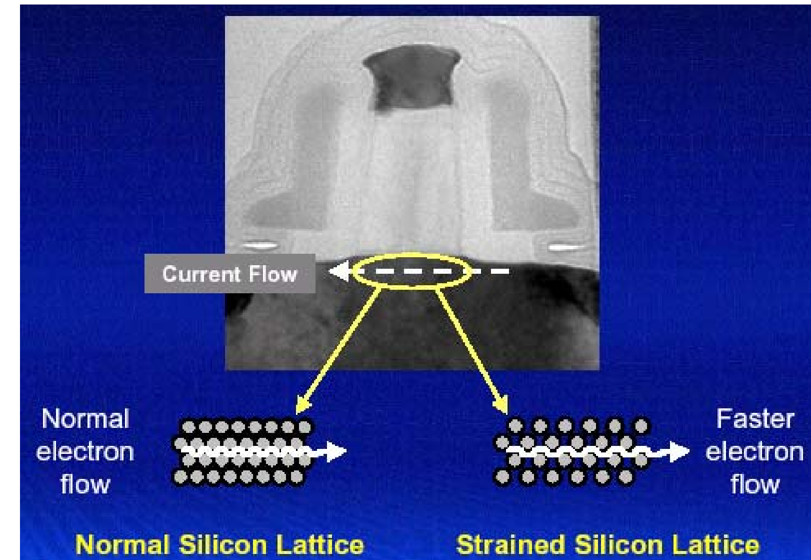






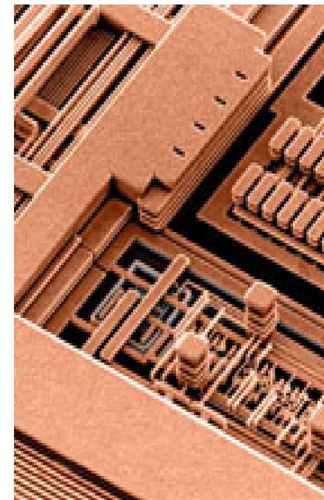


– Use of strained silicon
  - Mobility increased.

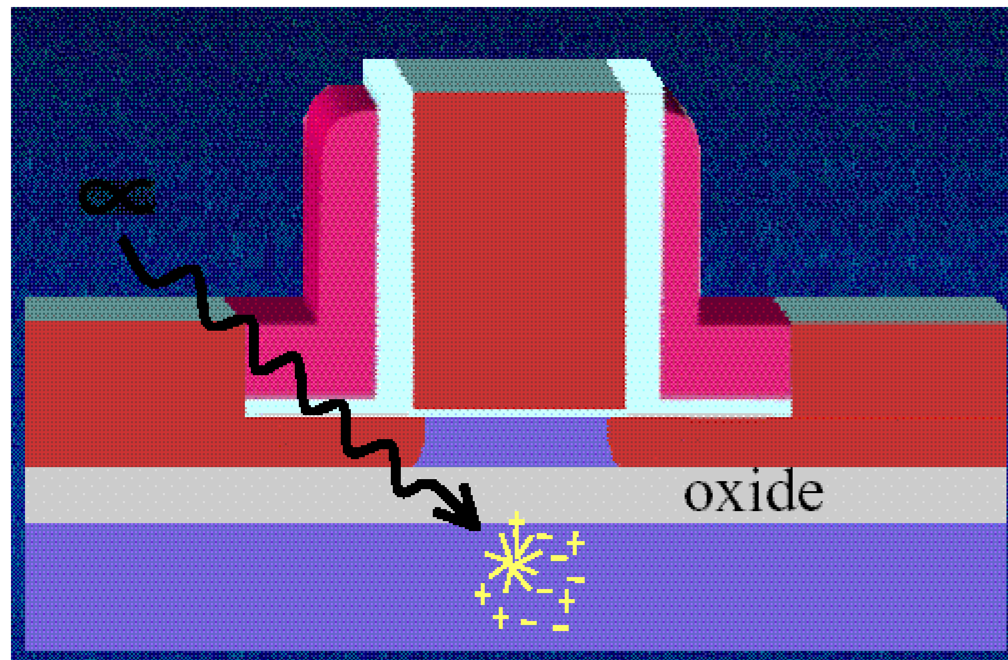


– Copper interconnect

– Low dielectric constant (low K) insulation materials to decrease interconnect capacitance (but hard to exchange SIO_2)

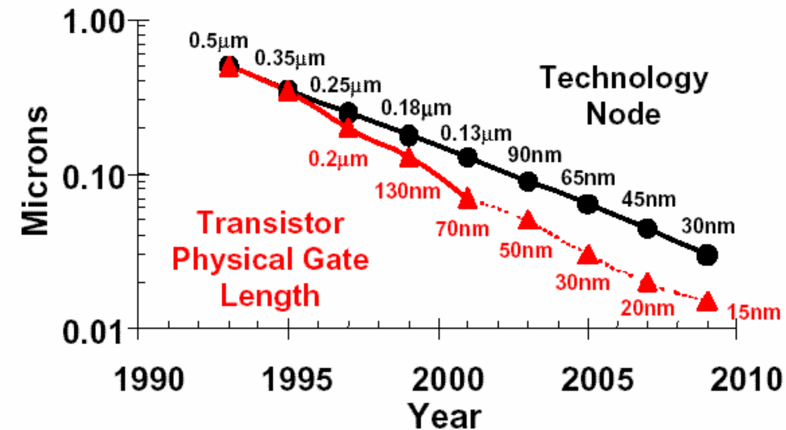


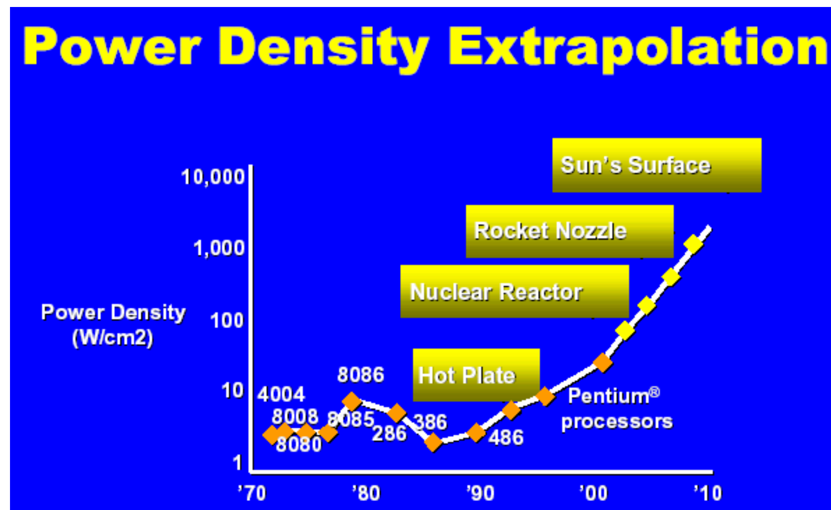
- Is the bit storage in ever smaller technologies reliable ?.
  - Noise immunity at lower supply voltages and lower critical charge.
  - Single event upset from background radiation
    - Bulk technologies: large volume from where generated charge can upset storage
    - Fully depleted SOI: Very small volume where charge can be collected
    - SEU upset in highly integrated SRAM based FPGAs can occur once per ~80days.

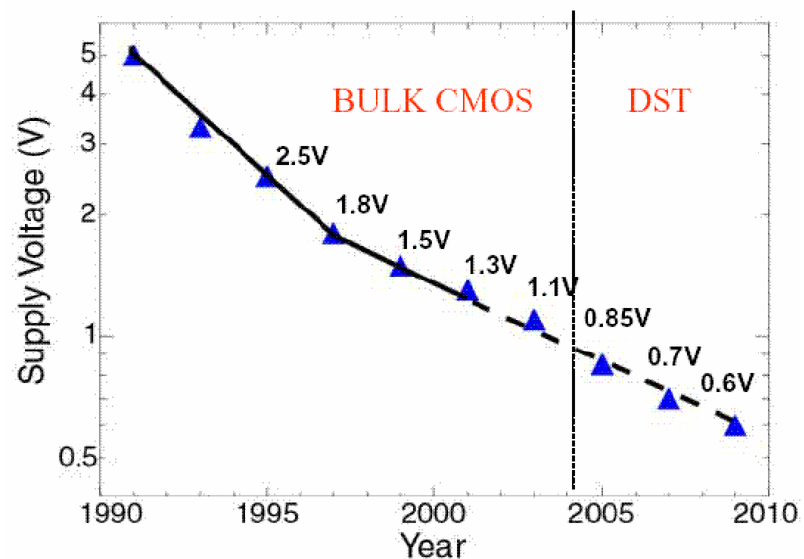


When will classical CMOS have to give up ?

- With cautious optimism it is considered that technology improvements may extend MOSFET to the 22nm technology (9nm effective gate length) by 2016.
  - 1 billion transistors
  - Operating speeds up to 1 THz.
- Other problems:
  - Power density
  - Low supply voltage
  - Atomic scale problems

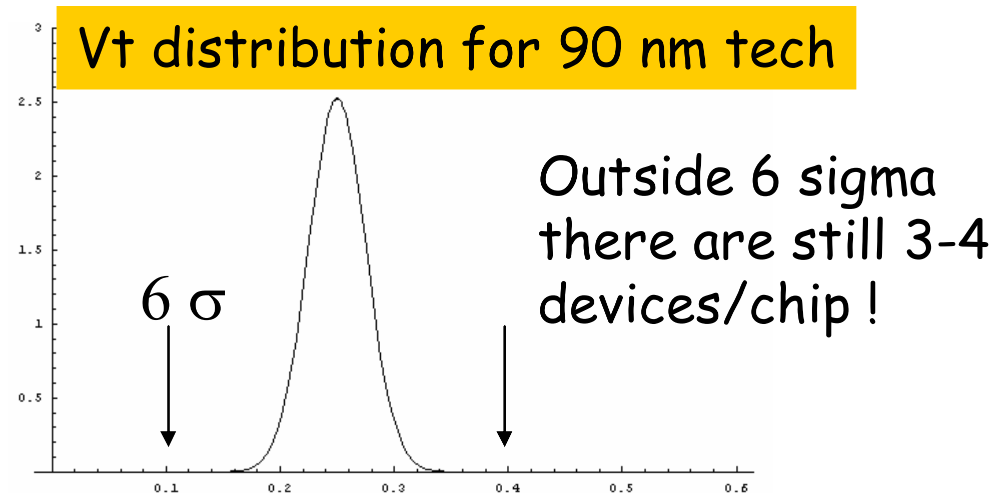


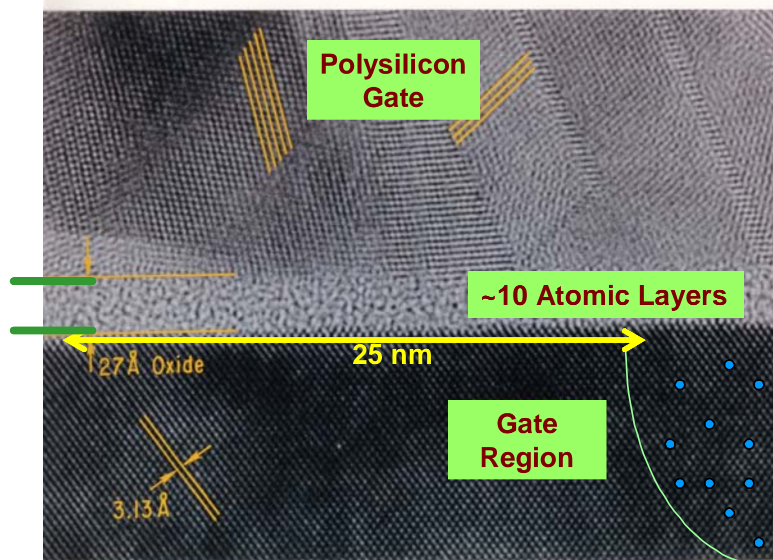


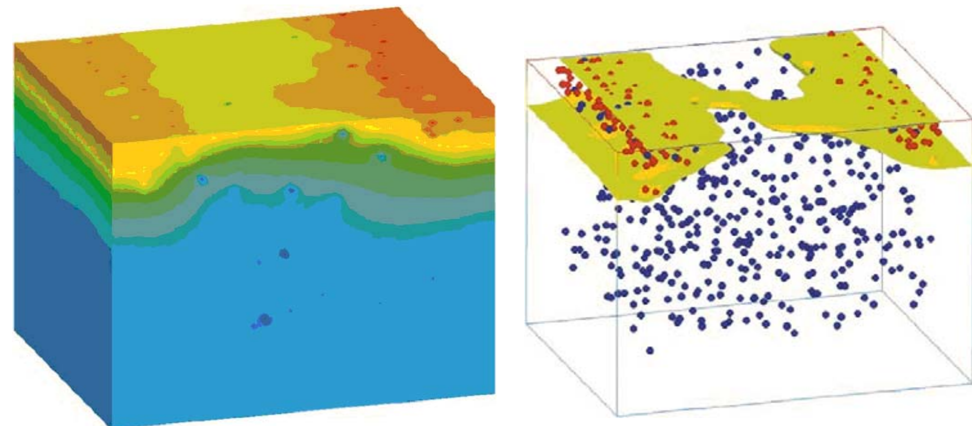


Atomic scale problems

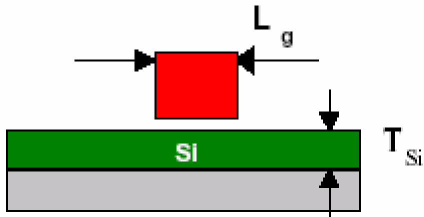
- Only few atoms thickness in gate oxide
  - Tunneling
  - Pin wholes
- Only few dopants within gate region
  - Large Vt variation

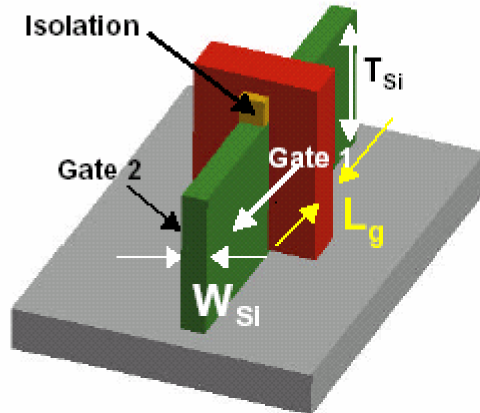


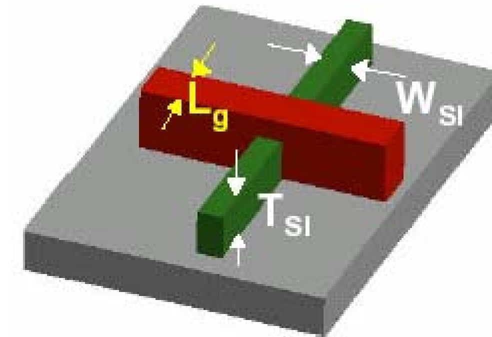


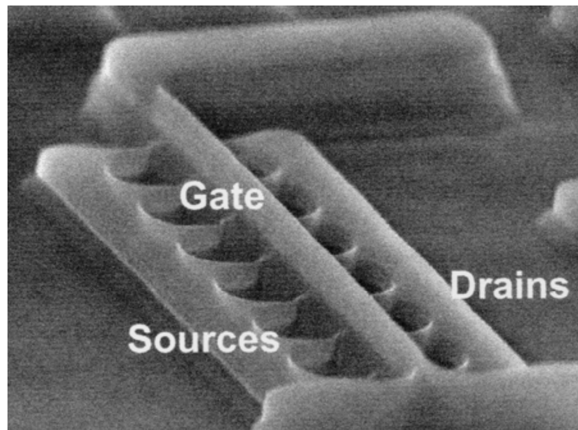


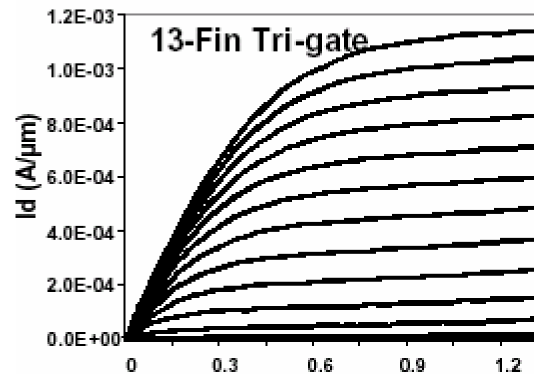
Vertical and/or 3D transistors

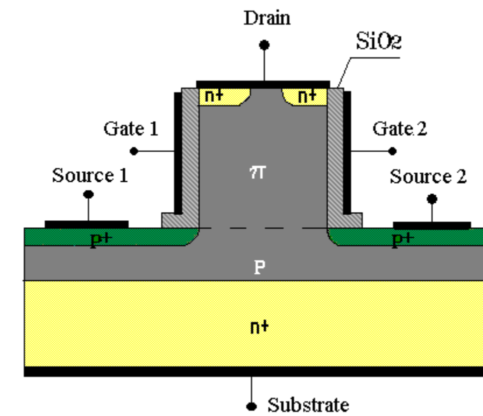








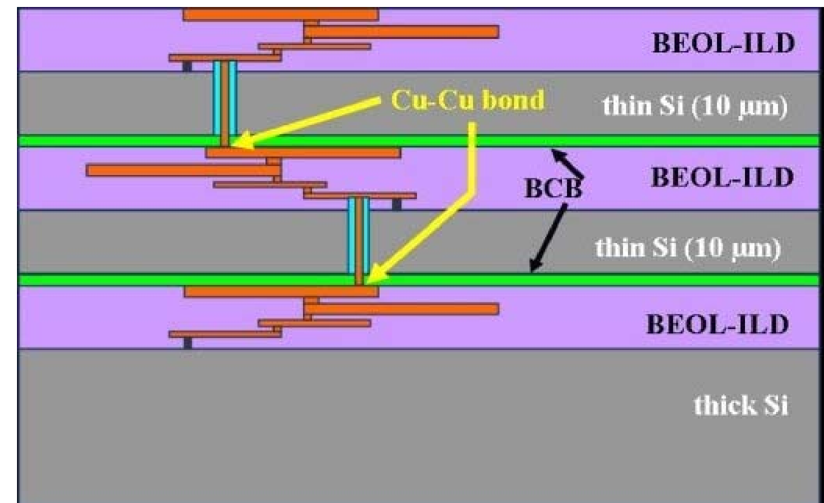


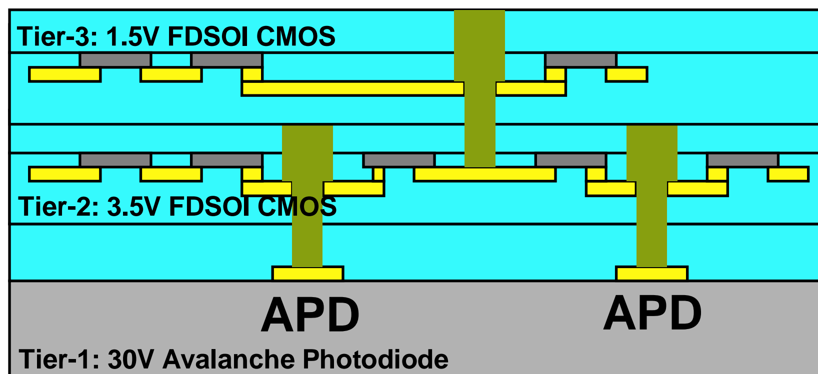


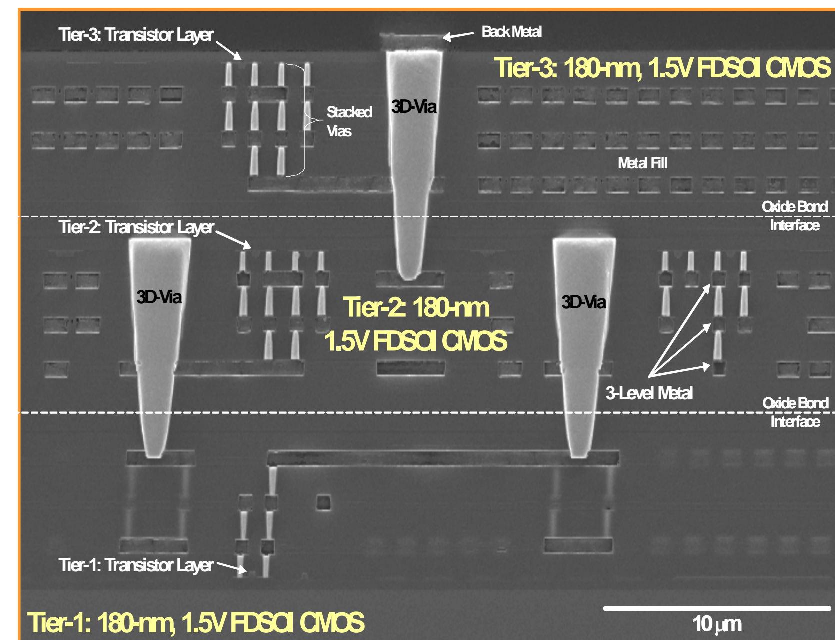
Vertical CMOS transistor

3D packaging

- Multiple transistor and connectivity layers (3)
- Problems:
  - Alignment , Yield, cost
  - Cooling
  - Will this be cost effective against single SOC ?.
- Special applications:
  - Active image sensors with mixed technologies

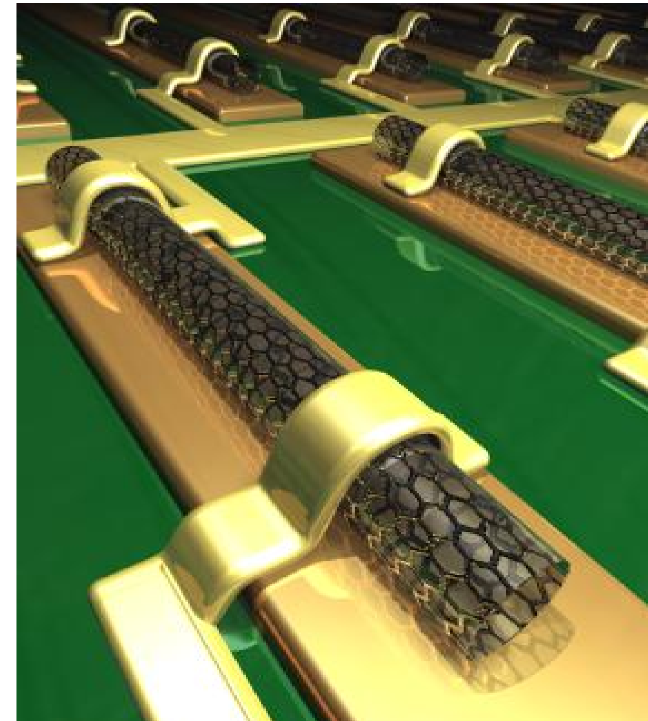




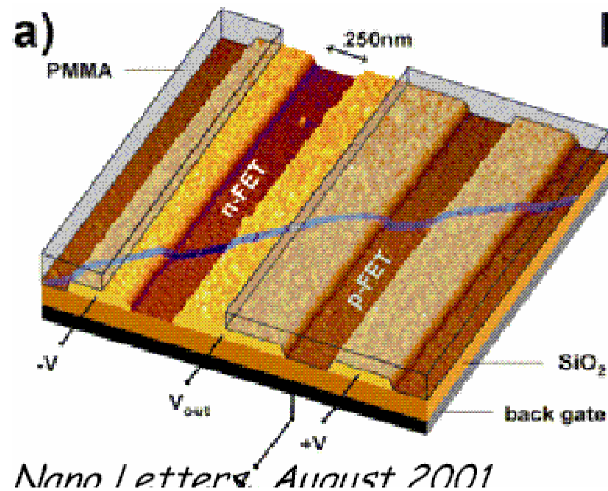


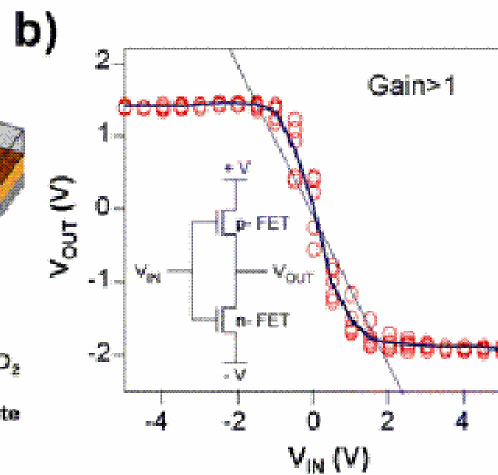
New technologies

- Which technology(ies) will take over after CMOS ?
  - Molecular devices ?
  - Quantum devices ?
  - Carbon nano tube devices ?
  - Optical devices ?
  - Single electron transistors ?



Nanotube transistor



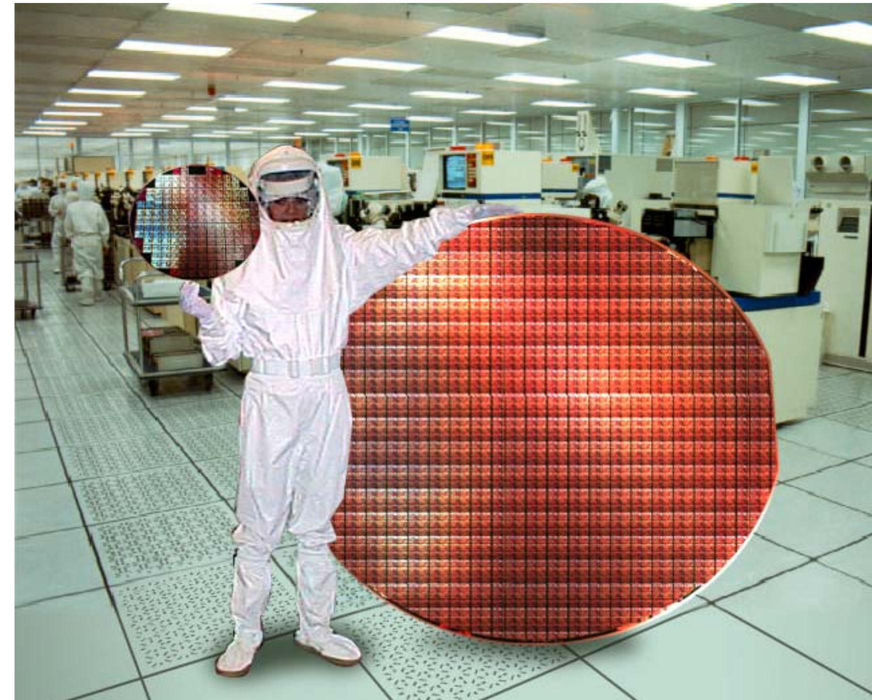


And you can make a working inverter out of this nanotube

But how do you produce such a thing in large volume with a billion devices at very low cost

Production facilities

- Moving to ever larger wafers (HOW BIG ?)
- Only few new fabs open per year
- Fab Cost 2-4 B$ today
  - Affordable only for DRAM and very high volume companies
  - Fab-less companies (Xilinx, Altera, etc.)
  - Expected to double every 3 years.
    within the next few generations the cost of a Fab. may become larger that the yearly total turnaround for the biggest IC companies (e.g. Intel)
- Technology lifetime 4-5 years
- Completely new Fab. needed for next generation technology
- The microelectronics industry is known to have its up and downs (~5 year period) but still continuously increase in value. This makes it hard to plan investments in fabrication facilities

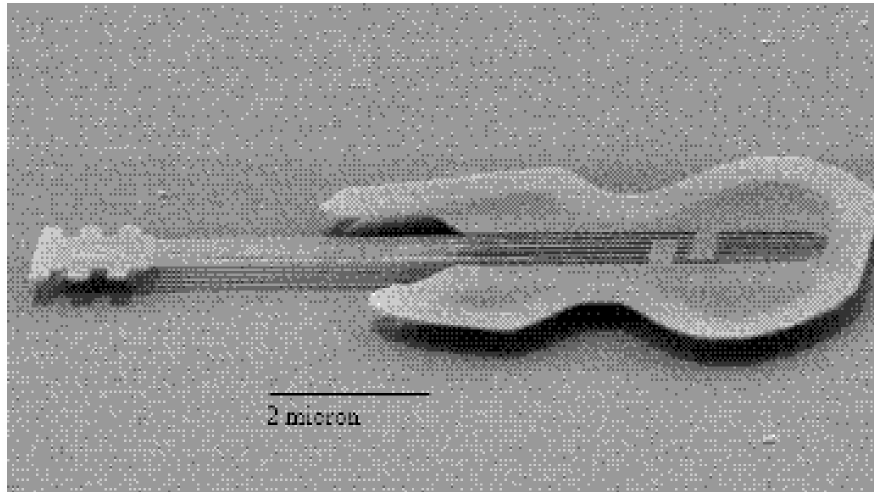


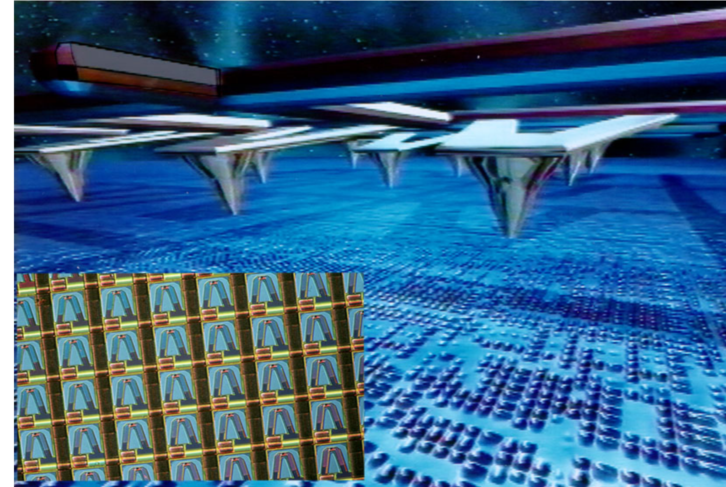
Moore’s Law in 1977 predicted a 57” wafer by 2003

Design

- Designs will be based on synthesis except memory, analog and special devices.
- Extensive use of IP blocks from specialized design houses
- Analog design will become increasingly difficult because of decreased power supply voltage and change of transistor characteristics.
  (the world is going digital but is at its origin analog)
- Place and route is the critical tool.
- Crosstalk between digital signals must be taken into account
- High performance tools will be needed for design and verification
- High performance tools will stay expensive and will probably become even more expensive.
- Design and prototyping costs will increase
  - Mask costs for 130nm: ½ - 1 M$
- New architectures to take advantage of increasing number of transistors (e.g. Vector processing, VLIW, multi core, ,)

What will the future look like ?





What will be the new killer applications for microelectronics ?

- Mobile phone with computer, Camera, WIFI, GPS, etc.
- High end computers for 3D video games
- Optical networking to the home
- Car electronics
- Home robots
- ????????????