The Abdus Salam
International Centre for Theoretical Physics

United Nations
Educational, Scientific
and Cultural Organization

International Atomic
Energy Agency

310/1780-22

ICTP-INFN Advanced Tranining Course on
FPGA and VHDL for Hardware Simulation and Synthesis
27 November - 22 December 2006

FPGA

Jorgen CHRISTIANSEN
PH-ED
CERN
CH-1221 Geneva 23
SWITZERLAND

Strada Costiera 11, 34014 Trieste, Italy - Tel. +39 040 2240 111; Fax +39 040 224 163 - sci_info@ictp.it, www.ictp.it

Field Programmable Gate Arrays: FPGA and Complex Programmable Logic Devices: CPLD

J. Christiansen,
CERN - EP/MIC
Jorgen.Christiansen@cern.ch

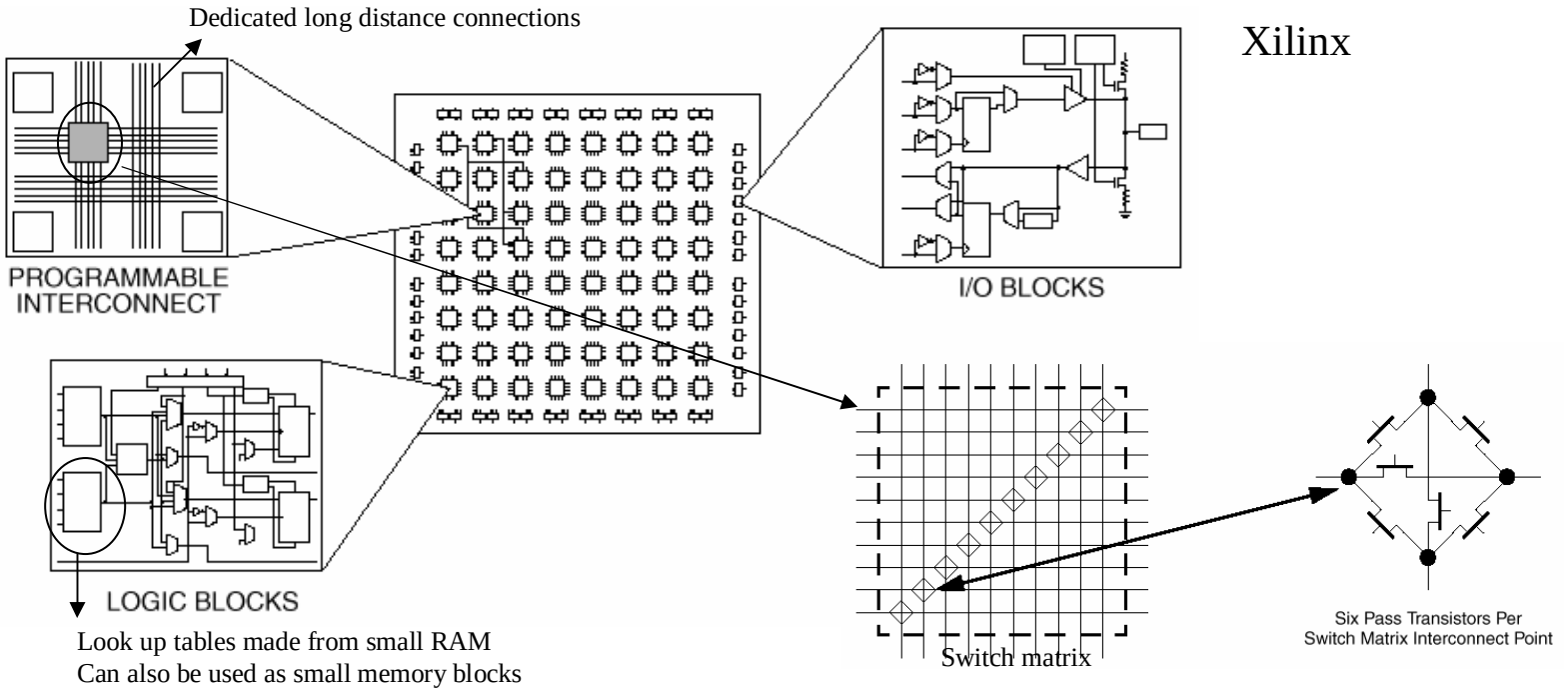
General

- Fully programmable digital integrated circuits:
  - One time programmable (antifuse or PROM based)
  - Re-programmable (SRAM or FLASH based)
  - Up to 10Million gates
  - Up to 2000 pins with programmable signal levels
- Built from:
  - Programmable logic blocks with few registers (flip-flops)
  - Programmable interconnects (limits performance)
  - Programmable inputs/outputs
  - Configurable memories
  - Special blocks: DLL, PLL, Processor, PCI interface, etc.
- Low development costs:
  - Relatively “Cheap” and “easy” to use PC based tools
  - Short development time (trial and error development possible)
  - No development of production test procedures
  - Production costs can be quite high for high gate count devices

General principle

- Logic blocks with programmable logic (LUT) and a few registers.
- Programmable interconnects using switching matrixes

  Several types of interconnects: clocks, short distance local connections, long distance connections across chip.



SRAM based (Xilinx, Virtex)

- Configuration controlled from small static memory cells
- Configuration loaded serially with associated checksum.
- FPGA must be reprogrammed at power up from special serial prom or from computer.
- A large amount of configuration bits required (Mbits for modern FPGAs)
- Special RAM blocks and multiplier available
- Problematic in radiation environment because of high risk of SEU in configuration bits

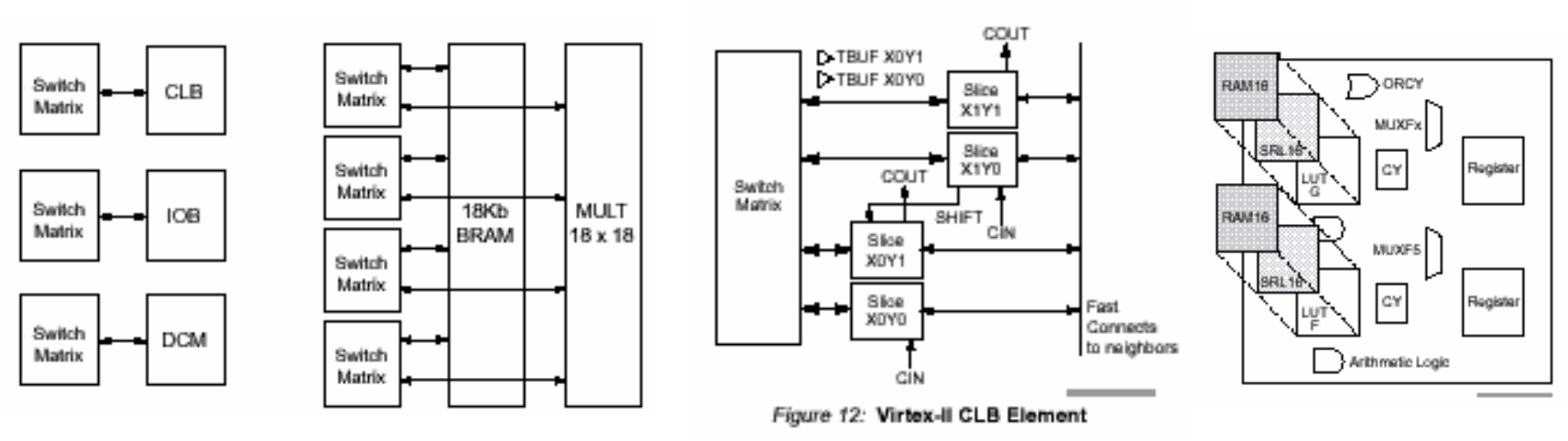
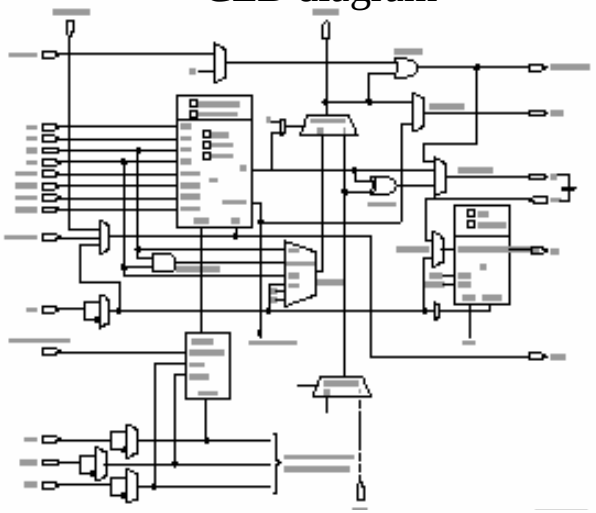
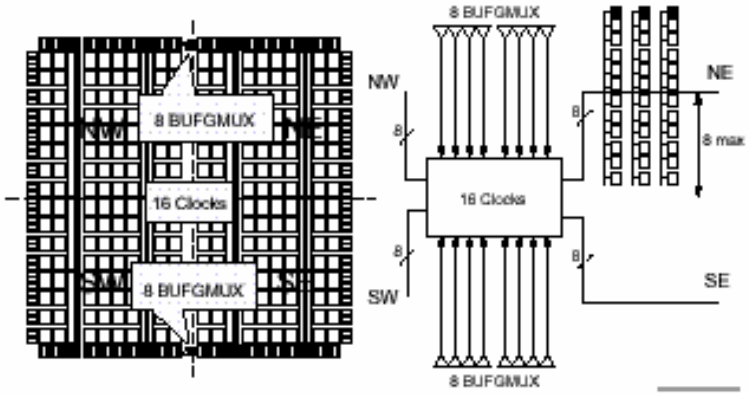


Figure 12: **Virtex-II CLB Element**

CLB = Configurable Logic Block

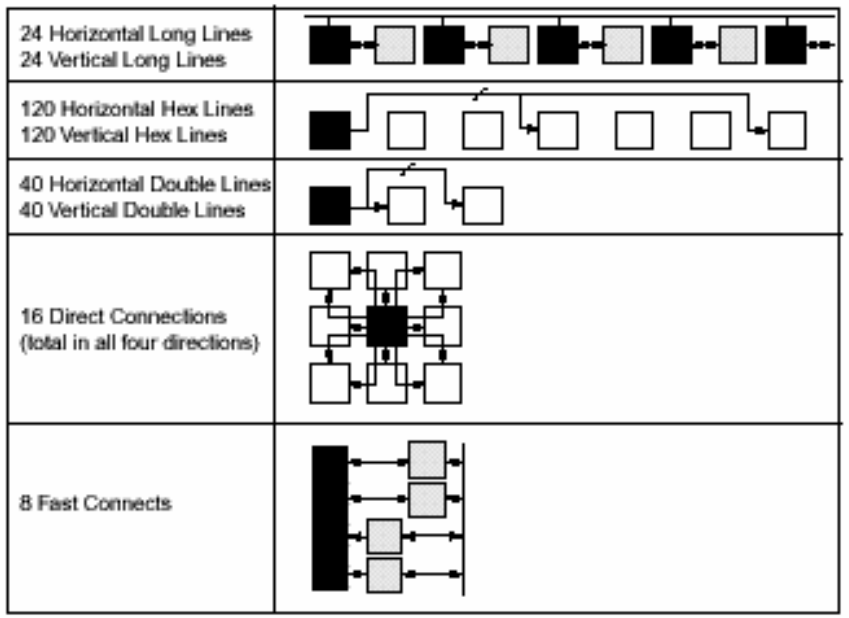
CLB diagram





Dedicated clock buffers with related routing

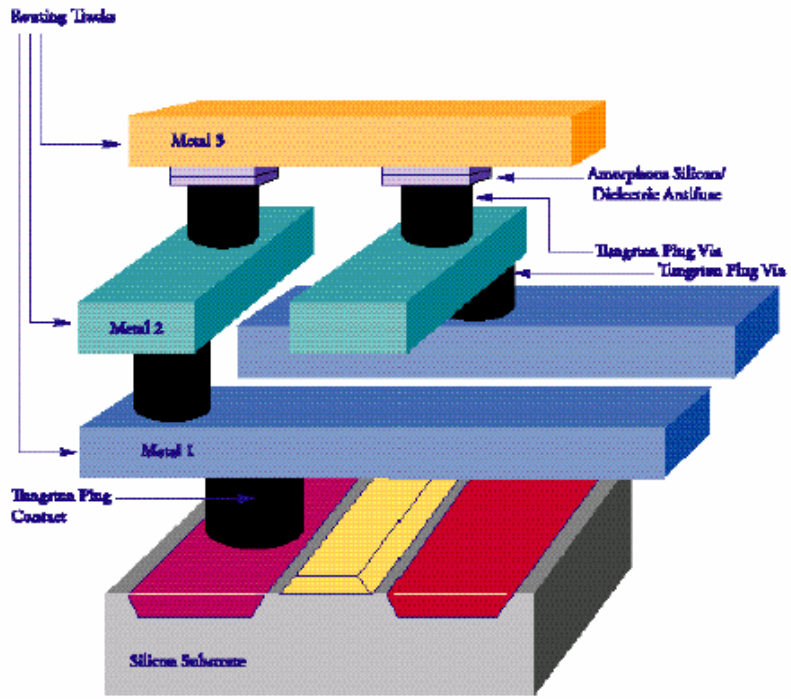
Several types of configurable interconnects

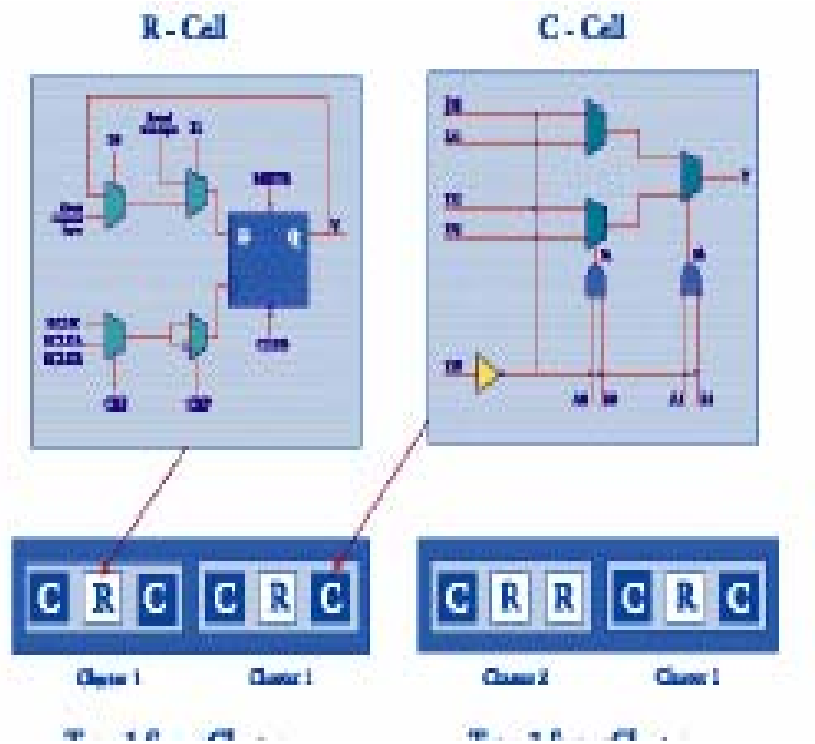


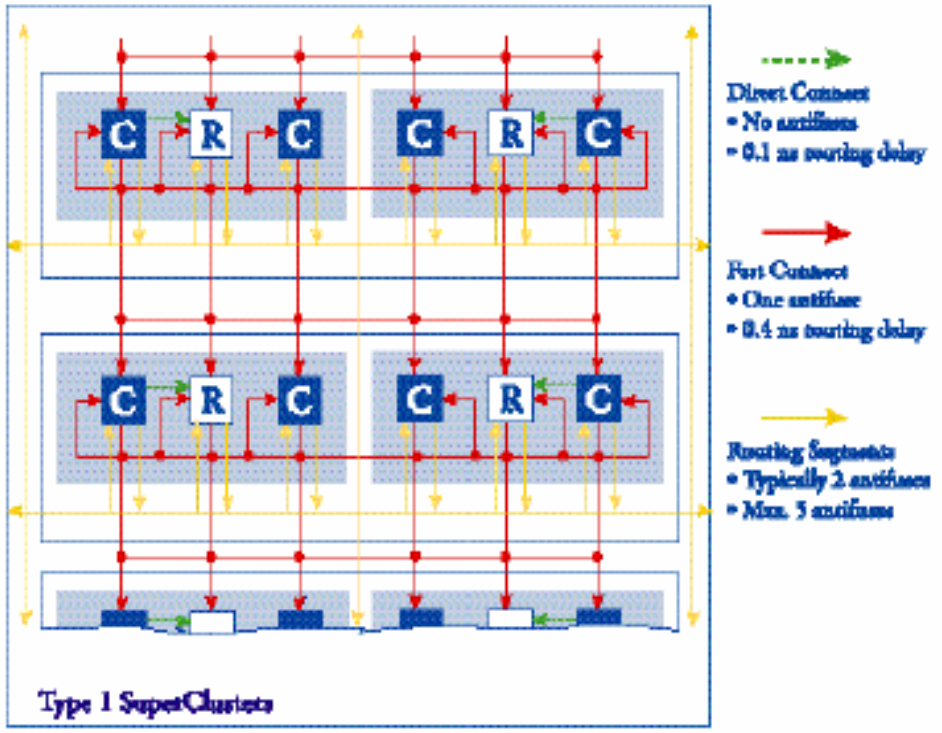
Plus a few similar configurations

Anti-fuse based (Actel)

- Logic and routing configured with antifuses
- In an antifuse a connection between metal layers is generated by applying a “destructive” voltage between the two nodes of the antifuse.
- Requires special processing to implement reliable antifuses
- Devices programmed once for all: Can not be reprogrammed and does not need reconfiguration after power is applied
- Less sensitive to SEU effects than SRAM based FPGA

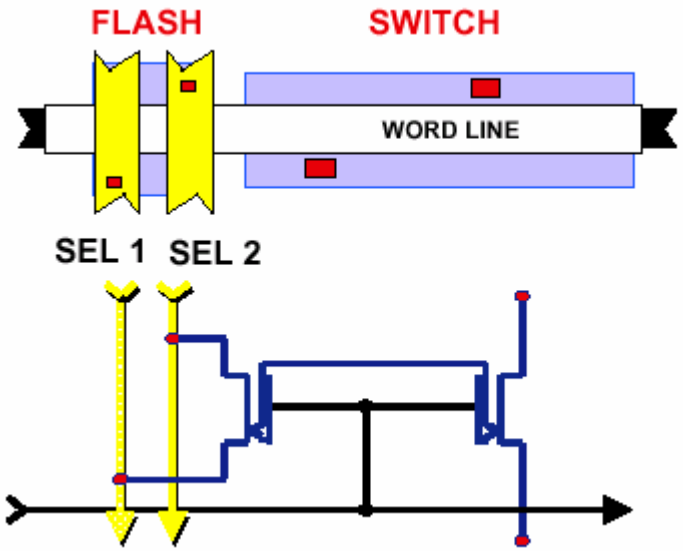


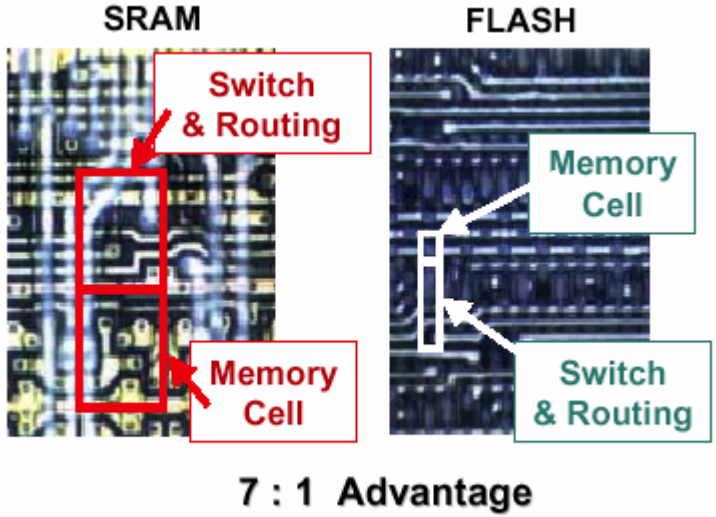

R - Cell
C - Cell
C R C C R C
C R R C R C


C R C C R C
C R C C R C
Direct Connect
• No antifuses
• 0.1 ns routing delay
Fast Connect
• One antifuse
• 0.4 ns routing delay
Routing Segments
• Typically 2 antifuses
• Max. 5 antifuses
Type 1 SuperClusters

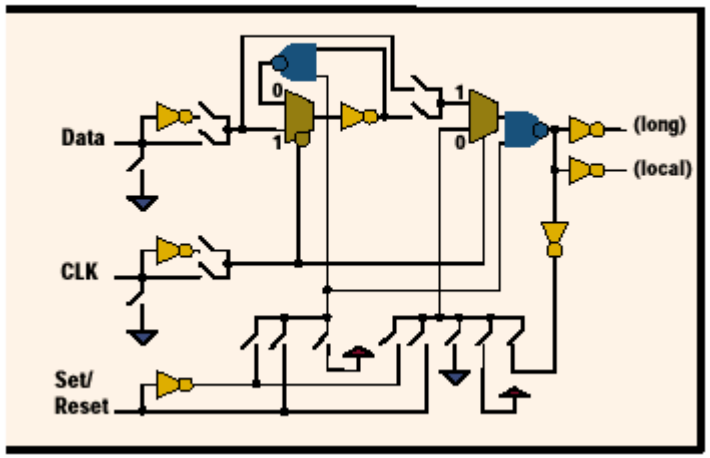
Flash based (Actel)

- Logic and routing configured with Flash memory
- Can be reconfigured when ever needed
- Does not loose configuration when powered down
- Needs technology with support for floating gates
- Uses fine grain cells which can be configured as logic or storage

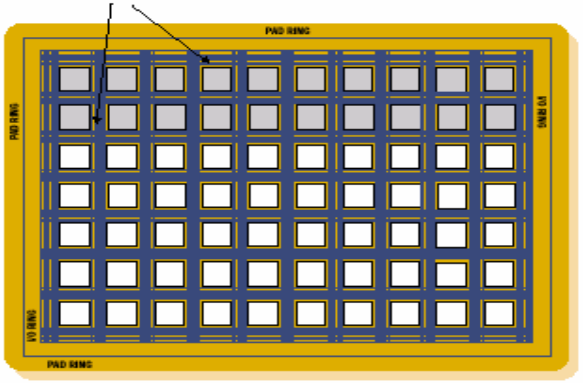




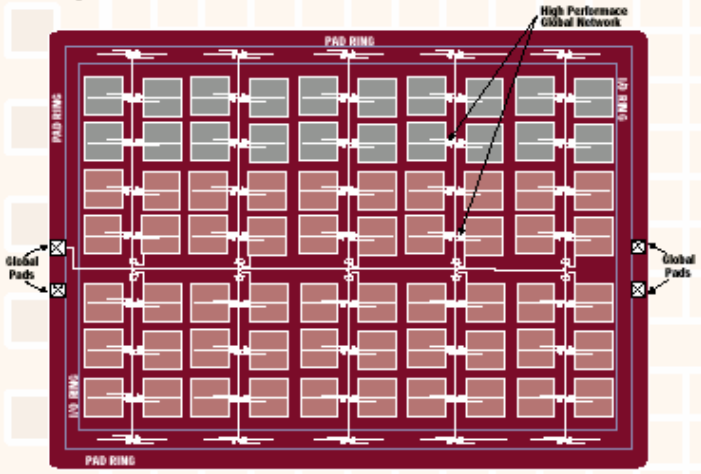
ProASIC Logic Tile

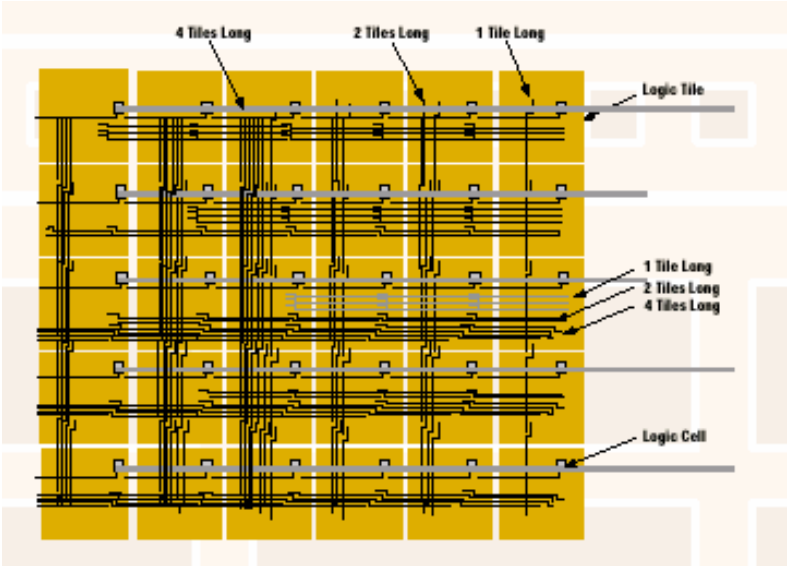


High Speed Bus Resource



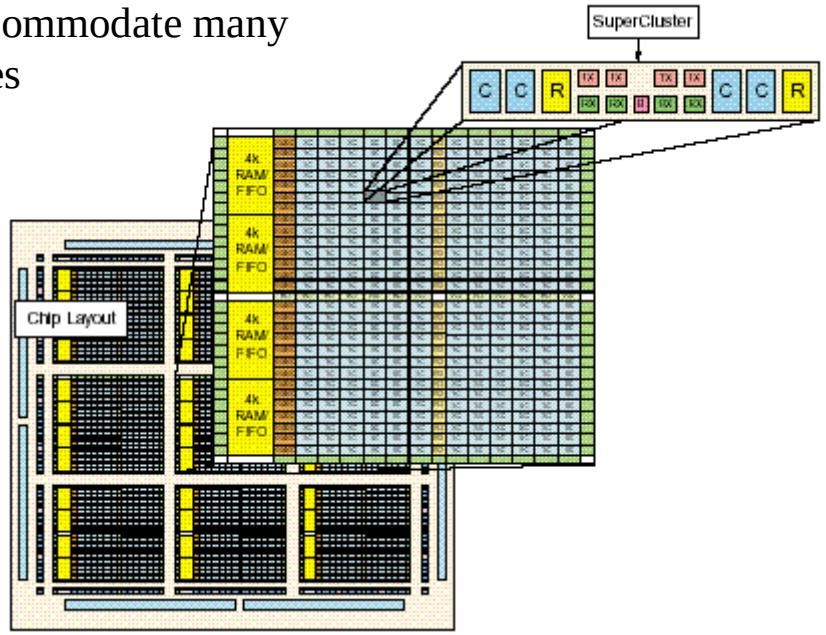
High Performance Global Networks



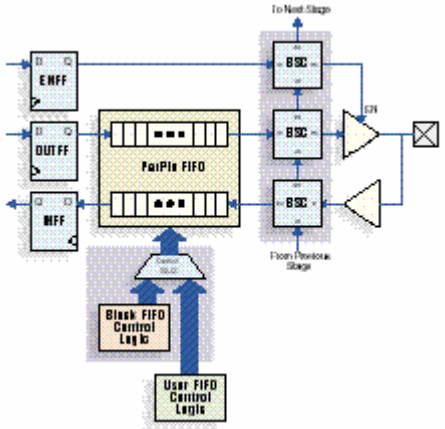


New Antifuse series

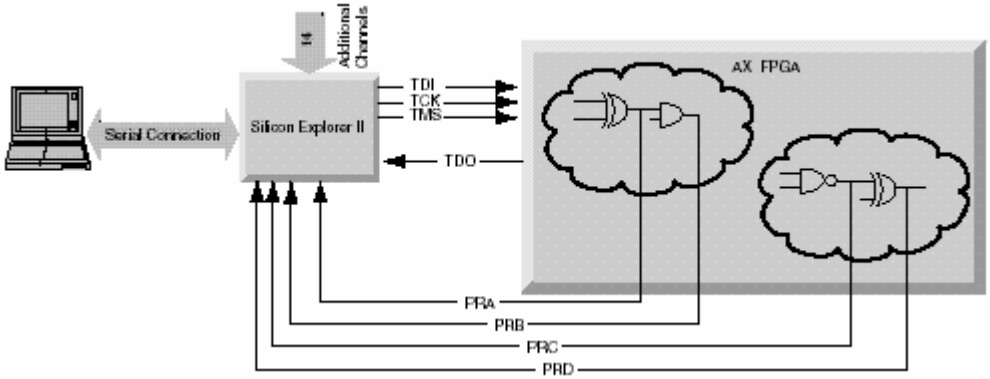
Multilevel Hierarchy to Accommodate many gates



I/O pins with buffer capability

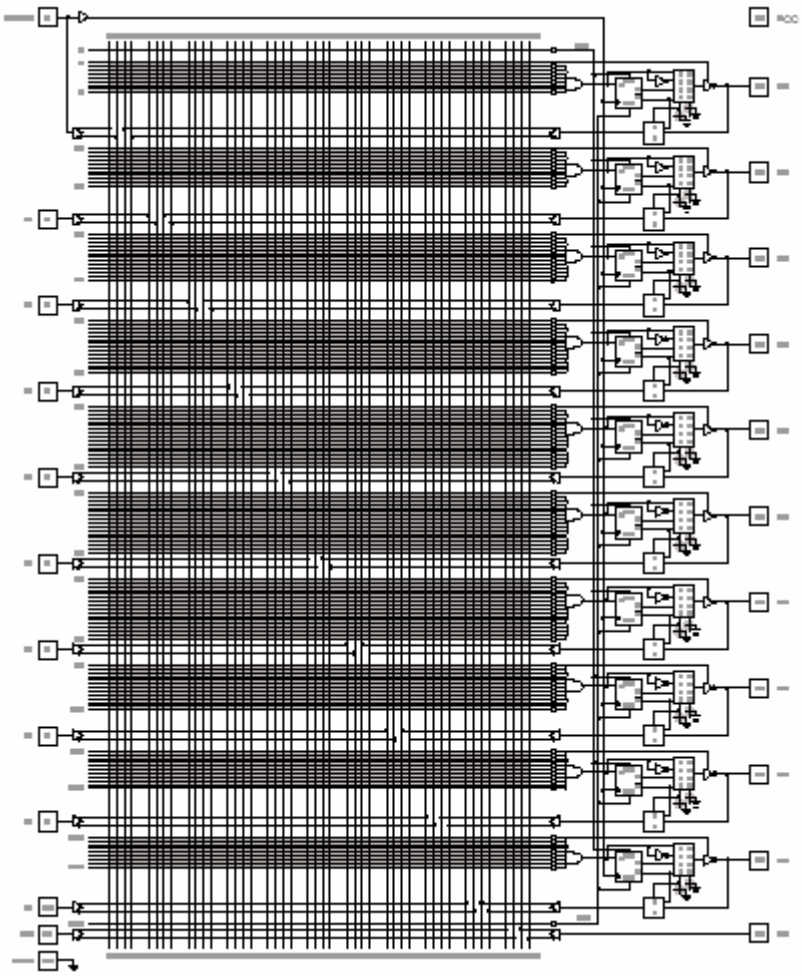


Built in probing capability for debugging

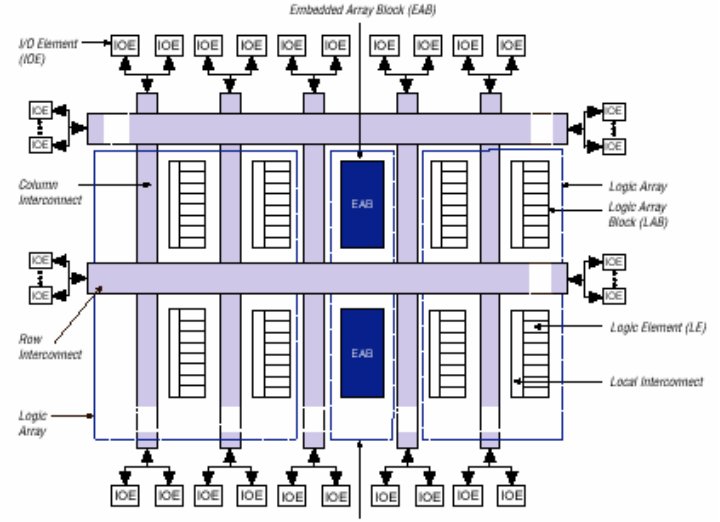


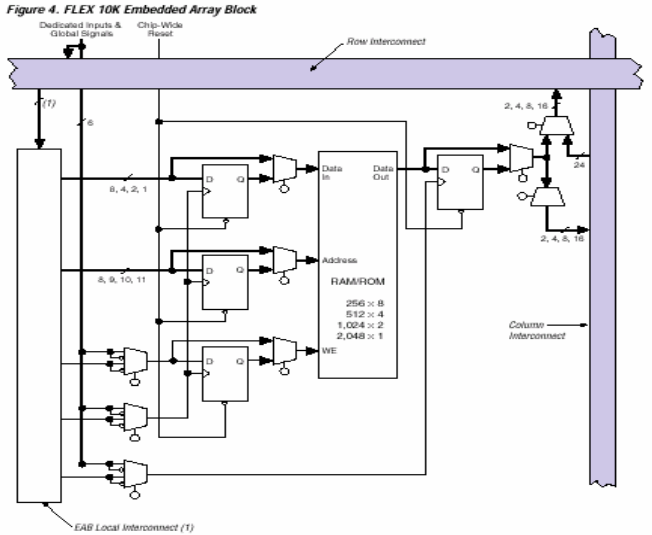
Programmable Logic Devices

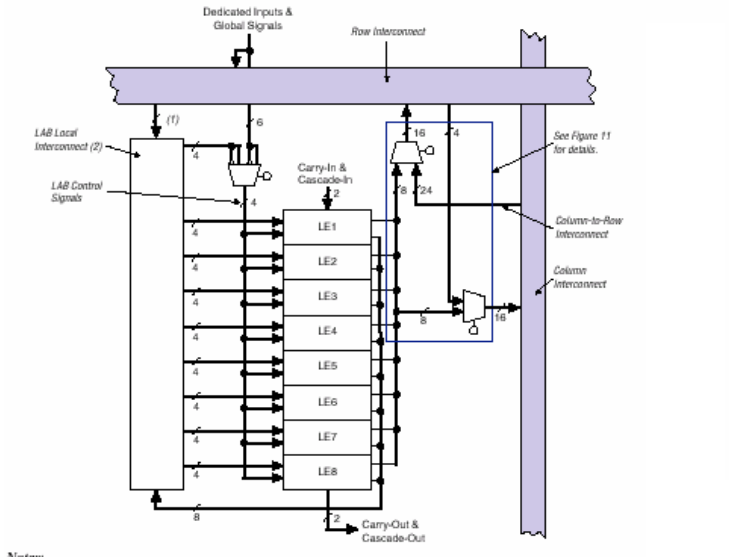
- Traditionally made with programmable And – Or fuse arrays with registers at the output.
  Previously called PAL (Programmable Array Logic)
- Complex PLDs (CPLD) contains multiple And – Or blocks with configurable interconnect.

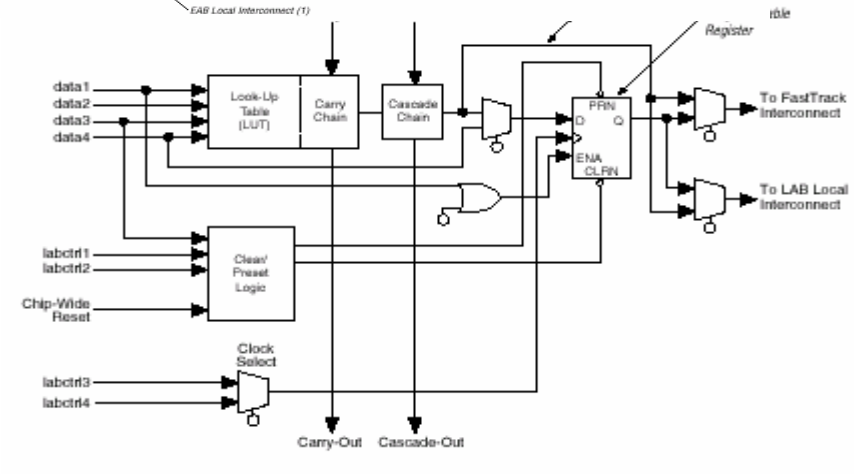


Complex PLD (CPLD)



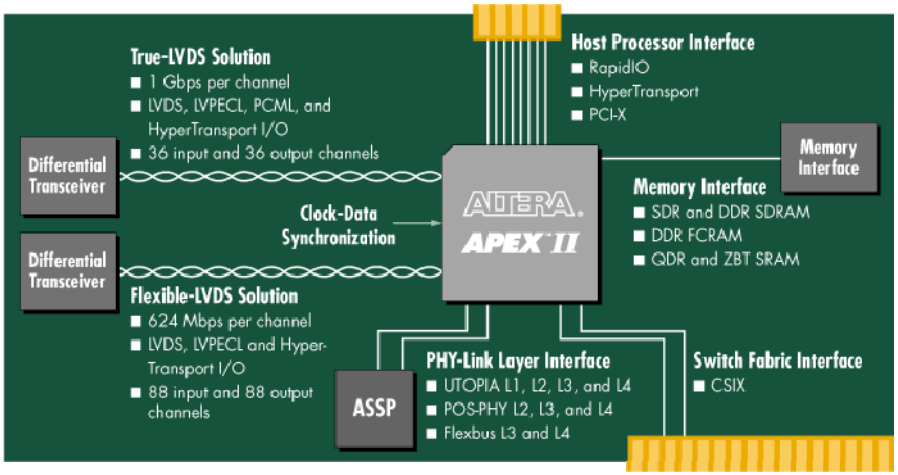




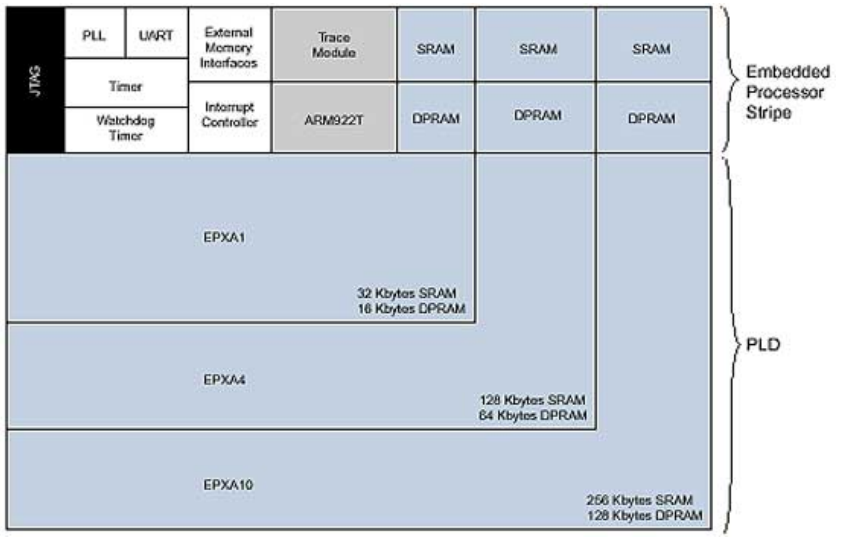


Specialized CPLDs

High speed interconnects



On-chip lower power micro-processor



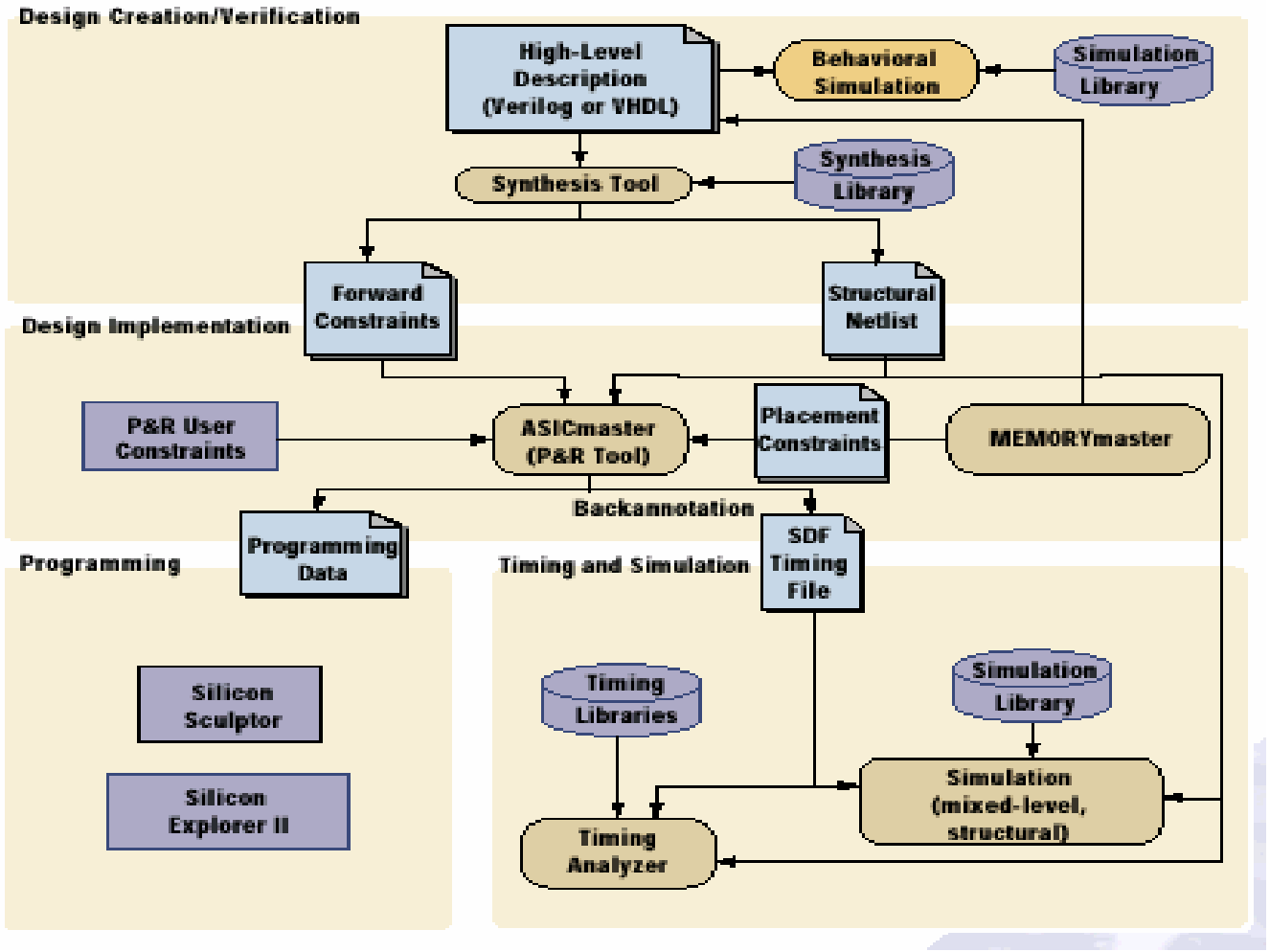
Difference between FPGAs and CPLDs ?

- FPGAs are configured at a fine grain level from many equivalent logic blocks (array of configurable gates)
- CPLDs often consist of a limited set of complex reconfigurable blocks.
- Special CPLDs exists for specialized applications

Design

- Based on Synthesis together with specialized Place and Route tool.
- Small local blocks can run quite fast.
- Large complicated blocks has limited speed because of interconnect delays.
- General functional blocks optimized for given FPGA architecture often given as macro blocks: Counters, adders, multipliers, FIFO's, etc.
  - Important to use such blocks in synthesis to obtain good performance
- Dedicated timing estimator/calculator: LUTs fixed delays, F-F fixed delays, interconnects depends on length and number of routing switches.
- If design gets close to full utilization then design time increases significantly (problem with place and route).

Typical design flow



Applications

- Low to medium volume products
- Reconfigurable computing: Compile algorithm into hardware implementation in FPGA.
  - Soft border between hardwired and soft coded
- ASIC prototyping: ASIC design synthesized into array of FPGAs for early verification at reduced operating speed.
- Special purpose signal processing not covered by available DSPs.
- Everybody who can not afford to develop an ASIC or who can not wait for an ASIC to be developed.
- Some FPGA’s can be quickly mapped into real ASIC if sufficient quantities to justify this.

General trends

- Fast introduction of new improved FPGA's/CPLDs
- Takes full advantage of modern technologies (problematic for antifuse that requires special processing steps)
- Large scale production of same circuit keeps production costs relatively low even though IC area is large.
- Introduction of IP blocks (microprocessor, PCI interface, etc.)
- Introduction of very high speed IO blocks (multi gigabit/s).
- Special versions for radiation applications (space).
- Number of effective gates and operation speed from manufactures must be taken with a large "grain of salt"