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RVI_06

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RECONFIGURABLE VIRTUAL INSTRUMENTATION PLATFORM

A BLOCK-BASED OPEN SOURCE APPROACH

USING FPGA TECHNOLOGY

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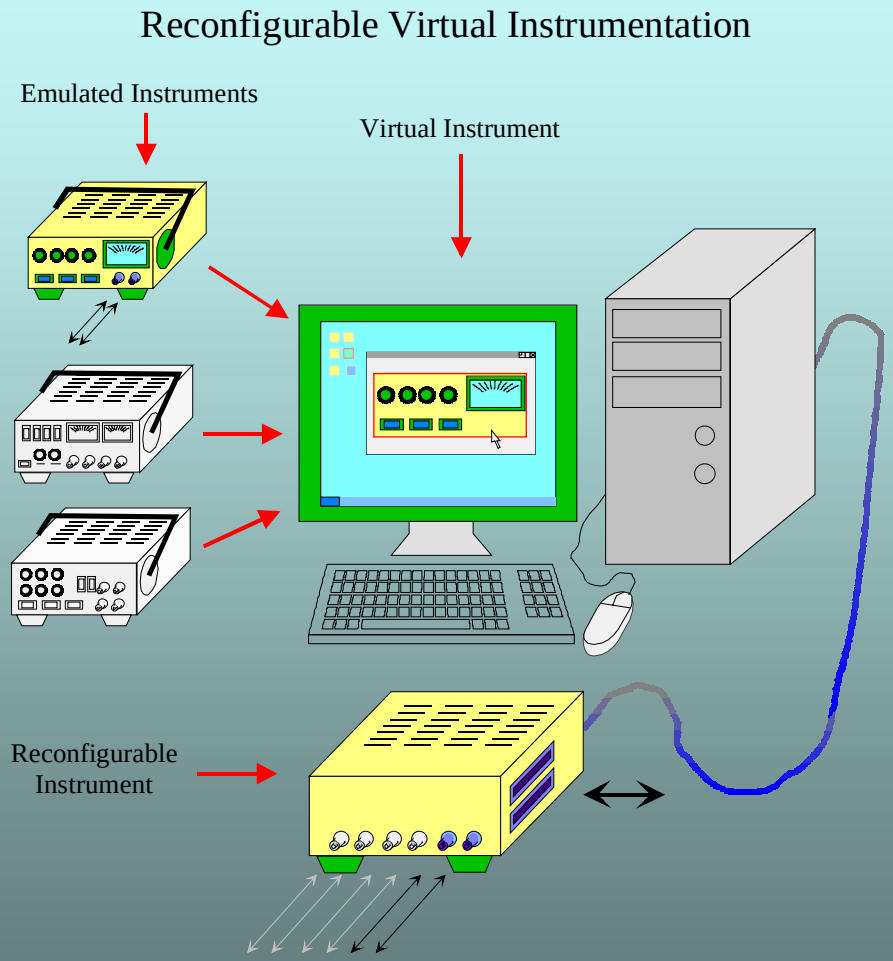
An artistic view of an RVI System

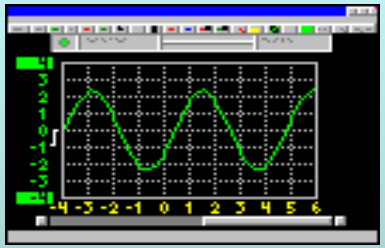


- The RVI system can be seen as a “magic-box” connected to a PC through a standard port
- High-level software application
  - select a virtual instrument from a library of instruments
  - configures the RVI system to convert it into the selected instrument with its associated console

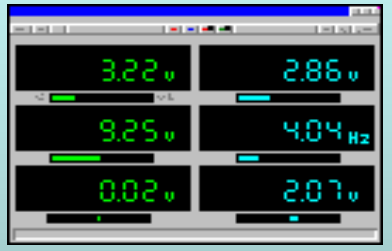
Reconfigurable Virtual Instrumentation

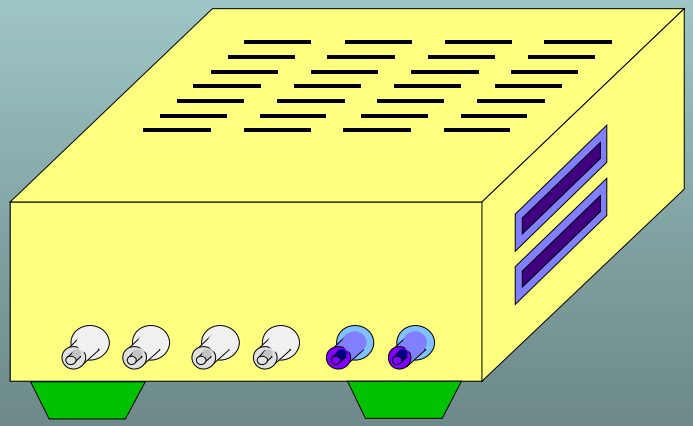
Function generator

Oscilloscope

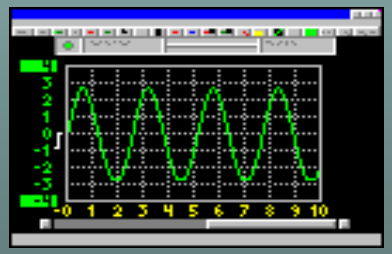


Multimeter

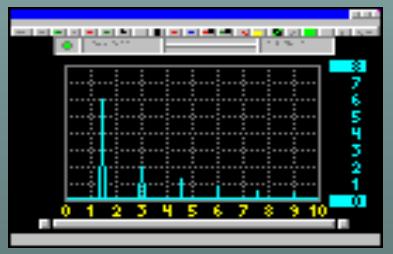




Transient recorder



Spectrum Analyzer



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Proposal for an RVI system

Goal

low-cost reusable common hardware/software platform for the emulation and evaluation of multiple electronic and scientific instrumentation systems

Hardware & Software modularity

- Block-based design methodology
- Hierarchical structure

Common standardized global architecture

- Block interfaces definition
- Clear mechanism of blocks interaction

Open Source & Open Cores

- Sharing the design effort and results by a large community of user and contributors with different expertise's and backgrounds (EE, Physicist, Comp. Sci. , DSP experts, etc)

RVI SYSTEM ARCHITECTURE

- ***Reconfigurable Instrument***
  - a versatile hardware device that can be reconfigured into different electronic instruments using a software tool

- ***Virtual Instrumentation***
  - a hardware and software combination that allows the emulation of an instrument through a custom virtual console and a graphical user interface

Challenges involved in RVI

A suitable hardware platform

- the magic box -

- Flexibility and Adaptability
  - to wide variety of requirements
- Upgradeability
  - must be able to take advantage of new electronics devices and facilities
  - mitigate the obsolescence of the hardware

A complete software chain

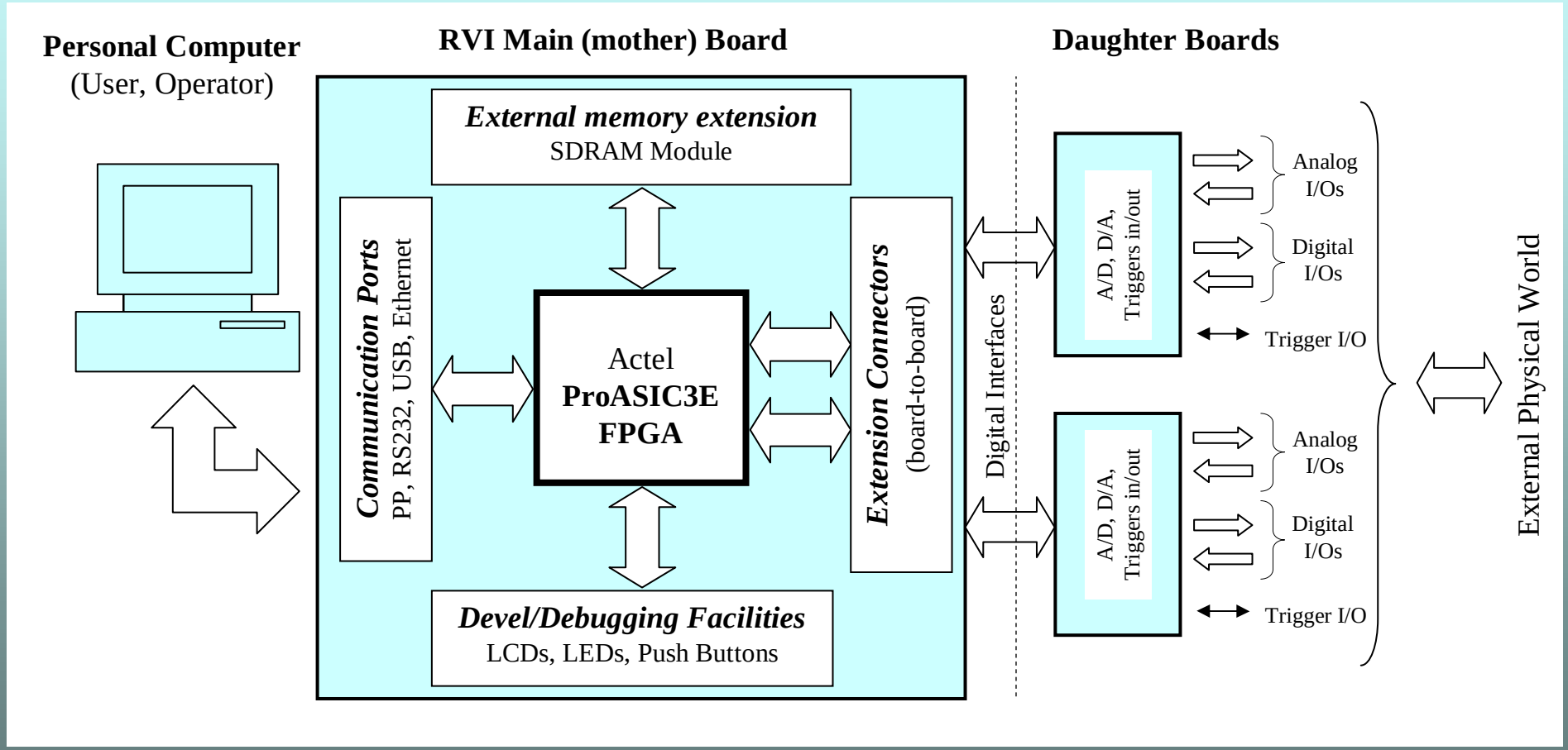
- from FPGA cores to GUI -

- Portability and Adaptability
  - Linux, Windows, others OS
  - FPGA vendors and families
  - PP, USB, Serial, etc.
  - expansion of the potential users/developers base
- Upgradeability
  - Migration to new version

High-Level RVI System Architecture

- Hardware sub-system
  - RI connected to PC through a physical connection.
- Software sub-systems
  - software related to the PC
  - the code corresponding to the FPGA of the RI

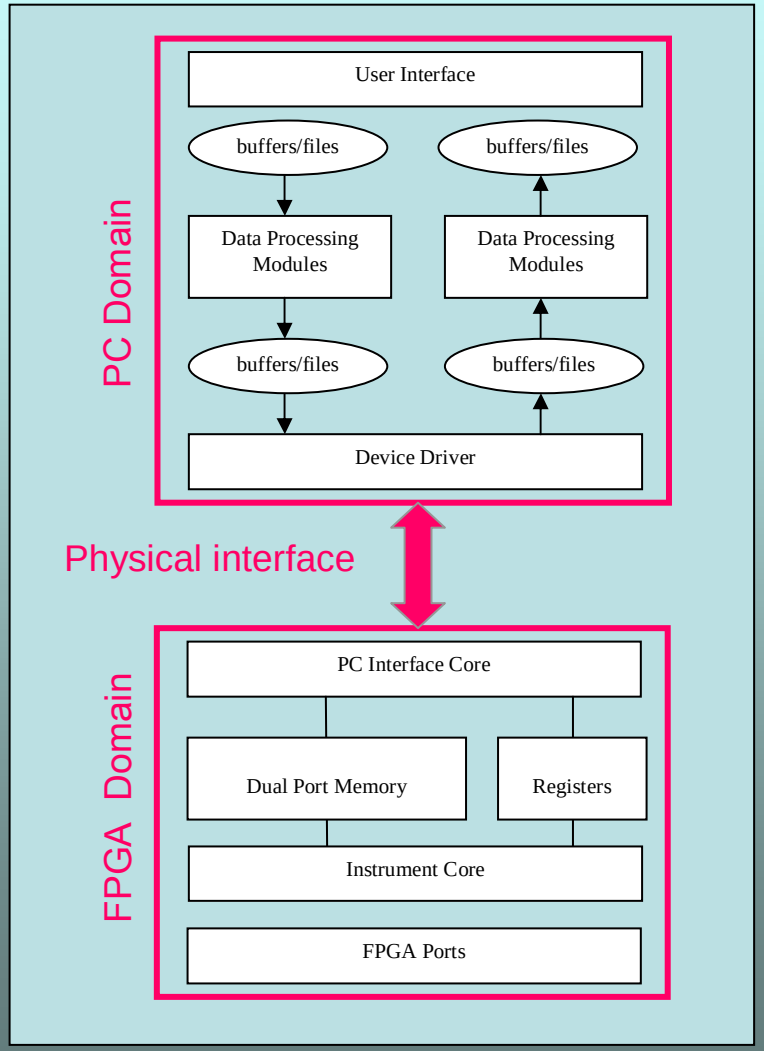
RVI Hardware System



Reconfigurable Instrument

- **RVI mother board** *http//www.ictp.it/~fpga*
  - FPGA device (ACTEL AP3E family)
  - a block of communication ports
  - an extension memory
  - debugging facilities and miscellaneous components
  - two high quality board-to-board connectors with 54 pins directly connected to the FPGA gp-I/O
- **Low Performance Daughter Board**
  - dual channel 10-bits 20 MSPS ADC (AD9201, Analog Devices),
  - dual channel 14-bit 1 MSPS DAC (LTC1654, Linear)
- **High Performance Daughter Board**
  - single channel 14-bits 125 MSPS ADC (LTC2255, Linear)
  - single channel 16-bit 50 MSPS DAC (LTC1668, Linear)

The Global Software Architecture



- ***Computer Software***

  user interface, port management, and offline data elaboration programs and utilities

- ***Synthesizable Hardware Description Code***

  management of the physical connection with the PC, ADC and DAC operations, data generation and acquisition, real-time online data processing, and on-board real time data handling

The Computer Software

- collection of independent modules hierarchically organized
- basically, the CS provides:
  - a generic RVI graphical and textual user interface
  - a library of virtual instruments with custom user interfaces
  - data storage facilities
  - physical communication control (drivers)
- optionally, the CS could also provide:
  - an internet connection for remote instrument control and operation
  - specific data analysis packages and other facilities
  - a friendly interface with a general purpose in-chip logic analyzer for development and debugging.

Synthesizable Hardware Description Code

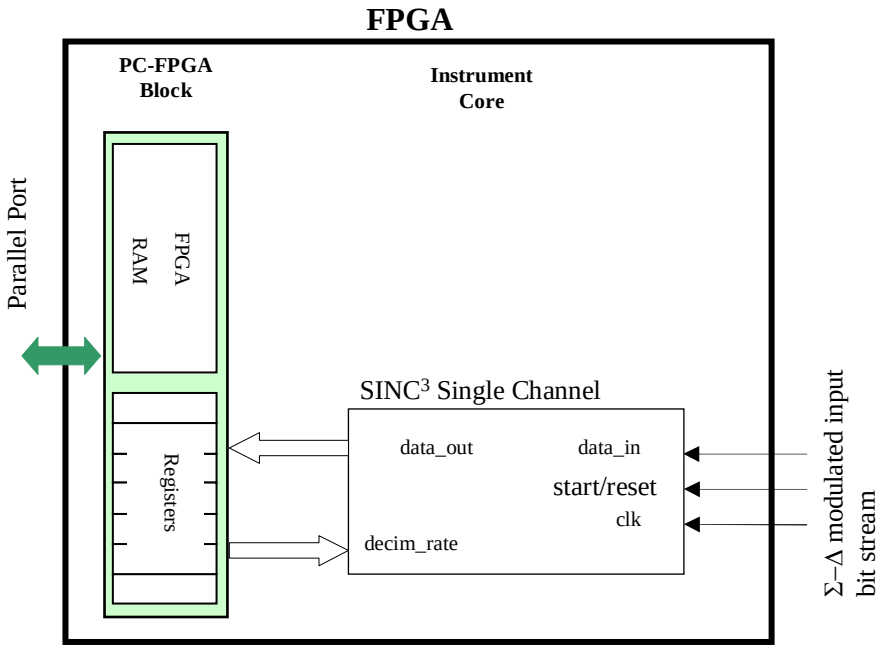
- a synthesis friendly VHDL description
- basically, the SHDC provides:
  - PC-FPGA communication block
  - the instrument core
  - external hardware specific interface block
  - FPGA port assignment (and other constraints) description file.
- optionally, the SHDC could include:
  - an external SDRAM module controller, an on chip logic analyzer and stimuli generator modules for debugging and development, and physical as well as timing constraints files.

Integrating a reconfigurable instrument core in an RVI system

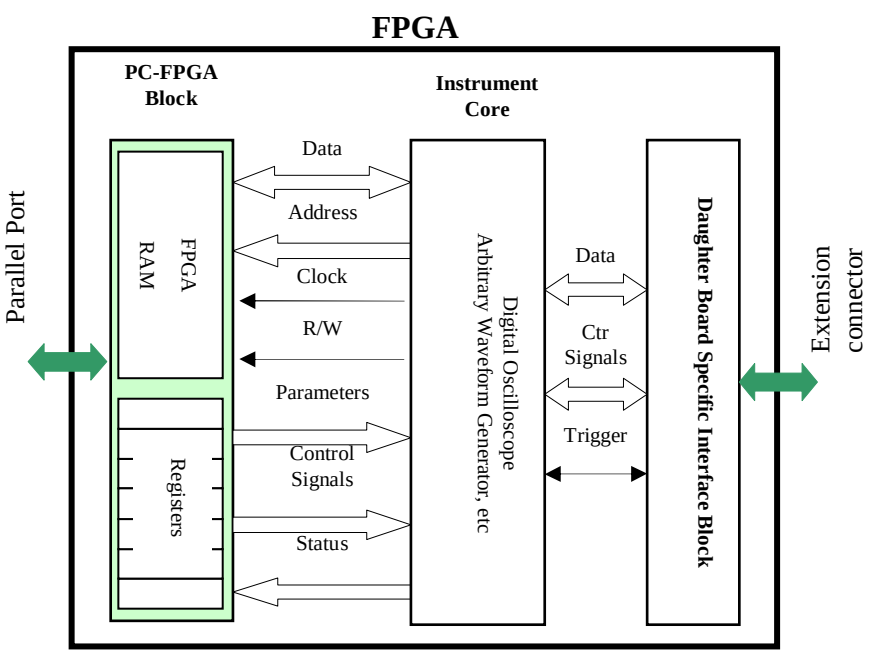
- The core must comply with
  - the standardized interfaces of the PC-FPGA communication block and the external hardware specific interface block
  - a common mechanism of interaction

- If the three main blocks: PC-FPGA communication block, instrument core, and the external hardware interface respect both previous conditions, then each block can be updated or upgraded independently and can be reused in different contexts.

Architecture for Single Instruments
Implementation Examples



Block diagram of the FPGA architecture for a Reconfigurable Σ–Δ demodulator for Anolog to Digital conversion.

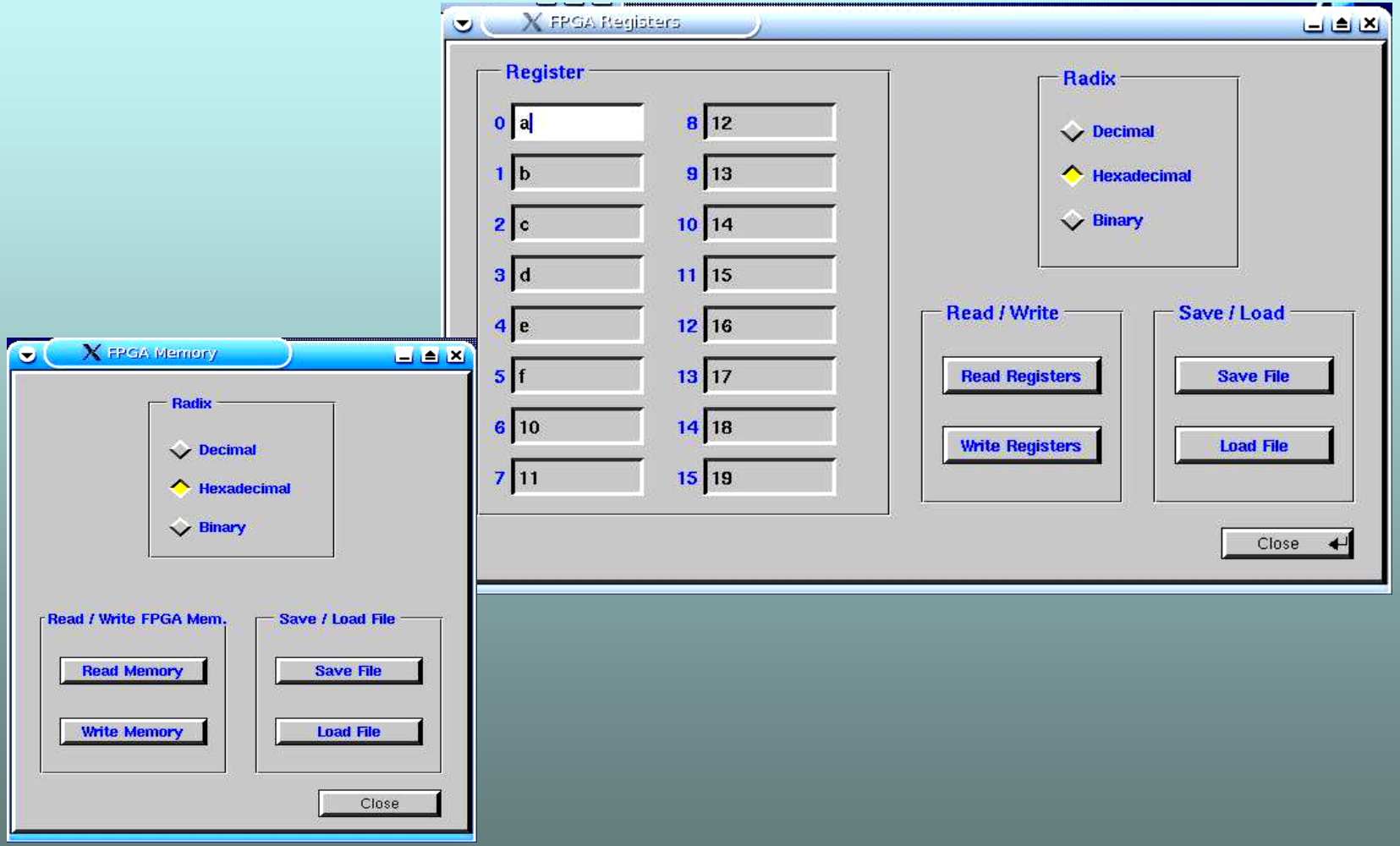


Block diagram of the FPGA architecture for a Reconfigurable Virtual Arbitrary Waveform Generator or Digital oscilloscope.

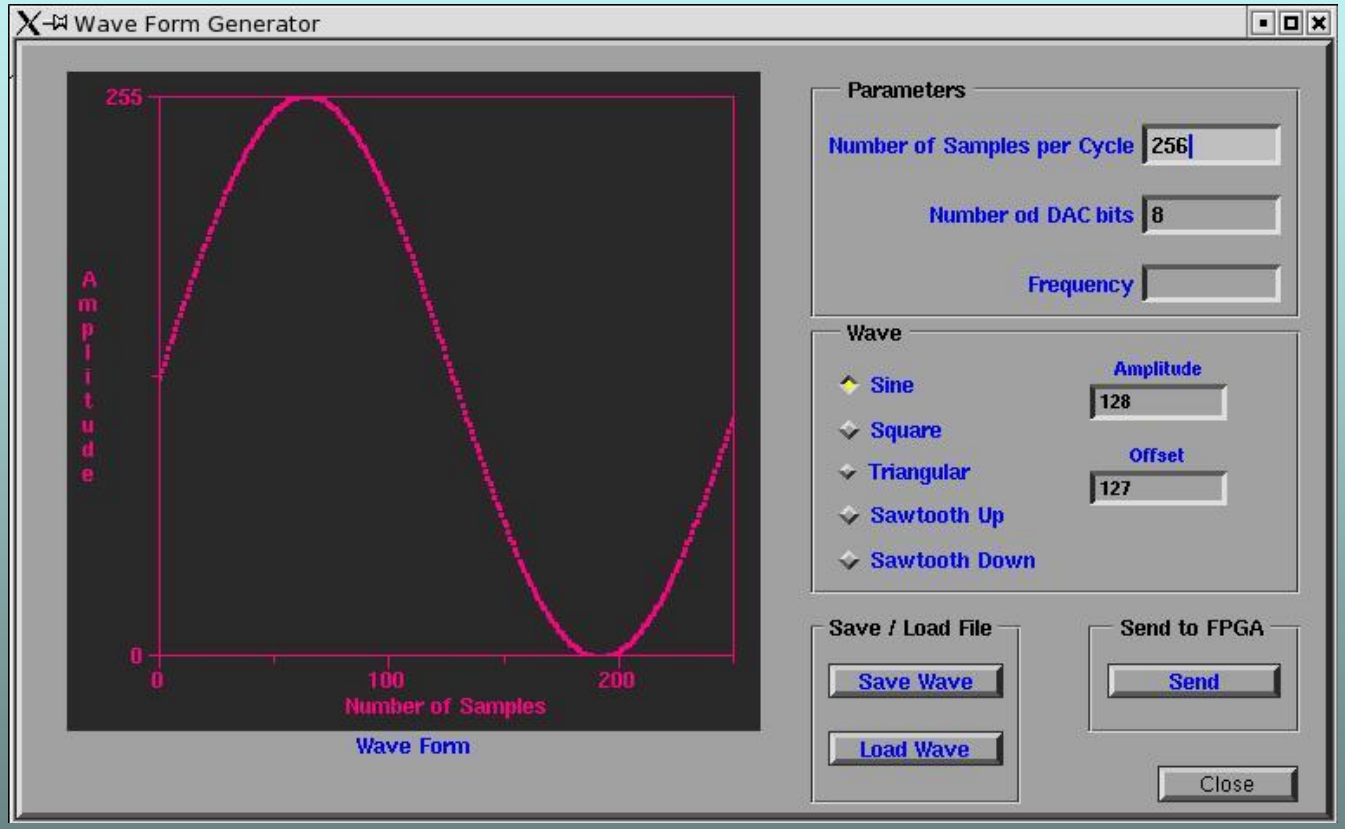
PC-FPGA Communication Block

- The communication between the PC and the Core Instrument is done in two ways:
  - by reading and writing data into the dual port memory.
  - by reading and writing into registers (read-only reg. for the Core Instrument, read-only reg. for the PC and reserved reg. to handle the RVI communication protocol).
- Depending on the core instrument:
  - the RI may send an interrupt signal to the PC to trigger a specific action.
  - the PC can do polling on specific registers to check whether there's a request for a given action.

General Purpose Debugging Interface



GUI for a Wave Form Generator



- DAC (Linear 1668)

  14bit @ 1MSPS

A possible FPGA Global Architecture for RVI

1) PC <-> FPGA communication

2) External Hardware

3) Instruments cores

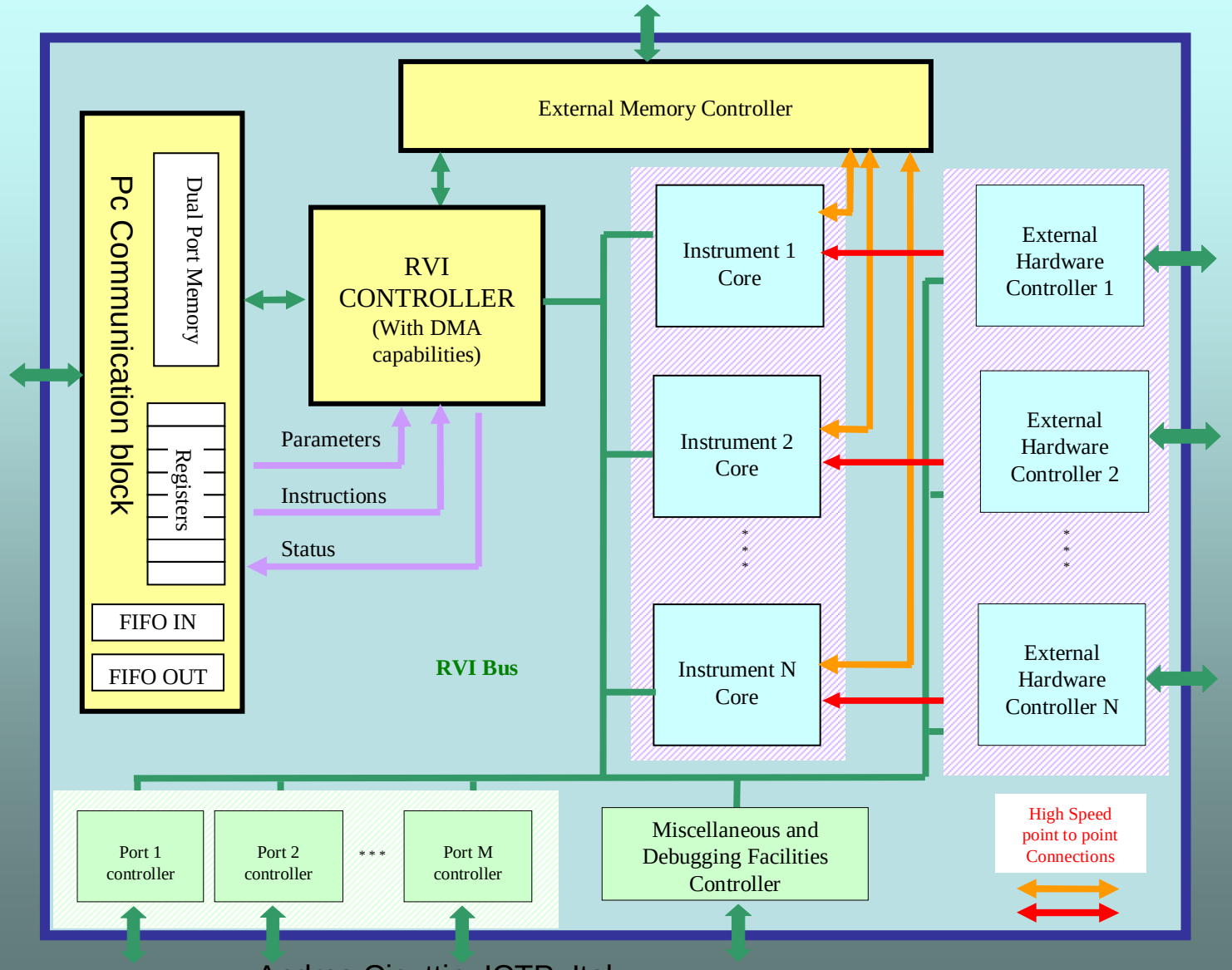
4) External memory

5) Standard Ports

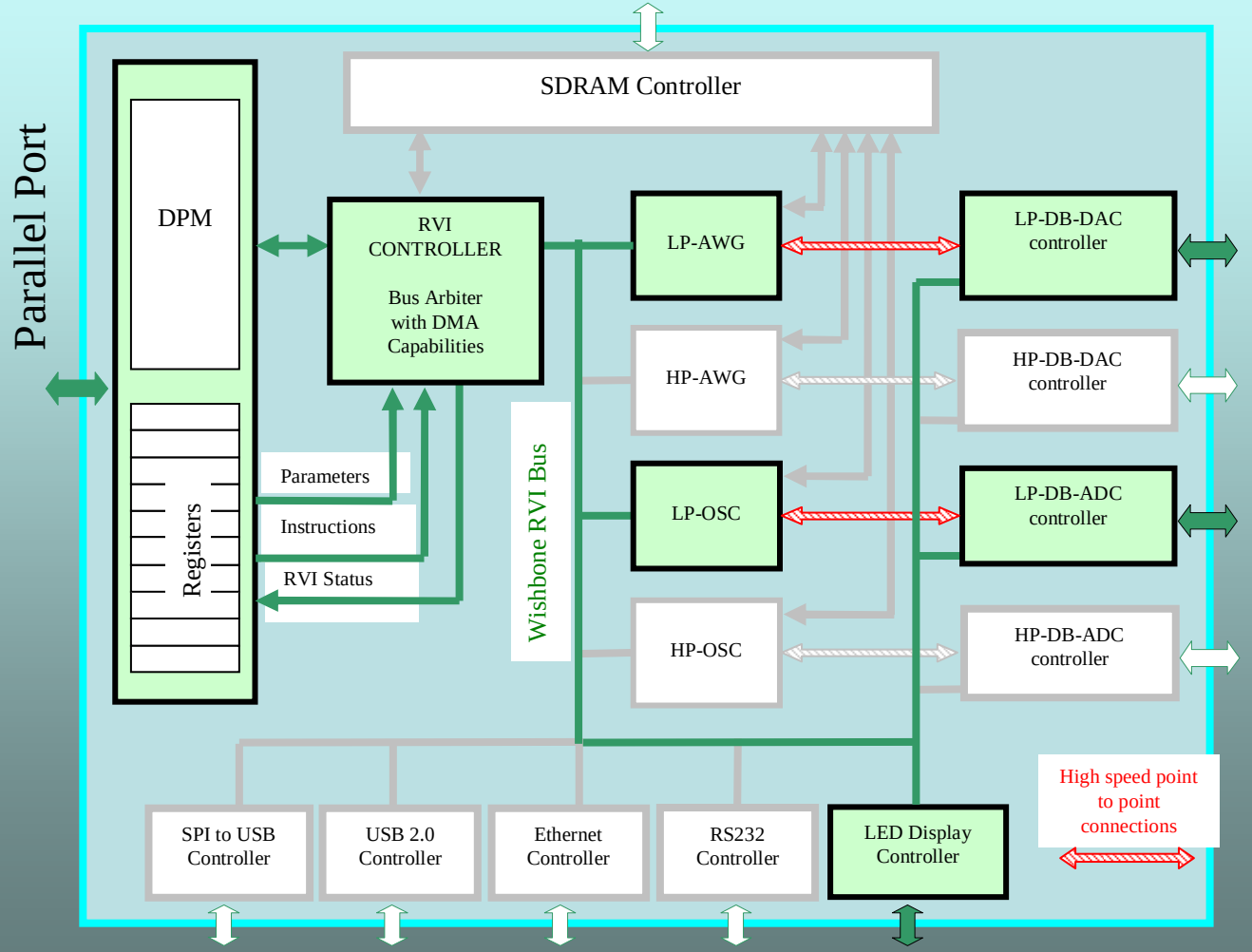
6) Debugging Facilities

7) Global bus and interconnections

8) RVI Control



Concrete architecture for our RVI hardware platform



Conclusion

- **FPGA technologies are opening up new opportunities including in the field of scientific instrumentation**

  reasonable hardware cost/performance ratio

  high effort required to develop all the software/hardware chain of new systems

  wide freely available collection/library of standardized functional blocks (at PC and FPGA levels)

Conclusion

- **RVI Platform**

  Many areas of applications from basic research to Industry

  Emulation of:
  - standard general purpose instruments
  - sophisticated instrumentation for custom specific applications

  Low cost solution for universities and research institutions in developing countries

Conclusion

- **The RI could be seen as a parallel coprocessor of the PC**

Reconfigurable Computing

Accelerate execution of time consuming or time critical tasks
- online digital signal processing
- real time hardware control

Conclusion

- **Open Source & Open Core Approach**

  Is Affordable and Accessible

  Stimulates Scientific Research and Production of Intellectual Properties

  Encourages South-South and Industry-Academy cooperation

  Creates new business opportunities based on free software and double licensing schemes