



The Abdus Salam  
International Centre for Theoretical Physics



**310/1780-2**

**ICTP-INFN Advanced Training Course on  
FPGA and VHDL for Hardware Simulation and Synthesis  
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## ***DIGITAL DESIGN 2***

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***These lecture notes are intended only for distribution to participants***

# Outline

## ■ Digital CMOS Design

- Boolean Algebra

- Basic Digital CMOS Gates

- Combinational and Sequential Circuits

- Coding - Representation of Numbers



# Basic CMOS Gates

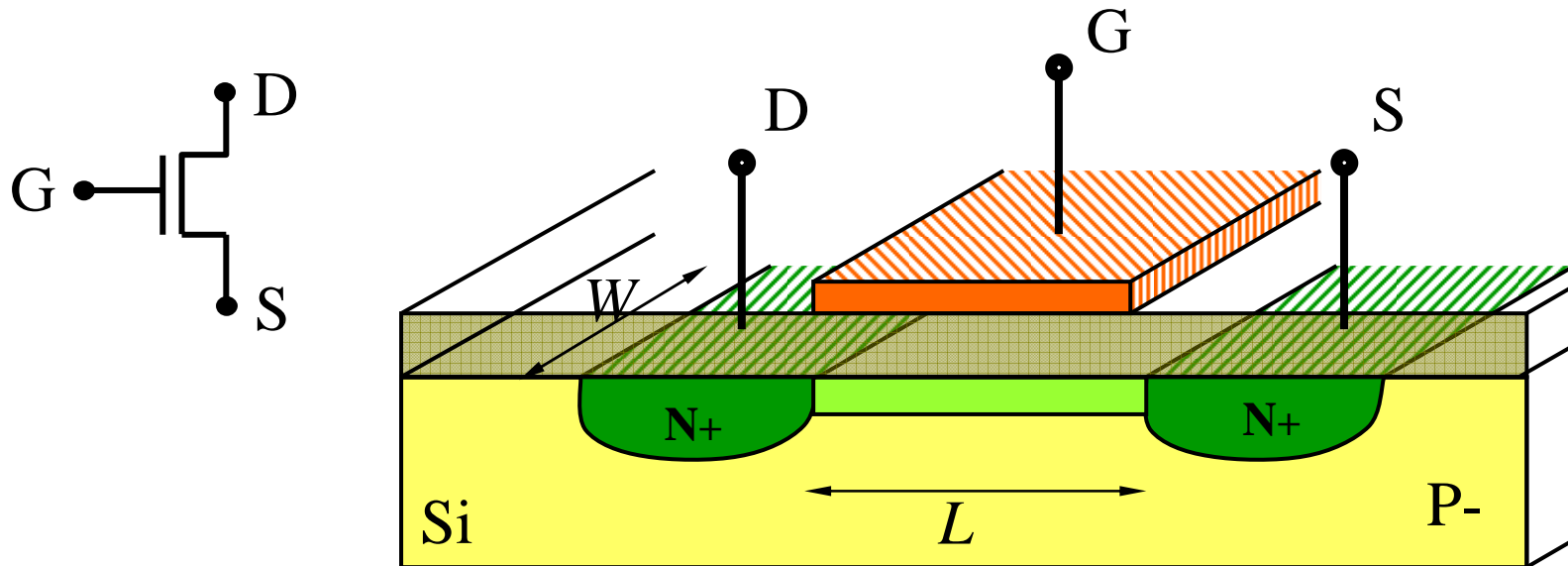
How to implement Boolean functions  
in CMOS technology ?

Which functionality is available



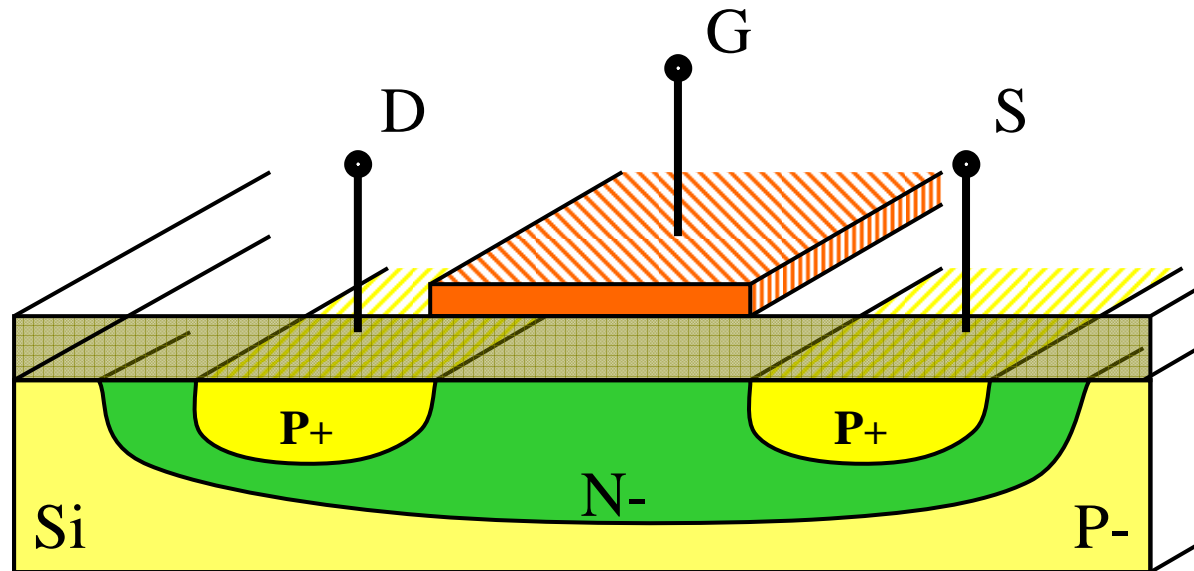
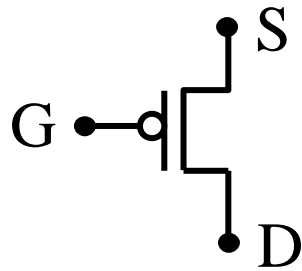
# Basic CMOS Gates

## N-MOS transistor



# Basic CMOS Gates

## ○ P-MOS transistor



# Basic CMOS Gates

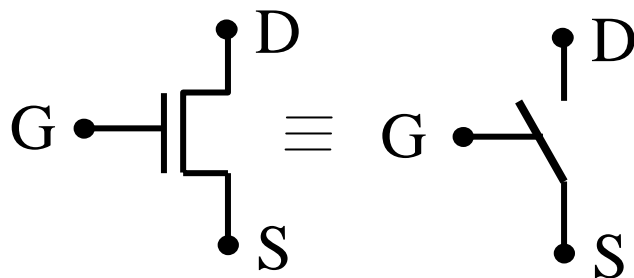
The electrical behaviour of a MOS transistor  
is very complex

Design of a multi-million transistor circuit ?

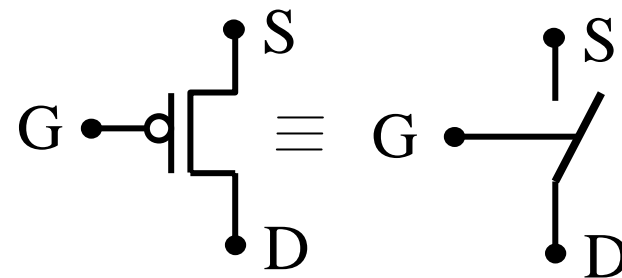


# Basic CMOS Gates

In digital circuit a MOS transistor can be modeled as a switch



$D = S$  when  $G = 1$



$D = S$  when  $G = 0$

## Basic CMOS Gates

When driving a MOS transistor can be seen as a Resistor

$$R \propto \frac{L}{W}$$

For the same size, a P-MOS is twice more resistive than an N-MOS





## Basic CMOS Gates

The N-MOS and P-MOS are not exactly symmetric

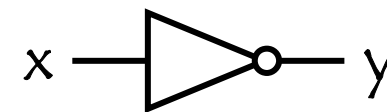
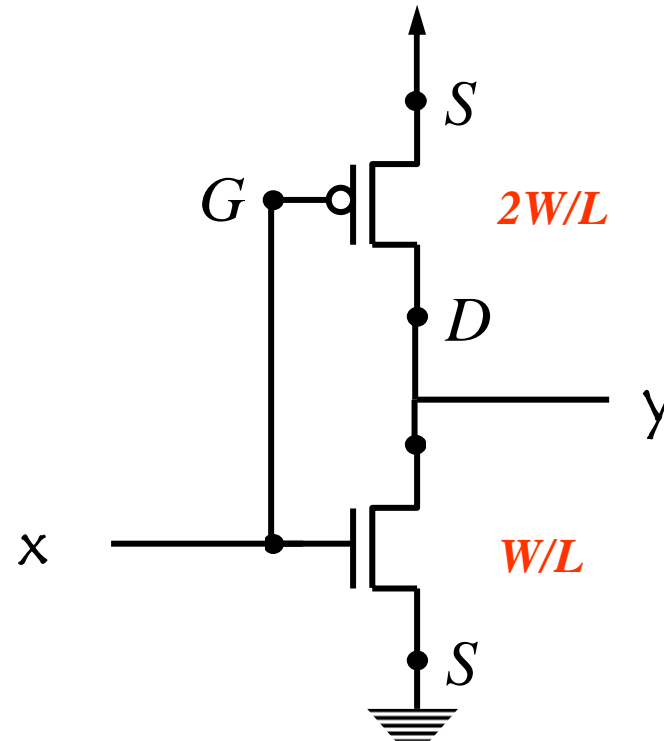
A N-MOS is a good transmitter of 0

A P-MOS is a good transmitter of 1



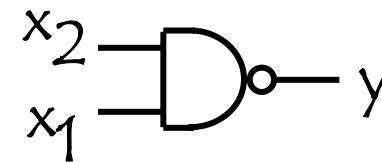
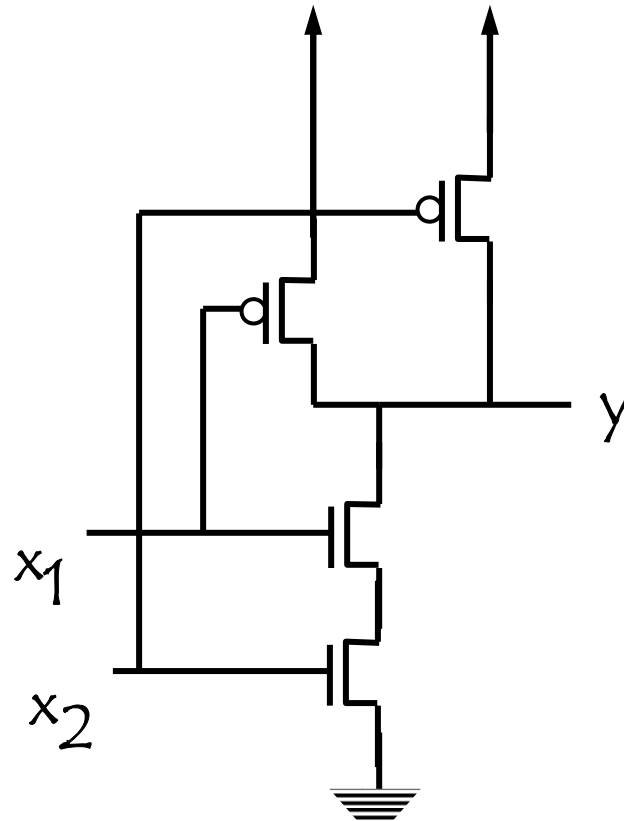
# Basic CMOS Gates

$$y = \text{Not } x$$

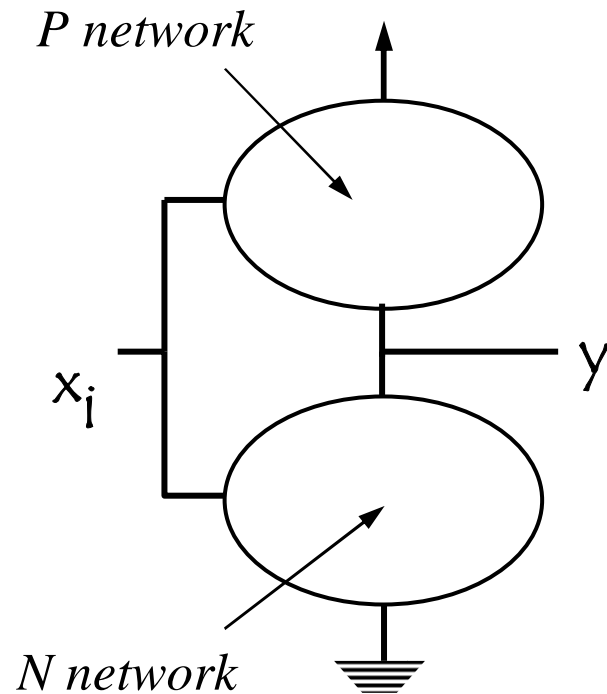


# Basic CMOS Gates

$$y = \overline{x_1 \cdot x_2}$$



# Basic CMOS Gates



The P-network must be the dual of the N-network

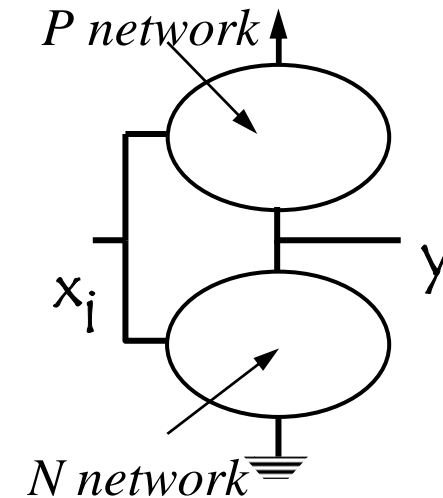
Series  $\longrightarrow$  Parallel  
Parallel  $\longrightarrow$  Series

Take care of the size of transistors

## Basic CMOS Gates

- To set the output to 0 a path has to be created through the N network
- A series of N-transistor must be conducting

$$\prod x_i = 1$$



Only negative (inverting) functions can be created

## Basic CMOS Gates

Implementing a Boolean function with a CMOS gate ?

- The function must be inverting in regard of all the variables
- Put the function in the form of  $f = \bar{g}$
- Design the N-network of  $g$



## Basic CMOS Gates

### Implementing a Boolean function with a CMOS gate ?

- In the expression of  $g$  each  $'.'$  are two paths in series
- In the expression of  $g$  each  $'+'$  are two paths in parallel
- The P-network is the dual network of the N-network
- **Avoid putting more than 3 transistors in series**



# Basic CMOS Gates

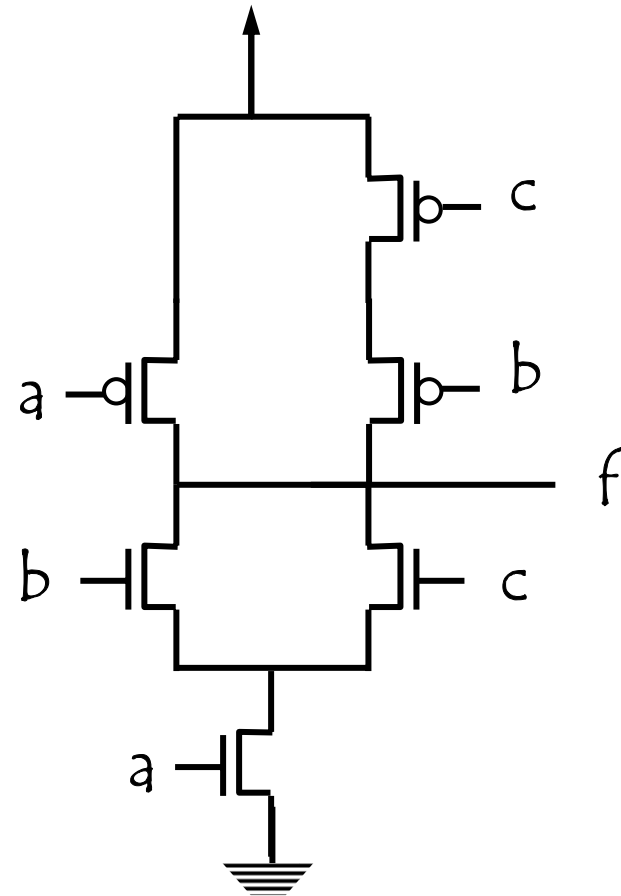
Example :

$$f = \bar{a} + (\bar{b} \cdot \bar{c})$$

$$f = \bar{a} + \overline{(b+c)}$$

$$f = \overline{a \cdot (b+c)}$$

$$g = a \cdot (b+c)$$





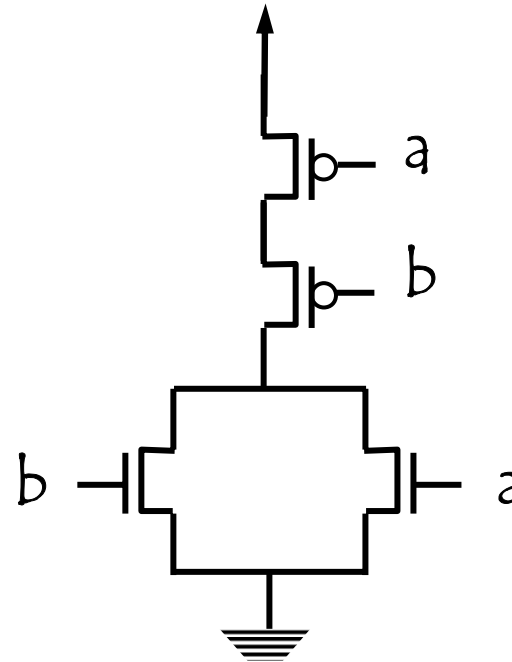
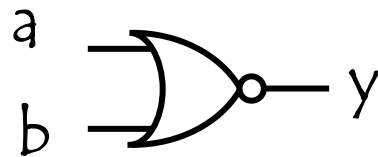
# Basic CMOS Gates

Some gates :

Inverter :  $f = \bar{a}$

Nand :  $f = \overline{a.b}$

Nor :  $f = \overline{a+b}$

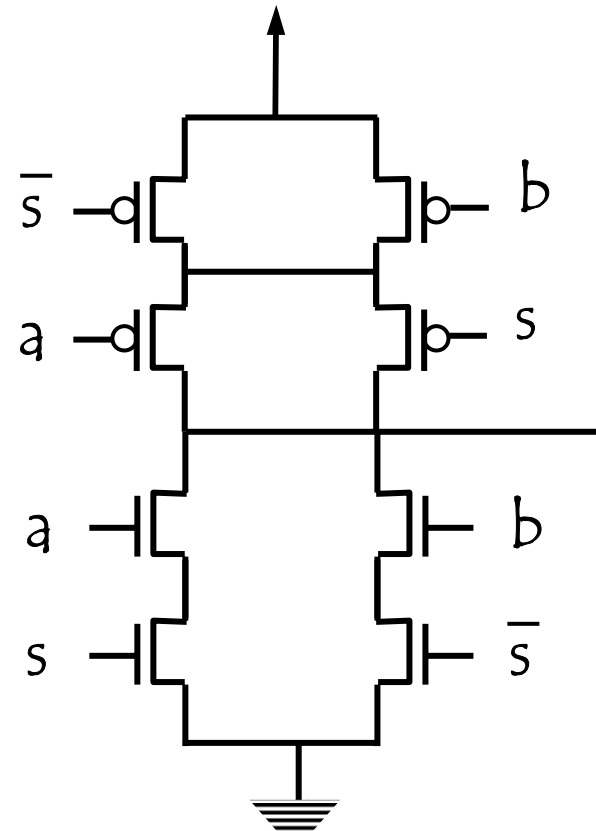
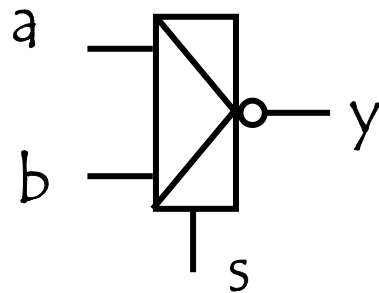


# Basic CMOS Gates

Some gates :

Multiplexer :

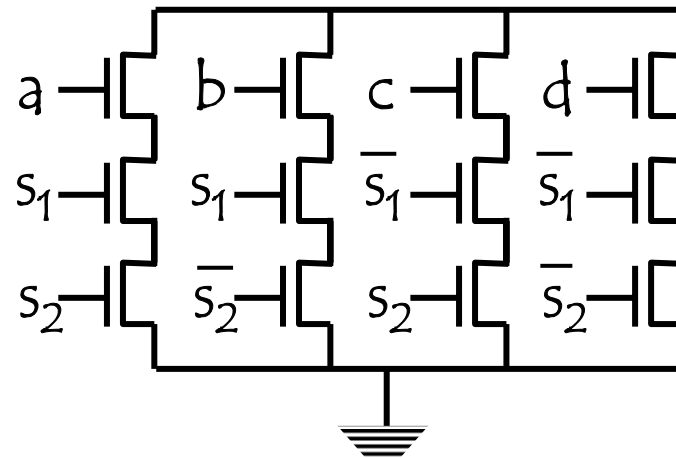
$$f = a.s + b.\bar{s}$$



# Basic CMOS Gates

Some gates : Multiplexer :

$$f = a.s_1.s_2 + b.s_1.\bar{s}_2 + c.\bar{s}_1.s_2 + d.\bar{s}_1.\bar{s}_2$$

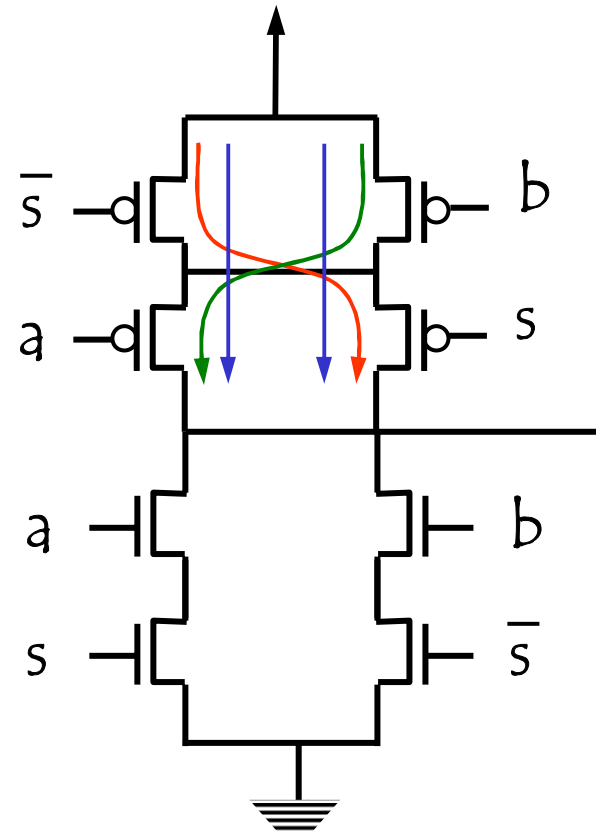


# Basic CMOS Gates

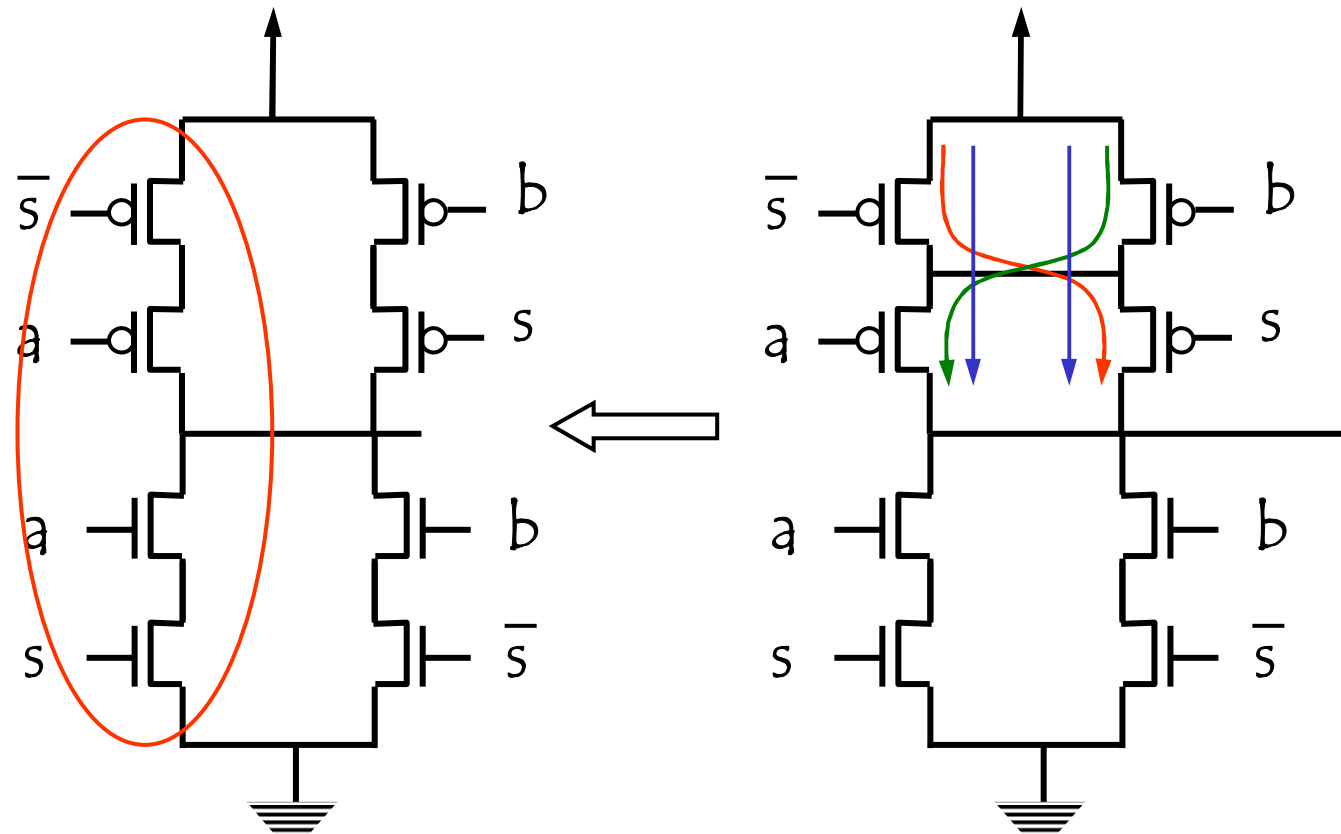
Some gates :

Multiplexer :

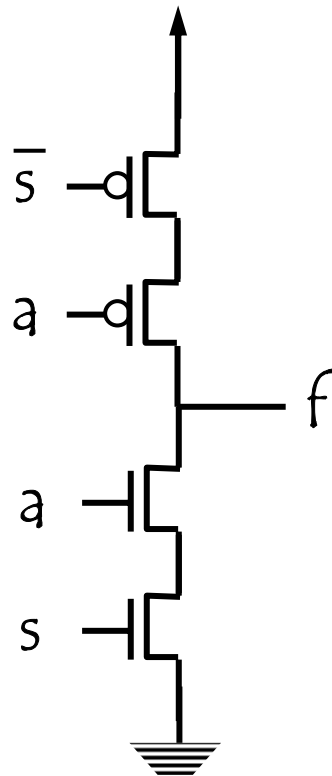
$$f = \overline{a.s} + b.\overline{s}$$



# Basic CMOS Gates

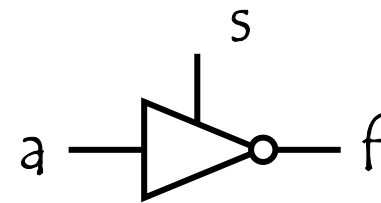


# Basic CMOS Gates



If  $s = 1$   
 $f = \overline{a}$

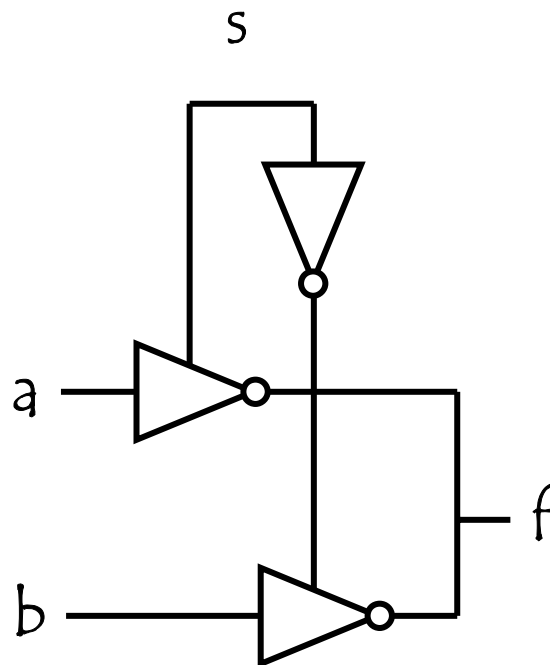
If  $s = 0$   
 $f$  is not defined



Tri-state driver

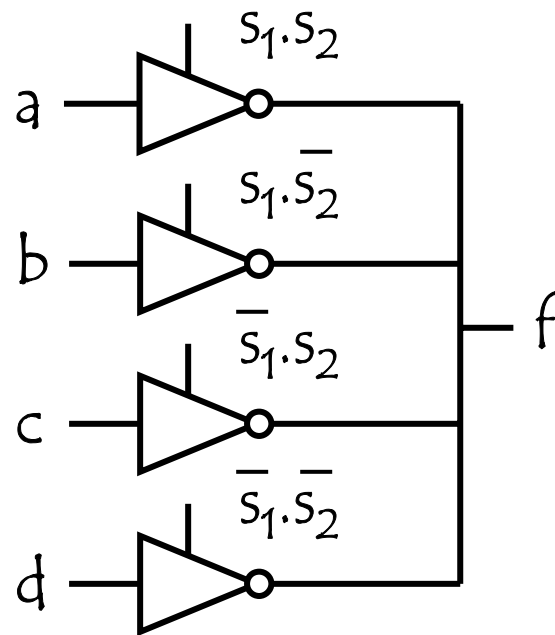
# Basic CMOS Gates

Some gates : Multiplexer :



# Basic CMOS Gates

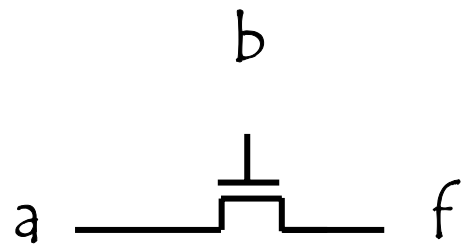
Some gates : Multiplexer :





# Basic CMOS Gates

Some gates :



If  $b = 1$     If  $b = 0$   
 $f = a$          $f$  is not defined

→ If  $a = 0$  then  $f = 0$   
→ If  $a = 1$  then  $f = 1$

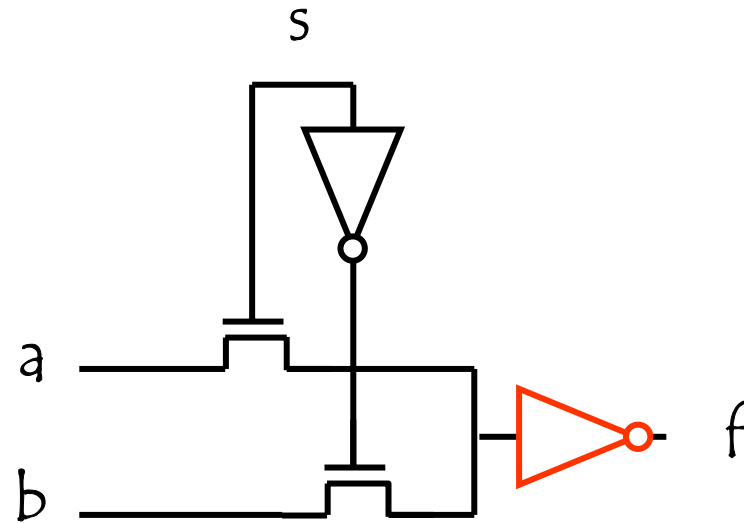
Pass-transistor

# Basic CMOS Gates

Some gates :

Multiplexer :

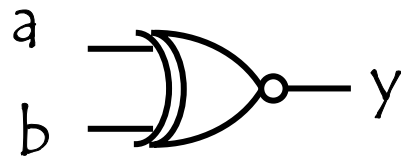
$$f = a.s + b.\bar{s}$$



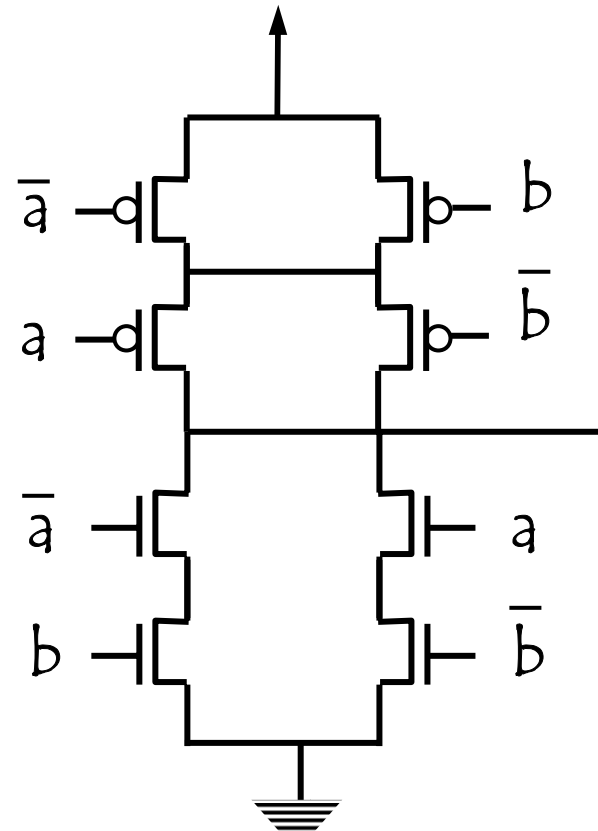
# Basic CMOS Gates

Some gates :

$$\text{Nxor} : f = \overline{\bar{a}.b + a.\bar{b}}$$



I need  $\bar{a}$  and  $\bar{b}$



# Basic CMOS Gates

Some gates :

Nxor with Pass-transistors :

$$f = \overline{\overline{a} \cdot b} + a \cdot \overline{b}$$

a	b	f
0	0	1
0	1	0
1	0	0
1	1	1

