The Abdus Salam
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Energy Agency

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ICTP-INFN Advanced Traning Course on
FPGA and VHDL for Hardware Simulation and Synthesis
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VHDL & FPGA – Session 6

Nizar ABDALLH
ACTEL Corp.
2061 Stierlin Court
Mountain View, CA 94043-4655
U.S.A.

ProASIC3 ProASIC3E

Actel

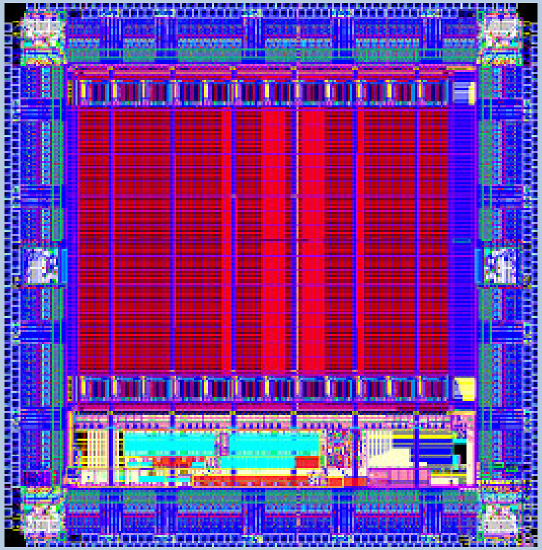
Actel's 3rd Generation
Flash FPGA Family

Designing with ProASIC3
Agenda

- Family Overview
- Architecture Overview
- System-Level Considerations
- Software for PA3
  - **Designer Flow**
  - **Clock Conditioning Circuitry**
  - **Using Globals**
  - **Using I/Os**
- Programming and Hardware Tools

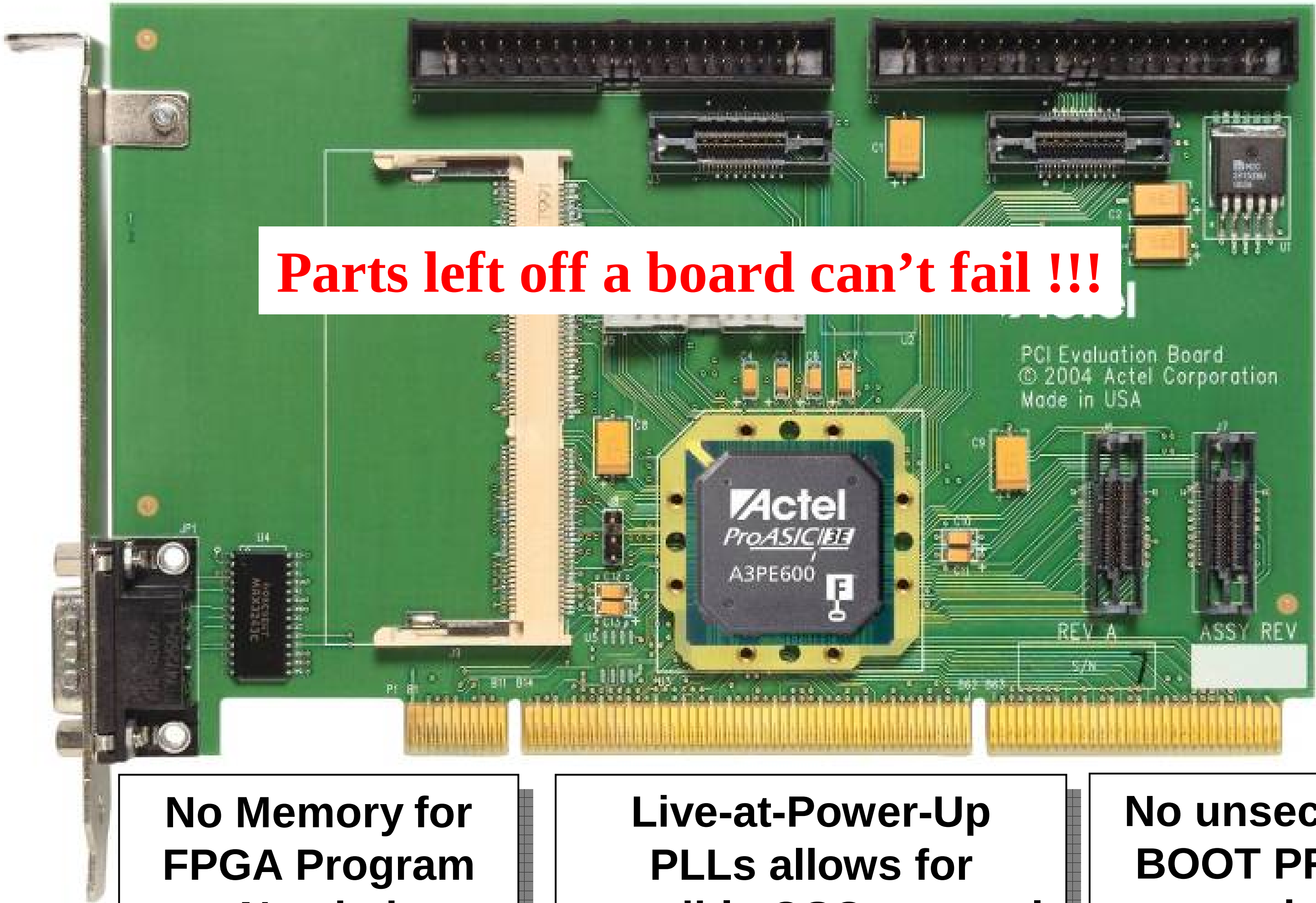
ProASIC3
The Value Market FPGA

- World's Lowest-cost FPGA Solution
  - **130nm 7LM Flash-Based CMOS FPGA**
  - **Lowest *Total* System Cost**
    - **Flash Technology Eliminates SRAM FPGA Cost Penalty**
- Unique Set of ASIC-like Attributes
  - **High Performance – *Twice* that of ProASIC^PLUS^**
  - **On-Chip User Nonvolatile Flash Memory**
  - **Highly Secure**
  - **High Reliability / Firm-Error Immunity**
  - **Single Low-Power Chip, Live at Power-Up**



Single Chip – Lower System Cost ProASIC3

Live-at-Power-Up CPLD Functions moved to FPGA



Parts left off a board can't fail !!!

No need for SRAM FPGA brown-out protection

Smaller (Single Voltage) power supply needed

No Memory for FPGA Program Needed

Live-at-Power-Up PLLs allows for possible OSC removal

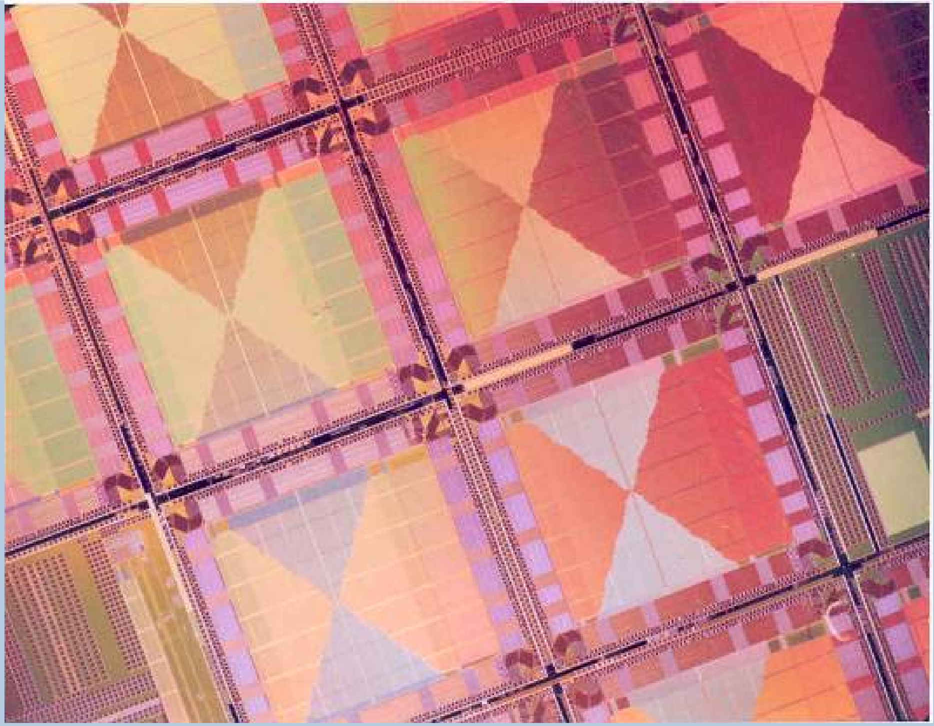
No unsecured BOOT PROM needed

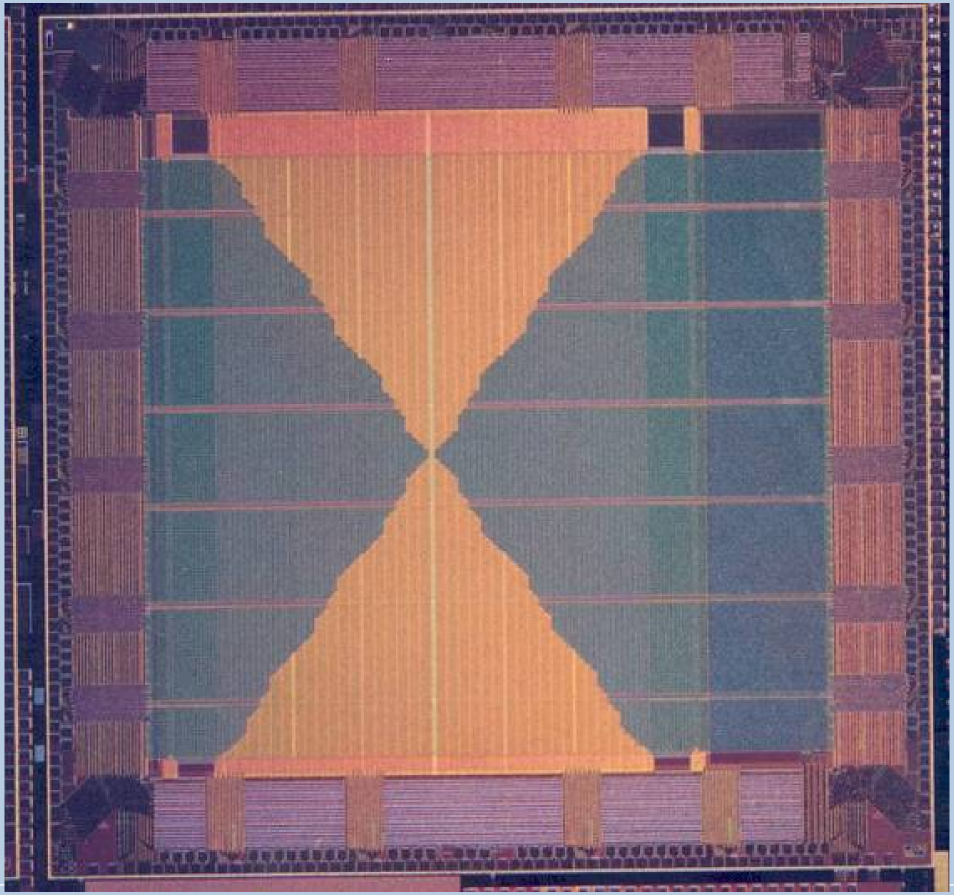
ProASIC3/E Family

	A3P 030	A3P 060	A3P 125	A3P 250	A3P 400	A3P 600	A3P 1000	A3PE 600	A3PE 1500	A3PE 3000
System Gates	**30K**	**60K**	**125K**	**250K**	**400K**	**600K**	**1M**	**600K**	**1.5M**	**3M**
Tiles (D-FF)	**768**	**1536**	**3072**	**6144**	**9216**	**13824**	**24576**	**13824**	**38400**	**75264**
Ram K Bits	**-**	**18**	**36**	**36**	**54**	**108**	**144**	**108**	**270**	**504**
4608-bit blocks	**-**	**4**	**8**	**8**	**12**	**24**	**32**	**24**	**60**	**112**
Flash (ROM) bits	**1K**	**1K**	**1K**	**1K**	**1K**	**1K**	**1K**	**1K**	**1K**	**1K**
Secure (AES) ISP	**No**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
PLLs	**-**	**1**	**1**	**1**	**1**	**1**	**1**	**6**	**6**	**6**
Globals	**6**	**18**	**18**	**18**	**18**	**18**	**18**	**18**	**18**	**18**
I/O	**Std, HS**	**Std+**	**Std+**	**Std+/LVDS**	**Std+/LVDS**	**Std+/LVDS**	**Std+/LVDS**	**Pro**	**Pro**	**Pro**
I/O Banks (+ JTAG)	**2**	**2**	**2**	**4**	**4**	**4**	**4**	**8**	**8**	**8**
Single Ended and Double Ended I/O (pairs)										
QN132	**81**									
VQ100	**79**	**71**	**71**	**68/*13***						
FG144		**96**	**97**	**97/*22***	**97/*22***	**97/*22***	***97/22***			
TQ144		**86**	**104**							
PQ208			**133**	**151/*34***	**151/*33***	**154/*35***	**154/*35***	**147/*49***	**147/*65***	**147/65**
FG256				**157/*34***	**178/*38***	**179/*45***	**179/*45***	**165/*68***		
FG484					**194/38**	***227/56***	**288/*68***	**270/*132***	**280/*136***	**280/*136***
FG676									**425/*204***	
FG896										**604/*296***

Architecture

ProASIC3E Die





ProASIC3
Architectural Features

- Core Cell
- Routing Resources
- Clock Conditioning Circuits (CCCs) and PLLs
- Embedded Features
  - **RAM/FIFOs**
  - **FROM**
  - **AES**
- I/Os
  - **Standards**
  - **Options (Pull-ups, Pull-downs, Drive Strength, Slew Rates, DDR Send/Receive)**

ProASIC3 vs. ProASIC3E
Architectural Differences

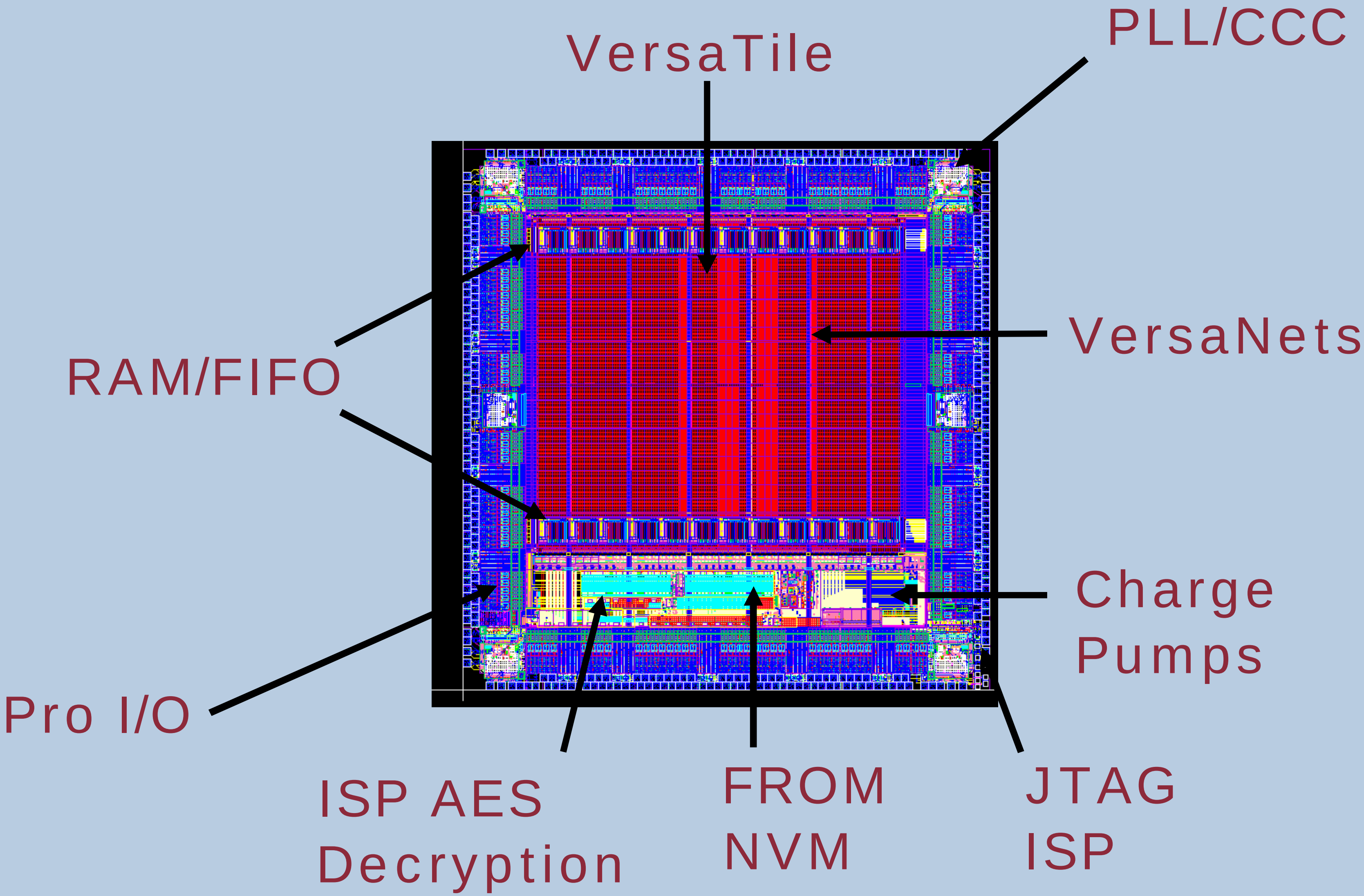
I/O

- **ProASIC3E – Pro I/Os**
  - **All Supported Standards**
- **ProASIC3 – Advanced I/Os**
  - **All Single-Ended Standards with Limited LVDS Support**
    - ***Smaller Devices – No LVDS***
    - ***Larger Devices – 2 Banks with LVDS Support***

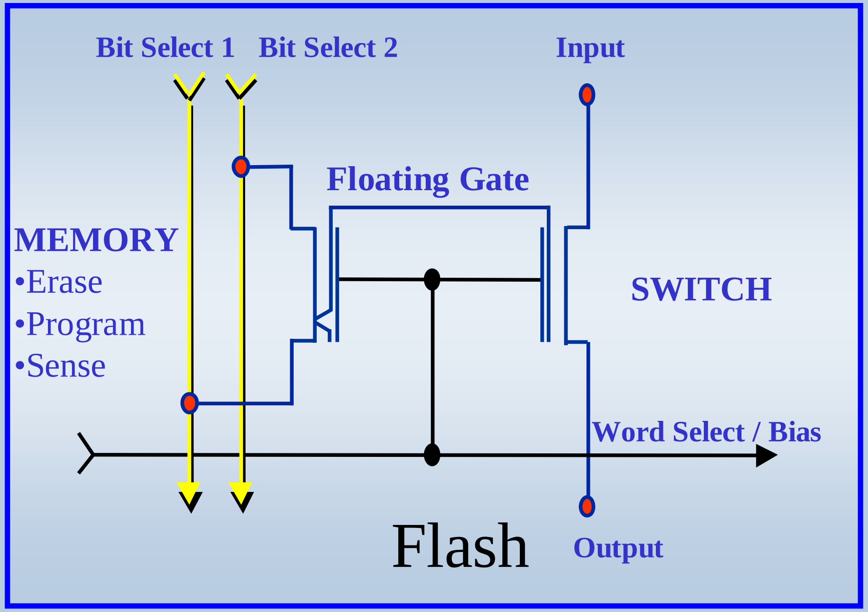
PLL

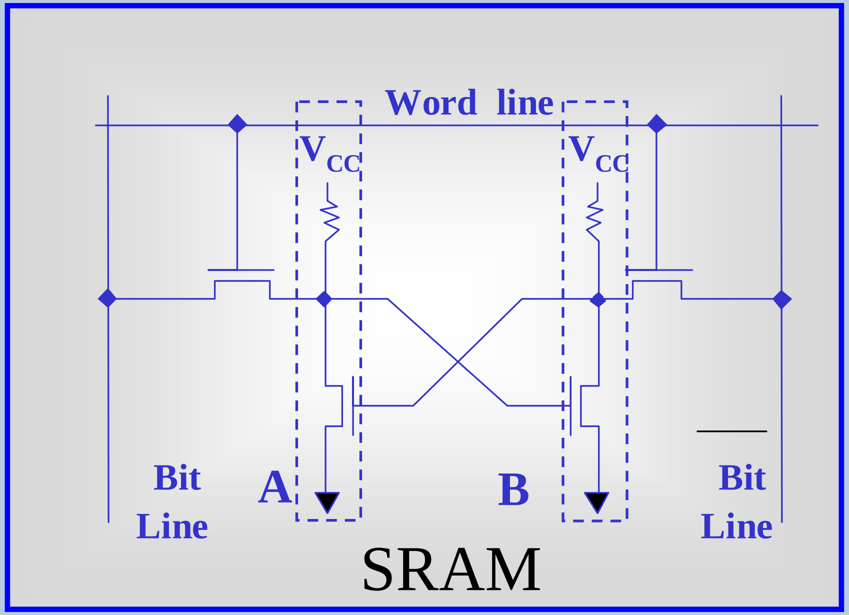
- **ProASIC3E – 6 PLLs**
- **ProASIC3**
  - **All Devices Except A3P030 – 1 PLL**
  - **A3P030 – No PLL**

ProASIC3
Typical Floorplan



Flash Switch





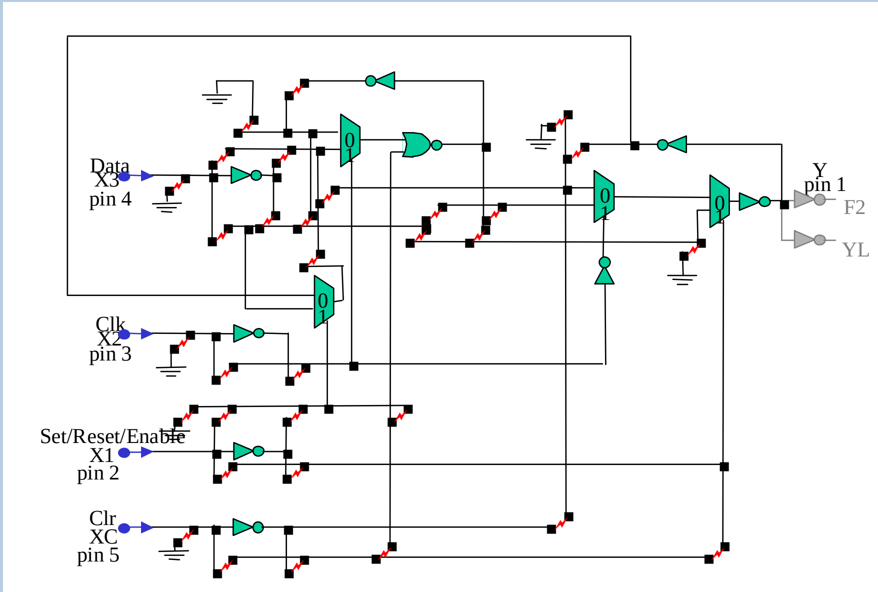
■ Flash Advantages

- **Smaller size - more switches for greater routing flexibility**
- **Low power: less capacitance and resistance**
- **Re-programmable <u>and</u> non-volatile**

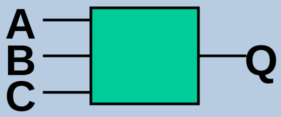
Core Cell

ProASIC3
Fine-Grained Architecture

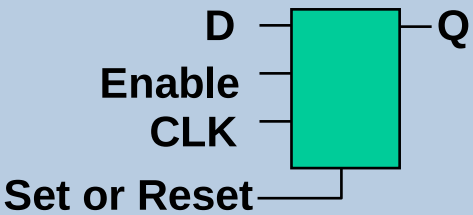
- **Up to 75,264 VersaTiles**
  - **Each VersaTile Can Be**
    - **3-input Combinatorial Gate**
    - **Latch**
    - **D-Flip-flop with Enable**
  - **Register-intensive Applications Handled Easily**
- **All Input Signals Can Be Inverted**
  - **Easier Technology Mapping and Netlist Optimizations**



Combinatorial
Any Function of 3 Inputs (3 LUT Equivalent)



Sequential
D Flip-Flop With Enable and Set or Reset



From APA to ProASIC3
Impact of Core Cell Changes

- **Improved Tile Utilization vis-à-vis APA**
  - **8.2% - Enable FF**
  - **9.2% - LUT3 Mapping**
  - **~10% for Typical Design**
    - **Impact Can Be Significantly Higher**
- **Improved D-FFE**
  - **Eliminates One Logic Level in Path IF 4th Input (SET/CLR) Is Accessed via VersaNet Global Network**

NOTE: If 4th Input NOT on Global, D-FFE 'Demoted' to Two-Tile Flip-Flop!

Routing

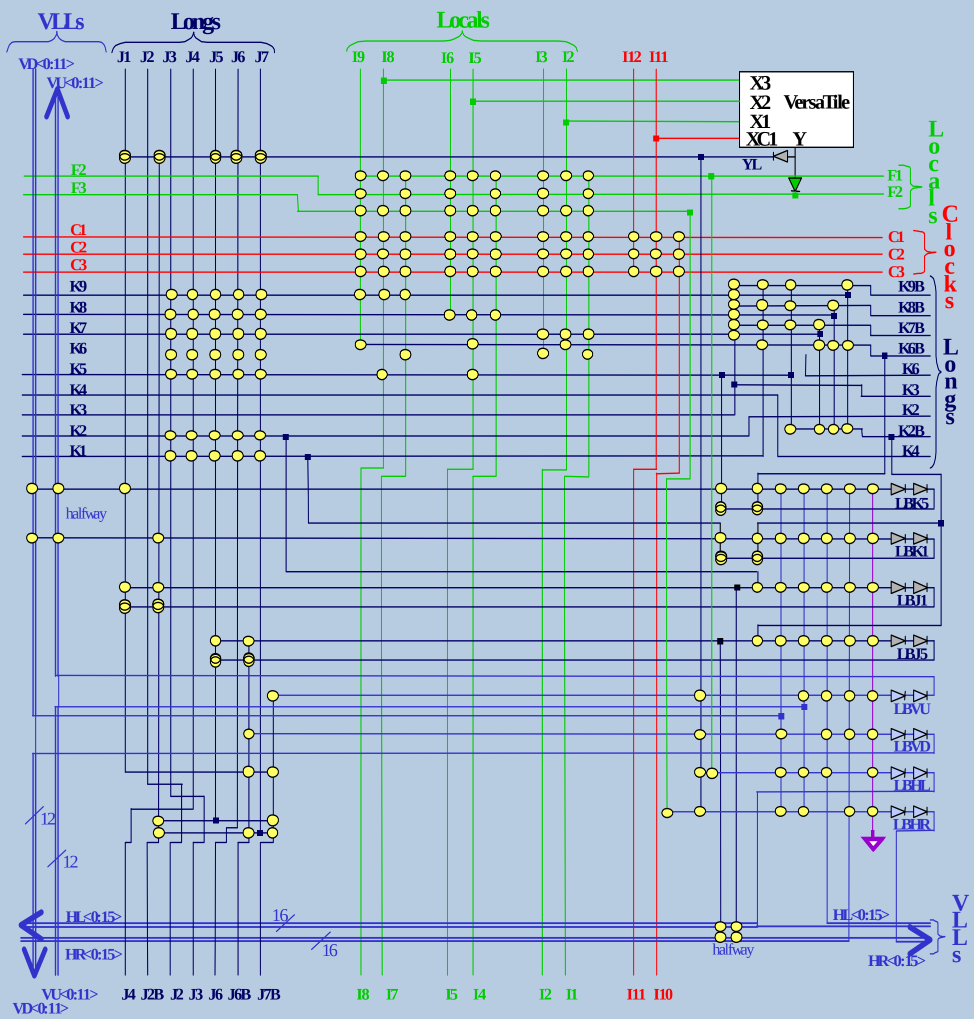
Actel

ProASIC3
Routing Resources

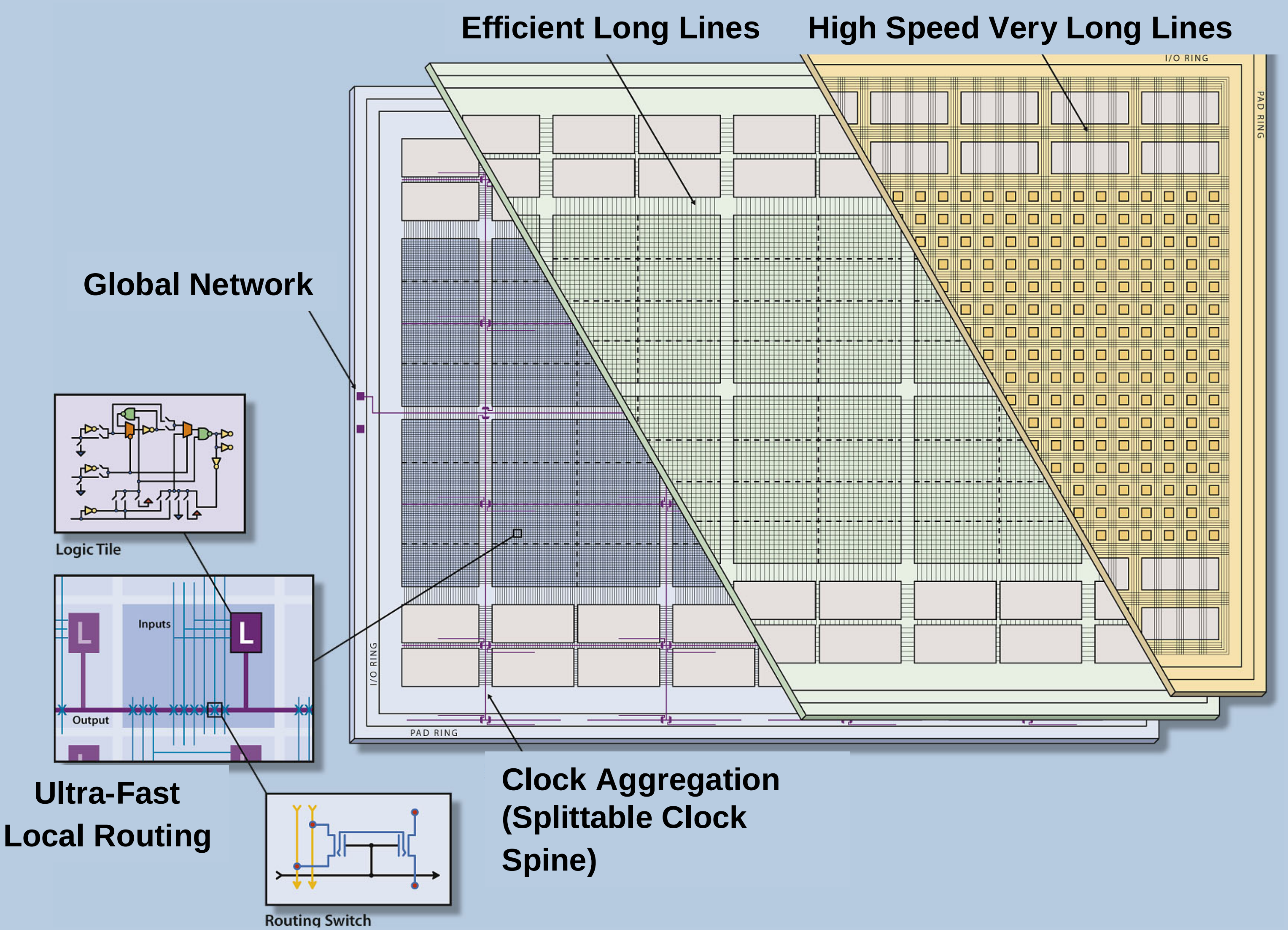
- **Enhanced High-performance Routing Hierarchy**
  - **Ultra-fast Local Network (VersaTile-to-VersaTile)**
  - **Efficient Discrete Long-line Network (1, 2 and 4 VersaTiles Long)**
  - **High-speed Very-long-line Network**
  - **<u>Nine</u> Low-skew *VersaNet* Global Networks**
  - **Support Very High Silicon Utilization without Significantly Impacting Performance**
- **High Efficiency and Flexibility**
  - **Multiple Routing Path Alternatives for Low Congestion**
  - **Short Corner-to-corner Delays**
  - **Enables Rapid Timing Convergence**

ProASIC3/E
Routing Overview

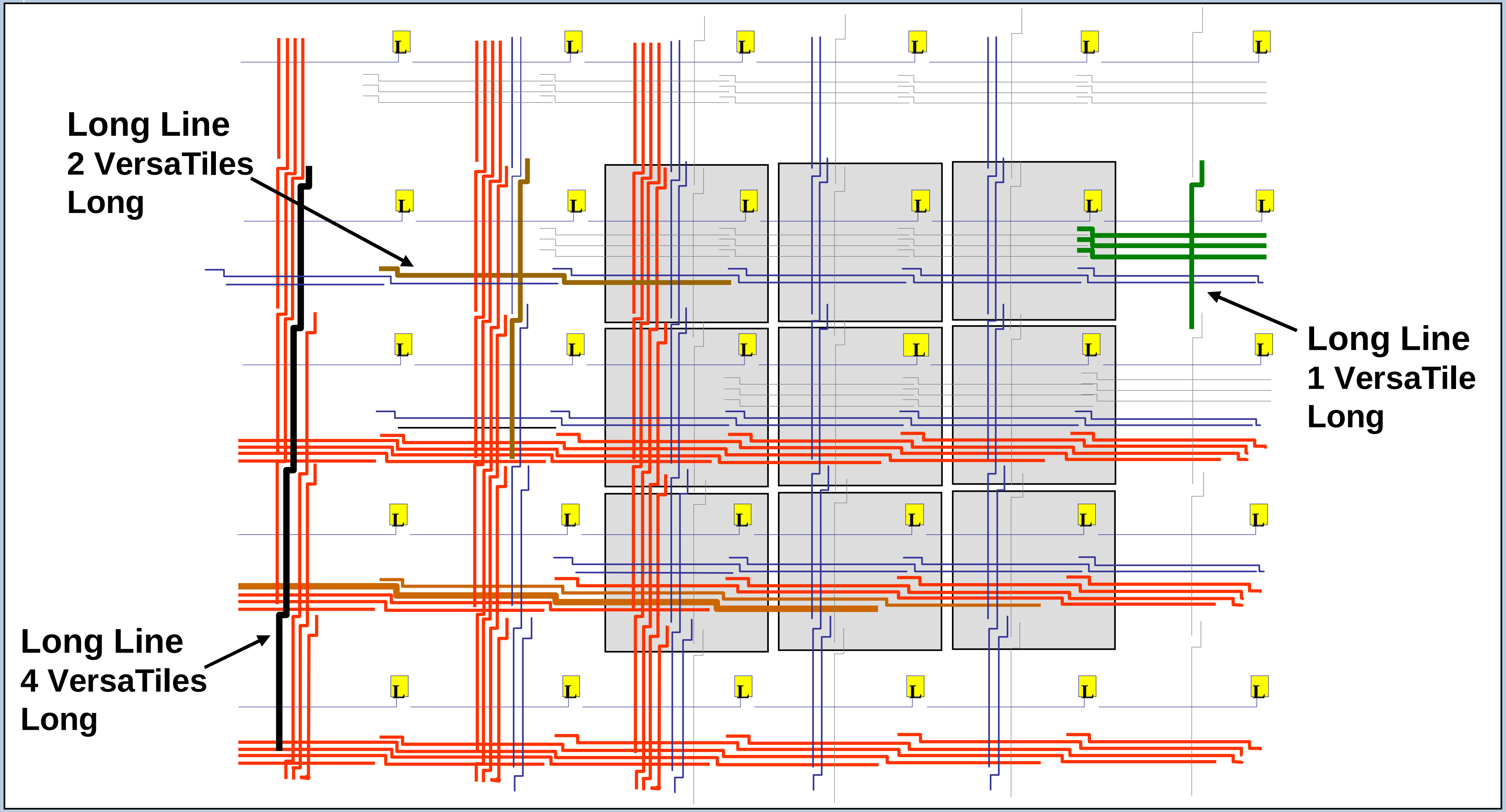
- **Locals (No Change from APA)**
  - **Guaranteed Access to All Neighbors**
- **Longs**
  - **4 Drivers instead of 1 (Allow Connecting 4-Longs and 2-Longs in Horizontal and Vertical Directions)**
- **Very-Longs**
  - **4 Drivers (to Go in 4 Directions)**
  - **Direct Access from VersaTile**
  - **2x16x16 Long Horizontal**
  - **2x12x12 Long Vertical**
  - **'Escape' Halfway**
  - **Completely Buffered**
- **Clocks:**
  - **6 Globals**
  - **3 Locals**



Flash Routing Resources
Hierarchy

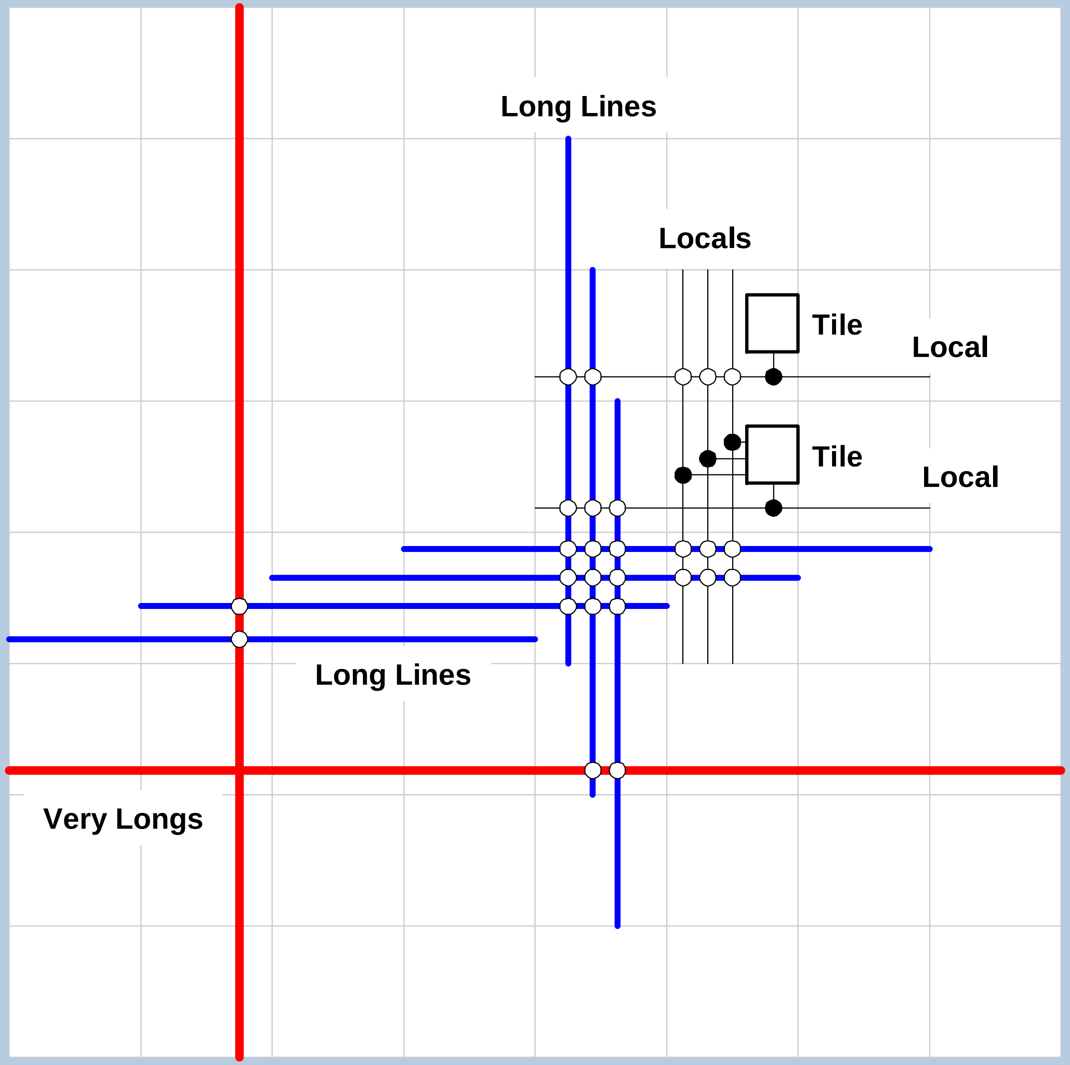


Flash Routing Resources
Long Lines



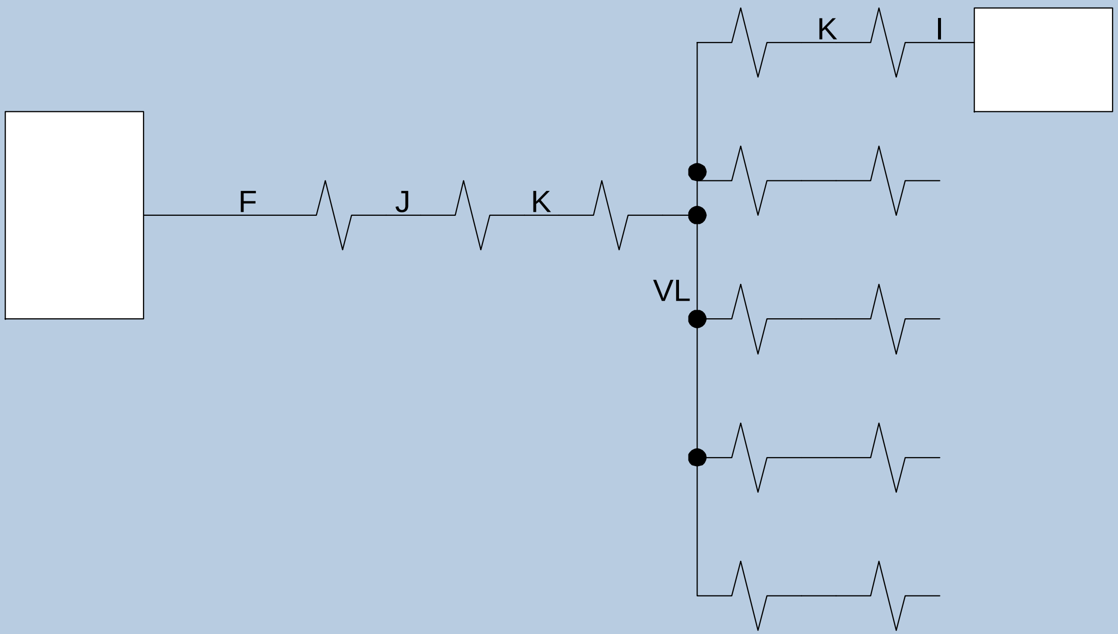
Long Lines for Longer Distances or Higher-Fanout Nets

Flash Routing
Simplified Architecture

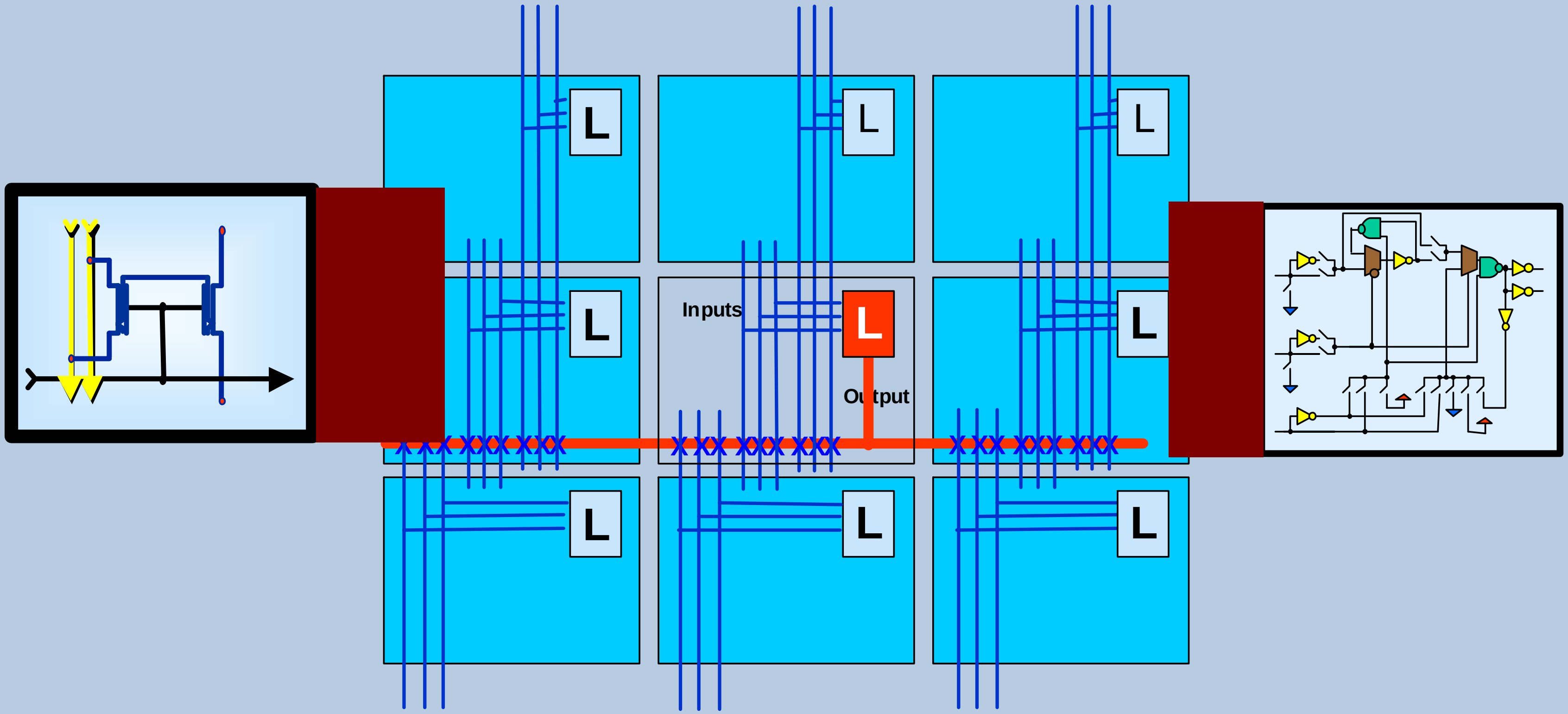


Flash Routing
Switch Requirements

- Nearest Neighbor (F/I Locals) – 1 FLASH Switch
- Local Connection (J/K Longs) – 3 FLASH Switches
- Long Connections (Very Long Lines) – 5+ FLASH Switches



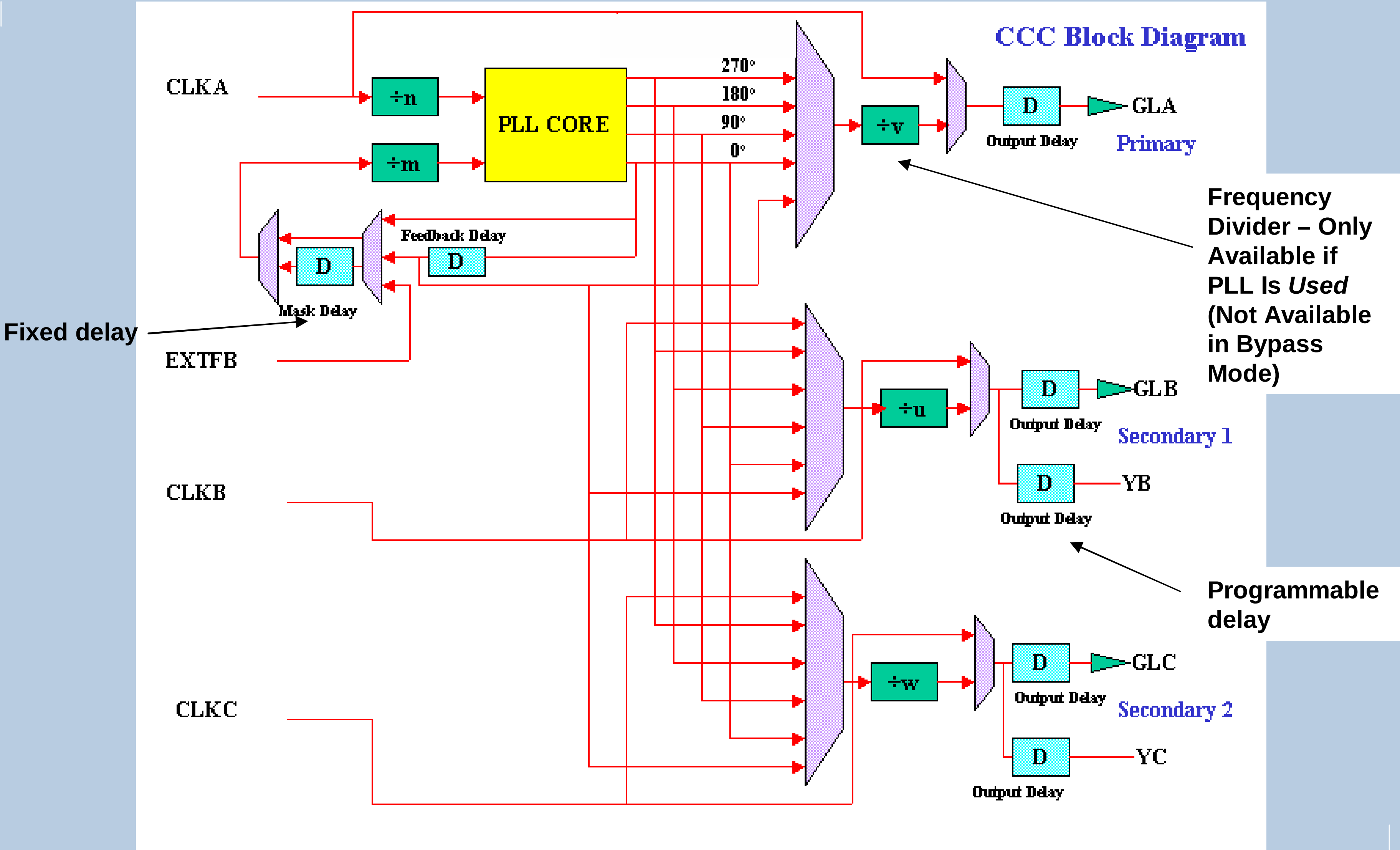
Flash Routing Resources
Local Routing



Local Lines Connect VersaTile Output to Nearest-Neighbor VersaTile, I/O Buffer, or Memory Block

Clocks, Globals PLLs and CCCs

Clock Conditioning Circuitry



Clock Conditioning Circuitry
Summary of Features

- 3 Global MUX Blocks
  - **Steer Signals from Global Pads and Core into Global Networks**
- PLL
  - **One on ProASIC3 Devices and Six on ProASIC3/E Devices**
- Delay Blocks (6 Programmable and 1 Fixed)
  - **Provide Phase Advancement/Delay**
- 5 Frequency Divider Blocks
  - **Provide Frequency Multiplication/Division (PLL ONLY)**
- Dynamic Shift Register
  - **Provides CCC Dynamic Reconfiguration Capability (Not Shown)**
- Clock Phase Adjustment
  - **0°, 90°, 180°, and 270° (PLL ONLY)**
  - **Programmable Delay/Advance (160 ps steps from –7.56 ns to +11.12 ns) – Clock Skew Minimization**
- Clock Frequency Synthesis Capabilities

PLL and CCC
Hardware Support

- All Devices Have 6 Clock Conditioning Circuitry (CCC) Blocks, BUT …
  - **… Some Have CCCs without PLLs AND …**
    - **ProASIC3E PQ208 – 4 Corner CCCs Do Not Have PLLs**
    - **ProASIC3**
      - ***All But A3P030 – Only West Central CCC Has PLL***
      - ***A3P030 (Lowest-density Device) – NO PLLs***
  - **… All Non-PLL Functionality Still Available**
      - ***Delay Elements***
      - ***Global Access from I/O or Internal Signal***
  - **CCC Bypass PLL**
    - **Does Not Support Divider Mode**
      - ***Note: This Behavior Is NOT Compatible with APA!***
      - ***Use Additional Logic to Divide Clock***

Global and Quadrant Clocks

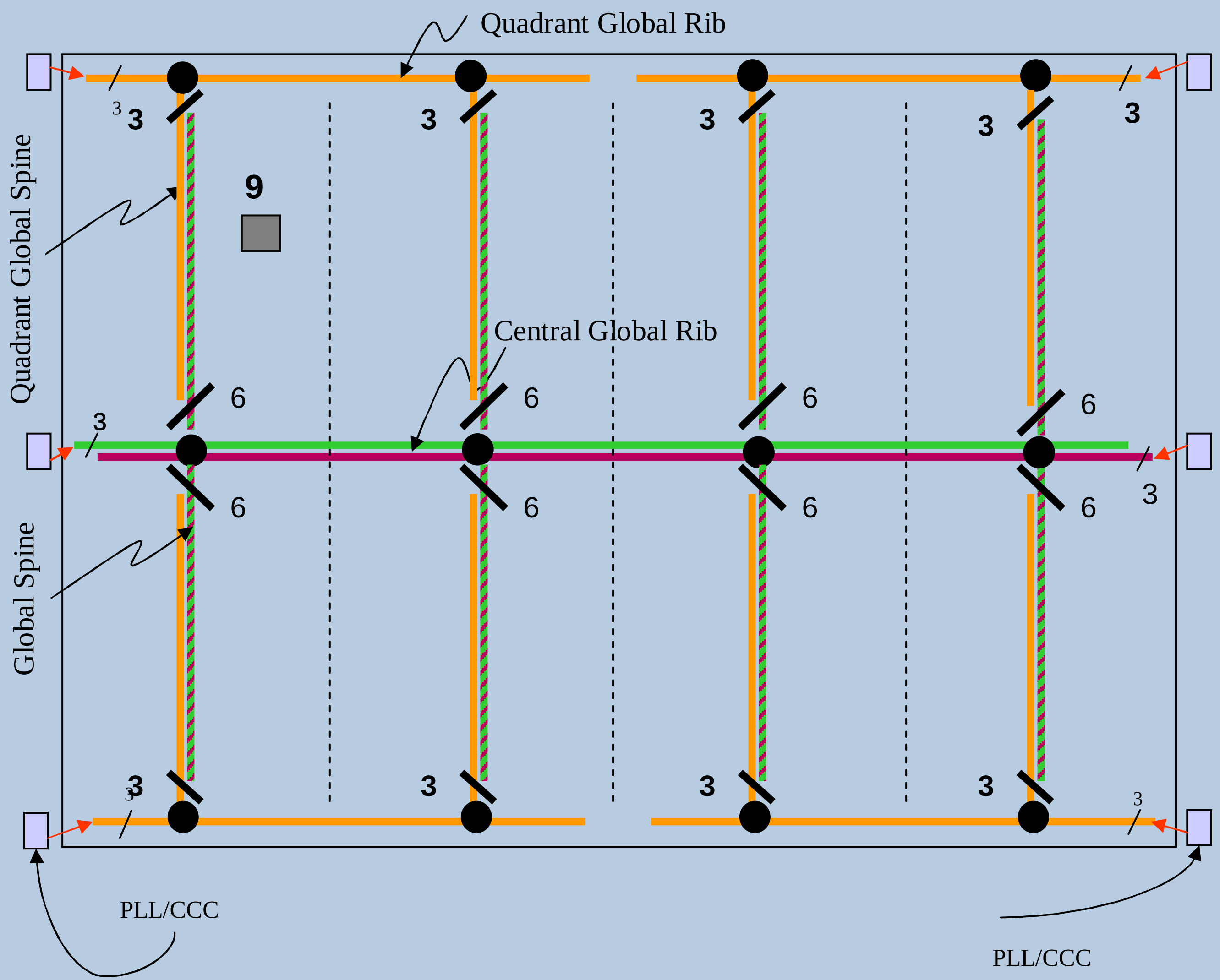
6 Global Clocks

- Reach All Tile Ports (Routed Clock)
- Global Clock Networks Serve All Tiles Including RAM, I/O, AUX and CCC Tiles
- Driven by Clock Conditioning Circuitry (CCC) in Middle Left and Middle Right of Die

12 Quadrant Clocks (3 per Quadrant)

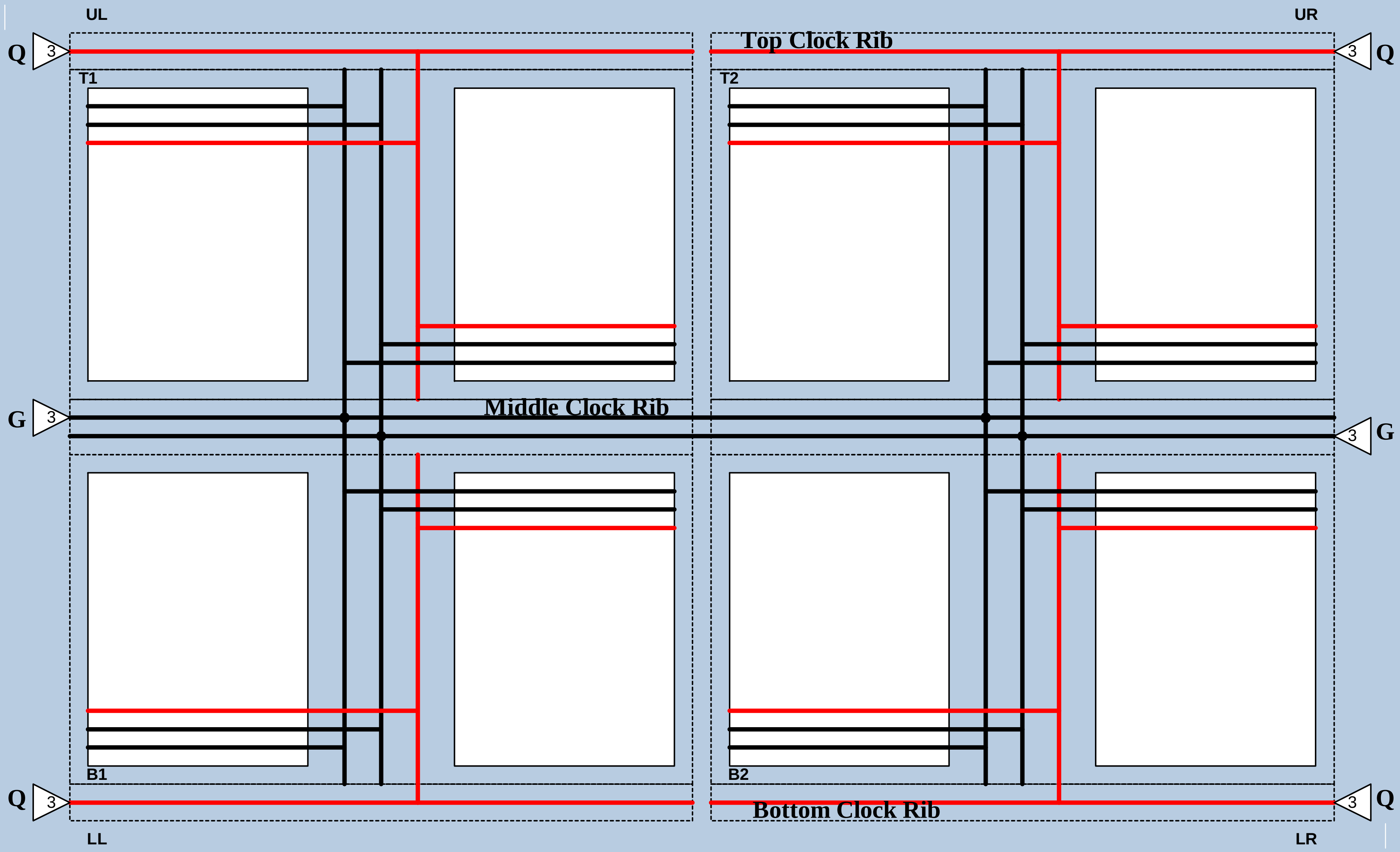
- Cannot Access Middle Two Rows
- Quadrant Clock Networks Serve All Tiles Including RAM, I/O, AUX and CCC Tiles
- Driven by Clock Conditioning Circuitry (CCC) in Four Corners of Die

Global Distribution Network



- Left and Right CCCs Provide 6 Global Clocks (Access from I/Os in Middle of Left and Right Sides)
- 12 Quadrant Clocks (3 per Quadrant – Access from I/Os in 4 Corners)
- Access to 9 Global Resources in Each Tile – Up from 4 in APA
- Access from PLLs and Internal Signals
- Reduces Delays and Minimizes Resource Usage

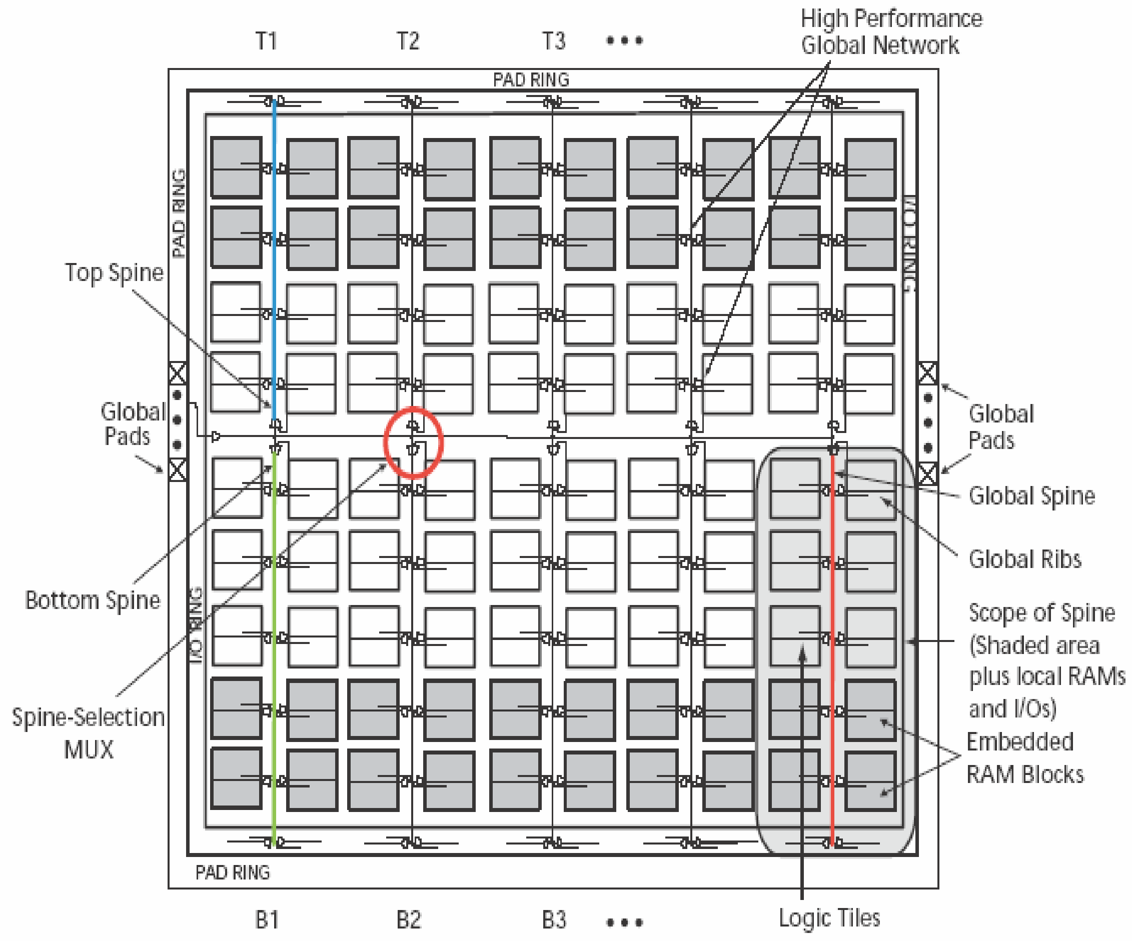
Global Distribution Network
Simplified View



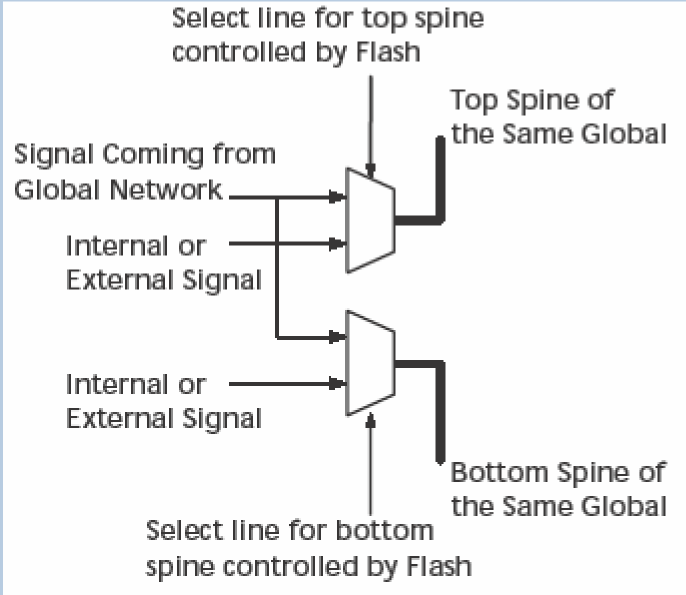
Clock Aggregation
Hardware Support

- Dedicated Clock Tile “Ribs” with Dedicated Routing/MUXing Resources in North, South and Central Regions of Chip
- I/Os Can Also Access North and South Ribs
- Clock Aggregation Allows Signal (Internal or I/O) to Access …
  - **… Single Spine**
  - **… Double Spine**
  - **… Quadruple Spine**
- More to Come in Software Section

Clock Aggregation
Diagram



- **Allows Multi-Spine Clock Domains**
- **MUX Tree Allows Long Lines or I/Os to Access Domains of One, Two, or Four Global Spines**



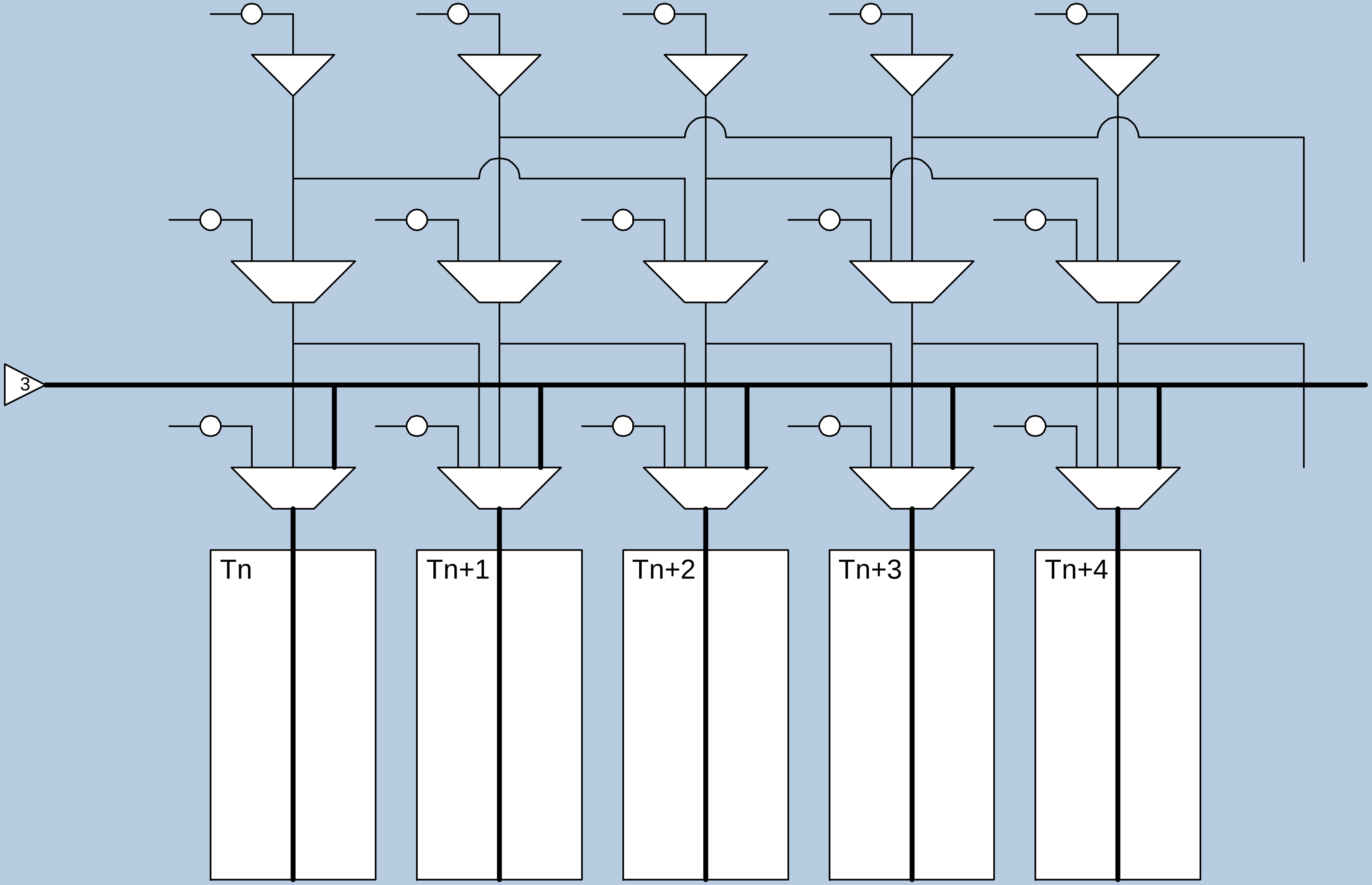
Spine Selection Mux

Local Clocks

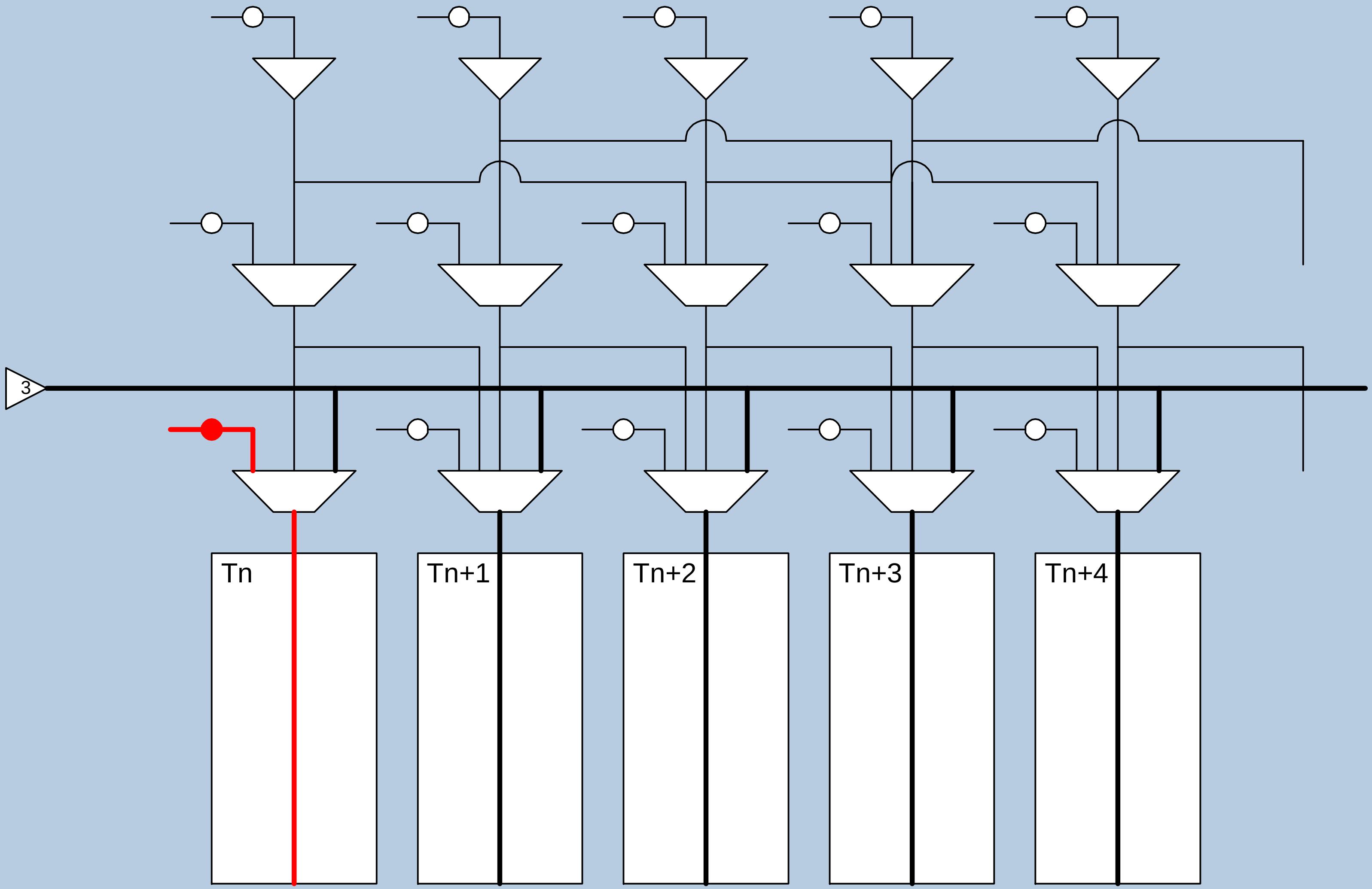
Portion of Global and Quadrant Clock Networks Driven by Clock Spine Drivers

- **Global Clock Spine Drivers**
  - **Access Top and Bottom Spine Regions from Middle Clock Ribs**
  - **No Control Dependency between Top and Bottom Spines**
    - ***If T1 Is Assigned to Net, then B1 Is Not Wasted and Can Be Used by Global Clock Network (Unlike APA!)***
  - **Local Clock Networks Cannot Access Middle Two Rows UNLESS Local Clock Uses BOTH Top AND Bottom SIMULTANEOUSLY**
    - ***Example – (T1:B1)***
- **Quadrant Clock Spine Drivers**
  - **Access Top Spine Regions from Top Clock Ribs**
  - **Access Bottom Spine Regions from Bottom Clock Ribs**
  - **Cannot Access Middle Two Rows**

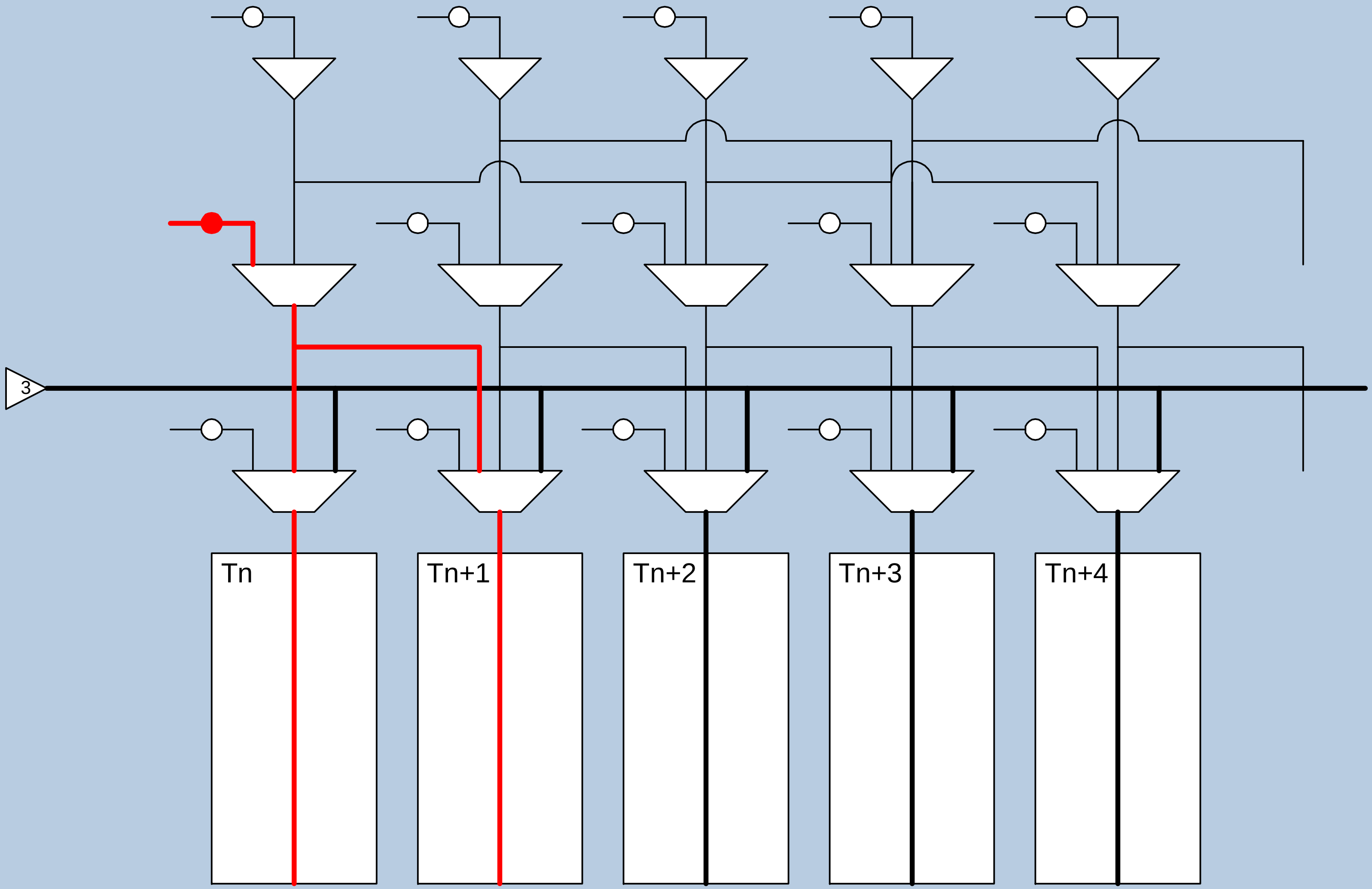
Local Clock Aggregation
MUX Structure



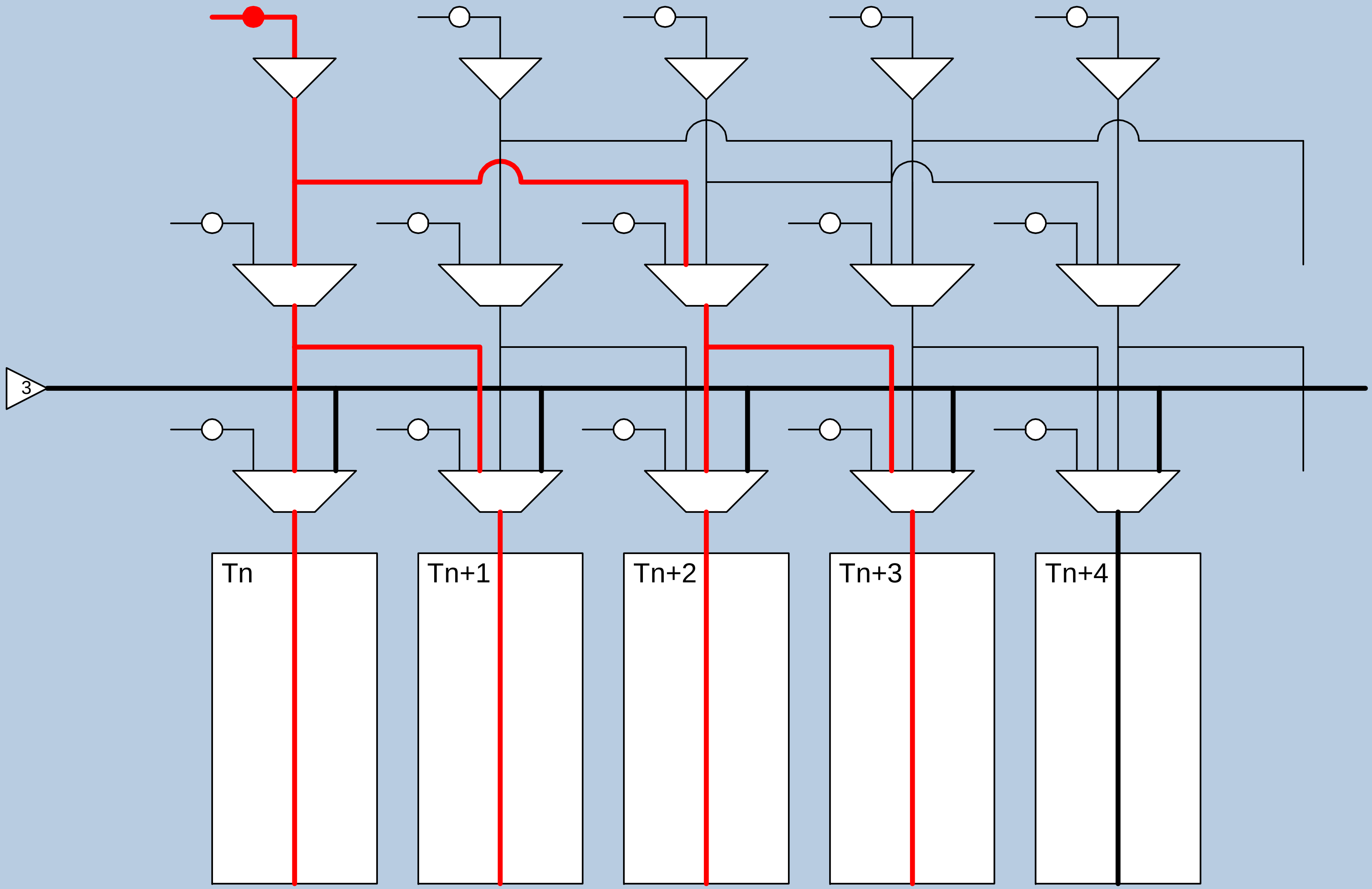
Local Clock Aggregation
1-Spine



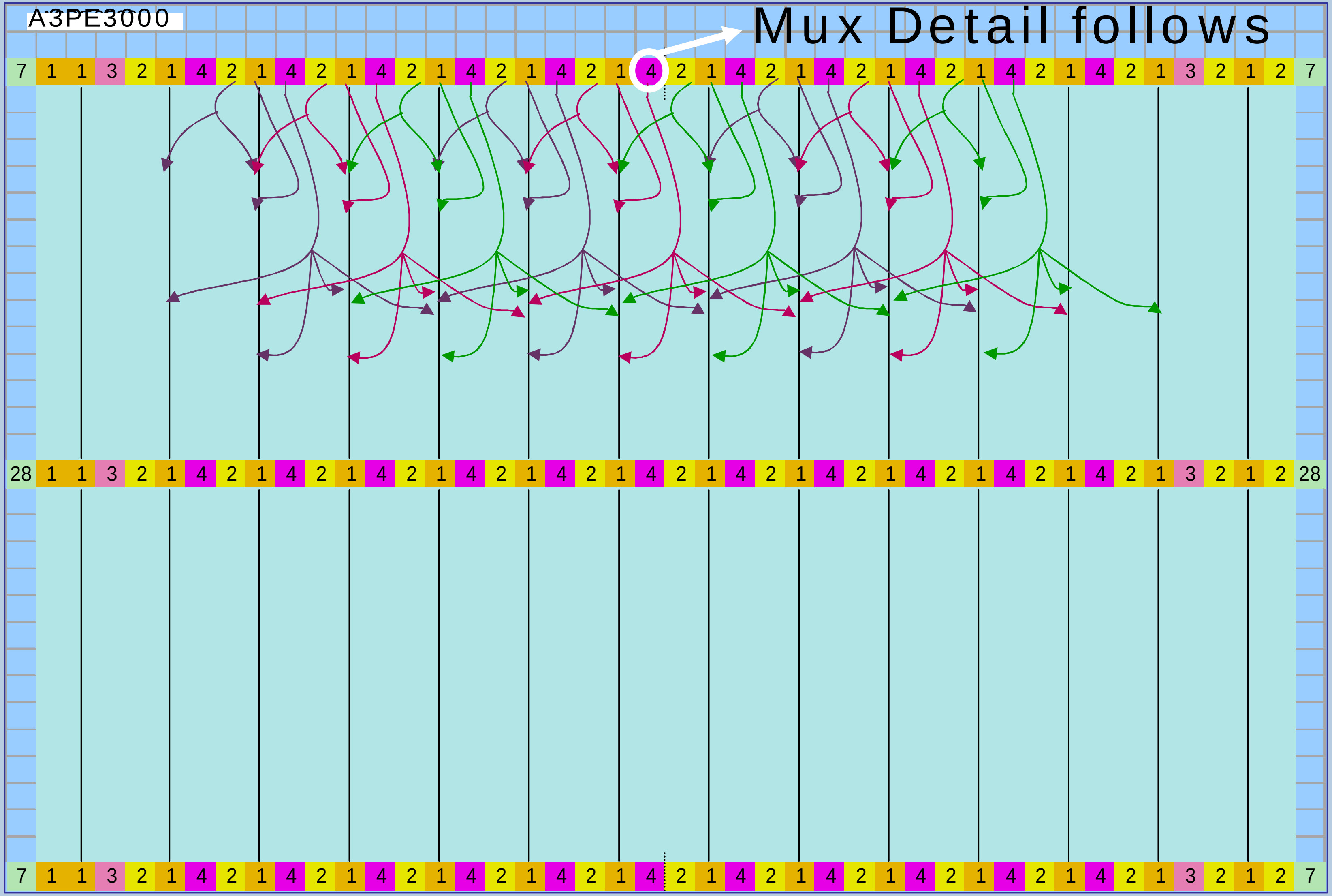
Local Clock Aggregation
2-Spine



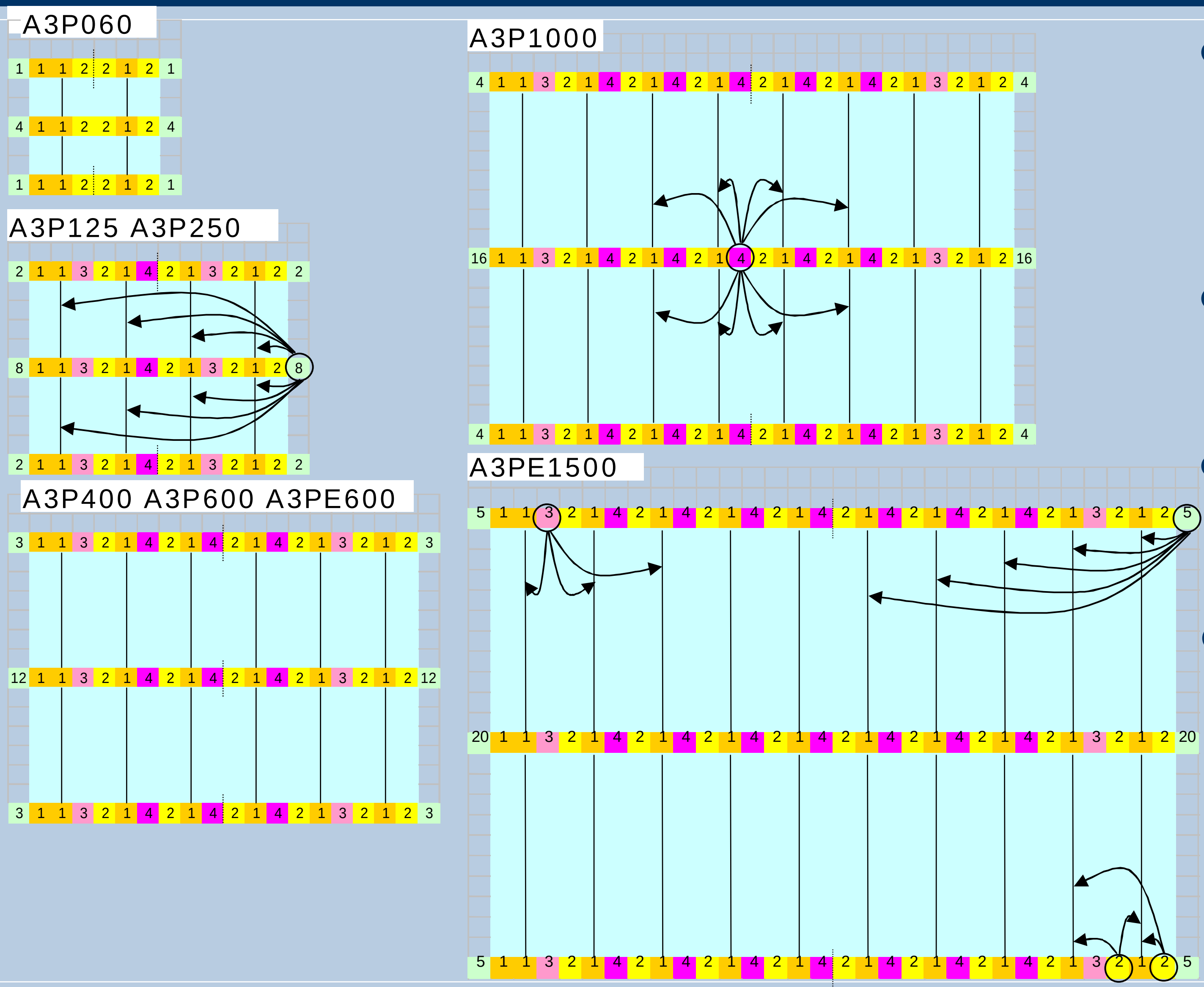
Local Clock Aggregation
4-Spine



Clock Aggregation: Big Devices



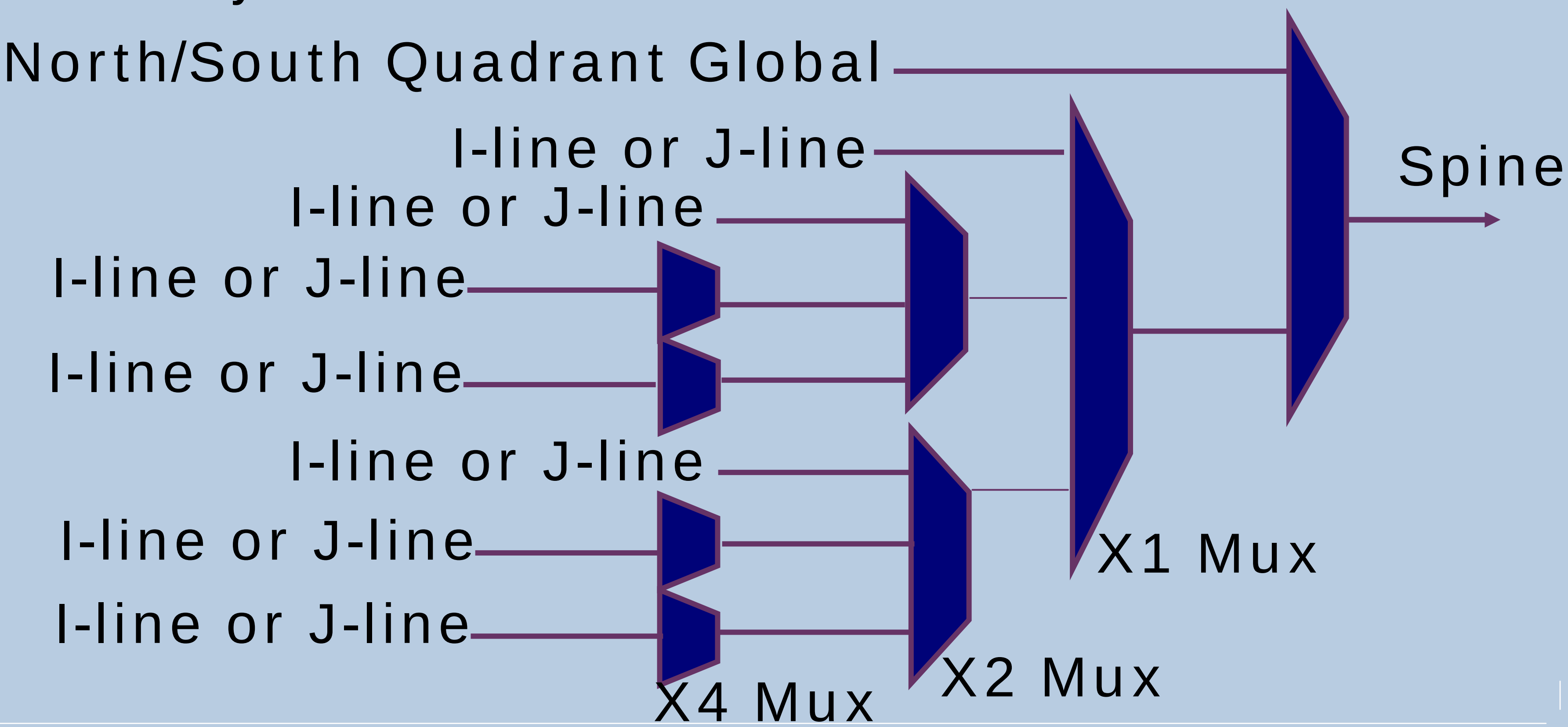
Clock Aggregation 'Corner Cases'



- **East and West PLL: access to all spine regions. (from 4 to 28 regions)**
- **Single spine access from tiles around spine (orange)**
- **Double spine access from left of spine (yellow)**
- **Quadruple spine access from right of spine (purple)**

Clock Aggregation
Quadrant global mux detail

- **Spine can be driven from**
  - **I/O**
    - ***X1 6 I/O, X2 5 I/O (left), X4 5 I/O (right)***
  - **Quadrant Global Network**
  - **Array interconnect**



RAM/FIFO

ProASIC3/E Embedded Memory

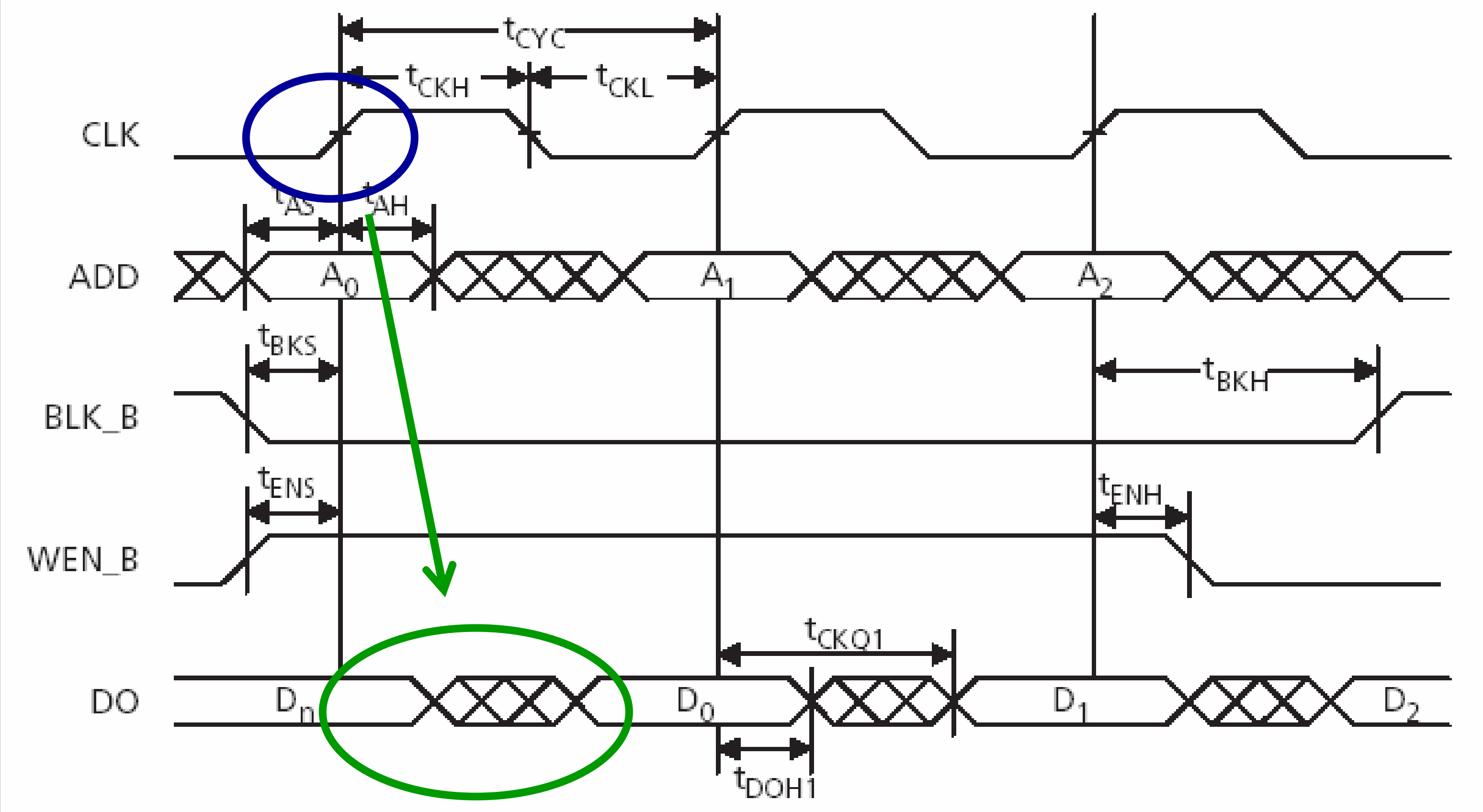
- Up to 504K Bits Arranged in up to 112 Individually-programmable 4608-bit Embedded Memory Blocks
  - **2 Read and 2 Write Ports – True Dual-port**
  - **Synchronous Operation Up to 350 MHz**
  - **Fully programmable**
    - **Programmable aspect ratio**
      - ***4kx1, 2kx2, 1kx4, 512x9, 256x18***
    - **Cascadeable in Width and Depth**
    - **ACTgen Tool Automates Memory Generation**
    - **Independent Read and Write Port Widths**
- FIFO Capability
  - **Integrated Decoder, FIFO Controller, and Flag Logic**
  - **Programmable FIFO Depth and Flag Thresholds**
- Changes from ProASIC^{PLUS}
  - **No Asynchronous Read and Write Operations**
  - **No Parity Checking and Generation**
  - **Resetting RAM Block Outputs Is Possible in ProASIC3**

ProASIC3/E
Two RAM Elements

- **RAM4K9 – True Dual-port RAM which Supports**
  - **Variable Aspect Ratios – 4096x1, 2048x2, 1024x4 or 512x9**
    - **Independent Read and Write Port Widths**
  - **Dual-port Options – Both Read, Both Write, One Read & One Write; Same Clock Frequency or Two Different Clock Frequencies**
  - **Pass-through of Write Data or Hold Old Data on Output**
- **RAM512x18 – Two-port RAM which Offers**
  - **Variable Aspect Ratios – 512x9 or 256x18**
    - **Independent Read and Write Widths**
  - **Dedicated Read and Write Ports**
- **Both Elements Have**
  - **Synchronous Write**
  - **Synchronous Read – Pipelined or Non-Pipelined**
  - **Active-low Asynchronous Output Reset**

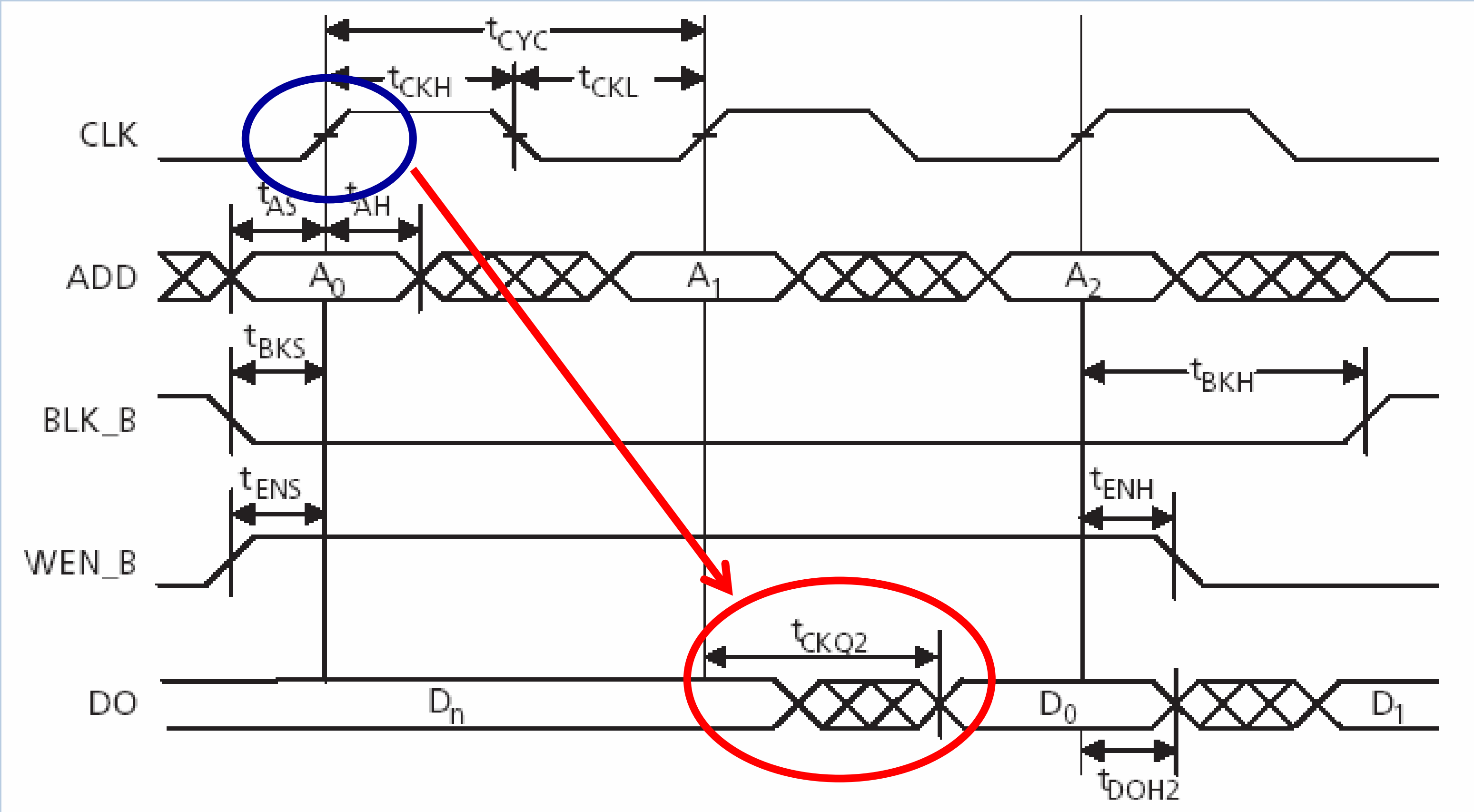
Note: A3P030 Has NO RAM!

ProASIC3/E RAM
Read Cycle – Flow-Through Output



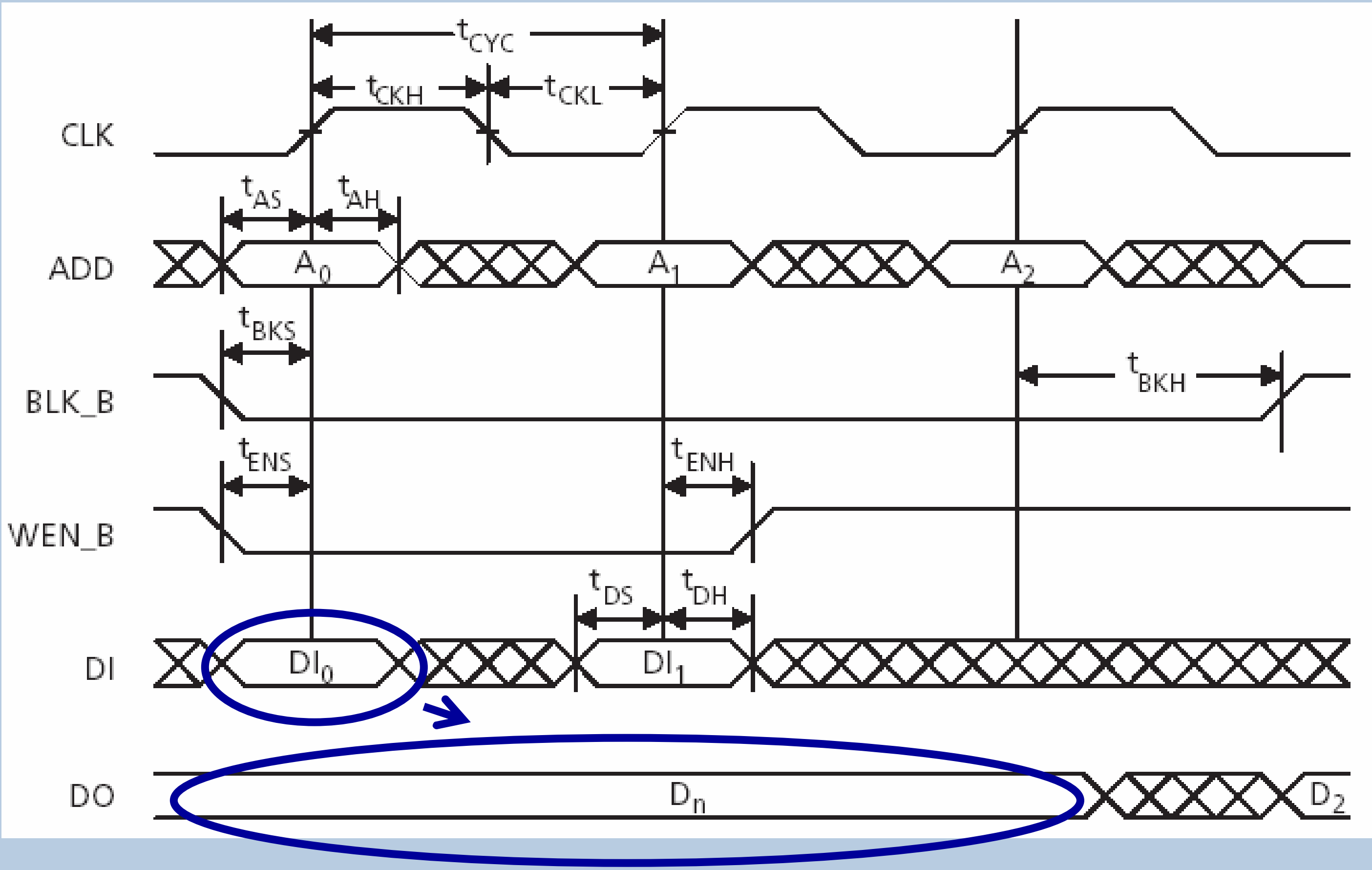
Flow-Through
CLK1 – Addr -> Data

ProASIC3/E RAM
Read Cycle – Pipelined Output



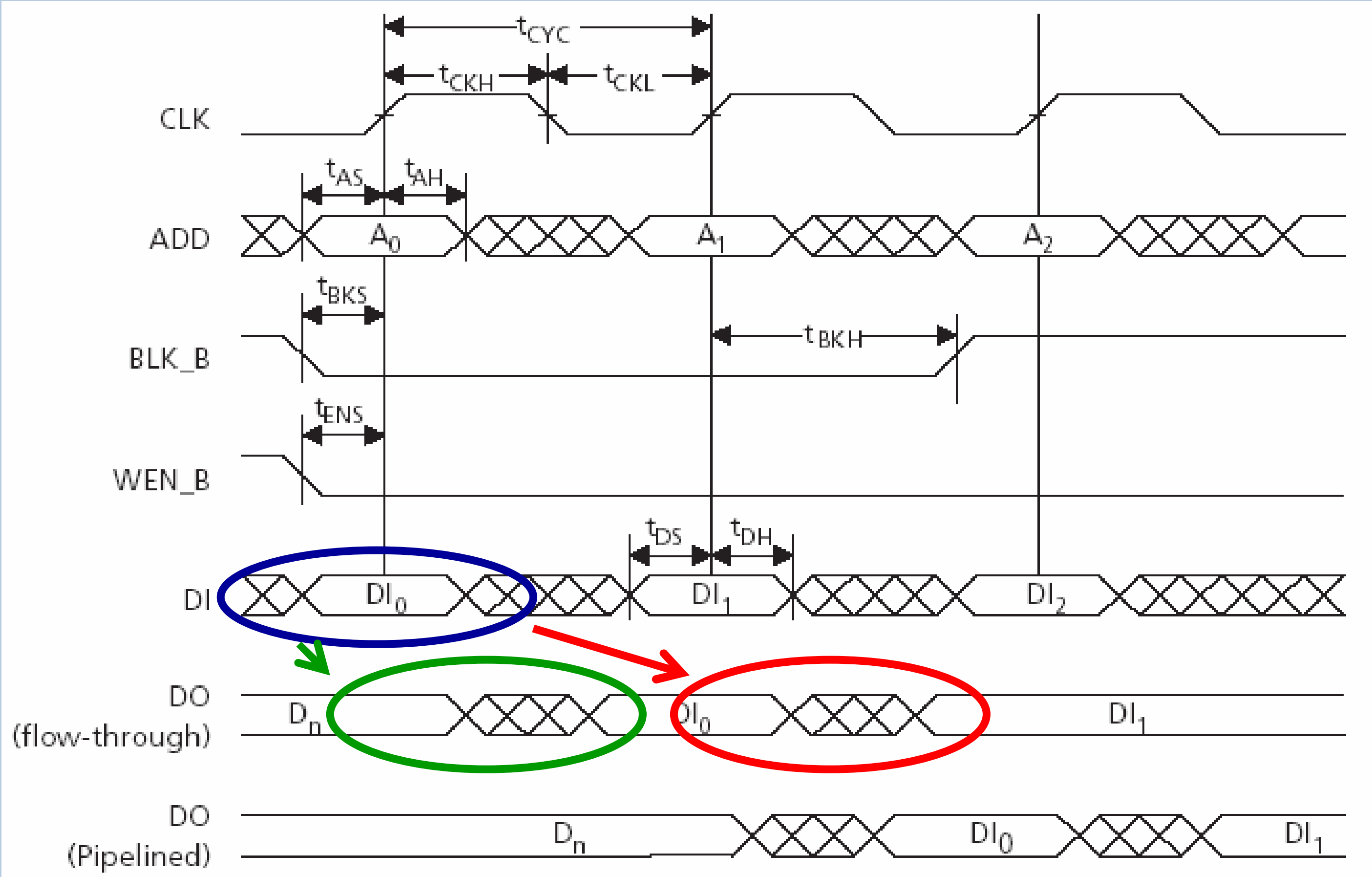
Pipelined
CLK1 – Addr
CLK2 –> Data

ProASIC3/E RAM
Write Cycle – Output Retained



Output Retained
CLK1 – Addr & Data

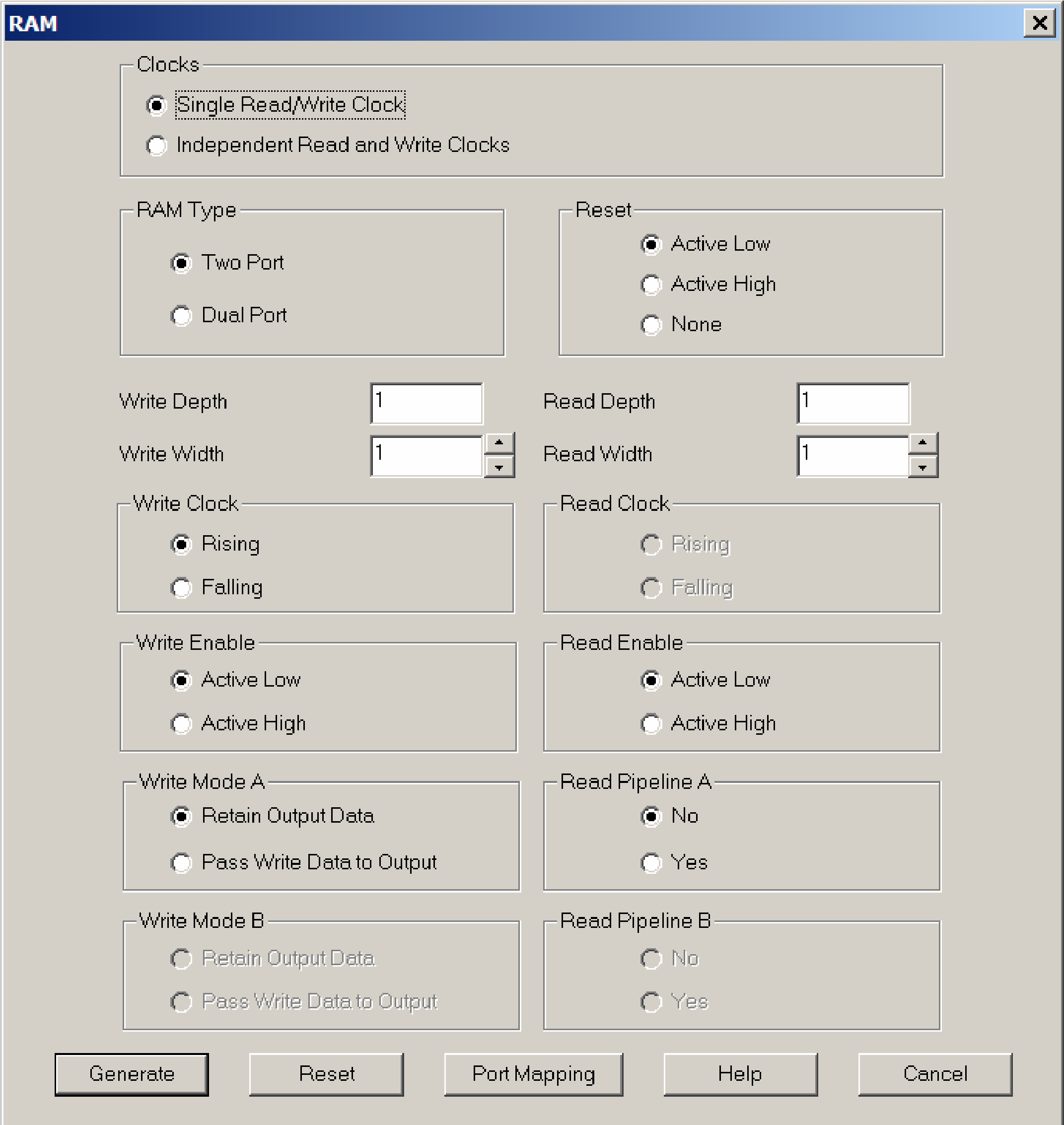
ProASIC3/E RAM
Write Cycle – Output as Write Data



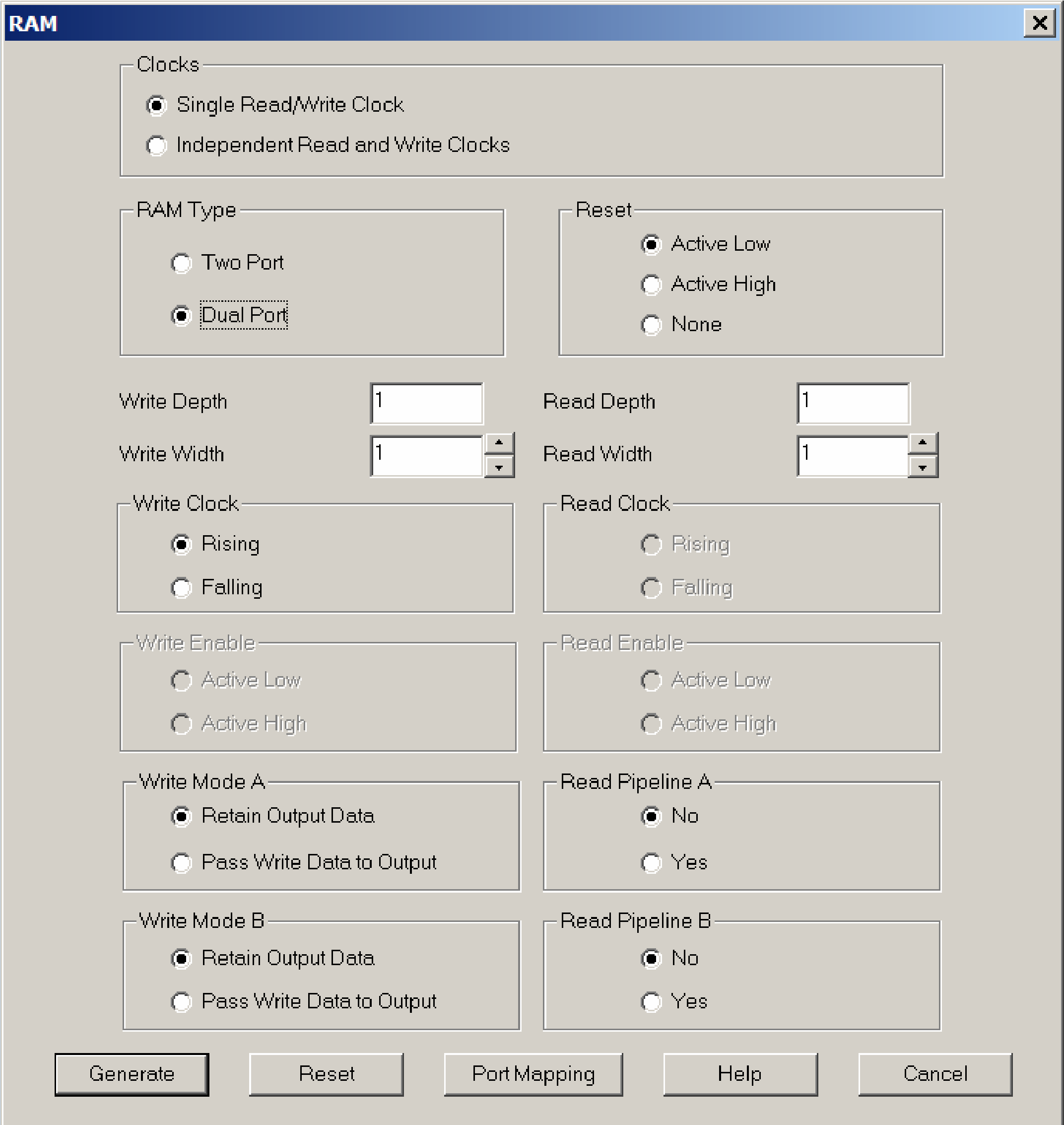
Flow-Through
CLK1 – Addr & Data -> Data

Pipelined
CLK1 – Addr & Data
CLK2 –> Data

ProASIC3/E Two-Port RAM
Generation in ActGen



ProAScope3/E Dual-Port RAM
Generation in ActGen



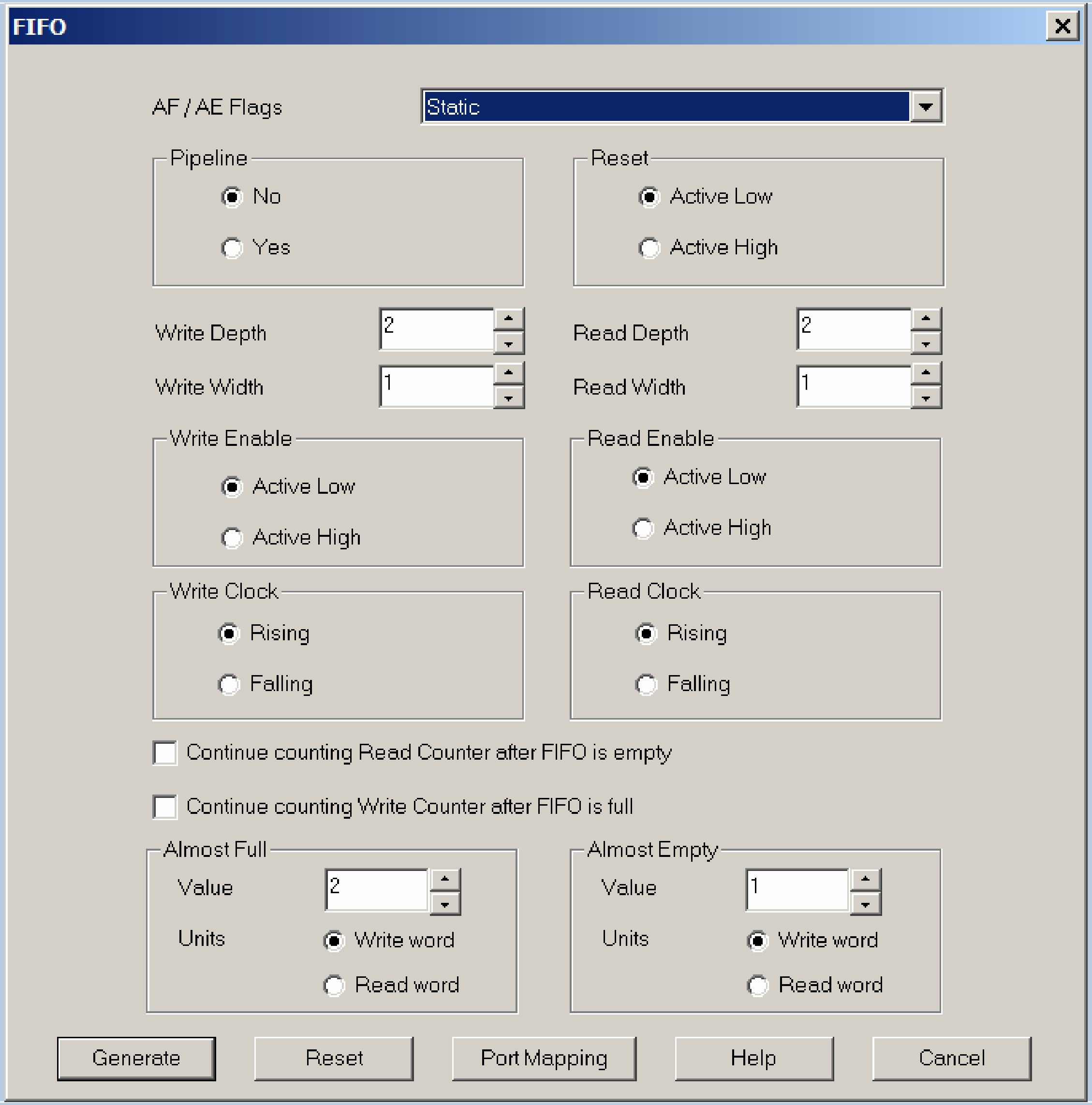
ProASIC3 Memory
FIFO

ProASIC3/E Has One FIFO Element

- **FIFO4Kx18 Supports**
  - **Variable Aspect Ratios – 4096x1, 2048x2, 1024x4, 512x9, or 256X18**
    - ***Independent Read and Write Port Widths***
  - **Four FIFO Flags – Empty, Full, Almost-empty, Almost-full**
    - ***FIFO Empty/Full Flags Synchronized to Read Clock and Write Clock, Respectively***
    - ***Programmable Threshold Values of ‘Almost’ Flags***
  - **Active-low Asynchronous Reset**
  - **Active-low Block Enable**
  - **Active-low Write Enable and Active-high Read Enable**
  - **FSTOP and ESTOP – FIFO Counters Can Count after FIFO Is Full or Empty**
    - ***Allows Writing to FIFO Once and Repeatedly Reading Same Contents without Rewriting Contents***

Note: A3P030 Has NO RAM!

ProASIC3/E FIFO
Generation in ActGen



FlashROM and FlashPoint

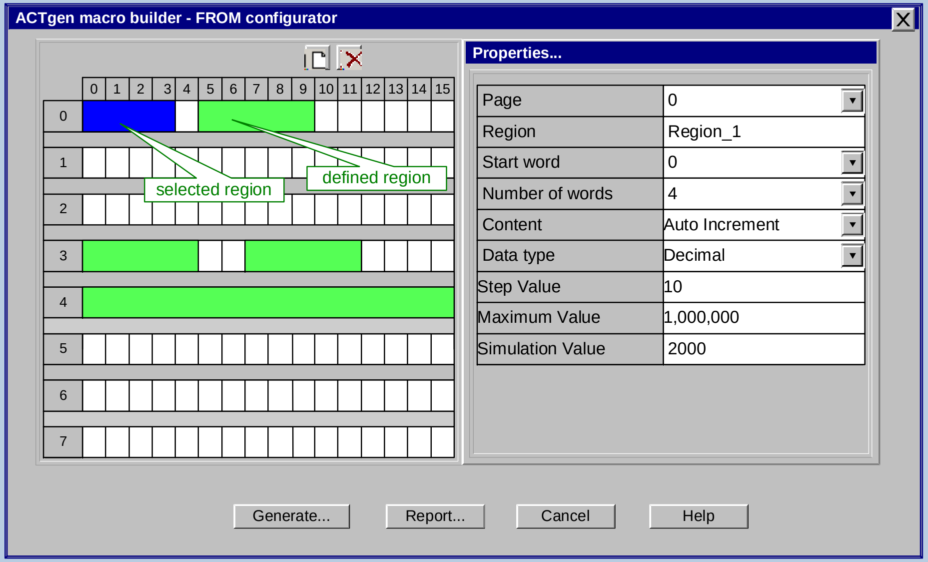
ProASIC3
Only FPGA with Flash ROM (FROM)

FROM Features

- **1024 total bits**
- **128 bits x 8 pages**
- **Extensive device serialization support in software**

FROM Applications

- **Internet Protocol addressing**
- **Device serial numbers**
- **Subscription model**
- **System calibration settings**
- **Secure crypto key storage**
- **Asset management tracking**
- **User preference storage**
- **Date stamping**
- **Versioning**



Subscription use model

OEM programs Device Master Key (AES decryption key) and FROM with a unique TAG

Part is deployed in ‘box’

‘Customer’ requests additional feature by supplying credit card details and <u>TAG</u> value of ‘box’ over Internet

OEM verifies payment and looks up DMK based on TAG supplied

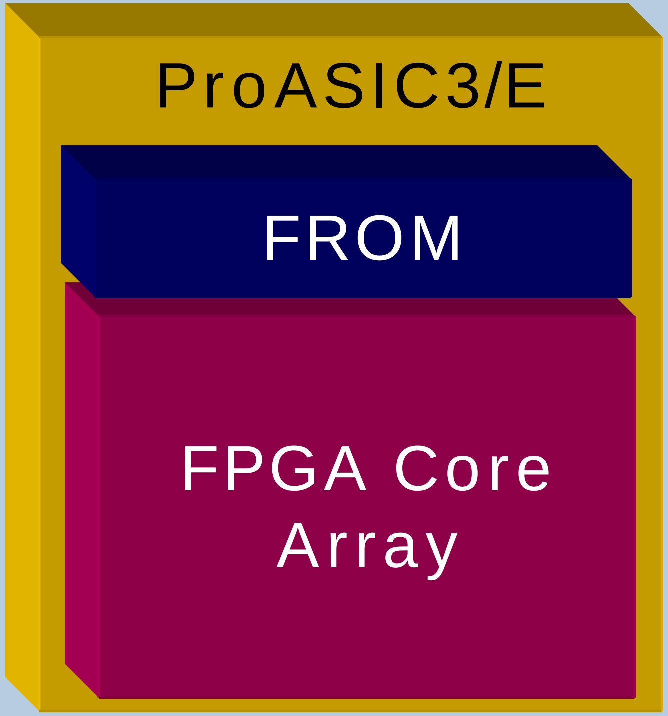
New feature-enabled design is encrypted with DMK and sent to customer via Internet, satellite or direct to ‘box’ for secure ISP

New feature is enabled and will only work with the DMK supplied

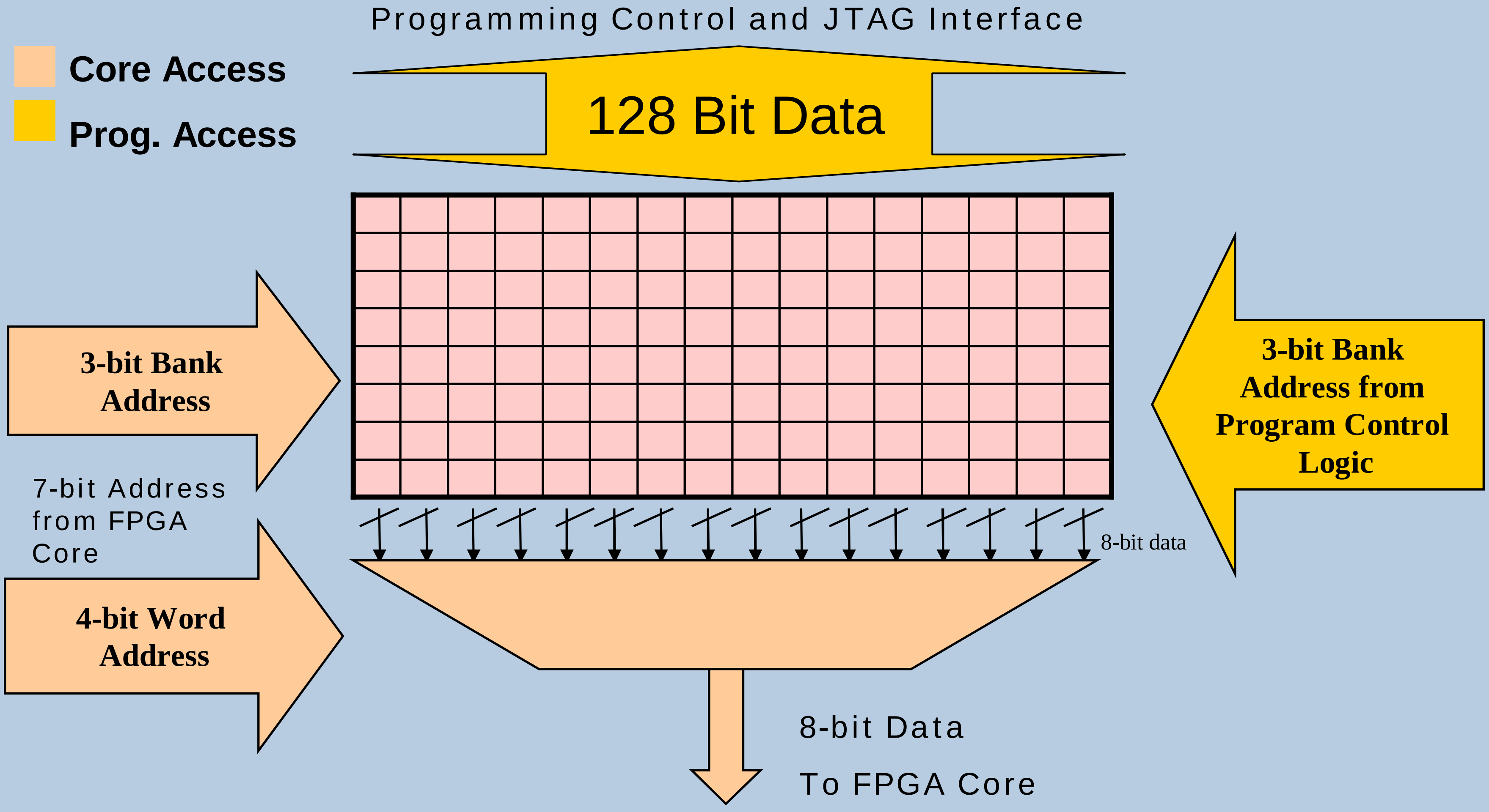
Profitable aftermarket feature up-sell is preserved and controlled by OEM

FlashROM (FROM) Memory

- 8 pages of 128 bits (8x128!!!)
- FPGA Core and FlashROM Memory Can Be Programmed Separately
  - **Allows Changing FROM without Erasing Core**
  - **Core Powered Down during FROM Programming**
- Example Applications
  - **IP Addressing**
  - **User/System Preference Storage**
  - **Device Serialization**
  - **Inventory Control**
  - **Subscription Models (Set-top Boxes)**
  - **Secure Key Storage**
  - **Presets**
  - **Date Stamping**
  - **Version Management**



FlashROM
Logical View



Every 128-bit Bank Can Be Reprogrammed Independently

FlashROM
Organization

Bank # 3 MSB of ADDR (READ)		Byte Number in Bank 4 LSB of ADDR (READ)															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0																
	1																
	2																
	3																
	4																
	5																
	6																
	7																

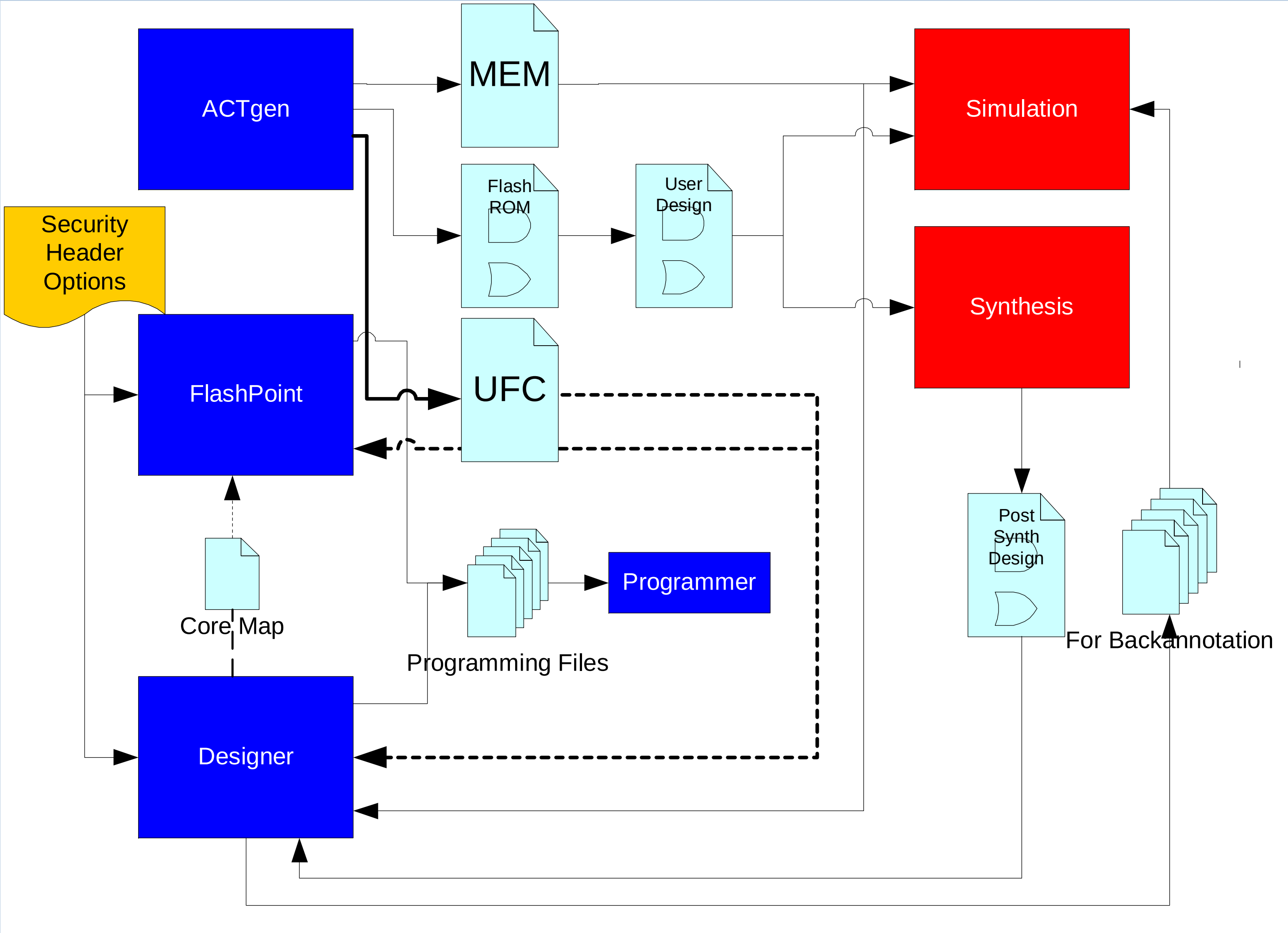
For Programming

- 8 Banks of 128 bits Each
- Each Bank Individually Programmable via External JTAG

For Reading

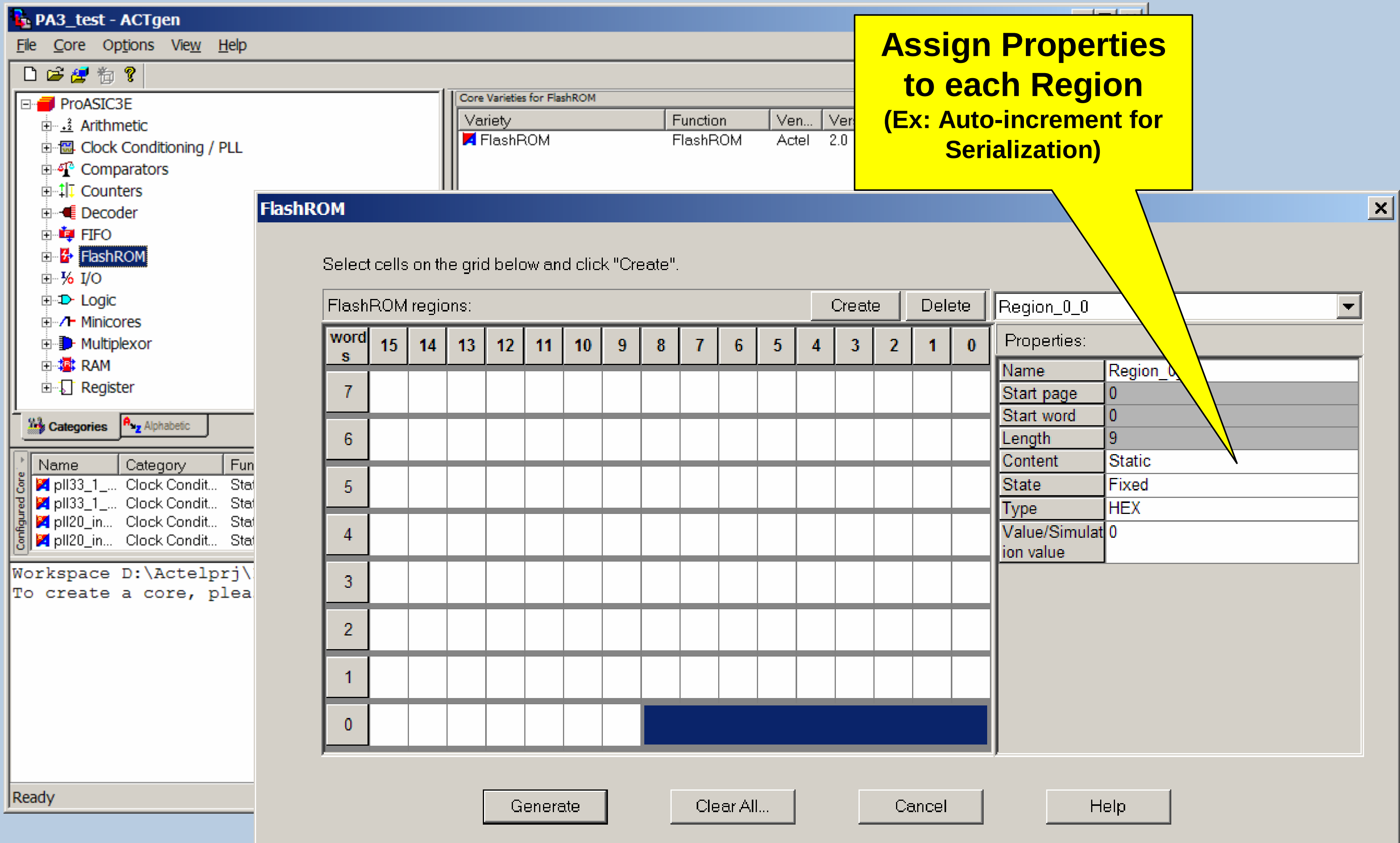
- Asynchronous Read Done on Byte Boundaries with Nominal 10 ns Access Time
- 7-bit Address and 8-bit Data Interface with FPGA Core
  - Upper 3 Address Bits Select Bank
  - Lower 4 Address Bits Select One of 16 Bytes

FlashROM
Memory Design Flow



FlashROM Memory Configurator

Starting from ActGen

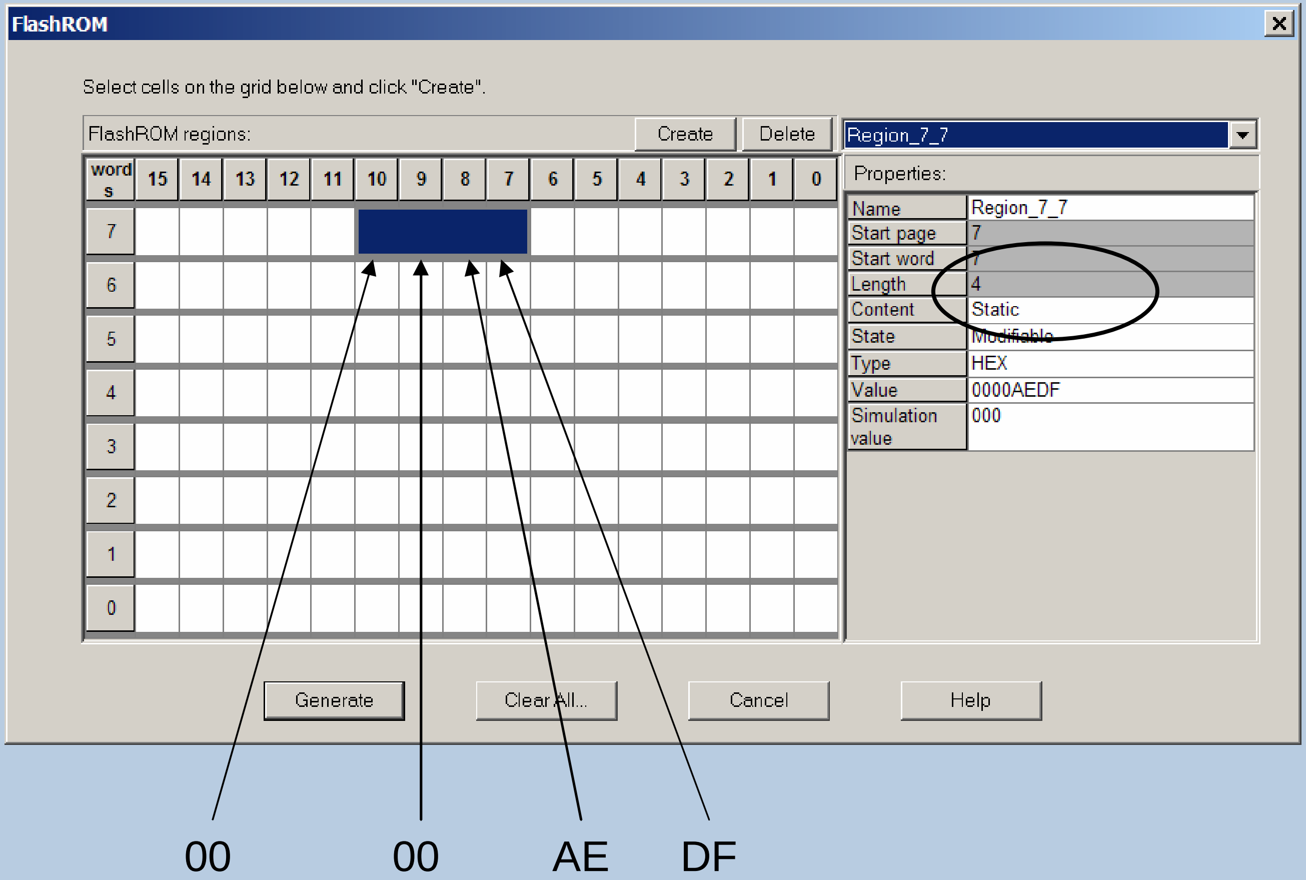


Assign Properties to each Region

(Ex: Auto-increment for Serialization)

FlashROM Memory Configurator
Example

FROM “Floor Planner”



- User Selects Properties and Data Style for each Page/Region of FROM

Data Can Be:
- Static
- Read from External File
- Variable with Built-in Auto-increment / decrement Function
- Fixed or Modifiable

Programming & Security

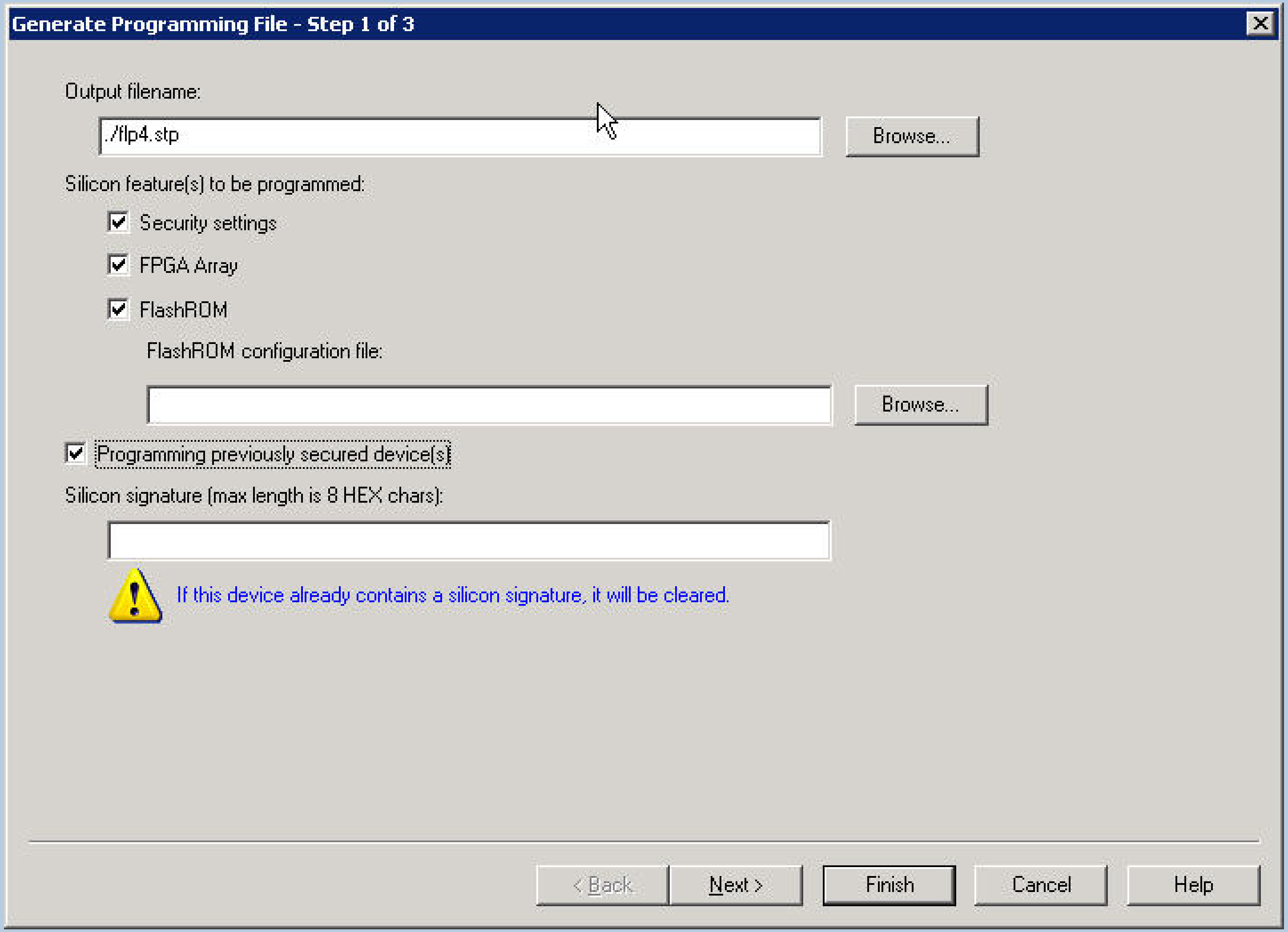
Device Programming Scenarios

- **First-time Programming**
  - **Specify Security Information**
- **Re-programming**
  - **Specify Previously-used Security Information**
- **Changing Security Settings**

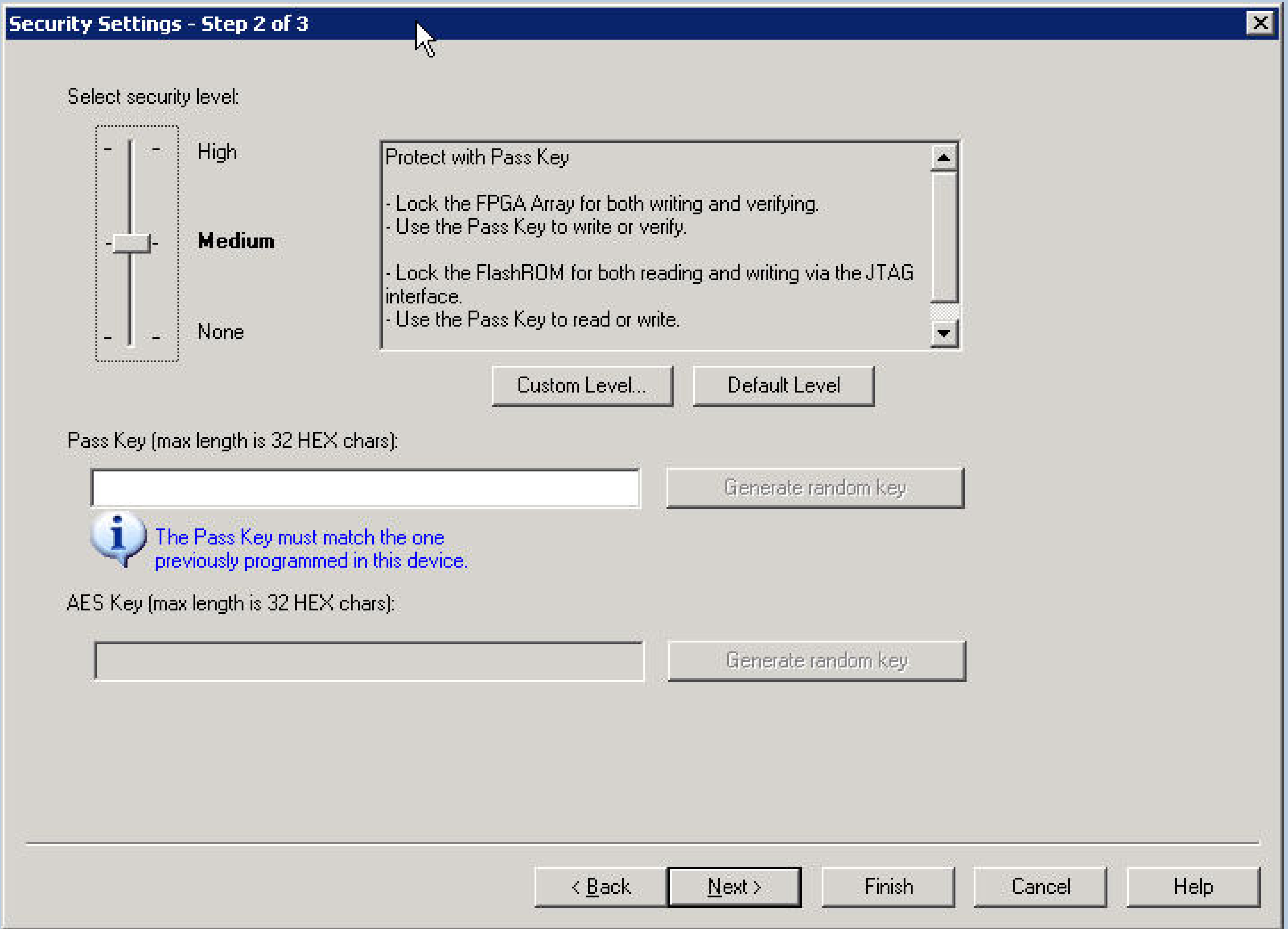
Environments

- **Trusted Programming Environment**
  - **Users May Have Access to Pass Key and AES Key**
- **Un-trusted Programming Environments**
  - **Never Expose Pass Key or AES Key**
  - **Never Program Security Settings**

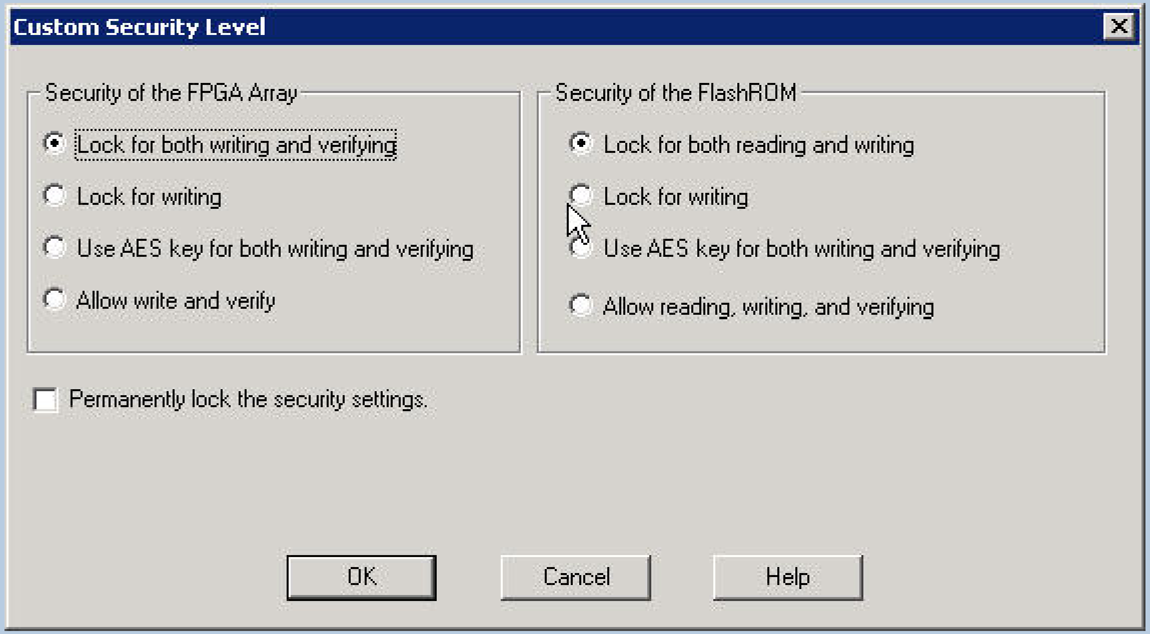
FlashPoint
Start-up Screen



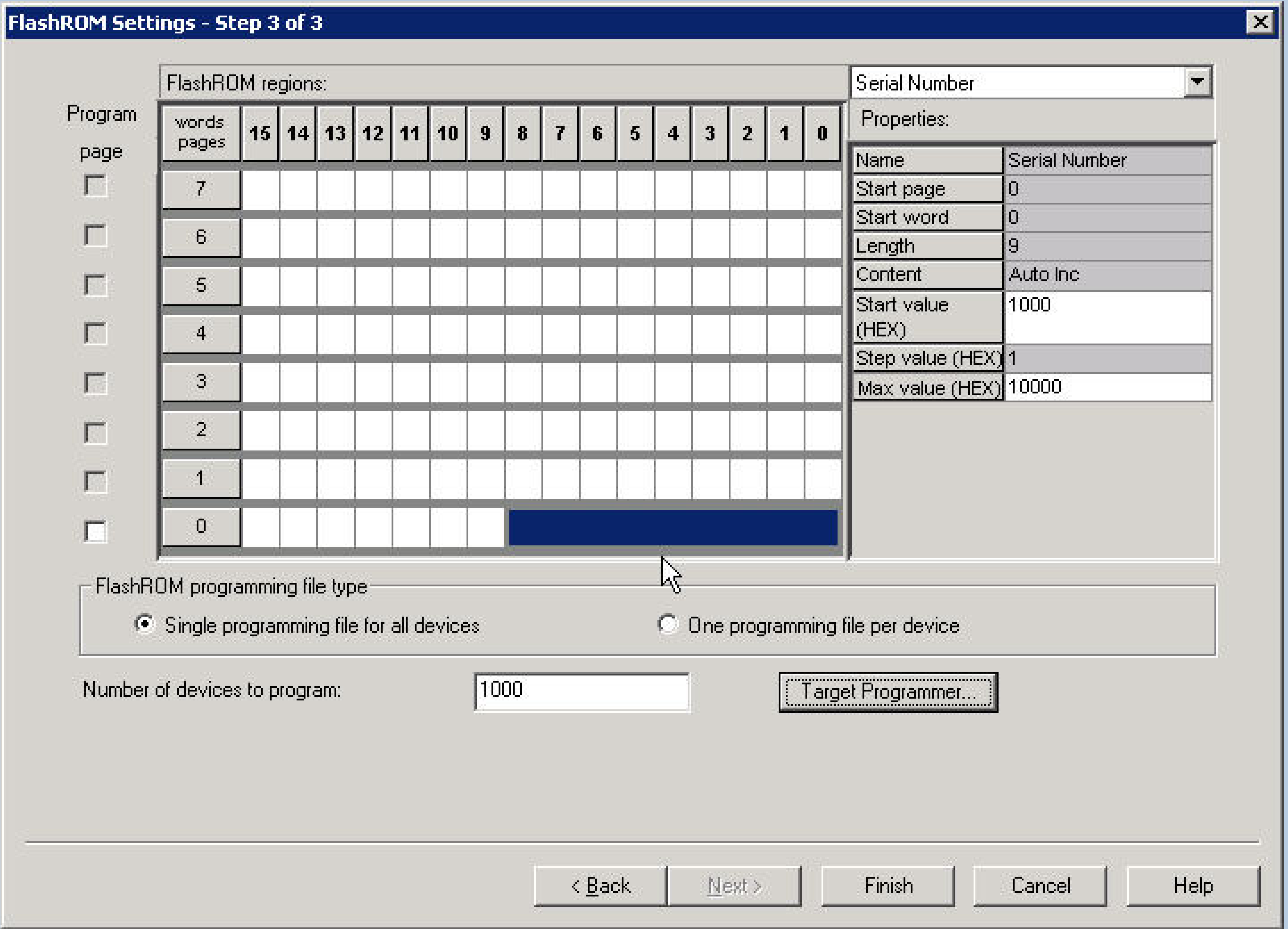
FlashPoint
Security Settings



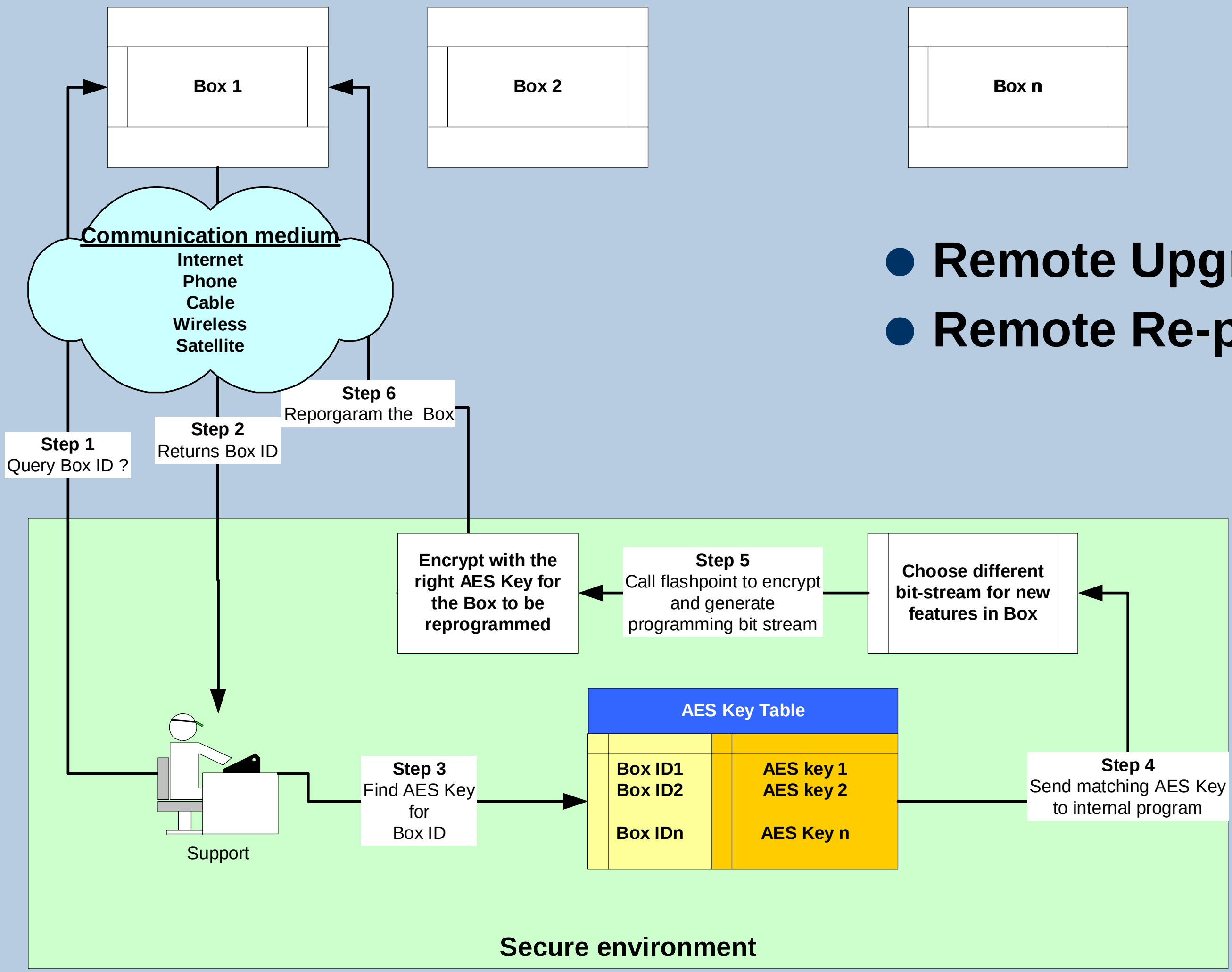
FlashPoint
Custom Security Level



FlashPoint
FlashROM



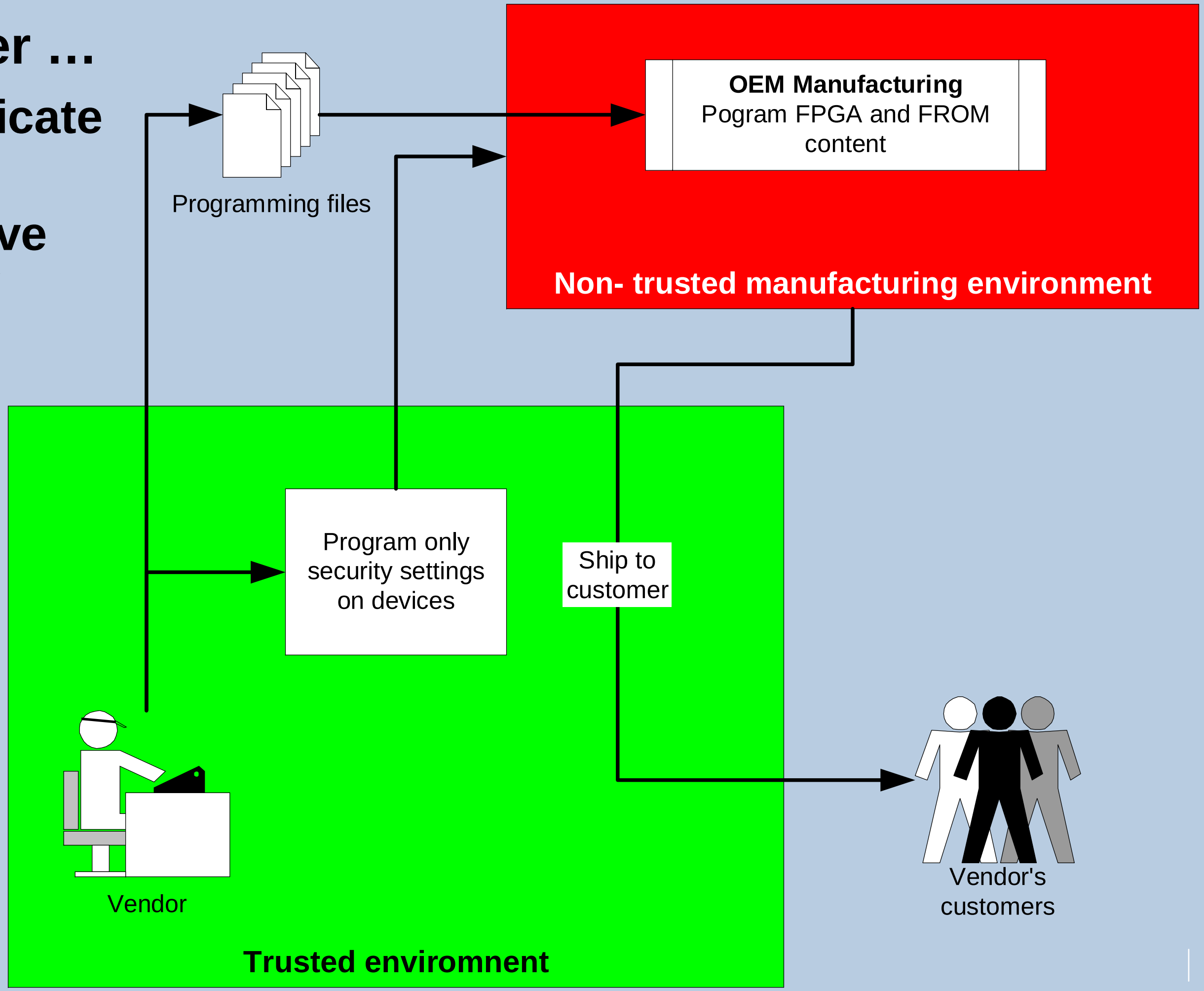
Security Use Model 1
Subscription Example



- Remote Upgrade Features in Box
- Remote Re-programming

Security Use Model 2
Secure OEM Manufacturing Example

- **OEM Manufacturer …**
  - **… Cannot Duplicate Product**
  - **… Does Not Have Encryption Key**



ProASIC3 I/Os

I/O Functions
PA3/E

Regular I/Os

- **Input, Output, Tristate and Bidirectional Buffers**

Registered I/Os

- **Built-in Input, Output and Output-Enable Registers**
  - **Each Register Equivalent to 1-tile Core Flip-flop**
- **Architecture Restrictions**
  - **SINGLE CLR/PRE Port Shared by All Three Internal Registers**
  - **One CLK and One E Port – Used for Input Register**
  - **Second CLK and Second E Port – Shared by Output and Output-enable Registers**

DDR I/Os

- **Built-in Input and Output DDR Registers**
- **Architecture Restrictions**
  - **SINGLE CLR/PRE Port Shared by Input and Output DDR Functions**

Technology Banks

I/O Technology Banks

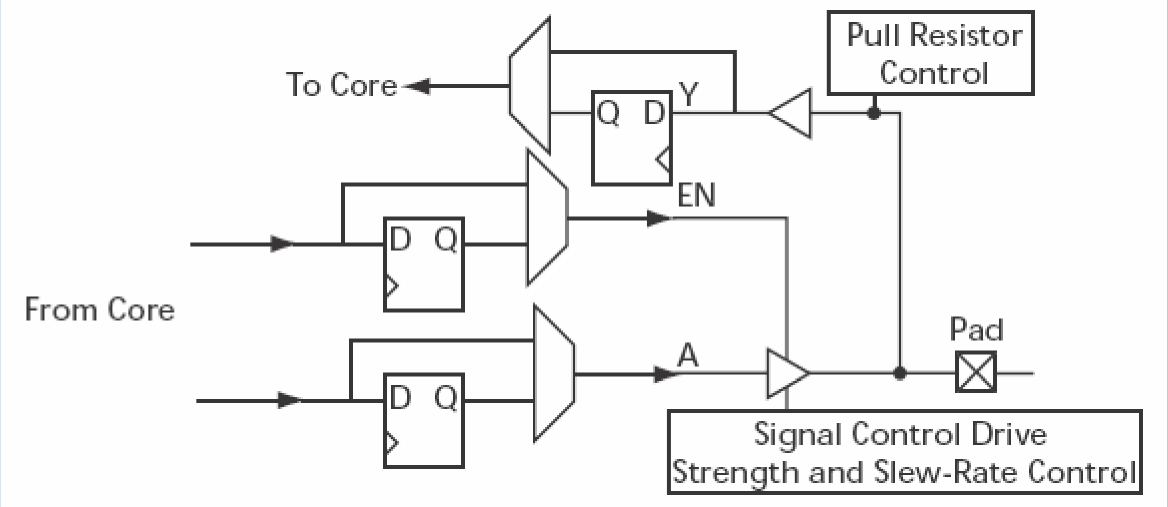
- **User I/Os Partitioned in Multiple Technology Banks**
  - **Number of Banks Die-dependent**
    - ***Eight Banks in ProASIC3E Family***
    - ***Two or Four Banks in ProASIC3 Family***
  - **Each Bank Has its Own VCCi Power Supply PAD**

Mini VREF Banks

- **I/O Technology Banks Partitioned in Multiple Mini VREF Banks**
  - **Each VREF Bank Contains ~16 User I/Os**
  - **Each User I/O in VREF Bank Can Be Configured as VREF Power Supply PAD (i.e., VREF Pin)**
  - **Only One VREF Pin Needed per VREF Bank**

ProASIC3 I/O Tile

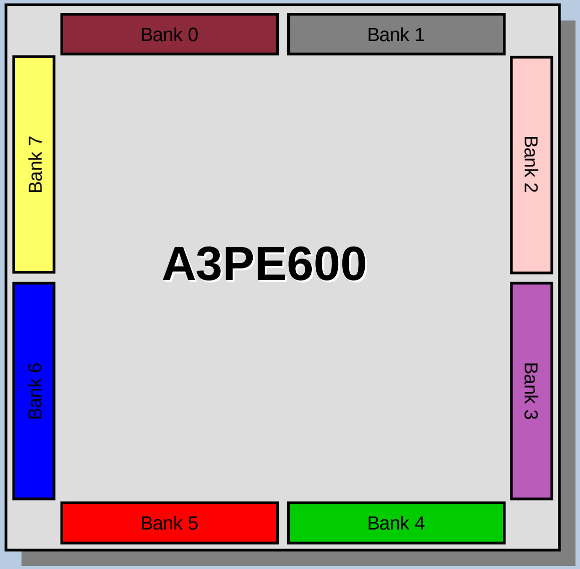
- 3 Registers per I/O (Input, Output, and Enable)
  - Allow Implementation of Single- and Double-data-rate Transmissions



- ProASIC3E I/O Tile Designed to Support DDR

ProASIC3E Pro I/Os

- Bank-Selectable
- Multiple I/O Standard Support
  - **HSTL1, SSTL2/3, GTL+, LVTTL, LVCMOS**
  - **High-Speed 700Mb/s LVDS with External Resistors**
  - **LVPECL I/O**
  - **Hot Swappable**
  - **1.5v - 3.3v Configurable**
- DDR Send/Receive Mode



ProASIC3 Advanced I/Os

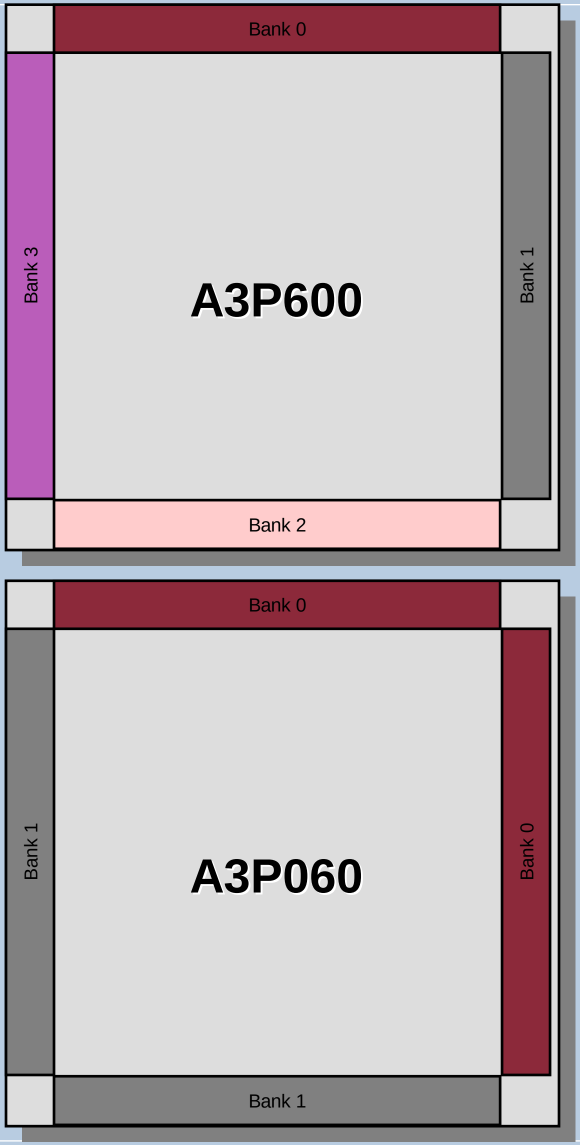
■ Bank-Selectable

■ Multiple I/O Standard Support

- **Single-ended**
  - **LVTTL, LVCMOS**
  - **PCI, PCI-X (except A3P030)**
- **Differential**
  - **Supported by A3P250-A3P1000 East/West Banks**
  - **High-Speed 700Mb/s LVDS with External Resistors**
  - **LVPECL I/O**
- **Hot Swappable – A3P030 only**
- **2 Programmable Slew Rates, 3 Drive Strengths, Weak Pull-up / Pull-down Circuits**

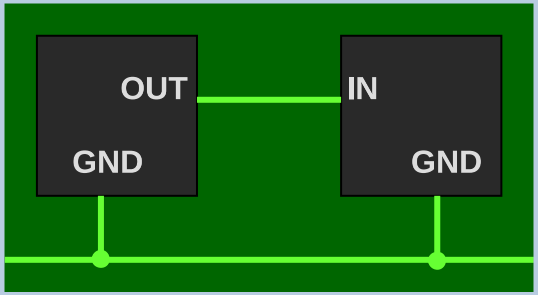
■ DDR Send/Receive Mode

- **On LVDS-supported A3P250-A3P1000 East/West Banks**

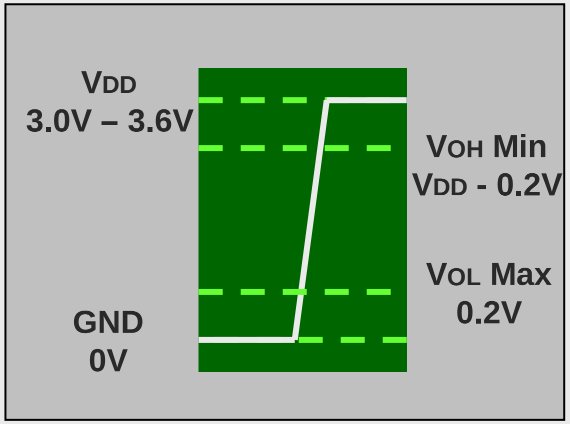


Single-Ended I/O Standards

- Traditional TTL / CMOS / LVTTL / LVCMOS
- I/O Referenced to System GND
- Switching >200MHz Causes Excessive Noise and Power Consumption



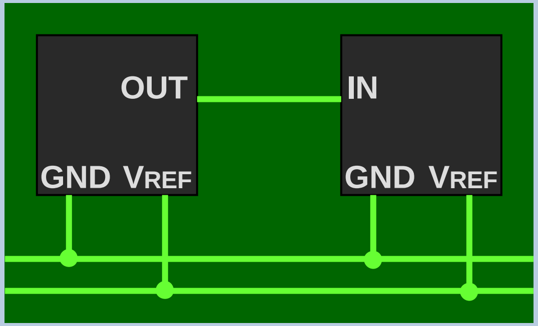
Example: 3.3V LV-CMOS Output



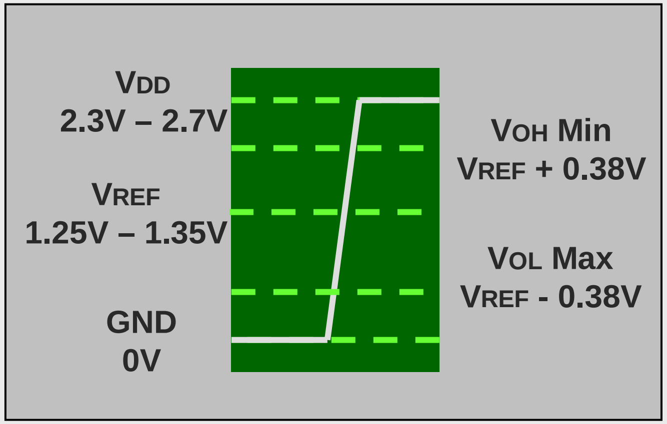
Minimum 2.6V Output Swing

Single-Ended Referenced Standards

- **SSTL and HSTL**
  - **Stub Series Terminated Logic, High-Speed Transceiver Logic**
  - **I/O Referenced to Common Reference Voltage (approximately Mid-rail)**
  - **Smaller Voltage Swing than LVTTL or LVCMOS**
  - **Good for Data Switching up to 300MHz**



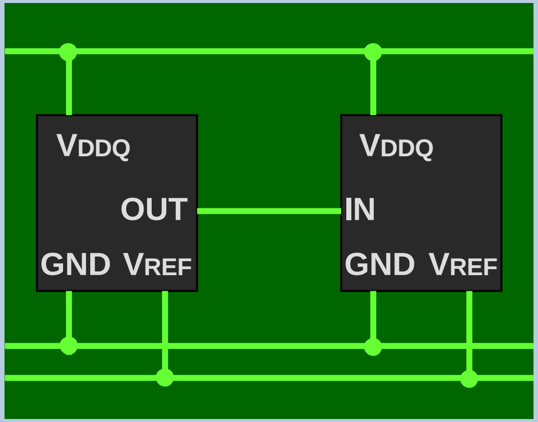
Example: SSTL2 (2.5V) Output

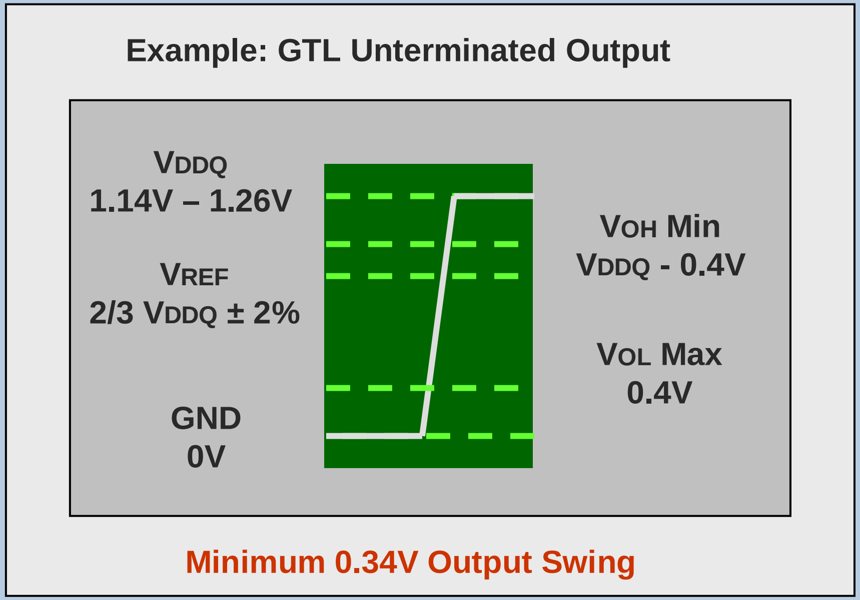


Minimum 0.76V Output Swing

Single-Ended Referenced Standard

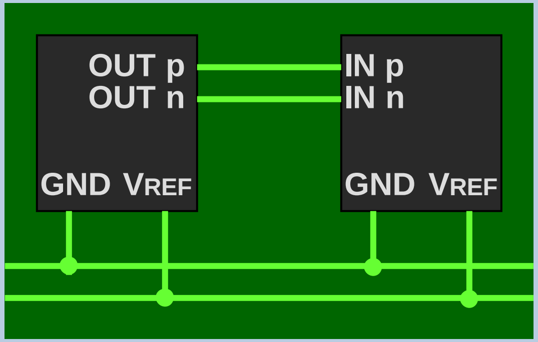
- GTL and GTL+
  - Gunning Transceiver Logic
  - Special Case of Single-Ended Referenced Standard
  - Common Reference Voltage and High-level Rail
  - Smaller Voltage Swing than HSTL or SSTL
  - Patented by Intel – Requires License to Use!



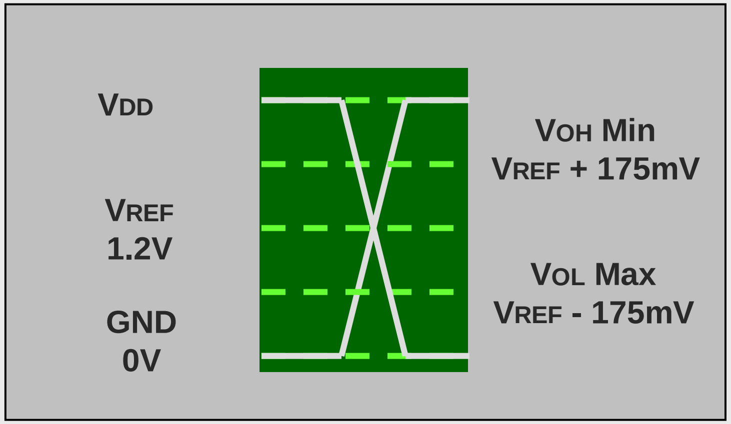


Differential Standards

- LVDS and CML
  - Low-voltage Differential Signaling, Current Mode Logic
  - Uses Two Conductors per Signal (Called "Signal Pair")
  - Signals in Signal Pair Are Referenced to each Other and to Common Reference Voltage
  - Smaller Swing than HSTL or SSTL, as Small as GTL
  - Much Better Noise Immunity than Single-Ended Standards



Example: IEEE 1596.3 LVDS



Minimum 0.35V Output Swing

I/O Output Drive & Slew Options

ProASIC3E Support ONLY

	OUT_DRIVE Drive (mA)
PCI	PCI
PCIX	PCI
HSTL-I	8
HSTL-II	15
SSTL2-I	17
SSTL2-II	21
SSTL3-I	16
SSTL3-II	24
GTL33	25
GTL25	25
GTLP33	51
GTLP25	40
LVDS	24
LVPECL	24

ProASIC3 and ProASIC3E Support

	OUT_DRIVE (mA)							SLEW	
	2	4	6	8	12	16	24		
LVTTL	X	X	X	X	**X**	X	X	**HIGH**	**LOW**
LVCMOS25	X	X	X	X	**X**	X	X	**HIGH**	LOW
LVCMOS25_50	X	X	X	X	**X**	X	X	**HIGH**	LOW
LVCMOS18	X	X	X	X	**X**	X	N/A	**HIGH**	LOW
LVCMOS15	X	X	X	X	**X**	N/A	N/A	**HIGH**	LOW

X – Supported by ALL ProASIC3 devices except A3P030
X – Supported only by ProASIC3E devices
•User can select drive strength (in mA) in software tools

I/O Performance Goals

Std.	Performance
PCI	200 Mhz
PCIX	200 Mhz
HSTL-I	300 Mhz
HSTL-II	300 Mhz
SSTL2-I	300 Mhz
SSTL2-II	300 Mhz
SSTL3-I	300 Mhz
SSTL3-II	300 Mhz
GTL+ 3.3	300 Mhz
GTL+ 2.5	300 Mhz
GTL+ 1.8	300 Mhz
GTL 3.3	300 Mhz
GTL 2.5	300 Mhz
GTL 1.8	300 Mhz
LVDS	350 Mhz
LVPECL	300 Mhz

Standard	1X	2X	3X	4X	5X
LVTTL/LVCMOS 3.3	33 Mhz	100 Mhz	180 Mhz	200 Mhz	200 Mhz
LVCMOS 2.5	33 Mhz	66 Mhz	133 Mhz	180 Mhz	250 Mhz
LVCMOS 1.8	x	33 Mhz	100 Mhz	133 Mhz	200 Mhz

Key:

- (purple) ProASIC3 & ProASIC3E
- (green) ProASIC3E & East and West Banks of ProASIC3 250,400, 600 & 1000
- (pink) ProASIC3E *Only*

I/O Timing
Difference between PA3 and PA3E

- **ProASIC3 I/Os MUCH Faster than ProASIC3E!**
  - **PCI Output Buffer Example (-2, High Slew)**
    - ***Pro I/O (PA3E) = 2.08ns***
    - ***Regular I/O (PA3) = 1.635ns***

Input Buffers

	N-S I/O	
Standard	Tph (%)	Tpl (%)
TTL 3.3v	-16.0%	-21.6%
CMOS 1.5	-17.1%	-13.4%
CMOS 1.8	-14.0%	-15.6%
CMOS 2.5	-11.2%	-8.9%
PCI	-13.1%	-17.0%
PCIX	-11.6%	-10.0%

	E-W I/O	
Standard	Tph (%)	Tpl (%)
TTL 3.3v	-15.5%	-22.5%
CMOS 1.5	-16.6%	-13.9%
CMOS 1.8v	-13.7%	-16.0%
CMOS 2.5v	-10.9%	-9.1%
PCI	-12.7%	-17.6%
PCIX	-11.2%	-10.4%
LVDS (typ)	-13.7%	-24.7%
LVPECL (typ)	-13.6%	-14.1%
LVDS (min)	-19.9%	-23.9%
LVPECL (min)	-11.7%	-17.2%
LVDS (max)	-22.1%	-22.1%
LVPECL (max	-12.5%	-15.9%

Output Buffers

	N-S I/O	
Standard	Tph (%)	Tpl (%)
TTL3.3v	-8.3%	-12.6%
CMOS 1.5v	-8.3%	-13.2%
CMOS 1.8v	-8.1%	-13.1%
CMOS 2.5v	-8.1%	-13.1%
PCI	-13.2%	-18.7%

	E-W I/O	
Standard	Tph (%)	Tpl (%)
TTL 3.3v	-2.2%	-5.2%
CMOS 1.5v	-2.4%	-8.1%
CMOS 1.8v	-2.4%	-7.6%
CMOS 2.5v	-2.3%	-6.3%
PCI	-2.6%	-7.2%
PCIX	-2.6%	-7.2%
LVDS	-2.8%	-2.1%
LVPECL	-2.0%	-1.6%

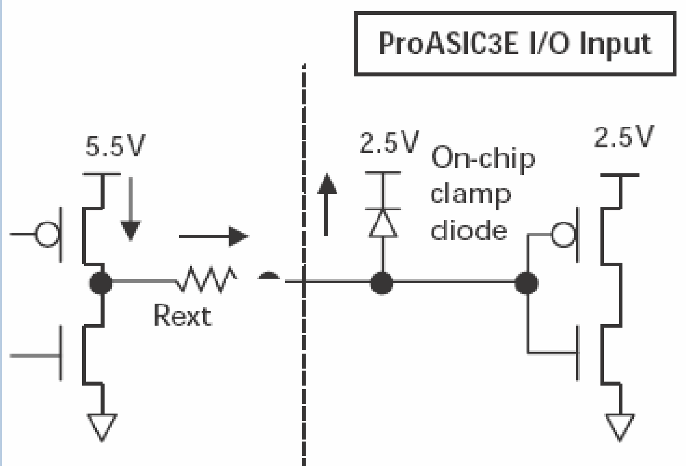
Tables Indicate PA3 Improvement in Delay vs. PA3E

I/O Features Comparison
ProASIC3/E

I/O Standard	Clamp Diode	Hot Insertion	5V Input Tolerance	Input/Output Buffer
LVTTL/LVCMOS 3.3v	No	Yes	Yes[1]	Enabled/Disabled
PCI 3.3v, PCIX 3.3v	Yes	No	Yes[1]	
LVCMOS 2.5v	No	Yes	No	
LVCMOS 2.5/5.0v	Yes	No	Yes[1]	
LVCMOS 1.8v	No	Yes	No	
LVCMOS 1.5v	No	Yes	No	
Voltage-referenced input buffer	No	Yes	No	
Differential LVDS/LVPECL	No	Yes	No	

1) Can be implemented with resistor divider, IDT bus switch, or external resistor

- I/O Absolute Maximum Voltage Rating is 3.6V, and Any Voltage above 3.6V Will Cause Long-term Gate Oxide Failures
- All 5V-tolerance Solutions Limit Voltage at I/O Input to 3.6V or Less

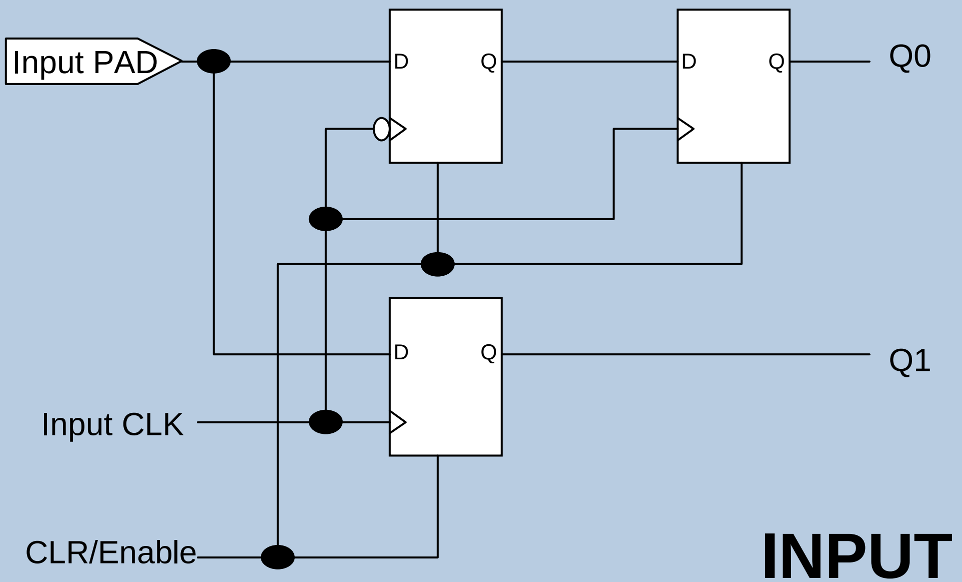


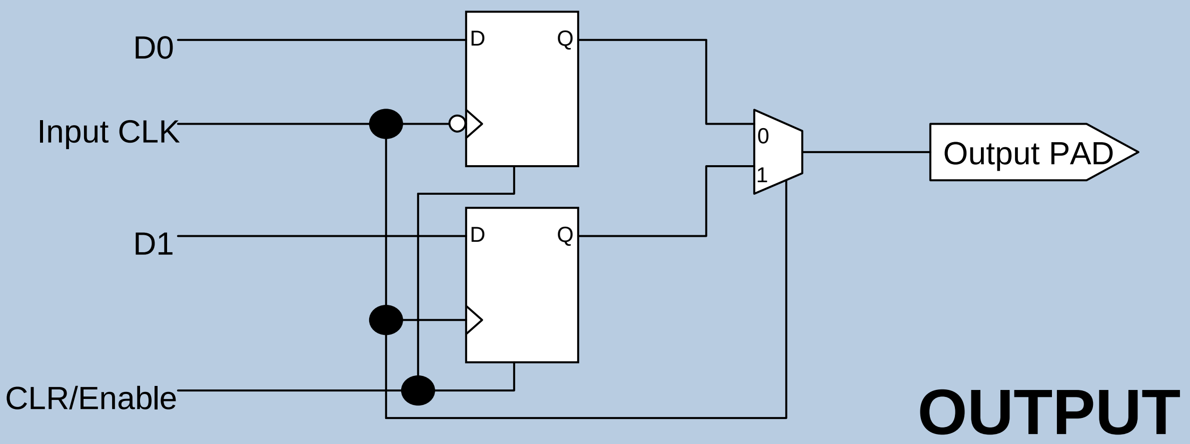
LVCMOS 2.5V/5.0V I/Os

I/O Attributes
ProASIC3E

IO_THRESH	I/O Standard
SLEW	Slew Rate (HIGH, LOW)
OUT_DRIVE	Output Drive Strength (Nominal in mA)
SKEW	Tristate-Enable Delay Enable
RES_PULL	Resistor Pull Circuit
OUT_LOAD	Output Load (to 1023 pF)
REGISTER	Register Combining
IN_DELAY	Input Delay Enable
IN_DELAY_VAL	Delay Value (3-bit Resolution)
SCHMITT_TRIGGER	Schmitt-Trigger Input Enable

Double Data Rate (DDR)





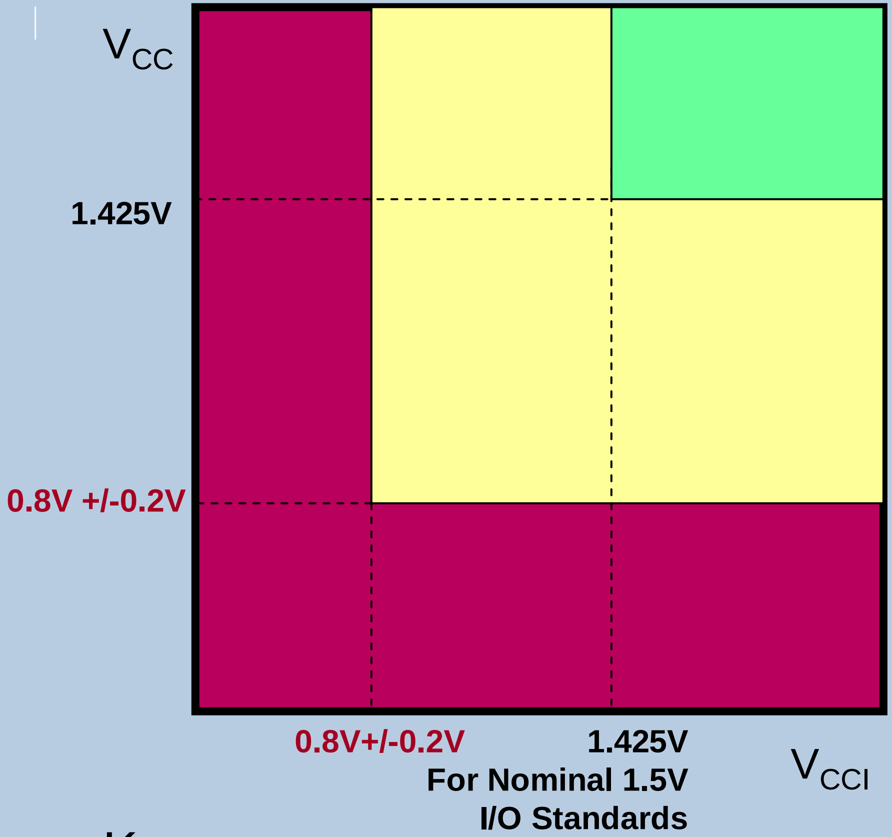
- In DDR Mode, New Data Is Present on Every Clock *Transition*
- ProASIC3/E Provide I/O Tile Support for DDR on Input AND Output Sides
  - **350MHz Input and Output**
  - **HSTL, SSTL, LVDS, and LVPECL**

I/O Banks and User I/O Counts
ProASIC3/E

		A3P 060	A3P 125	A3P 250	A3P 400	A3P 600	A3P 1000	A3PE 600	A3PE 1500	A3PE 3000
	I/O	Std	Std	Std. + 2 banks LVDS	Std. + 2 Banks LVDS	Std. + 2 Banks LVDS	Std. + 2 Banks LVDS	Pro	Pro	Pro
	I/O Banks (+ JTAG)	2	2	4	4	4	4	8	8	8
Single Ended and *Double Ended I/O (pairs)*	VQ100	63	63	63/*12*						
	FG144	97	97	97/*22*	97/*22*	97/*22*	97/*22*			
	TQ144	97	105							
	PQ208		131	155/*36*	155/ *36*	155/ *36*	155/ *36*	145/*66*	145/*66*	145/*66*
	FG256			155/*36*	183/*40*	183/*40*	183/*40*	165/*81*		
	FG484					235/*54*	293/*70*	274/*125*	293/*136*	293/*136*
	FG676								445/*210*	
	FG896									600/290

System-Level Considerations

I/O Power-Up/Down



Key

- Not Functional – I/Os Tri-stated
- Functional – *I/Os Don't Meet Spec*
- Functional – I/Os Meet Speed/Performance Specs

- **ProASIC3 I/Os Enabled If and Only If …**
  - **… Vcc/Vcci above Minimum Trip Points**
    - ***Ramping Up – 0.6v to 1v***
    - ***Ramping Down – 0.5v to 0.8v***
    - ***Vcc and Vcci Have ~200mV of Hysteresis to Avoid Perpetual Current Stage Activation/Deactivation***
  - **… Chip in Operating Mode**
- **During Programming, I/Os Become Inputs with Pull-ups**
- **Outputs Activated ~100ns after Inputs (Programming Complete)**
- **PLL and Charge Pump Power Supplies Have NO Effect on I/O Behavior**

Hot Insertion

Hot Swapping Is Insertion or Removal of Card into/from Powered-up System

Level	Description	Power Applied to Device?	Bus State	GND connected to Device	Circuitry Connected to Bus pins
1	Cold Swap	No	-	-	-
2	Hot Swap during Reset	Yes	Held In reset	Must be made and maintained for 1 ms before, during, after insertion/ removal	-
3	Hot Swap with Bus Idle	Yes	Held idle (no active I/O processes during insertion/removal	Same as level 2	Must remain glitch-free during power-up/power down
4	Hot Swap on Active Bus	Yes	Bus may have active I/O processes, but device being inserted or removed must be idle	Same as level 2	Same as level 3

PA3E Meets LEVEL 4 : Active I/O Processes Are Unaffected by Swapping Activity

Software for PA3

Designer Software Flow

Actel

Import and Compile

MultiView Navigator

Layout

Import

Netlist

- **VHDL, Verilog and EDIF**

Physical Design Constraints (PDC)

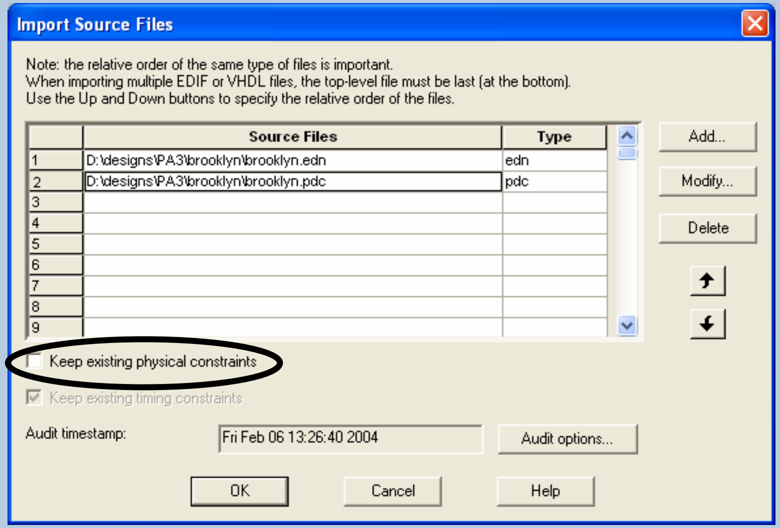
- **Pre-compile PDC Import (Source File, Audited)**
  - **Floorplanning Constraints**
  - **Netlist Optimization**
    - ***I/O Register Combining***
    - ***Global Promotion/Demotion***
    - ***Local Clock Assignment (Spine, Quadrant)***
    - ***Buffer Deletion***
- **Post-compile PDC Import (Auxiliary File)**
  - **Floorplanning Constraints *ONLY***
    - ***I/O Attributes***
    - ***Placement***
    - ***Region***

Synopsys Design Constraints (SDC)

- **Pre-compile SDC Import (Source File, Audited)**
- **Post-compile SDC Import (Auxiliary File)**

Import
Merge

- **User PDC Constraints Merged with Existing Constraints**
- **Keep Existing Constraint – OFF**
  - **Only Placement (Unfixed) Kept from Previous Run**
  - **New PDC Constraints Never Conflict with Previous Initial Placement**
- **Keep Existing Constraint – ON**
  - **If No DRC Error, then *USER* PDC Wins!**
  - **If DRC Error, then:**
    - ***If Abort on PDC Error is ON, then Abort***
    - ***If Abort on PDC Error is OFF, then***
      - ***Warn that Constraint Cannot Be Satisfied and Proceed***
  - **I/Os Cannot Move if Fixed from Previous Run**



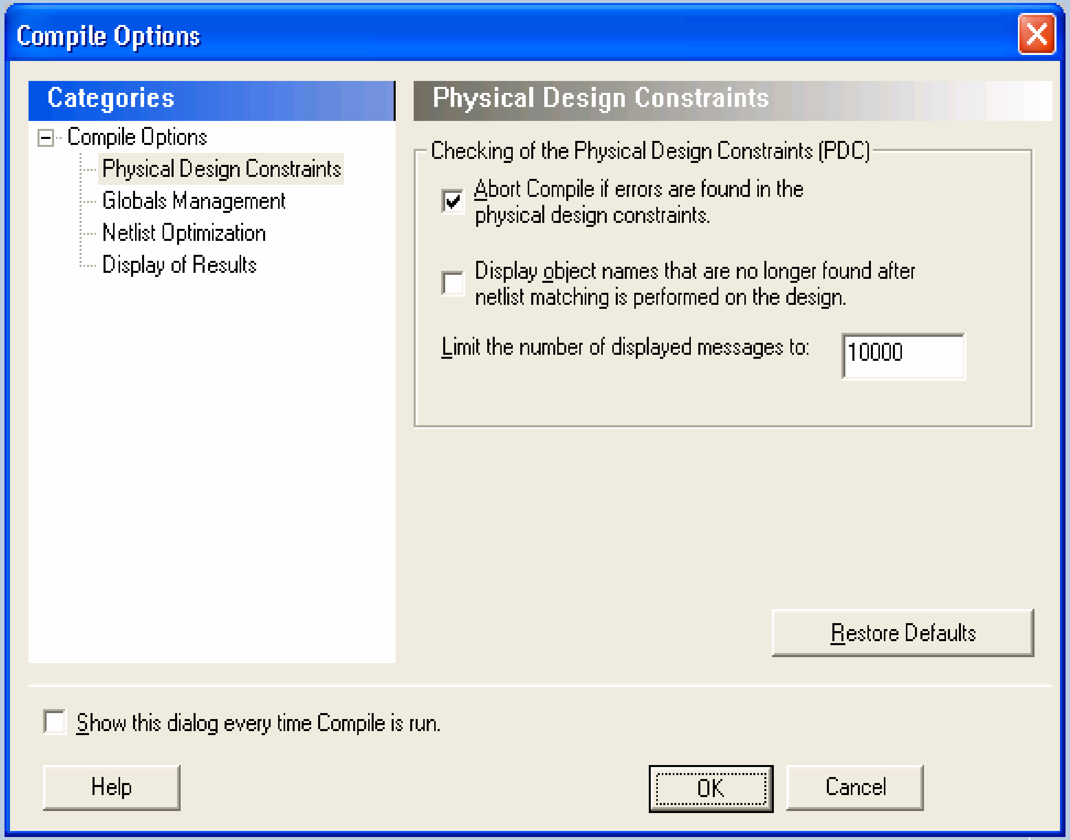
Compile Options

Flow

- Displayed by Default when User Clicks on Compile Button (New in 6.1)
- All Compile Options Accessible using Tcl Options in Script Mode

Categories

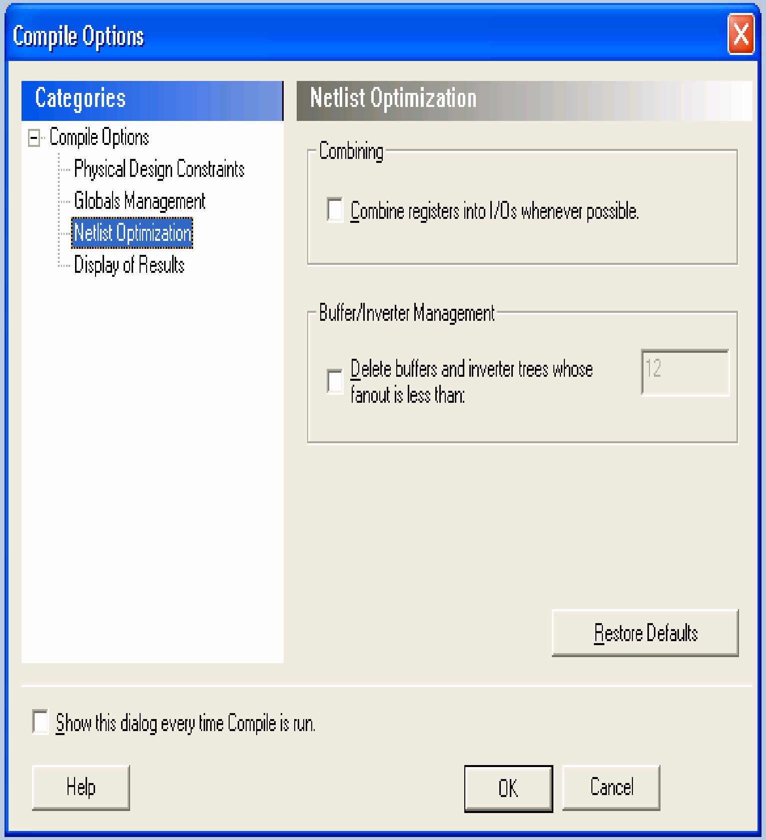
- Physical Design Constraints
- Globals Management
- Netlist Optimization
- Display of Results



Compile Options (cont.)

Netlist Optimization

- **I/O Register Combining**
  - **Compile Opportunistically Combines I/Os and Registers if Architecture Rules Are Satisfied**
- **Buffer/Inverter Deletion**
  - **Inverters Treated like Buffers (only Polarity May Change)**
  - **Buffer (Inverter) Trees Deleted if and Only if Resulting Fanout of Net Is Less than Maximun Fanout Value Specified**
    - ***To Remove ALL Buffers and Inverters …***
      - ***… Select Delete Buffer/Inverter Tree Option***
      - ***Set Maxfanout = 100000 (infinite)***



Compile Task Order

- Standard Netlist DRC
  - Unconnected Inputs, Multiple Drivers on Same Net…
- Tie-off
- Logic Combining
- Removing Unused Logic Cones
- Automatic Global Promotion
- User-defined Global Demotion (from PDC)
- User-defined Global Promotion (from PDC)
- Automatic Global Promotion
- Buffer Deletion
  - Buffers *Always* Removed on Global Nets
- Enable Flip-flop Re-mapping
  - CLR/SET Global Connection Architecture Rule
- I/O Register and DDR Combining
- Local Clock Legalization
  - Shared Instance between Non-overlapping Clock Regions

Compile Report

■ Standard Sections

- **Designer Parameters**
- **Netlist Optimization**
- **Device Utilization**

■ Advanced Sections

- **Advanced I/O**
- **Advanced Net**

Compile Report
Designer/Compile Parameters

```
Family      : ProASIC3E
Device      : A3PE600
Package     : Fully Bonded Package
Source      : D:\designs\PA3\brooklyn\brooklyn.edn
Format      : EDIF
Topcell     : brooklyn
Speed grade : -2
Temp        : 0:25:70
Voltage     : 1.58:1.50:1.42

Abort on PDC error                   : 1
Keep existing physical constraints   : 0

combine_register                     : 0
promote_globals                      : 1
promote_globals_min_fanout           : 200
set_max_globals                      : 6
demote_globals                       : 0
delete_buffer_tree                   : 0
delete_buffer_tree_max_fanout        : 12
localclock_max_shared_instances      : 12
localclock_buffer_tree_max_fanout    : 12
```

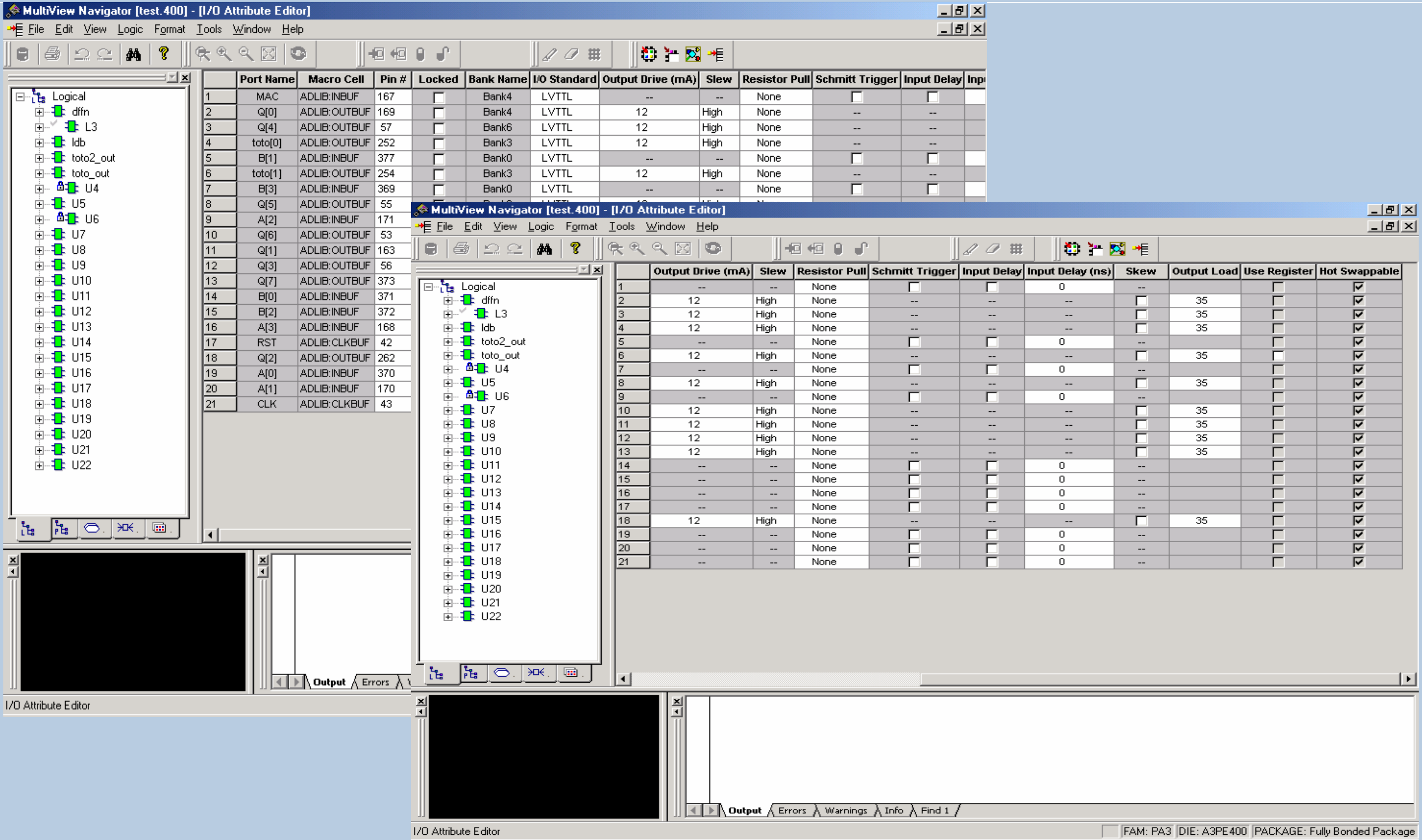
Compile Report
Netlist Optimization Report

```
Netlist Optimization Report
===========================

Optimized macros:
  - Dangling net drivers:   0
  - Buffers:                0
  - Inverters:              0
  - Tieoff:                 0
  - Logic combining:        47

    Total macros optimized  47

Warning: CMP503: Remapped 485 enable flip-flop(s) to a 2-tile implementation because
the CLR/PRE pin on the enable flip-flop is not being driven by a global net.
```

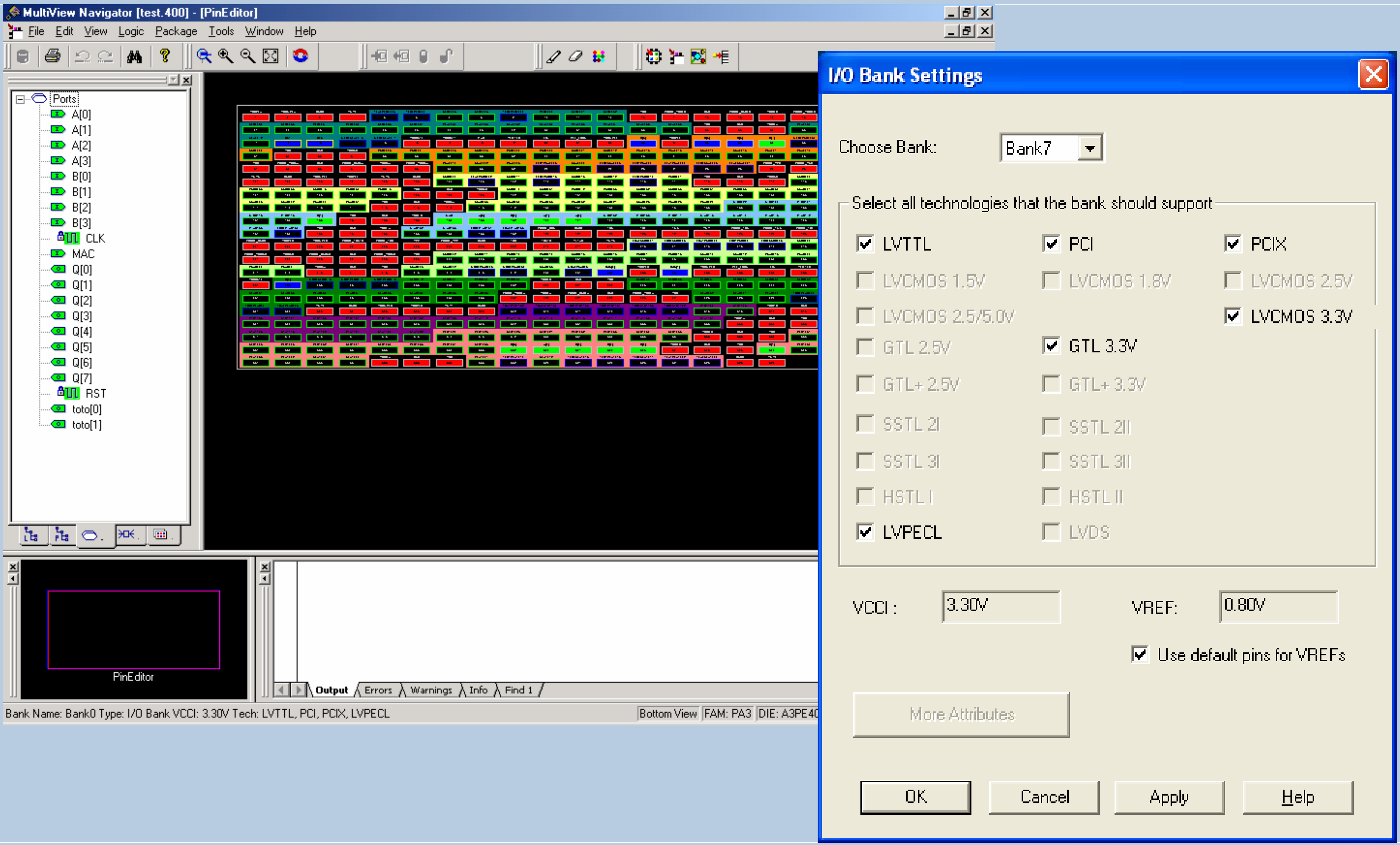
Compile Report
Device Utilization Report

```
Device utilization report:
==========================
    CORE                       Used:   9005  Total:  13824   (65.14%)
    I/O (W/ clocks)             Used:    104  Total:    270   (38.52%)
    GLOBAL (Chip+Quadrant)     Used:      6  Total:     18   (33.33%)
    PLL                        Used:      0  Total:      6   (0.00%)
    RAM/FIFO                   Used:      0  Total:     24   (0.00%)

Core Information:
    Type    | Instances    | Core tiles
    --------|--------------|-----------
    COMB    | 5863         | 5863
    SEQ     | 2657         | 3142

Global Information:
    Type            | Used    | Total
    ----------------|---------|-------------
    Chip global     | 6       | 6  (100.00%)
    Quadrant global | 0       | 12 (0.00%)
```

MultiView Navigator
I/O Attribute Editor

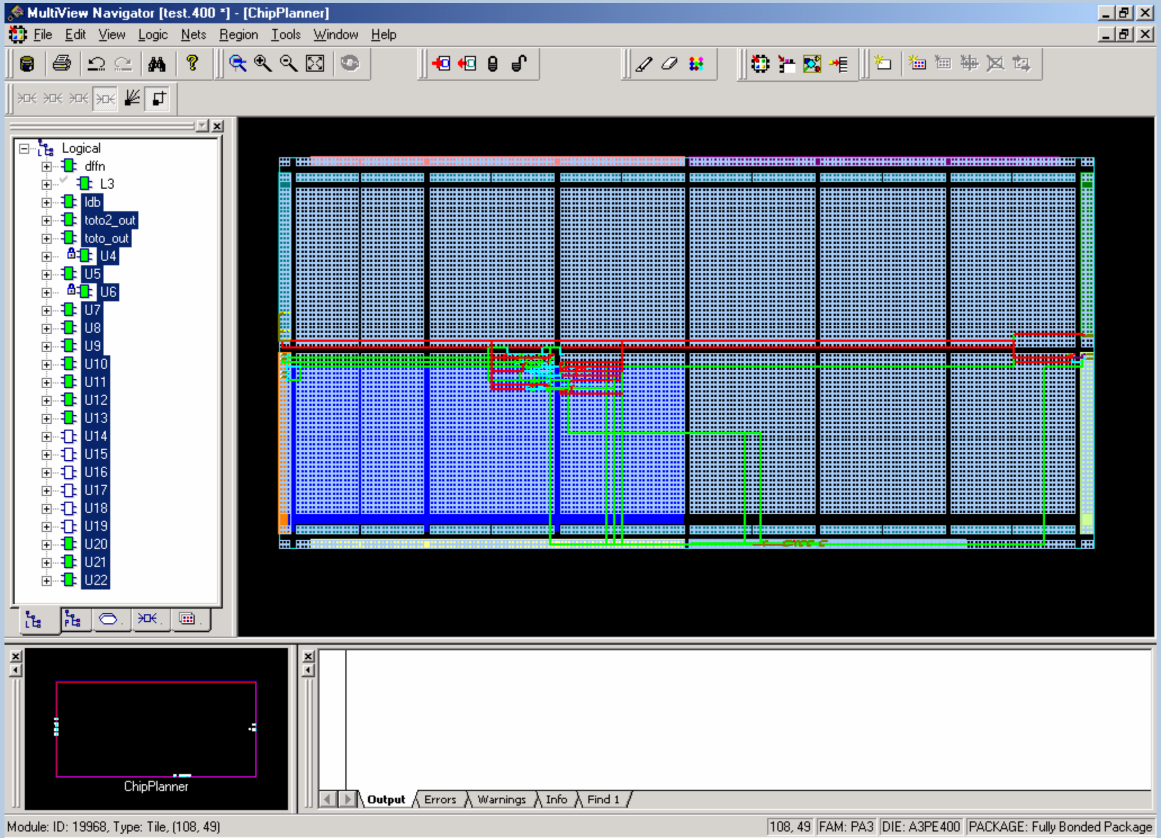


MultiView Navigator
PinEditor



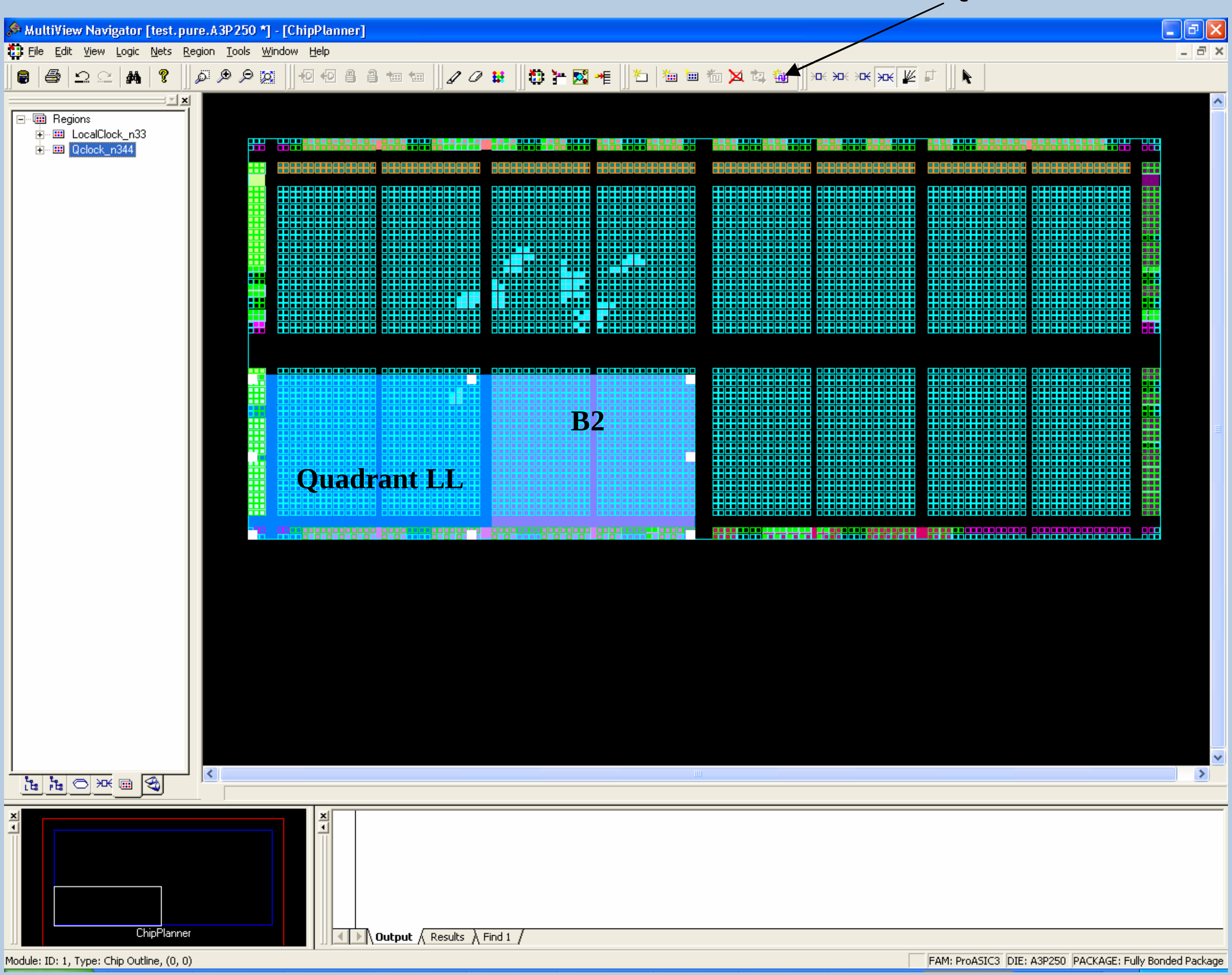
MultiView Navigator
ChipPlanner

- **Region Management**
  - **Inclusive**
  - **Exclusive**
  - **Empty**
  - **Rectilinear**
  - **Multi-types**
    - ***Core, I/O, RAM***
- **Quadrant Clock**
  - **Assignment to Clock Nets**
- **Local Clocks**
  - **Display Only**
- **Routing View**
  - **Display Only**



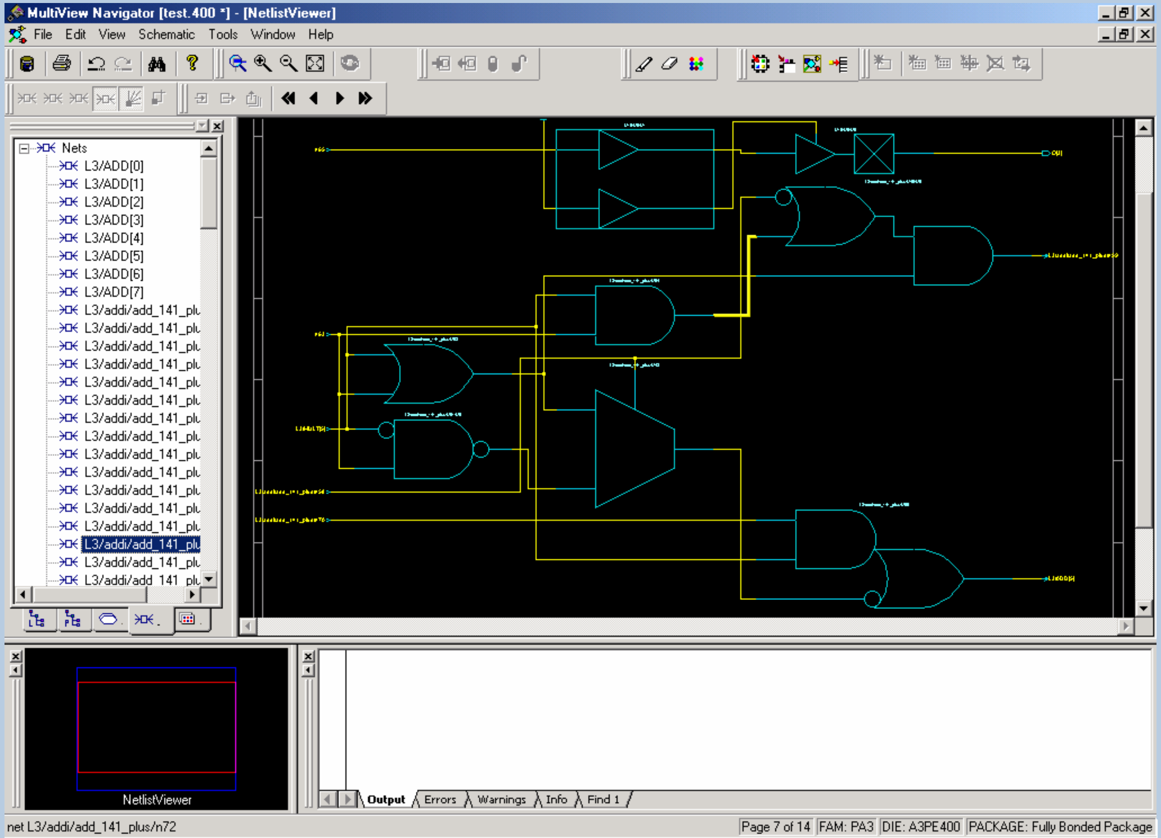
MultiView Navigator
ChipPlanner

Quadrant Clock Icon



MultiView Navigator
Netlist Viewer

- Pre-optimized View
- Post-optimized View
  - Back-annotation Netlist



Pre-layout Checker

Pre-layout Requirements

- **I/O Banks MUST have Vcci and Vref Assigned if Mixed Voltages Are Used in Design**
  - **Placer Does Not Automatically Assign Vcci and Vref Voltages to I/O Banks**
- **There No More than Six Unassigned Clock Macros**
  - **Quadrant Clocks Must Be Assigned Manually**
    - ***Clock Placer Does Not Automatically Assign Clock Macros to Quadrant Clock Locations***

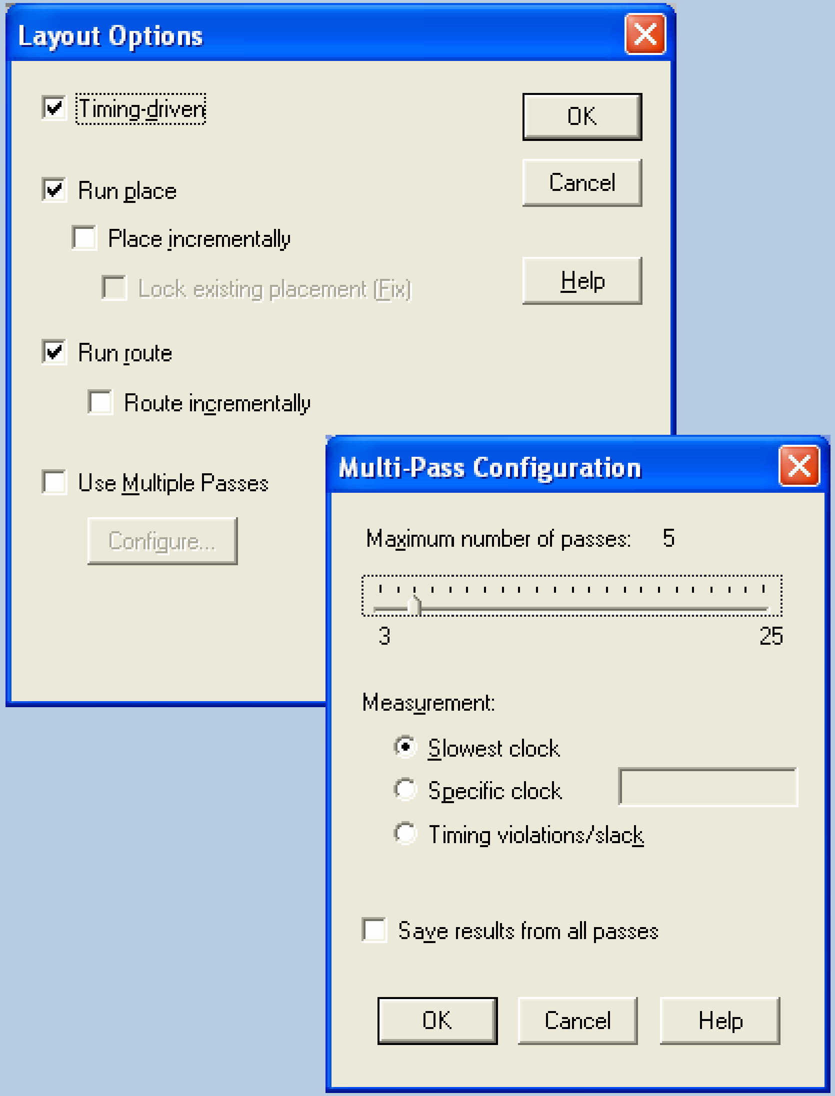
Pre-layout Checks

- **Infeasible Constraints Identified before Layout**

Layout

Layout Options

- **Timing Driven (On/Off)**
- **Incremental Placement**
  - **On/Off/Fix**
- **Incremental Route**
  - **On/Off**
- **Known Limitations**
  - **Router Cannot Run in Incremental Mode if there Has Been Change in Global Assignments**
    - ***Users Must Manually Uncheck Incremental Routing Option and Re-run Layout***
    - ***NOTE: In APA, this Happens Silently – User May Be Unaware that Routing Is Not Incremental***



Layout

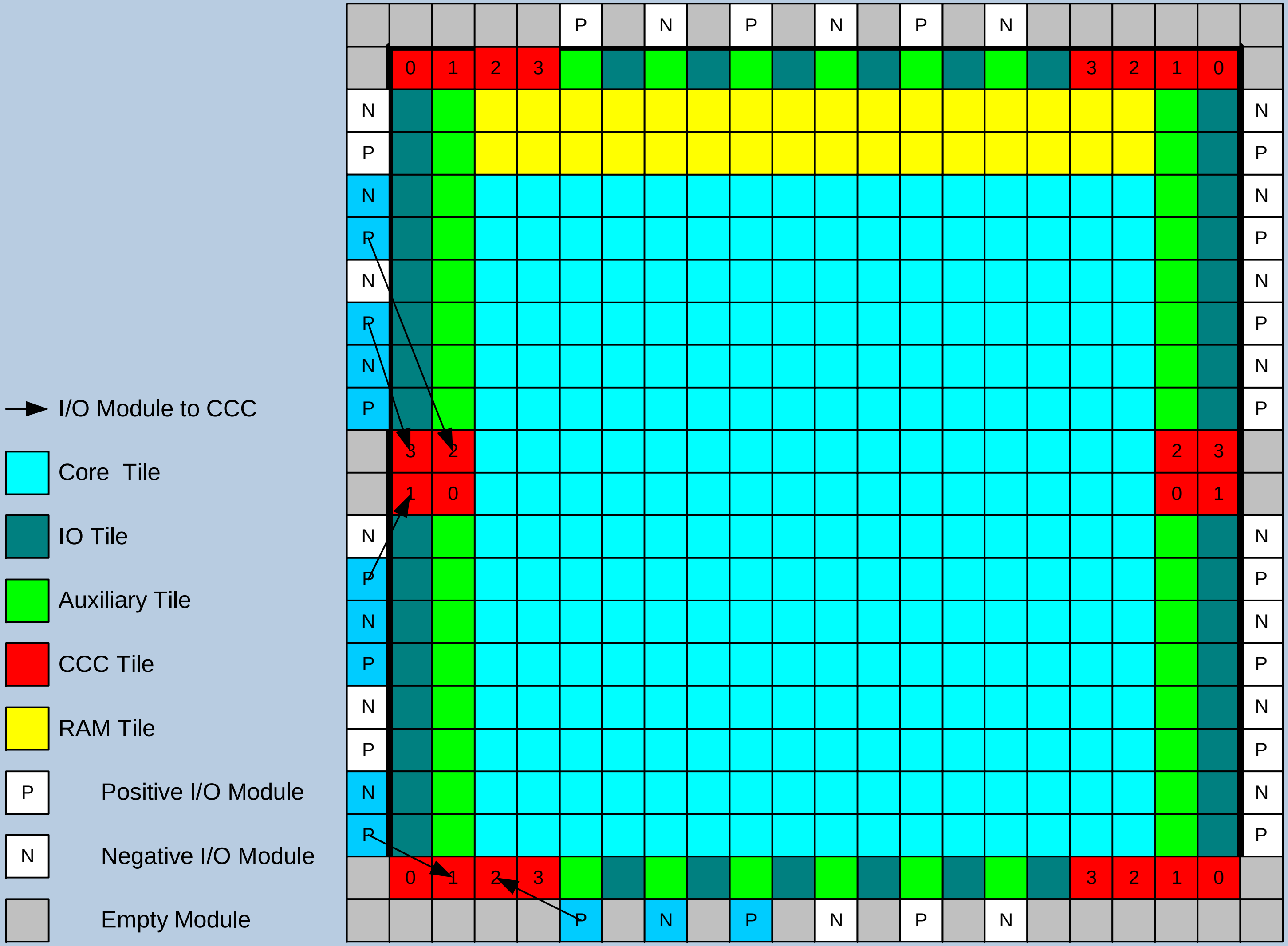
- Clock Placer
  - Automatically Places Chip-wide Global Clocks *ONLY*
- Aggregation Solver
  - Local Clock (Aggregation) Solver Guarantees that Router Does Not Demote any Local Clock
- Timing-Driven Placer
  - Use NGT-TDPR Integrated Flow
- Timing-Driven Router
  - Use NGT-TDPR Integrated Flow
- Incremental Place
- Incremental Route

Timing Flow

- SDC Constraints
- Pre-layout Timing
  - **Estimated Wire Load Model**
- Post-layout Timing
  - **AWE Calculator**
  - **Post-LPE Data Provided by DCT**
- Power Estimation and Back-annotation
  - **Use Post-compile Netlist**
    - **Export New Netlist File (VHDL/Verilog)**
    - **Export SDF File**

Clock Conditioning Circuitry

CCC Locations
Floor Plan



Clock Source Selection

- CLKBUF* (I/O->CCC-bypass)
  - 3 Possible I/O Locations for Each Global Location (GLA/B/C)
- CLKINT
  - 1 Core Input for Each Global Location (GLA/B/C)
- CLKDLY
  - I/O -> CLKDLY (Hardwired)
    - 3 Possible I/O Locations for Each Global Location (GLA/B/C)
  - I/O -> CLKDLY (External) or CORE -> CLKDLY
    - 1 Core Input for Each Global Location (GLA/B/C)
- PLL
  - I/O -> PLL (Hardwired)
    - 3 Possible I/O Locations for GLA
  - I/O -> PLLINT -> PLL (External) or CORE -> PLL
    - 1 Core Input for GLA

Clock Source Selection
Designer Software Flow

Compile

- **Create Hard Macros for CCC Macro including Hardwired-I/O Reference Clock (if Present) and Hardwired-I/O External Feedback Clock**
- **Remove Unused Globals from PLL Macro**
  - **PLL Hard Macro Uses Only Minimum Number of Tiles Required**
- **Mark Global Outputs from CLKBIBUF, CLKDLY and PLL Macros "Essential"**
  - **Assures These Global Outputs Can Never Be Demoted**

MVN

- **Can Drag and Drop CCC Hard Macros in ChipPlanner and PinEditor**
  - **When I/O Is Part of CCC Macro, Dropped Target Should Be I/O Module or Package Pin**

Clock Source Selection
Designer Software Flow

Place & Route

- **Fully-Automatic Clock Placement of up to 6 Chip-wide Globals**
  - **All CCC Macros Supported for Automatic Placement**
- **May Need to Assign Some Clocks to Quadrant Clocks Using MVN or PDC**

Timing

- **CLKINT, CLKBUF*, CLKDLY => Buffer-like Behavior**
  - **Back-annotation Supported**
- **PLL => Register-like Behavior**
  - **CLKA->GLA, CLKA->GLB/YB and CLKA->GLC/YC Arcs Computed Using Full PLL Configuration**
  - **Back-annotation Not Supported**
- **No Constraint Propagation through PLL Macros**

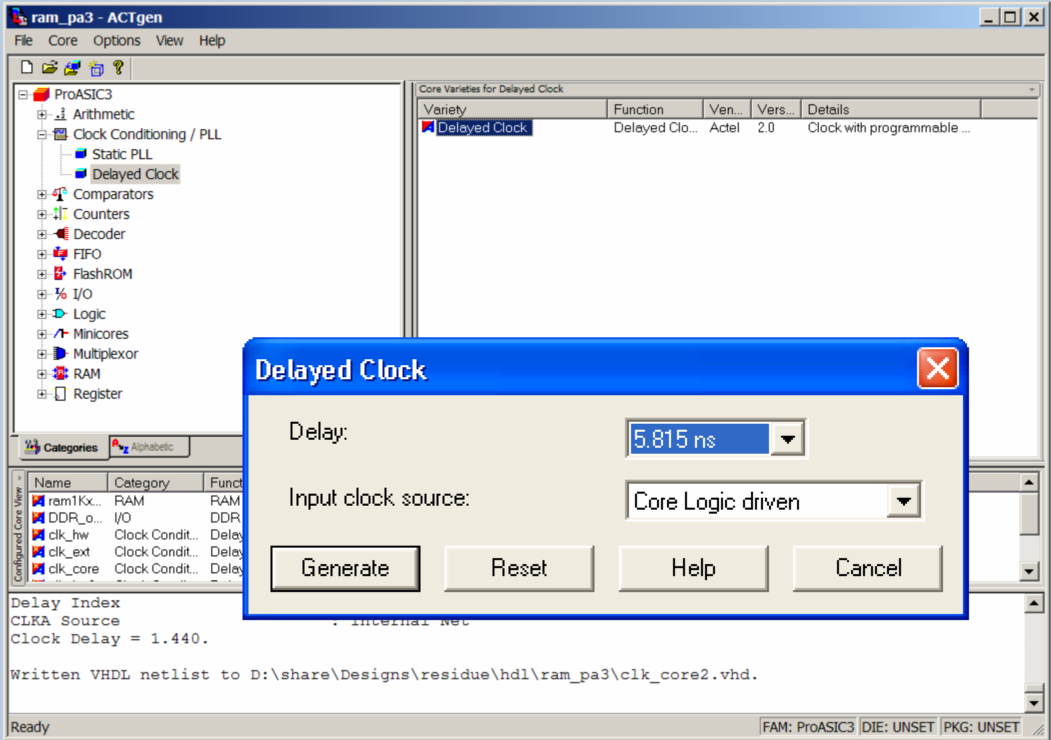
ACTgen Clock Delay Configurator

Delay Selection

- **Total Delay from Input to Output**
  - **Typical Numbers**
  - **Consistent with Timer and Timing Simulation Typical Numbers (NOT Perfectly Linear!)**

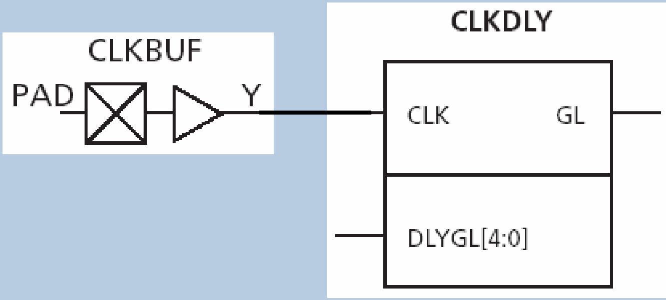
Clock Source Selection Options

- **Hardwired I/O**
- **Routed I/O**
- **Core Logic**

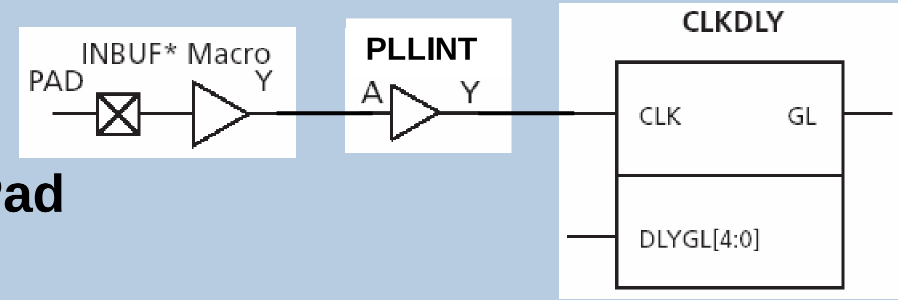


CLKDLY Clock Sources
Selection Options

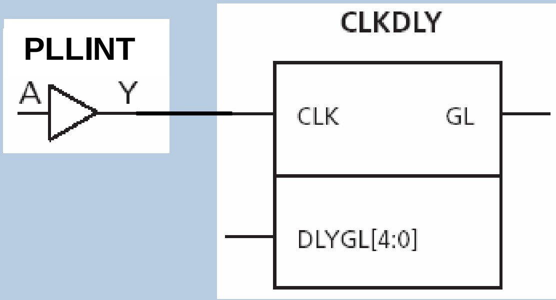
- **Hardwired I/O**
  - **Source – Clock Pad**



- **External I/O**
  - **Source – Regular I/O Pad**



- **Core Logic**
  - **Source – Internal Net**



ACTgen Visual PLL
Features

Clock Frequency Generator

- **On-the-fly Computation of All CCC Dividers to Obtain Closest Match to User's Frequency Requirements**
  - **Actual Frequency Reported**

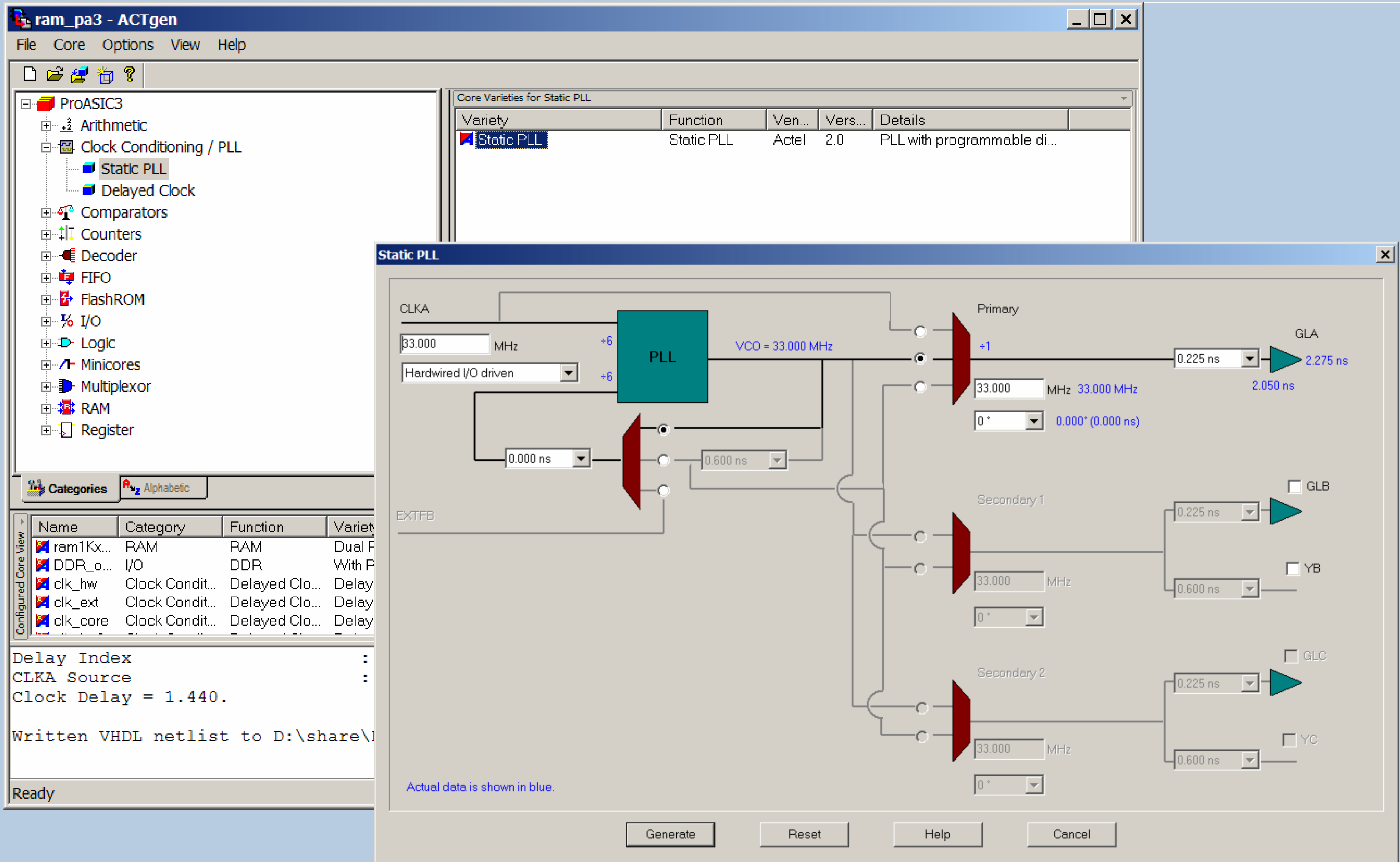
Clock Skew Management

- **On-the-fly Computation of Total Delay from Reference Clock to Any Generated Clock**
  - **Typical Numbers – Consistent with Timer and Timing Simulation**

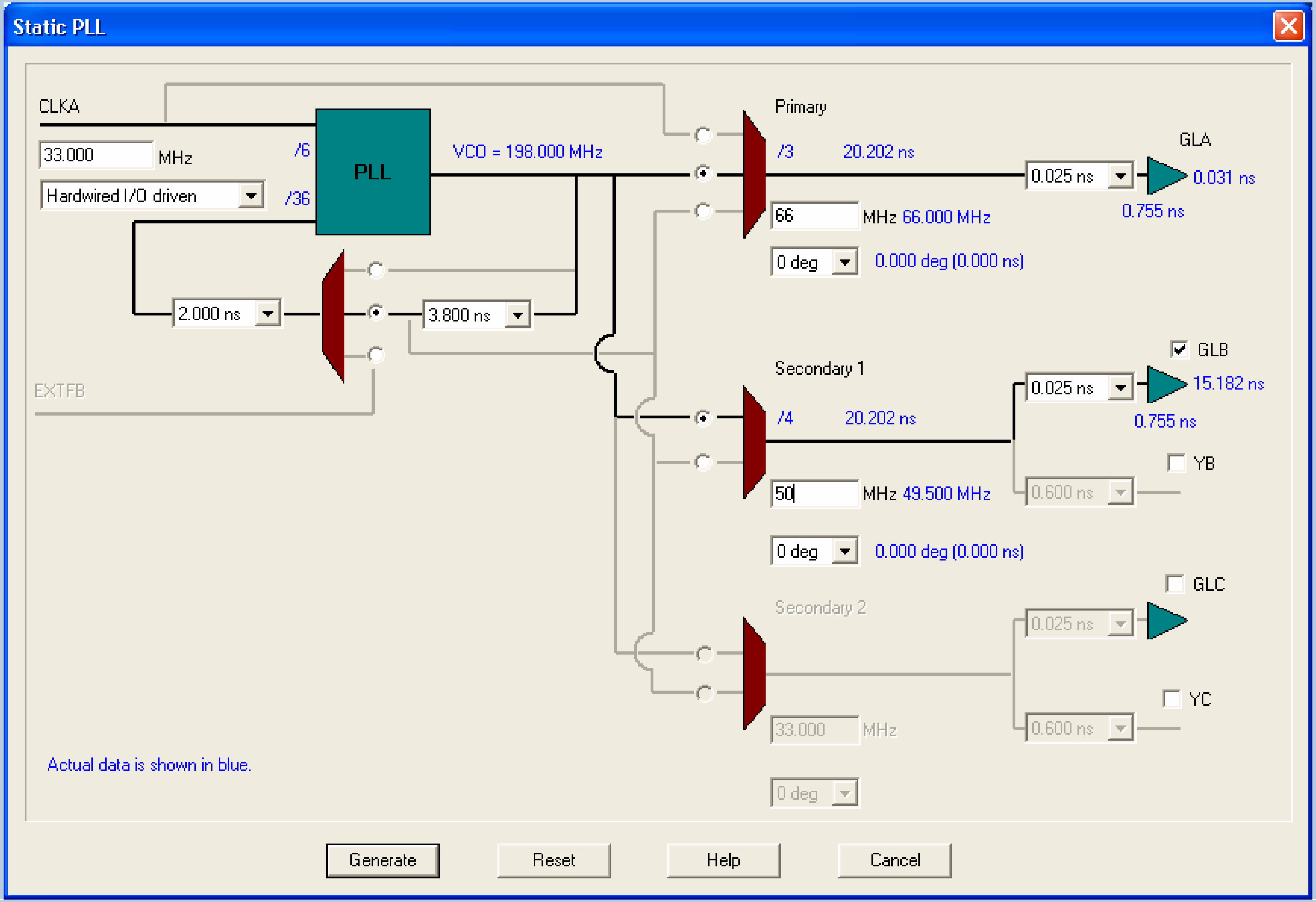
Clock Source Selection Options

- **Hardwired I/O**
- **External I/O**
- **Core Logic**

Visual PLL
Invoking from ACTgen



ACTgen Visual PLL
GUI



Globals Management

Global Clock Promotion
Synthesis

RTL Is Preferred Method of Defining which Signals Are Assigned to Clock Network

- **Clock Macro Instantiation (CLKBUF*, CLKINT, CLKDLY*, PLL)**
  - **Guaranteed Honored by Synthesis Tools and Designer Software**
- **Automatic Clock Inference (Synplicity)**
  - **May Not Give Expected Results**
    - ***Inferring Based Only on Fanout (Heuristic)***
    - ***Net Type (Clock/Reset) Not Considered***
    - ***Special Architecture Rules (i.e., Enable Flip-flop SET/CLR) Not Easily Defined***

Optimization Issue – Logic Duplication and Buffering of High-Fanout Nets

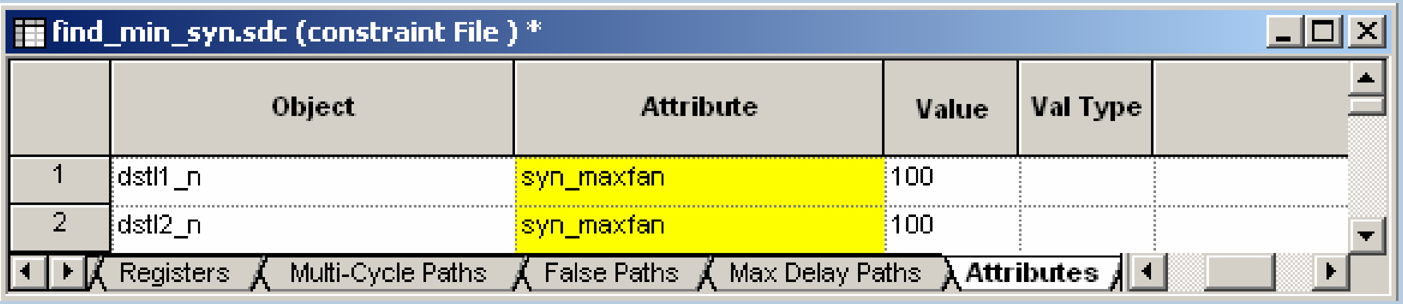
  - **Designer Does NOT Remove Buffers from High-fanout Nets**
  - **May Create Problems Assigning to Clock Networks in Designer Flow**
    - ***Nets Assigned to Local Clock Networks Are Not Optimized by Synthesis Tools***
    - ***Users Should Exclude Nets Intended for Spines from Buffering in Synplify***
    - ***Use `syn_maxfan` or `syn_noclockbuf` Attributes***

syn_maxfan
Synthesis Attribute

- Controls Maximum Fanout of Instance, Net or Port
  - **Limit Specified by this Attribute May Be Treated as Hard or Soft Depending on where it Has Been Specified**
    - **Soft Limit May Not Be Honored if it Degrades Performance**
  - **You Can Apply syn_maxfan Attribute to Module, Register, Instance, Port, or Net**
    - **syn_maxfan on *Net* Has Highest Priority**
    - **syn_maxfan on Block Has Higher Priority than Global Fanout Limit**

syn_maxfan
Attribute Usage

■ SCOPE Constraint Editor Usage



■ SDC File Syntax

define_attribute { object } syn_maxfan { integer }

- **Example: Limits Fanout for Signal clk to 200**

```
.   .   .
define_attribute {clk} syn_maxfan {200}

.   .   .
```

syn_maxfan
Attribute Usage (cont.)

Verilog Syntax

object /* synthesis syn_maxfan = "value" */ ;

- **Example:**

```
module test (registered_data_out, clock, data_in);
output [31:0] registered_data_out;  input clock;
input [31:0] data_in /* synthesis syn_maxfan=1000 */;
reg [31:0] registered_data_out /* synthesis syn_maxfan=1000 */;
// Other code
```

VHDL Syntax

attribute syn_maxfan of object : object_type is "value" ;

- **Example:**

```
entity test is
        port(clock : in bit;
             data_in : in bit_vector(31 downto 0);
             registered_data_out: out bit_vector(31 downto 0))
attribute syn_maxfan : integer;
attribute syn_maxfan of data_in : signal is 1000;
-- Other code
```

syn_noclockbuf
Synthesis Attribute

Selects/Deselects Automatic Clock Buffering

- **Value of '1' (or Boolean TRUE) Turns OFF Automatic Clock Buffering**
- **You Can Apply syn_noclockbuf Attribute to Module, Register, Instance, Port, or Net**

syn_noclockbuf
Attribute Usage

■ SCOPE Constraint Editor Usage

NOT IN PROJECT!! DDR_16_syn (constraint File) *

	Object	Attribute	Value	Val Type
1	clk_in1	syn_noclockbuf	1	
2	clk_in2	syn_noclockbuf	0	

False Paths / Max Delay Paths / **Attributes** / Other

■ SDC File Syntax

define_attribute { object } syn_noclockbuf { integer }

- **Example: Turns OFF Automatic Clock Buffering for Net `clk`**

```
. . .
define_attribute {clk} syn_noclockbuf {1}
. . .
```

syn_noclockbuf
Attribute Usage (cont.)

Verilog Syntax

object /* synthesis syn_noclockbuf = "value" */ ;

- **Example:**

```
module test (registered_data_out, clock, data_in);
output [31:0] registered_data_out;  input clock;
input [31:0] data_in /* synthesis syn_noclockbuf=1 */;
reg [31:0] registered_data_out /* synthesis syn_noclockbuf=1 */;
// Other code
```

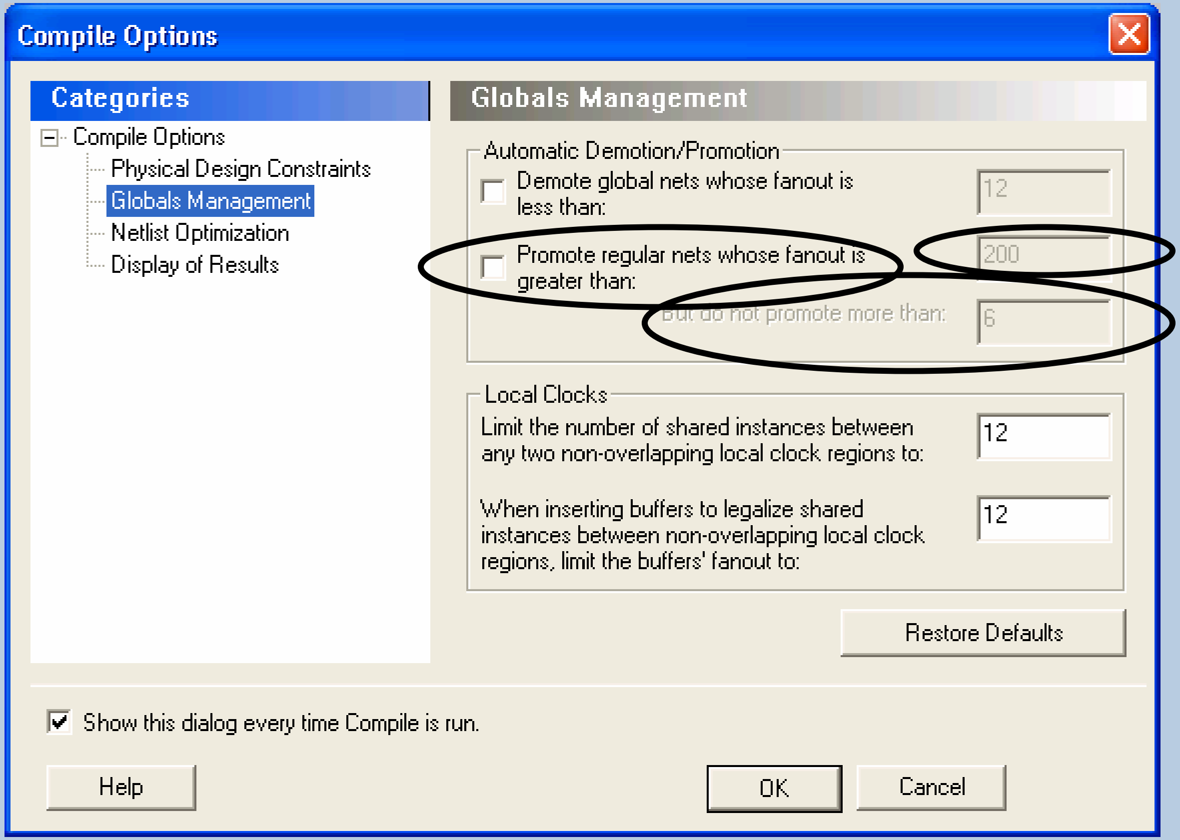
VHDL Syntax

attribute syn_maxfan of object : object_type is "value" ;

- **Example:**

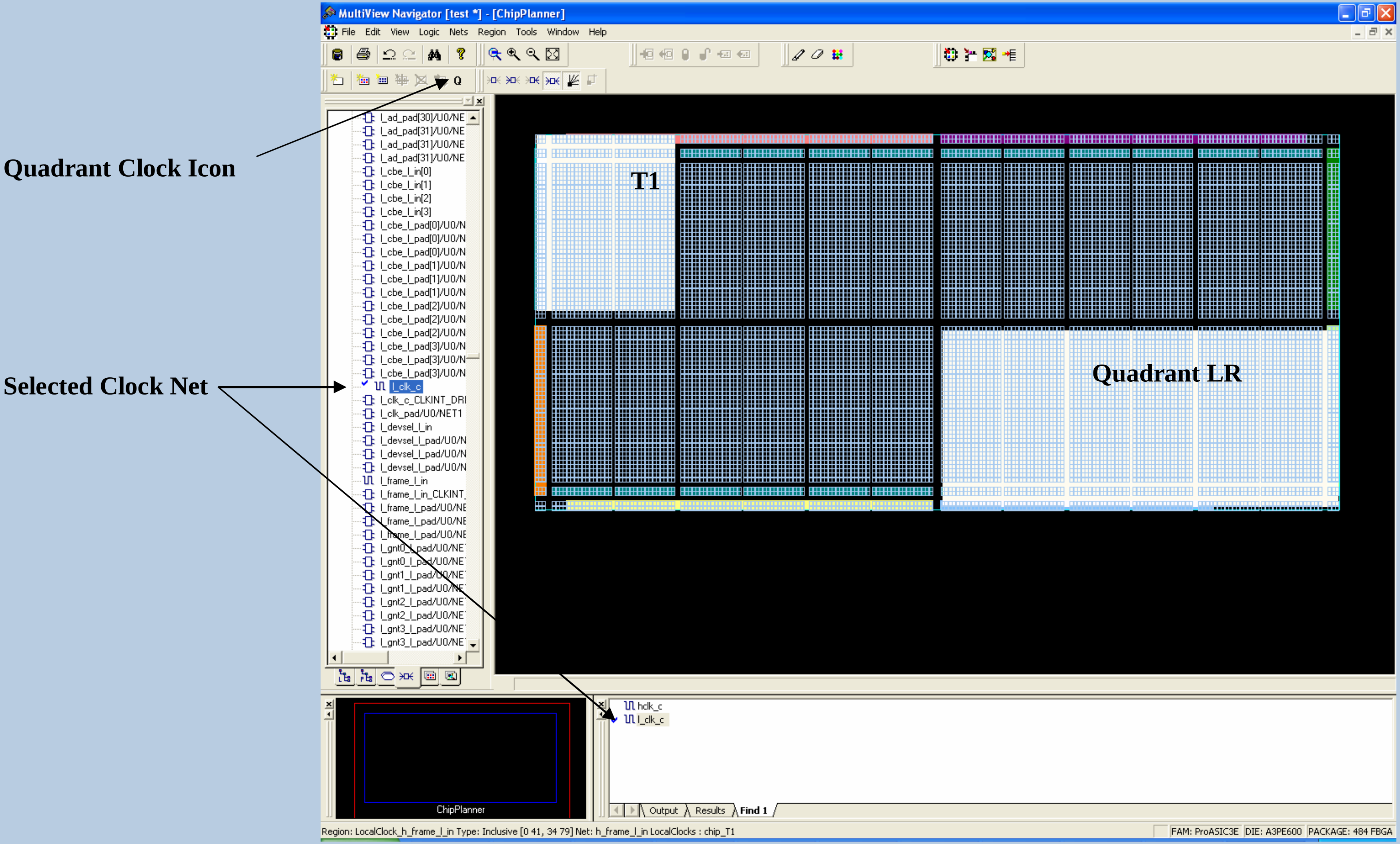
```
entity test is
        port(clock : in bit;
             data_in : in bit_vector(31 downto 0);
             registered_data_out: out bit_vector(31 downto 0))
attribute syn_noclockbuf : boolean;
attribute syn_noclockbuf of data_in : signal is true;
-- Other code
```

Automatic Global Clock Promotion
Compile Option

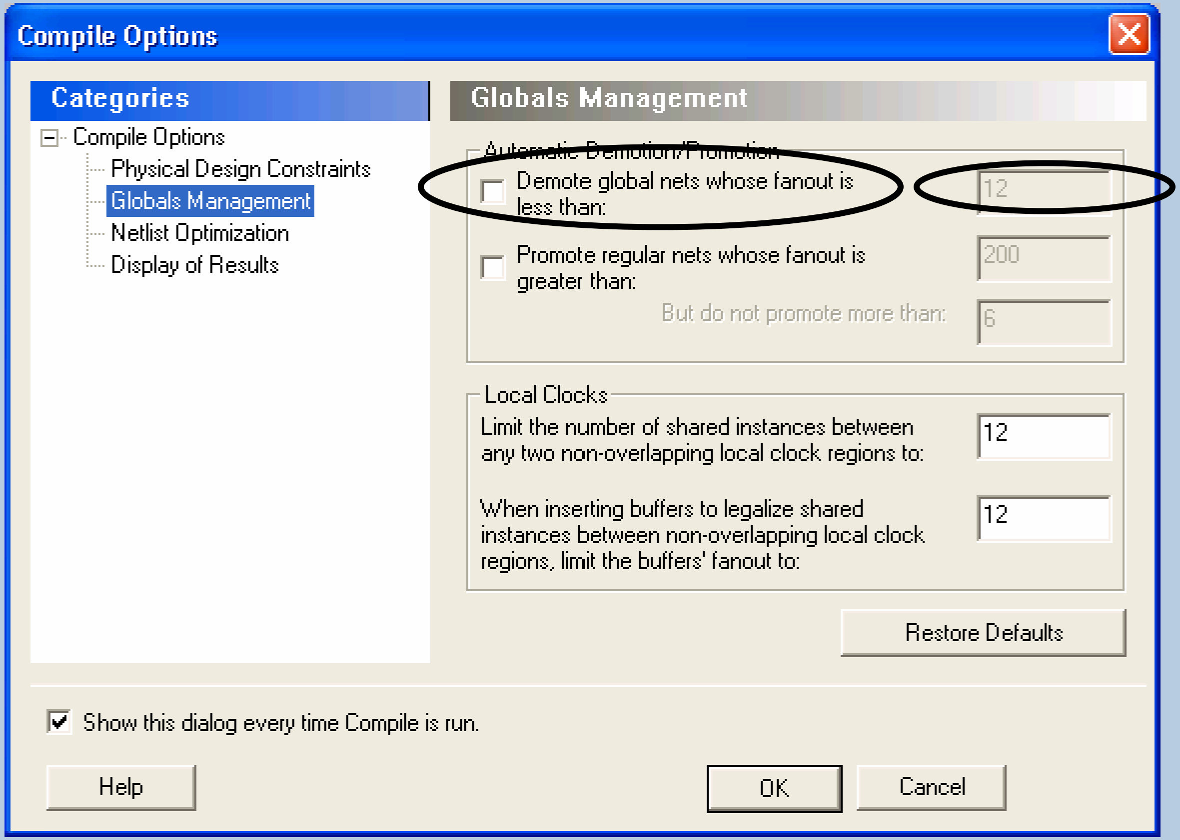


Note: Can Be Done with TCL Command

Global Clock Promotion
MultiView Navigator



Automatic Global Clock Demotion
Compile Option



Note: Can Be Done with TCL Command

Post-Compile Clock Reports
Device Utilization Report

```
Device utilization report:
==========================
    CORE                      Used:   9005  Total:  13824   (65.14%)
    I/O (w/ clocks)            Used:    104  Total:    270   (38.52%)
    GLOBAL (Chip+Quadrant)    Used:      6  Total:     18   (33.33%)
    PLL                       Used:      0  Total:      6   (0.00%)
    RAM/FIFO                  Used:      0  Total:     24   (0.00%)

Global Information:
    Type             | Used     | Total
    -----------------|----------|---------------
    Chip global      | 6        | 6  (100.00%)
    Quadrant global  | 0        | 12 (0.00%)
```

Post-Compile Clock Reports
Clock Net Information Report

```
The following nets have been assigned to a global resource:
    Fanout  Type          Name
    --------------------------
    1780    CLK_NET       Net   : l_clk_c
                          Driver: l_clk_pad/U0/U1_CLKINT/U_GL
                          Source: AUTO PROMOTED
    878     CLK_NET       Net   : hclk_c
                          Driver: h_clk_pad/U0/U1_CLKINT/U_GL
                          Source: PDC PROMOTED
    294     INT_NET       Net   : h_rst_l_c
                          Driver: h_rst_l_pad/U0/U1_CLKINT/U_GL
                          Source: NETLIST

The following nets have been assigned to a quadrant clock resource using
PDC:
    Fanout  Type          Name
    --------------------------
    24      INT_NET       Net   : l_frame_l_in
                          Driver: l_frame_l_pad/U0/U1_CLKINT/U_GL
                          Region: quadrant_UL

The following nets have been assigned to a local clock resource using PDC:
    Fanout  Type          Name
    --------------------------
    35      INT_NET       Net   : h_frame_l_in
                          Driver: h_frame_l_pad/U0/U1/U1
                          Region: chip_T1
```

Post-Compile Clock Reports
High-Fanout-Net Information Report

```
High fanout nets in the post compile netlist:
    Fanout  Type          Name
    --------------------------
    22      INT_NET       Net   : h_irdy_l_in
                          Driver: h_irdy_l_pad/U0/U1/U1
    16      INT_NET       Net   : dw_bfifo_addra[3]
                          Driver: dbrg/bfifoctl/bfifo_addra[3]
    16      INT_NET       Net   : bs_h_ad_oe_0[0]
                          Driver: bs_h_ad_oe_0[3]
    16      INT_NET       Net   : bs_l_ad_oe_0[0]
                          Driver: bs_l_ad_oe_0[0]
    16      INT_NET       Net   : N_1630
                          Driver: G_1622
    …

Nets that are candidates for clock assignment and the resulting fanout:
    Fanout  Type          Name
    --------------------------
    500     CLOCK_NET     Net   : h_irdy_l_in
                          Driver: h_irdy_l_pad/U0/U1/U1
    16      INT_NET       Net   : dw_bfifo_addra[3]
                          Driver: dbrg/bfifoctl/bfifo_addra[3]
    16      INT_NET       Net   : bs_h_ad_oe_0[0]
                          Driver: bs_h_ad_oe_0[3]
    …
```

I/O Management

Defining I/O Standards

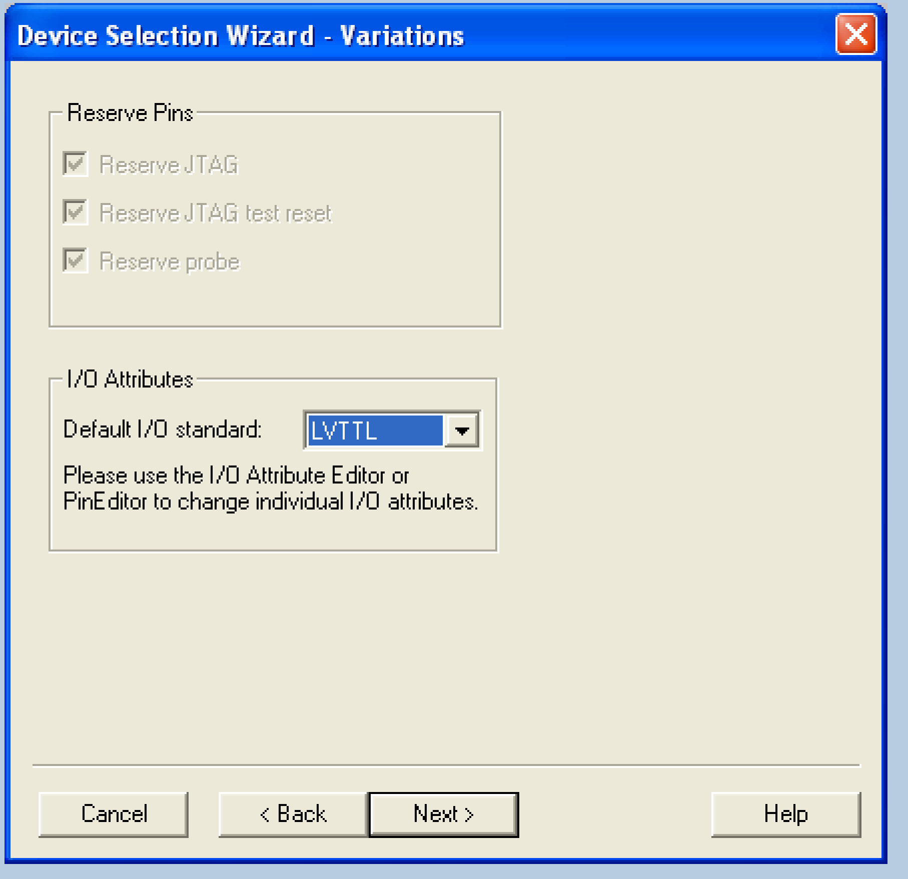
Synthesis

- **Using Generic Macros**
  - **May Instantiate Generic INBUF, OUTBUF, TRIBUF and BIBUF Macros**
  - **Synthesis May Automatically Infer Generic I/O Macros**
  - **LVTTL Is Default I/O Technology for these Macros**
    - ***Users Can Change Default Standard in Designer Software***
- ***May* Instantiate Specialized I/O Macros**
  - **I/O Technology Defined in Macro Name (See Data Sheet)**
    - ***Examples – INBUF_LVCMO25, OUTBUF_GTL25 …***
- **MUST Instantiate Differential I/O Macros (LVDS/LVPECL)**

Defining I/O Standards

■ Design Wizard

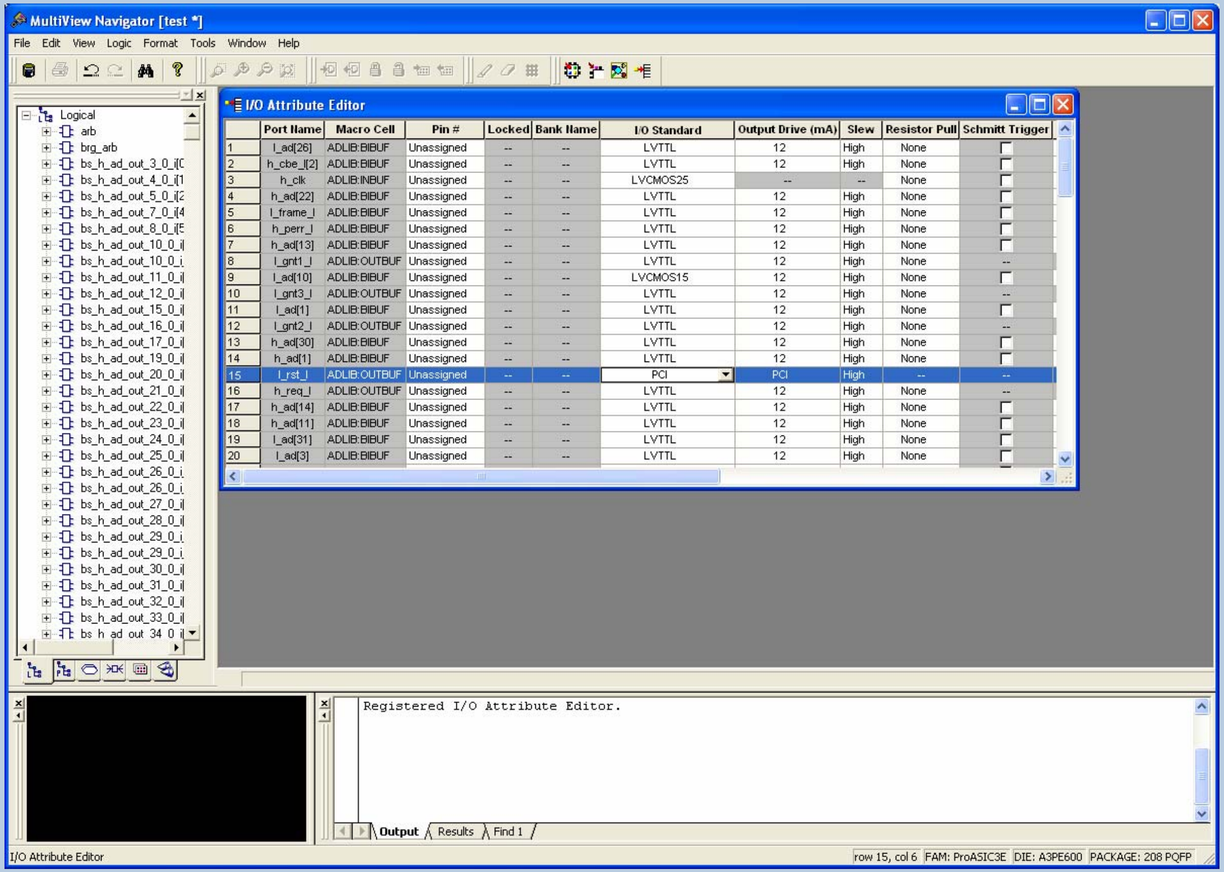
- **Set Single Default I/O Standard for *All* Generic I/O Macros**



Defining I/O Standards

■ I/O Attribute Editor

- **Change Default I/O Standard for *Each* Generic I/O Macro**



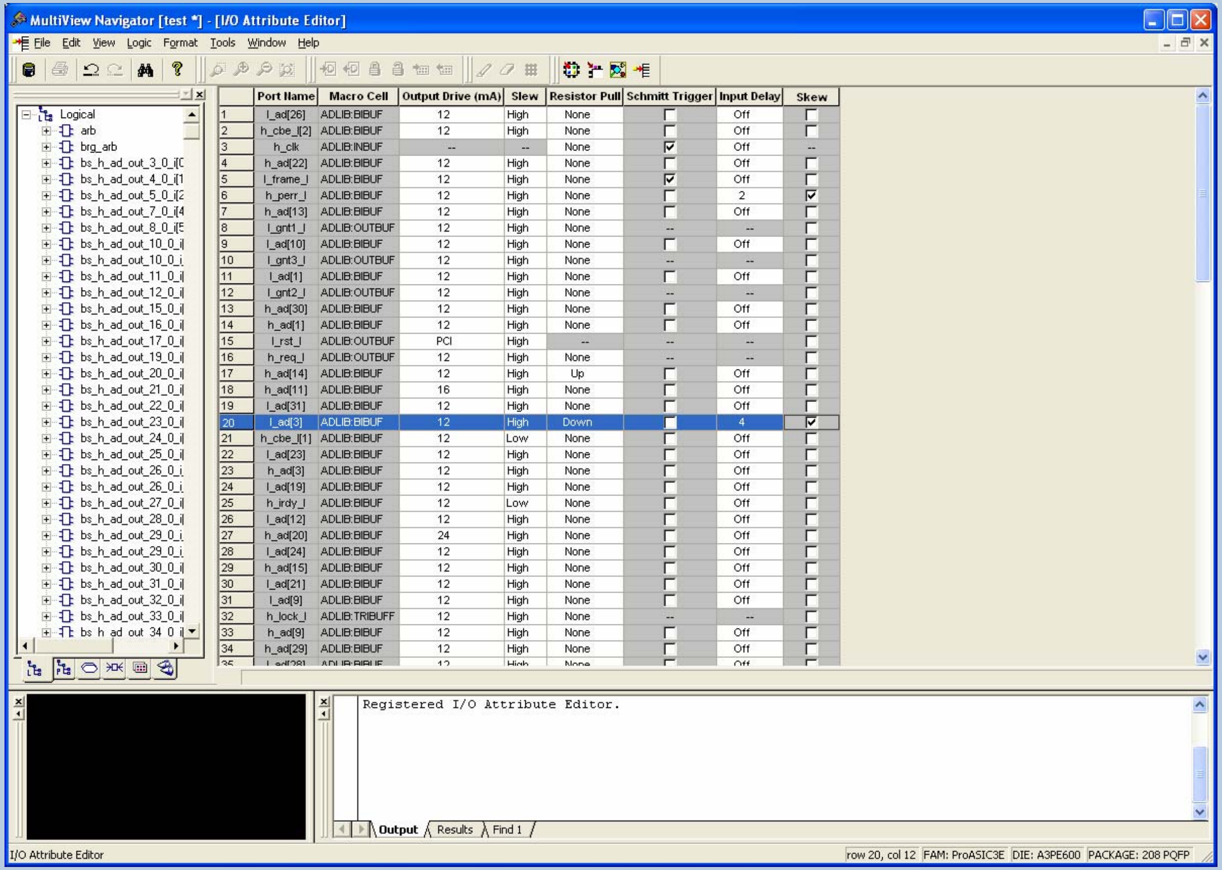
Defining Programmable I/O Attributes

- Synthesis
  - **User Can Instantiate Specialized I/O Macros**
    - **I/O Attribute Defined in Macro Name**
      - ***INBUF_…***

Defining Programmable I/O Attributes

I/O Attribute Editor

- **Users Can Change Default I/O Attributes for Each I/O Macro**



Enabling I/O Registers

DRC Requirements

- **MUST Meet Architectural Restriction**
  - **Fanout Between I/O and Register MUST Be 1**
  - **NOTE: Compile Does Not Give Error if This Restriction Is Not Met**
    - ***Instead, Register Function Is Implemented Using FPGA Core Tiles***

Using Global Compile Option

- **I/O Register Combining “Off” by Default**
- **Tcl Mode**
  - **Use “`–combine_register {1,0}`” to Enable/Disable Combining**
- **Interactive Mode**
  - **Use Compile Dialog Box Option**

Creating DDR I/O Function

Synthesis

- **Instantiate DDR_REG or DDR_OUT Macro**

DRC Requirements

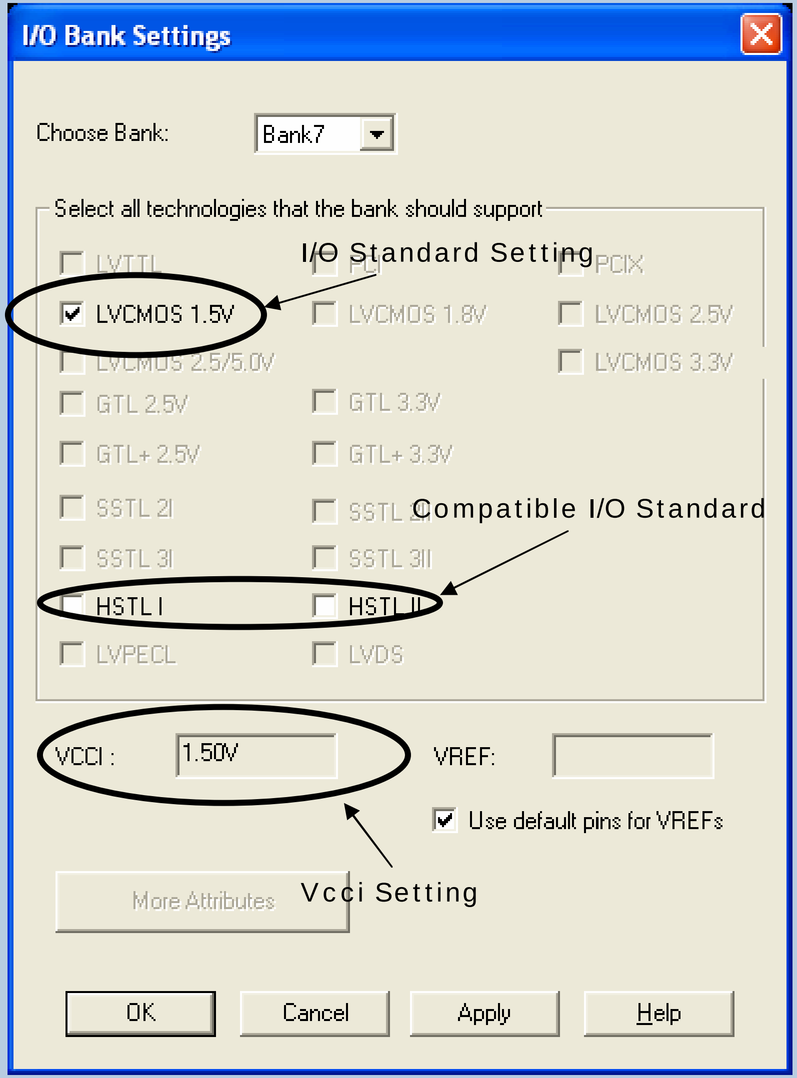
- **MUST Meet Architectural Restrictions**
  - **Fanout Between I/O and DDR Macro MUST Be 1**
  - **For Bidirectional Macro, Input DDR and Output DDR Must Share Common CLR Signal**
- **Compile DOES Give Error if These Restrictions Are Not Met**
  - **No Built-in DDR Functions in FPGA Array**
  - **Users Should Build DDR Functions from FPGA Gates if …**
    - ***… They Cannot Meet Architectural Restrictions***
    - ***… They Don't Want Built-in Logic for DDR Function***

Defining I/O Standard Bank Assignment
Rationale

- No Automatic Place & Route Flow for Mixed-I/O-Voltage Design
- Users MUST Provide Bank Assignment before Running Layout
  - **All Banks Require Vcci Voltage(s)**
    - **Each Compatible I/O Class (i.e., Same Vcci Requirement), Needs Enough I/O Pads Supplied by Bank Vcci**
  - **Voltage-Referenced I/Os REQUIRE Vref Assignment(s)**
    - **At Least ONE Vref for Each I/O Technology Bank**
    - **Vref Supplies Created by Setting User I/O as Vref Pin**
    - **Each Compatible Voltage-Referenced I/O Class (i.e., Same Vcci/Vref Requirement), Needs Enough I/O Pads Supplied by Bank Vcci and Vref Voltage Supply**

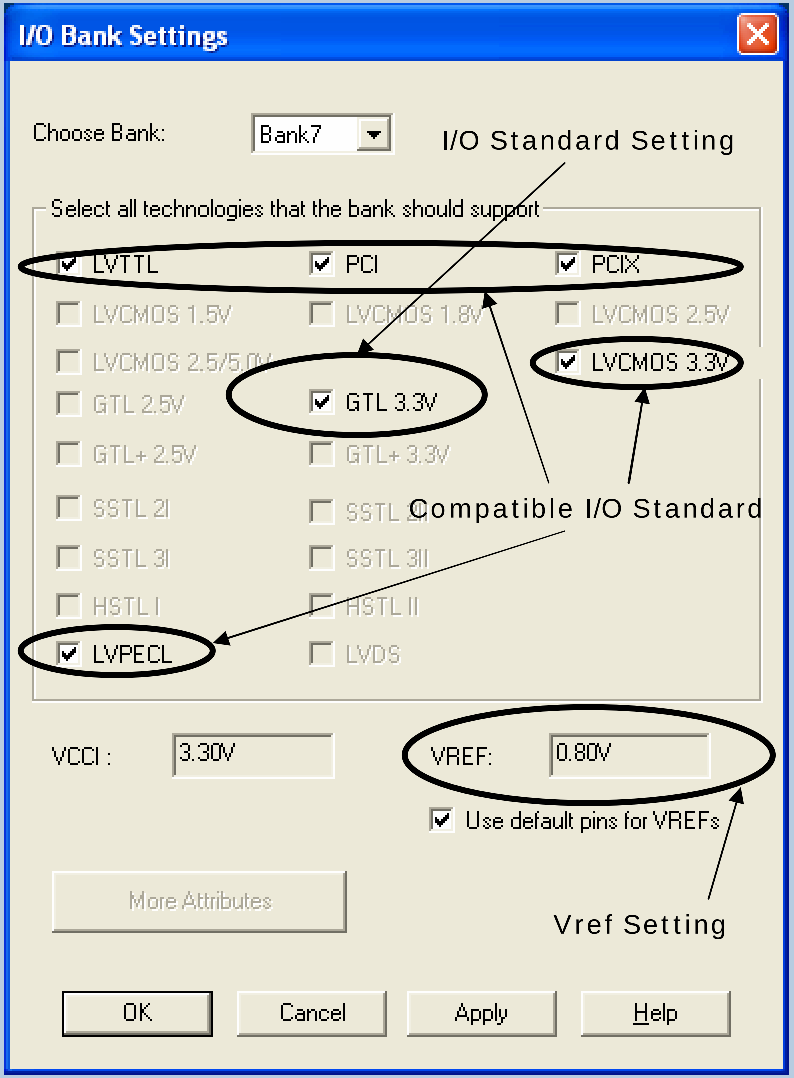
I/O Bank Settings
Assigning Vcci Voltage

- PinEdit or ChipEdit
  - **Use Bank Attribute Dialog Box**
- Physical Design Constraint (PDC)
  - **Import PDC Constraint in Pre- or Post-compile State**
    - **`set_iobank –vcci` *`vcci`***



I/O Bank Settings
Assigning Vref Voltage

- PinEdit or ChipEdit
  - **Use Bank Attribute Dialog Box**
- Physical Design Constraint (PDC)
  - **Import a PDC Constraint in Pre- or Post-compile State**
    - **`set_iobank –vref` *`vref`***



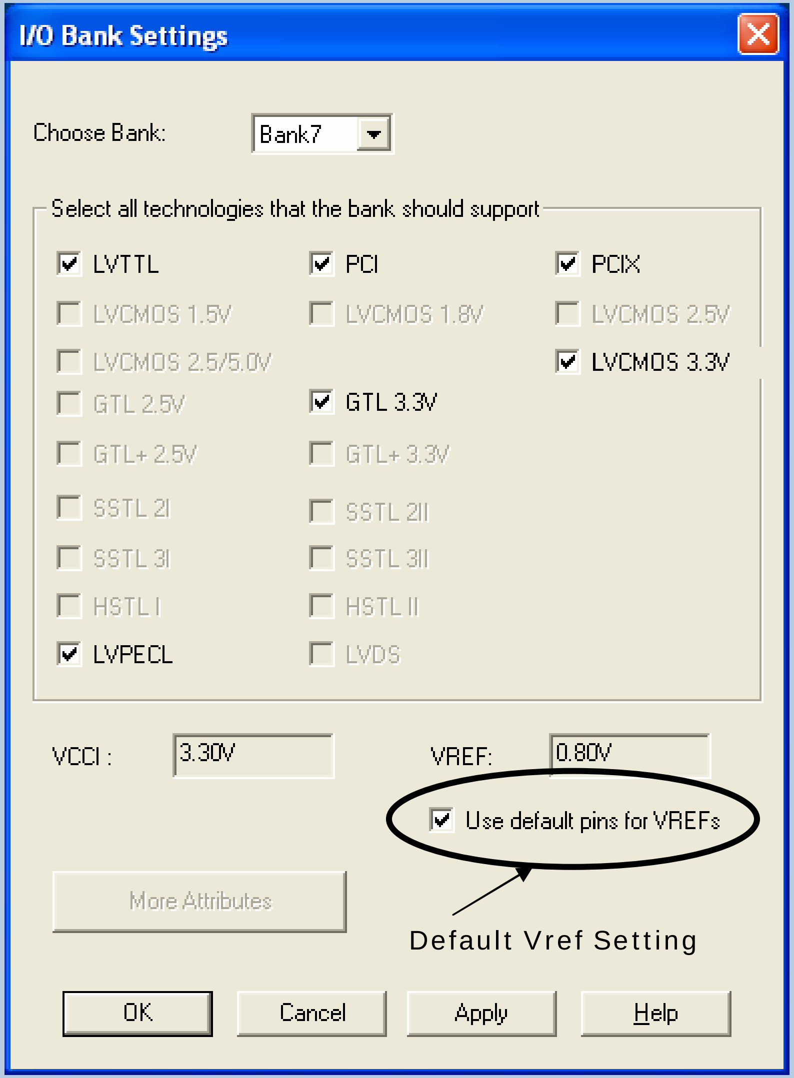
I/O Bank Settings
Assigning Default Vref Voltage Pins

PinEdit or ChipEdit

- **Use Bank Attribute Dialog Box**
  - **Default Setting**
  - **This Option Guarantees Full Vref Coverage of Bank**
  - **All Bonded I/O Pads in Bank Assigned Compatible Voltage-Referenced User I/O Macro**
  - ***May* Add Unnecessary Vref Pins**
    - ***Loss of Usable User I/Os***
    - ***See "Custom Vref Setting"***

Physical Design Constraint (PDC)

- **Import PDC Constraint in Pre- or Post-compile State**
  - ***set_vref_defaults* bank**



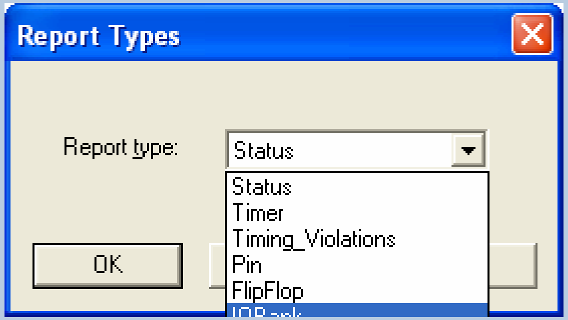
I/O Bank Settings
Custom Vref Setting

- Choose User I/O Pads as Vref Pins
- Must Create Enough Vref Pins to Allow Legal Placement of Voltage-referenced I/O Macros
  - **PinEdit or ChipEdit**
    - **Setting Vref Pin**
      - ***Select Package Pin or I/O Pad***
      - ***Right-click***
      - ***Select "Use Pin For VREF" Menu Option***
    - **Showing Vref Coverage of Given Vref Pin**
      - ***Select Vref Package Pin or Vref I/O Pad***
      - ***Right-click***
      - ***Select "Show VREF Range" Menu Option***
    - **Showing Complete Vref Coverage in Given Bank**
      - ***Select Bank which Is Already Assigned Vref Voltage***
      - ***Right-click***
      - ***Select "Show all Pins in a VREF Range" Menu Option***
  - **Using Physical Design Constraint (PDC)**
    - **Import PDC Constraint in Pre- or Post-compile State**
      - `set_vref [pkgpin]+`

Validating I/O Bank Assignments
I/O Bank Report

May Be Run …

- … from Menu – "Tools->Report…"
- … from Compile Report
  - Automatically Generated during Compile Command
- … from MVN
  - DRC Command Runs Pre-layout Checker
    - *If Infeasible I/O Bank Assignment Is Detected, then /O Bank Report Is Generated*
      - *Violations Highlighted in Report*
  - Commit Command Automatically Runs DRC Command



I/O Bank Report
Function

I/O Function:

Type	w/o register	w/ register	w/ DDR register
Input I/O	30	0	0
Output I/O	32	0	0
Bidirectional I/O	0	0	0
Differential Input I/O	2	0	0
Differential output I/O	0	0	0

I/O Bank Report
Technology

I/O Technology:

I/O Standard(s)	Voltages: Vcci	Voltages: Vccr	I/Os: Input	I/Os: Output	I/Os: Bidirectional
LVTTL	3.30v	N/A	0	32	0
LVCMOS25	2.50v	N/A	3	0	0
LVCMOS25_50	2.50v	N/A	3	0	0
LVCMOS18	1.80v	N/A	3	0	0
LVCMOS15	1.50v	N/A	3	0	0
PCI	3.30v	N/A	2	0	0
PCIX	3.30v	N/A	2	0	0
LVDS	2.50v	N/A	2	0	0
LVPECL	3.30v	N/A	2	0	0
HSTLI (Input/Bidirectional)	1.50v	0.75v	1	0	0
HSTLII (Input/Bidirectional)	1.50v	0.75v	1	0	0
SSTL3I (Input/Bidirectional)	3.30v	1.50v	2	0	0
SSTL3II (Input/Bidirectional)	3.30v	1.50v	2	0	0
SSTL2I (Input/Bidirectional)	2.50v	1.25v	2	0	0
SSTL2II (Input/Bidirectional)	2.50v	1.25v	2	0	0
GTL25 (Input/Bidirectional)	2.50v	0.80v	1	0	0
GTL33 (Input/Bidirectional)	3.30v	0.80v	1	0	0
GTLP25 (Input/Bidirectional)	2.50v	1.00v	1	0	0
GTLP33 (Input/Bidirectional)	3.30v	1.00v	1	0	0

I/O Bank Report
Bank Resource Usage

I/O Bank Resource Usage:

	Voltages		Single I/Os		Diff. I/Os		Vref I/Os		
	Vcci	Vccr	Used	Total	Used	Total	Used	Total	Vref Pins
Bank0	N/A	N/A	0	25	0	12	N/A	N/A	N/A
Bank1	N/A	N/A	0	15	0	7	N/A	N/A	N/A
Bank2	N/A	N/A	0	17	0	6	N/A	N/A	N/A
Bank3	N/A	N/A	0	16	0	7	N/A	N/A	N/A
Bank4	N/A	N/A	0	15	0	7	N/A	N/A	N/A
Bank5	N/A	N/A	0	22	0	10	N/A	N/A	N/A
Bank6	N/A	N/A	0	19	0	9	N/A	N/A	N/A
Bank7	N/A	N/A	0	18	0	7	N/A	N/A	N/A

Warning: I/OPRL1: 8 I/O Bank(s) have not been assigned any voltages.

The I/O modules located in these banks cannot be assigned any I/O macro.

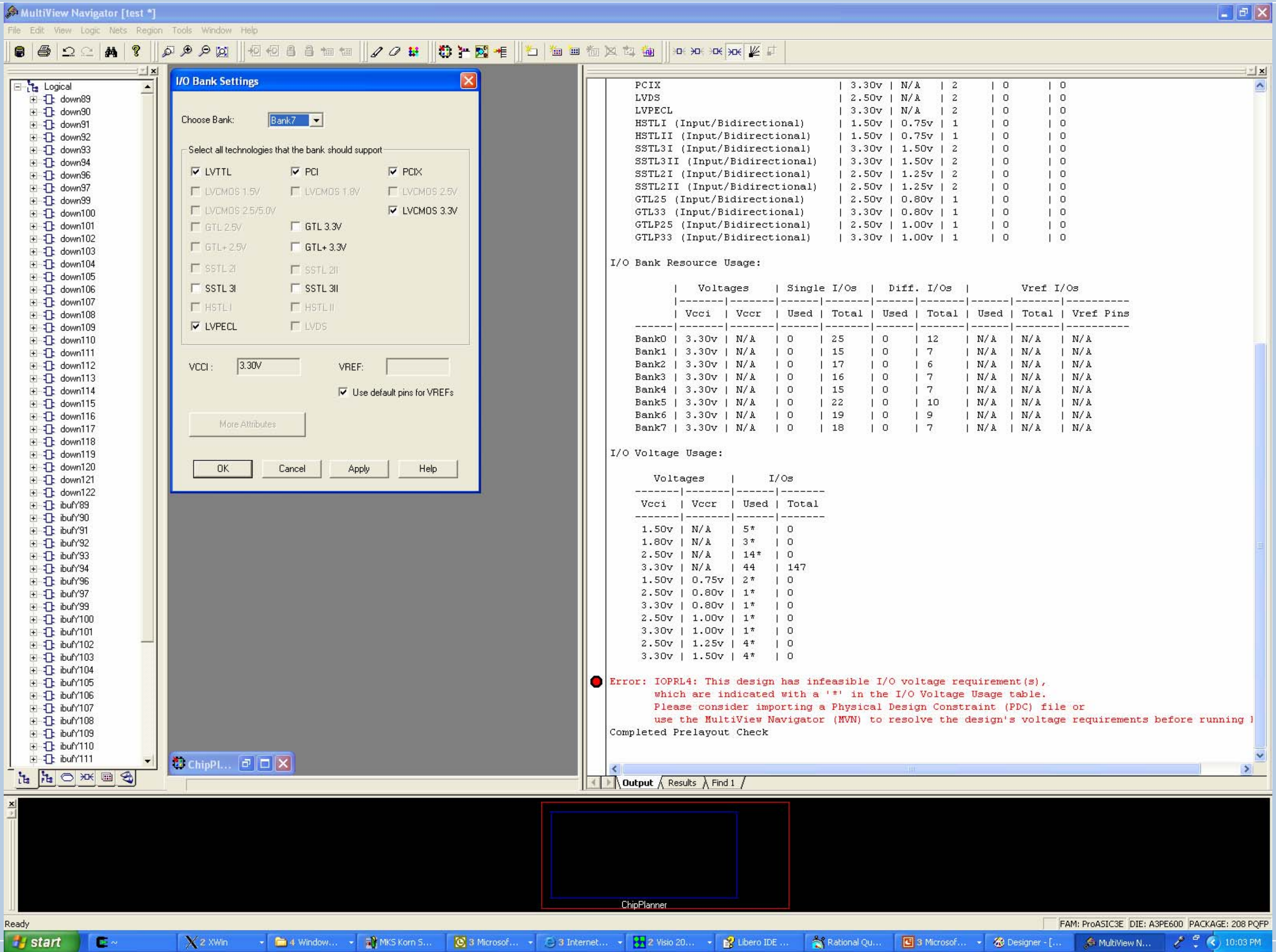
I/O Bank Report
Voltage Usage

```
I/O Voltage Usage:

       Voltages     |     I/Os
    -------|-------|------|-------
     Vcci  | Vccr  | Used | Total
    -------|-------|------|-------
     1.50v | N/A   | 5*   | 0
     1.80v | N/A   | 3*   | 0
     2.50v | N/A   | 14*  | 0
     3.30v | N/A   | 44*  | 0
     1.50v | 0.75v | 2*   | 0
     2.50v | 0.80v | 1*   | 0
     3.30v | 0.80v | 1*   | 0
     2.50v | 1.00v | 1*   | 0
     3.30v | 1.00v | 1*   | 0
     2.50v | 1.25v | 4*   | 0
     3.30v | 1.50v | 4*   | 0
```

Warning: I/OPRL3: This design has infeasible I/O voltage requirement(s) which are indicated with a '*' in the I/O Voltage Usage table.

Please consider importing a Physical Design Constraint (PDC) file or use the MultiView Navigator (MVN) to resolve thee design's voltage requirements before running layout.

Setting I/O Banks



Successful I/O Bank Assignment

test - Iobank Report

File Help

I/O Bank Resource Usage:

	Voltages		Single I/Os		Diff. I/Os		Vref I/Os		
	Vcci	Vccr	Used	Total	Used	Total	Used	Total	Vref Pins
Bank0	1.50v	0.75v	0	22	0	10	0	22	3
Bank1	1.80v	N/A	0	15	0	7	N/A	N/A	N/A
Bank2	2.50v	1.25v	0	15	0	4	0	15	2
Bank3	3.30v	1.00v	0	14	0	5	0	14	2
Bank4	2.50v	0.80v	0	13	0	5	0	13	2
Bank5	2.50v	1.00v	0	19	0	7	0	19	3
Bank6	3.30v	0.80v	0	17	0	8	0	17	2
Bank7	3.30v	1.50v	0	16	0	5	0	16	2

Final Bank Assignment

I/O Voltage Usage:

Voltages		I/Os	
Vcci	Vccr	Used	Total
1.50v	N/A	5	22
1.80v	N/A	3	15
2.50v	N/A	14	47
3.30v	N/A	44	47
1.50v	0.75v	2	22
2.50v	0.80v	1	13
3.30v	0.80v	1	17
2.50v	1.00v	1	19
3.30v	1.00v	1	14
2.50v	1.25v	4	15
3.30v	1.50v	4	16

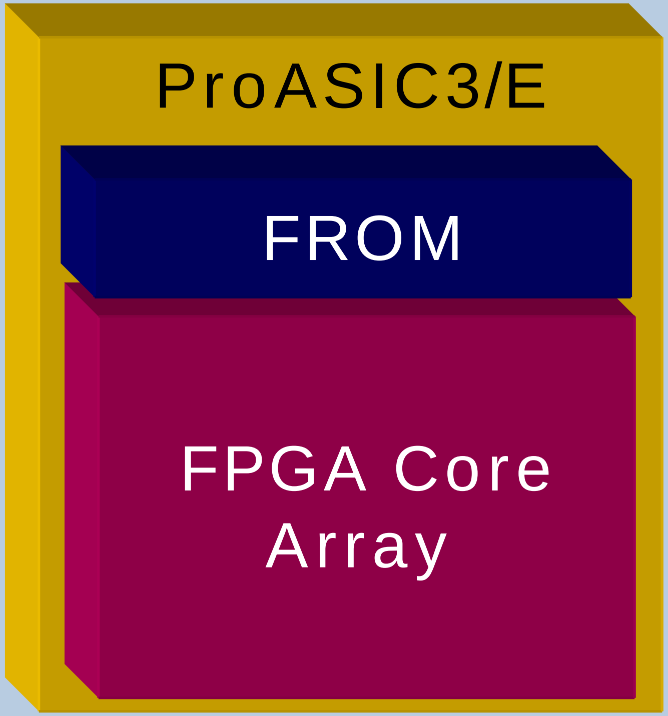
No Violation Reported

Programming and Hardware Tools

Actel

Simplified ISP

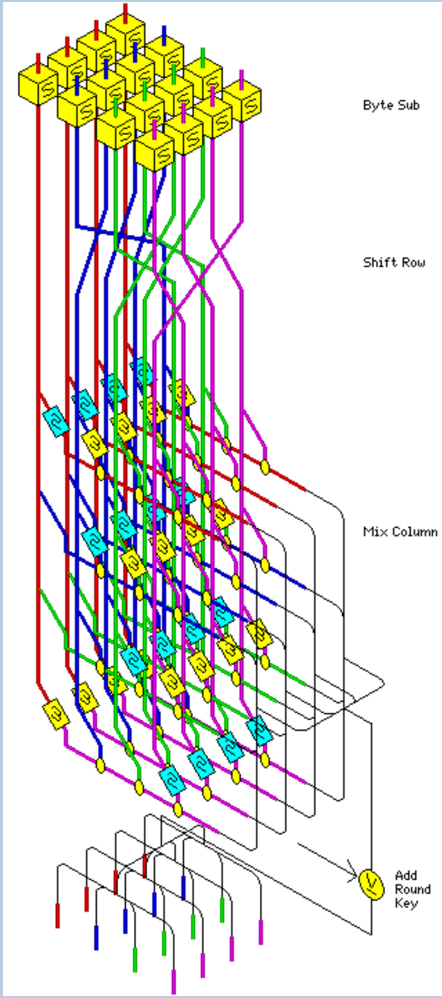
- **Single-pin Programming Supply Voltage Vpump = 3.3V (Nominal)**
  - **All Other Programming Voltages Generated On-chip**



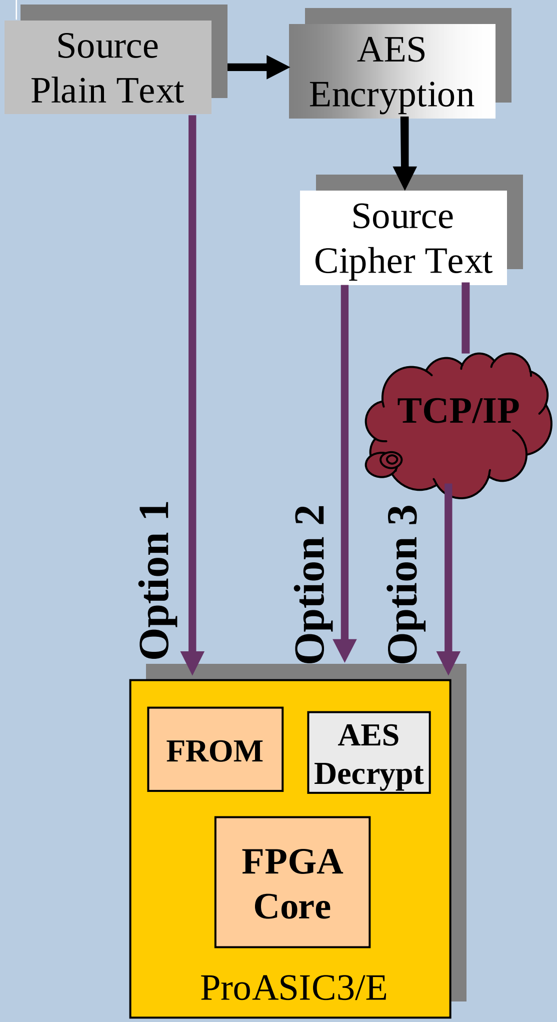
- **Programming via JTAG Port**
- **Separate V_{JTAG} Power Supply**
  - **1.4V to 3.6V**
- **Program and Erase Times**
  - **Estimated at <2min for Largest Parts and <30s for Smaller Parts**
- **Same Programming for both ProASIC3/E**

World's Best ISP

- Industry-standard IEEE1532 (JTAG) Programming
  - **Optional User Flash Programming via JTAG**
- Built-in Secure ISP
  - **ISP Supports Bitstreams Encrypted with 128-bit AES (FIPS-192) Block Cipher**
    - **NIST-approved to Replace DES and 3DES**
    - **3.4 x 10^{38} Possible 128-bit keys**
    - **Over 1000 Trillion Years to Crack 128-bit AES Key**
  - **AES Key Securely Stored during Programming in ProASIC3/E On-chip Flash and Cannot be Read Back**
  - **AES Core in ProASIC3/E Decrypts and Authenticates (MAC) Bitstream File prior to Programming**
  - **Allows Secure (and Authenticated) Remote Field Updates**



ProASIC3/E
Programming Options



- Secure ISP Using AES Programming
  - ✓ **OPTION 1 – Program ProASIC3/E Devices In-house with Plain Text**
  - ✓ **OPTION 2 – Program ProASIC3/E Devices In-house with AES Key Only – Final Programming Can Be at Un-trusted site (Contract Manufacturer) Using AES-encrypted Programming File**
  - ✓ **OPTION 3 – Re-program ProASIC3/E Devices Remotely Using AES-encrypted Programming File for Easy and Secure Field Upgrades**

- Built-in ProASIC3/E FlashROM Can Be Updated Independently Using AES-encrypted Programming File or Plain Text

PA3 ISP Programming HW

FlashPro3 Hardware

- **Small A3P/E-only Programmer with USB 2.0 High-speed Interface**
  - **10-pin JTAG ISP**
  - **Altera-compatible Interface**
- **Programs Devices in Less than 2 Minutes**
- **Powered by USB Connection**
  - **Parallel Programming Requires Powered USB Hub**
- **Variable TCK (up to 24 MHz)**
  - **Recommend <= 20MHz for PA3/E**
- **Optional Transition Board provides Adapter Cables for 26- and 10-pin SAMTEC**

PA3 ISP Programming SW

FlashPro v3.3 Software

- **Works with All FlashPro-series Programmers**
  - **FlashPro3, FlashPro Lite and FlashPro**
- **Supports A500K, APA and PA3/E with Appropriate Programmer**

ChainBuilder v1.1 Software

- **New Software for PA3/E Support in Addition to APA**

PA3 Programming Cycle Counter

Independent Count Maintained

- Read from PA3 Device
- Tracks Number of Times Device Has Been Programmed
- Reported in FlashPro Programming Log File

Use model

- No Display of Programming Cycle Count in GUI
- Stored Only in Log File
- Suggest Replacing Device at Certain Level

ISP Flows with FlashPro

ISP Modes

- **Sequential Programming**
  - **Program Multiple Devices in a Single JTAG Chain One at a Time**
- **Concurrent Programming**
  - **Simultaneously Program Multiple Devices in Single JTAG Chain**
  - **This Mode Not Possible with FlashPro v3.3 SW**
- **Parallel Programming**
  - **Simultaneously Program Multiple JTAG Chains with Multiple FlashPro3s**

Software

- **Designer (for the FPGA Array MAP File)**
- **ACTgen III (for FROM Configuration File)**
- **FlashPoint (STAPL Programming File Generator)**
- **FlashPro v3.3 Programming Software**

Programming flows for A3P/A3PE

Without FlashROM

Flashpoint

Select security settings

Generate programming file(s)

Sculptor/ FlashPro

Program Device
Single or Multiple programming files

With FlashROM

Actgen

Generate FROM

Define data regions

Setup serialization options

Flashpoint

Select security settings

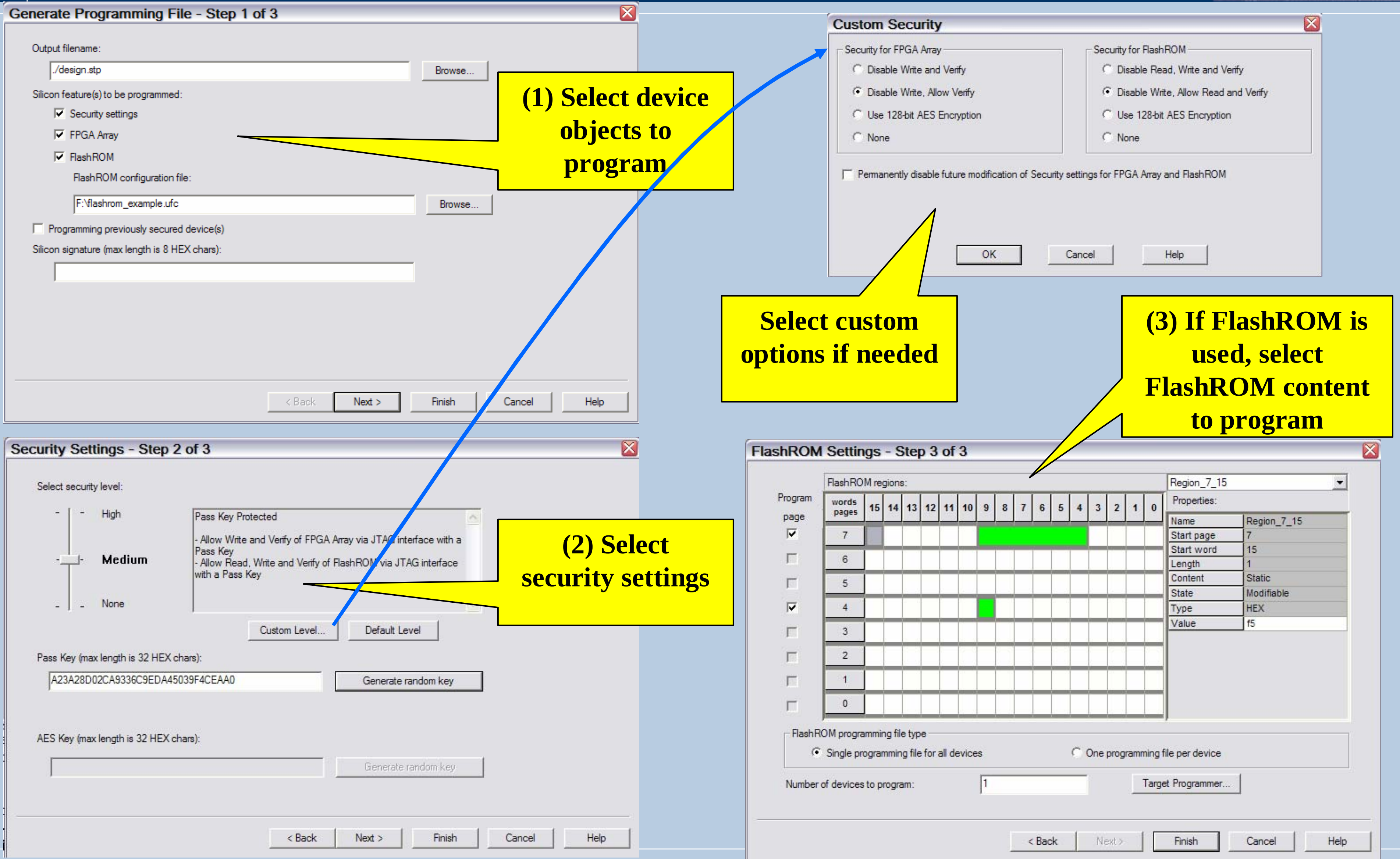
Select FlashROM data

Generate programming file(s)

Sculptor/ FlashPro

Program Device
Single or Multiple programming files

Using FlashPoint



Programming

File Sizes and Estimated Programming Times

		A3P 030	A3P 060	A3P 125	A3P 250	A3P 400	A3P 600	A3P 1000	A3PE 600	A3PE 1500	A3PE 3000
File Size MB	Plain	0.03	0.06	0.12	0.23	0.34	0.51	0.89	0.51	1.42	2.78
	AES	0.04	0.08	0.15	0.28	0.42	0.63	1.10	0.63	1.75	3.43
Programming Time (Plain Text) - FP3		<30Sec	<30Sec	<30Sec	<45Sec	<45Sec	<1min	<1min	<1min	<1.5min	<2min

ProASIC3 Starter Kit
Contents

- A3PE-EVAL-KIT – Main Part Number
  A3PE-PROTO-KIT – Pre-production with Socketed Board
- FlashPro3 Hardware
- FlashPro Software
- Evaluation Board with A3PE600-PQ208 Device
  - **A3PE-EVAL-BRD600-SA – No socket**
  - **A3PE-EVAL-BRD600-SKT – Socketed (Prototypes and Pre-production)**
- Universal Power Brick
  - **Same as in Existing APA and AX Starter Kits; 9V at 2A**
- Libero Software

PA3 Starter Kit
Board Description

Feature List

- **A3PE600-PQ208**
- **8-digit LCD Dot-matrix Display (Large 13.8mm Characters)**
- **13 LEDs**
  - **5 Power (1.5V, 1.8V, 2.5V, 3.3V, 5V (for LCD))**
  - **8 Status**
- **8 Switches**
  - **5 Push**
  - **2 Rotary**
  - **1 Reset**
- **2 Oscillators (One Unpopulated)**
- **Various Jumpers for I/O Bank Voltage Selection**
  - **1.5V, 1.8V, 2.5V, 3.3V**
- **2 CAT5E RJ45 Connectors for LVDS**
  - **4 Transmit Pairs and 4 Receive Pairs (16 Signals)**
  - **2 Transmit and 2 Receive Pairs per RJ45**
    - ***Loopback-capable via CAT5E Patch Cable***
    - ***Primary and Secondary***

A3P/A3PE Adapter Modules

- **Required by Silicon Sculptor II Programmer**
  - **Note – No A3P/A3PE Programming Support with SS I!**
- **PA3/E – Use Existing APA Modules**
  - **Redesign Not Required for SMPA-PQ208, SMPA-FG484, and Other SMPA Modules**
  - **Use Existing APA Modules**
    - **Caveat: One New Module Required for A3P030 New Package**
  - **Benefit**
    - **No Additional Cost to Existing Customers**

Summary

CCC Backup

Clock Source Selection (cont.)

■ Hardwired Reference Clock Placement (MVN/PDC)

- **I/O in I/O-CCC Hard Macro Is Master Cell for Placement Purposes**
  - ➢ **Placement Target Should Be I/O Module**
- **Can Be More than One I/O Module Target for Same CCC Chip Location**