The Abdus Salam
International Centre for Theoretical Physics

United Nations
Educational, Scientific
and Cultural Organization

International Atomic
Energy Agency

**310/1780-9**

**ICTP-INFN Advanced Tranining Course on
FPGA and VHDL for Hardware Simulation and Synthesis
27 November - 22 December 2006**

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# *LIBERO IDE-7.2.2.*

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***2061 Stierlin Court***
***Mountain View, CA 94043-4655***
***U.S.A.***

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# Lectures: Libero™ Integrated Design Environment

# Agenda

- Libero Overview
- 3rd Party Tools
- Designer Overview
- Programming
- Silicon Explorer

# Libero IDE Overview

- Complete Toolset for Actel FPGA Development
  - Project Manager
  - ViewDraw Schematic Capture
  - Synplify Synthesis
  - Testbench Generation
  - Mentor ModelSim Simulation
  - PALACE Physical Synthesis (Libero Platinum)
  - Actel Designer Design Implementation
    - Compile, Place & Route
    - Timing and Physical Constraints
    - Timing Analysis
    - Power Analysis
    - Back Annotation
    - Programming File Generation
  - FlashPro Programming Software
  - Silicon Explorer Debug Software

# Libero Tool Suite

- Integrated Design Environment

## Design Implementation

Synplify

- Synthesis

ViewDraw AE

Viewdraw

- Schematic Capture

Actel

- SmartGen Macro builder

## Design Verification

SynaptiCAD

SYNAPTICAD
WaveFormer Lite

- Stimulus

ModelSim

- Simulation

Actel

BCE

- Silicon Explorer Debugger

## Physical Implementation

PALACE

MAGMA

- Physical Synthesis

Actel Designer

- Place & Route

FlashPro

Flash Pro

- Programming

ONE CHIP is all you need

# Libero Gold

## World Class Fully-Integrated PC Development System

- Targets All Devices up to 1M Gates
- Tools:
  - **ViewDraw AE 7.70**
  - **SynaptiCAD WaveFormer Lite 10.04a**
  - **ModelSim AE 6.1b**
  - **Synplify AE 8.5f (1M gates)**
  - **Actel Designer 7.2 (1M gates)**
  - **FlashPro 4.2**
  - **ChainBuilder 1.1**
  - **Silicon Explorer 5.1**
- PC Platform
  - **Licensed to Disk ID (Node-Locked license)**
- 1 Year Free License!
  - **No Updates (Service Packs Available)**

### Tool Features

| | |
|---|---|
| Integrated Design Management | ✓ |
| Schematic | ✓ |
| VHDL | ✓ |
| Verilog | ✓ |
| Macro Generation | ✓ |
| Testbench Generator | ✓ |
| VHDL Simulation<br>Verilog Simulation | ✓ |
| Timing Simulation | ✓ |
| Static Timing Analysis | ✓ |
| Timing Driven Place and Route | ✓ |
| Push Button Place and Route | ✓ |
| Layout Editor | ✓ |
| Silicon Explorer | ✓ |
| Standard Industry Interfaces | ✓ |
| Third Party Design Libraries | ✓ |

### Platform Support

| | |
|---|---|
| Win2000 SP4 | ✓ |
| WinXP Pro SP2 | ✓ |

ONECHIP is all you need

# Libero Platinum

## World Class Fully Integrated PC Development System

- Targets *All* Actel Devices
- Tools
  - ViewDraw AE 7.70
  - WFL 10.04a with Reactive Testbench Generation
  - ModelSim AE 6.1b
  - Synplify Pro AE 8.5f (*No* Gate Limit)
  - Magma Palace 3.3
  - Actel Designer 7.2 (*No* Gate Limit)
  - FlashPro 4.2
  - ChainBuilder 1.1
  - Silicon Explorer 5.1
- PC Platform
  - Node-Locked License Tied to Disk-id or Hardware Keys
- Price:
  - $2495 First Year / $1995 Renewal
  - Free 45 day Evaluation License

**Tool Features**

| | |
|---|---|
| Integrated Design Management | ✓ |
| Schematic | ✓ |
| VHDL | ✓ |
| Verilog | ✓ |
| Macro Generation | ✓ |
| Testbench Generator | ✓ |
| VHDL Simulation<br>Verilog Simulation | ✓ |
| Timing Simulation | ✓ |
| Static Timing Analysis | ✓ |
| Timing Driven Place and Route | ✓ |
| Push Button Place and Route | ✓ |
| Layout Editor | ✓ |
| Silicon Explorer | ✓ |
| Standard Industry Interfaces | ✓ |
| Third Party Design Libraries | ✓ |

**Platform Support**

| | |
|---|---|
| Win2000 SP4 | ✓ |
| WinXP Pro SP2 | ✓ |

ONECHIP is all you need

# Libero IDE
## *Solaris and Linux Support*

- Libero Solaris, Libero Linux
  - Tools
    - Project Manager
    - Synplify AE
    - ModelSim AE VHDL & Verilog
    - PALACE AE
    - SmartGen
    - Designer
  - Supports All Devices
  - Solaris, Linux OS
  - License Type: Floating
    - Solaris: Host ID only
    - Linux: requires USB key for Synplify
  - 1 Year License: $4995
    - Incremental seats: $3500
  - Free 45 day Evaluation License

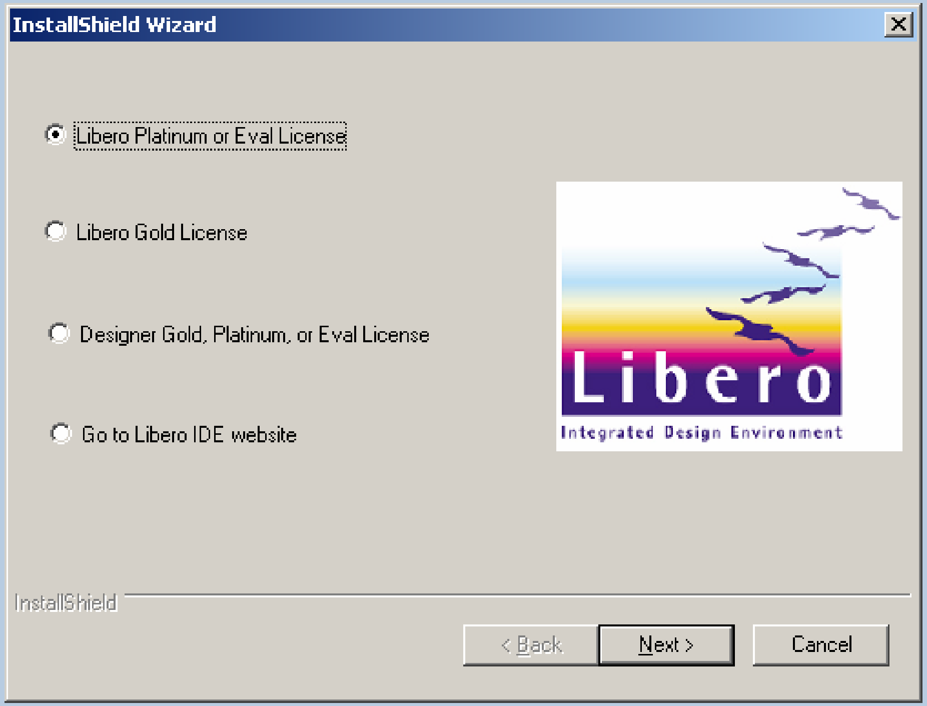
# Libero Edition Summary

| | Libero Gold | Libero Platinum (Windows) | Libero Platinum (Solaris / Linux) | Libero Platinum Eval |
|---|---|---|---|---|
| Device Support | All devices up to 1M Gates | All Devices | All Devices | All Devices |
| ViewDraw | AE | AE | - | AE |
| WaveFormer Lite | AE | Reactive Testbench | - | Reactive Testbench |
| Synthesis | Synplify AE | Synplify Pro AE | Synplify Pro AE | Synplify Pro AE |
| Magma Palace | - | Yes | Yes | Yes |
| ModelSim | AE | AE | AE | AE |
| Designer | Yes | Yes | Yes | Yes |
| FlashPro | Yes | Yes | - | No |
| Explorer | Yes | Yes | - | No |
| License Type | Disk ID | Key or Disk ID | Floating | Disk ID (Windows)<br>Floating (Solaris / Linux) |
| Price | Free | $2,495 | $4,995 | Free 45 day |

# Libero Installation

# Libero Installation
*Select Edition*

- Installation Wizard Makes Installation Easy!
- Select Appropriate Product from Libero Installation GUI
  - **Platinum or Evaluation**
  - **Gold**
- Request License when Installation Finishes



InstallShield Wizard

● Libero Platinum or Eval License

○ Libero Gold License

○ Designer Gold, Platinum, or Eval License

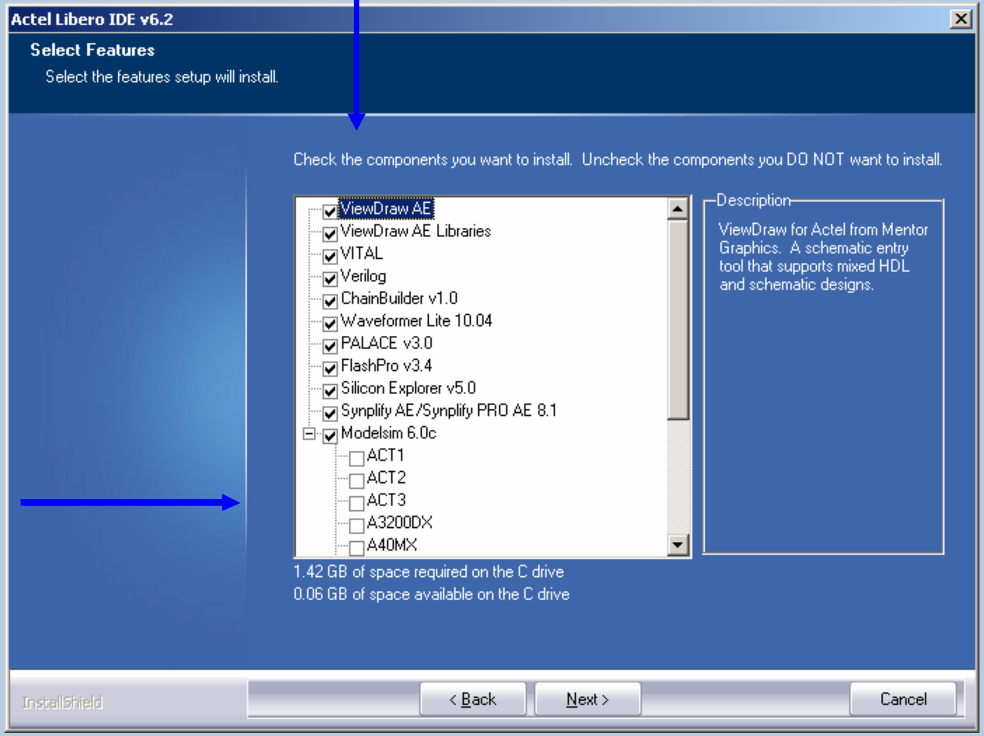
○ Go to Libero IDE website

# Libero Installation
*Component Selection*

- Select Design Components and Simulation Libraries to Install
  - **VHDL and Verilog Simulation Libraries Contained on CD**
    - **RECOMMENDATION: Only Install *Needed* Actel Family Libraries to Save Disk Space**
    - **Save Libero CD to Install Additional Actel Family Libraries for Future Designs**

Select components for installation

Select Actel simulation libraries



Actel Libero IDE v6.2

**Select Features**

Select the features setup will install.

Check the components you want to install. Uncheck the components you DO NOT want to install.

- ☑ ViewDraw AE
- ☑ ViewDraw AE Libraries
- ☑ VITAL
- ☑ Verilog
- ☑ ChainBuilder v1.0
- ☑ Waveformer Lite 10.04
- ☑ PALACE v3.0
- ☑ FlashPro v3.4
- ☑ Silicon Explorer v5.0
- ☑ Synplify AE/Synplify PRO AE 8.1
- ☑ Modelsim 6.0c
  - □ ACT1
  - □ ACT2
  - □ ACT3
  - □ A3200DX
  - □ A40MX

Description

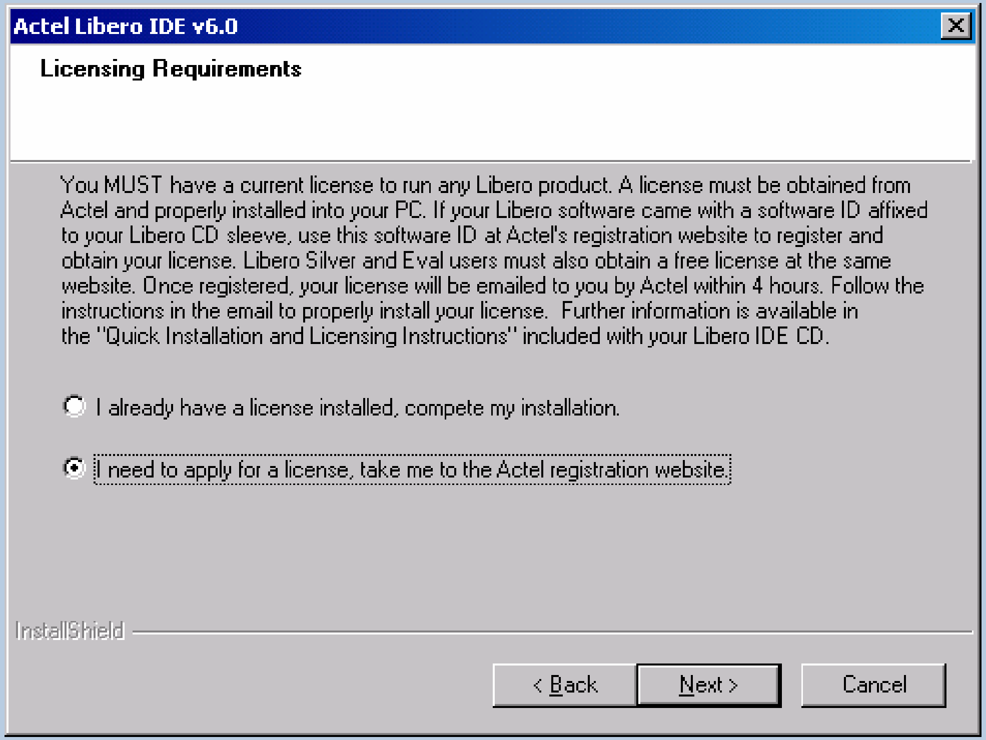
ViewDraw for Actel from Mentor Graphics. A schematic entry tool that supports mixed HDL and schematic designs.

1.42 GB of space required on the C drive

0.06 GB of space available on the C drive

# Final Installation Page

- Upon Installation Completion, User is Asked “Do you have a current license installed”?
  - If No (Default), Takes User Directly to Registration Web Site
    - Completing Registration or Clicking Off Browser Returns User to Final Install/Restart Page



Actel Libero IDE v6.0

Licensing Requirements

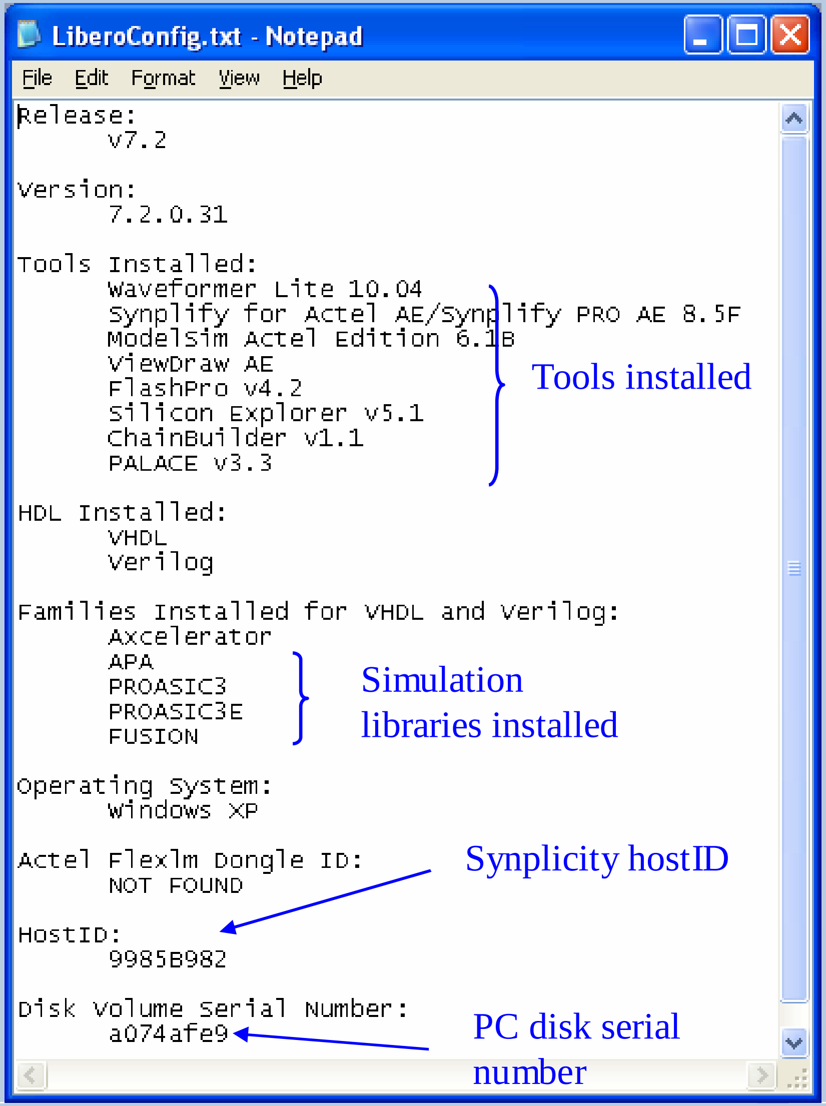
You MUST have a current license to run any Libero product. A license must be obtained from Actel and properly installed into your PC. If your Libero software came with a software ID affixed to your Libero CD sleeve, use this software ID at Actel's registration website to register and obtain your license. Libero Silver and Eval users must also obtain a free license at the same website. Once registered, your license will be emailed to you by Actel within 4 hours. Follow the instructions in the email to properly install your license. Further information is available in the "Quick Installation and Licensing Instructions" included with your Libero IDE CD.

○ I already have a license installed, compete my installation.

● I need to apply for a license, take me to the Actel registration website.

# Installation Summary

- Confirm Setup after Installation
  - **Start > Programs > Libero IDE v7.2 > About Your Installation**
- Includes Information Needed to Get License



```
Release:
       v7.2

Version:
       7.2.0.31

Tools Installed:
       Waveformer Lite 10.04
       Synplify for Actel AE/Synplify PRO AE 8.5F
       ModelSim Actel Edition 6.1B
       ViewDraw AE
       FlashPro v4.2
       Silicon Explorer v5.1
       ChainBuilder v1.1
       PALACE v3.3

HDL Installed:
       VHDL
       Verilog

Families Installed for VHDL and Verilog:
       Axcelerator
       APA
       PROASIC3
       PROASIC3E
       FUSION

Operating System:
       Windows XP

Actel Flexlm Dongle ID:
       NOT FOUND

HostID:
       9985B982

Disk Volume Serial Number:
       a074afe9
```

Tools installed

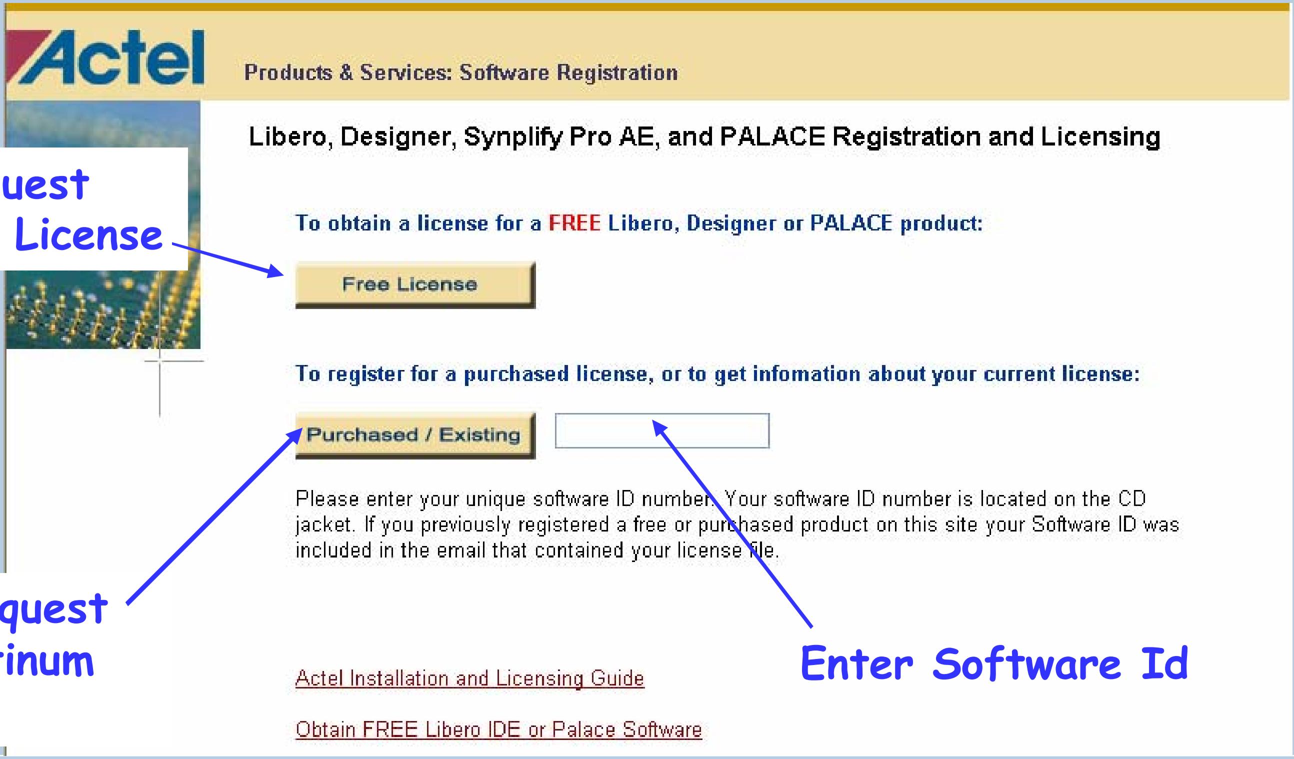
Simulation libraries installed

Synplicity hostID

PC disk serial number

# Obtaining a Libero License

- Request a Libero License via any of the Following Methods:
  - **http://www.actel.com/products/tools/sw.aspx**
- Libero License Sent via E-mail within 1 hour!
  - **Libero License Includes Synplicity License**



Products & Services: Software Registration

Libero, Designer, Synplify Pro AE, and PALACE Registration and Licensing

To obtain a license for a FREE Libero, Designer or PALACE product:

To register for a purchased license, or to get infomation about your current license:

Please enter your unique software ID number. Your software ID number is located on the CD jacket. If you previously registered a free or purchased product on this site your Software ID was included in the email that contained your license file.

Actel Installation and Licensing Guide

Obtain FREE Libero IDE or Palace Software

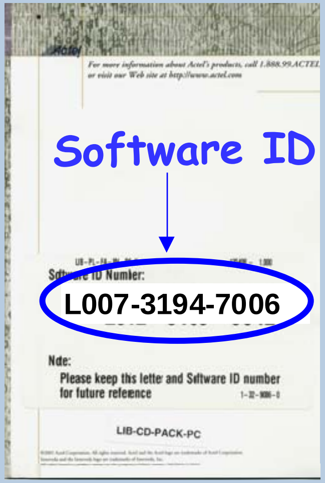
Click to request Libero Gold License

Click to request Libero Platinum License

Enter Software Id

# Libero Gold and Platinum Licenses

- Libero Gold License Is Node-Locked to PC Disk ID
- Libero Platinum License Requires Software ID
- Platinum License Types:
  - **Locked to Disk ID**
  - **Hardware Keys**
    - **One Key for Synplicity and One Key for All Remaining Software**
    - **Parallel Port or USB Options**



*For more information about Actel's products, call 1.888.99.ACTEL or visit our Web site at http://www.actel.com*

Software ID

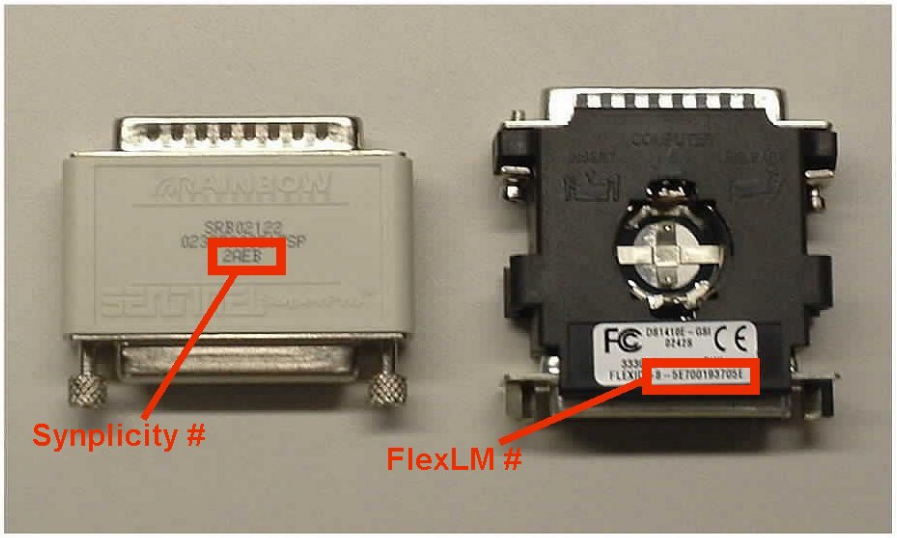
Software ID Number:

L007-3194-7006

Nde:

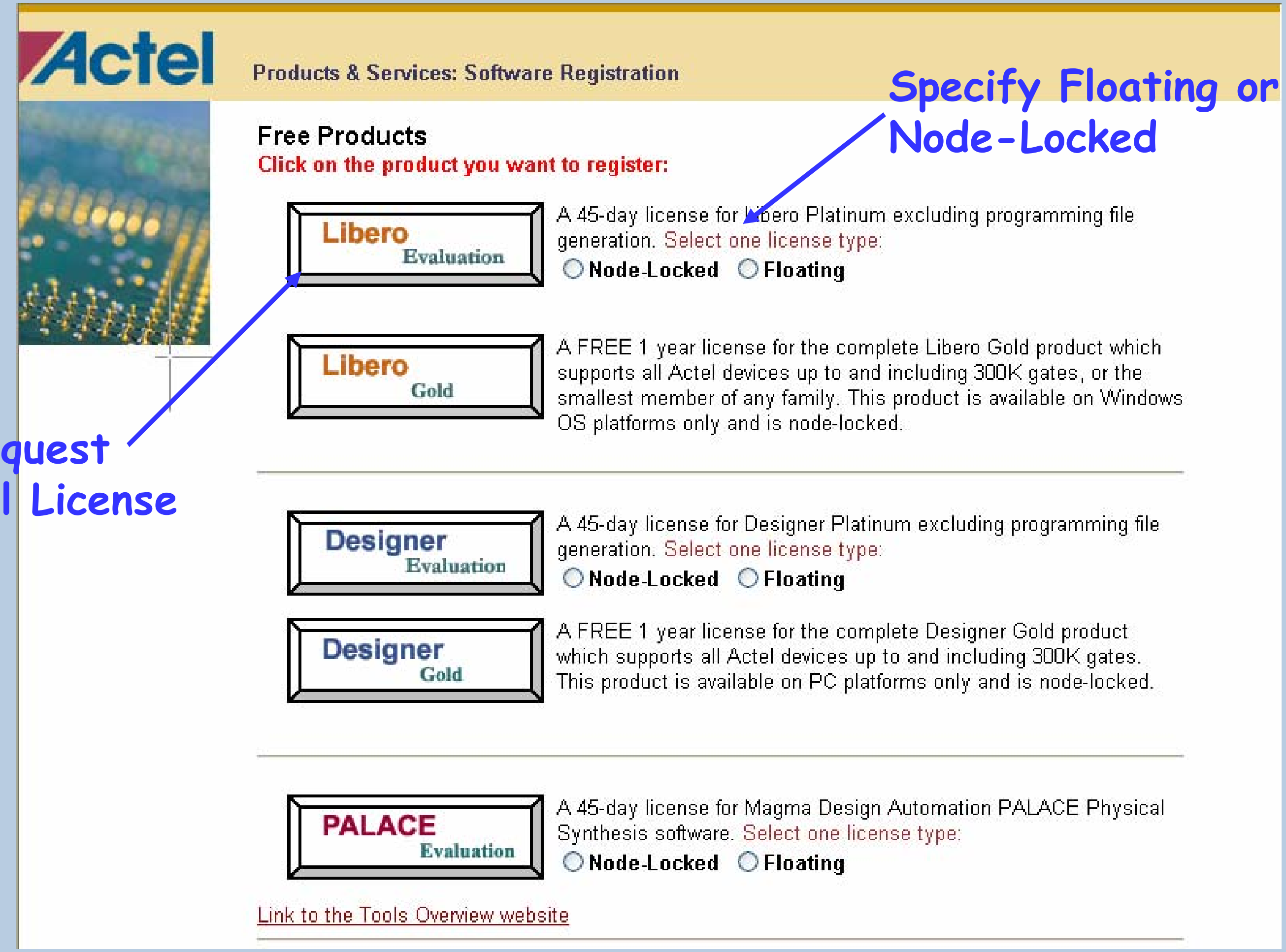
Please keep this lette and Sftware ID number for future refeence

LIB-CD-PACK-PC



# Libero Platinum Evaluation License

## Libero Platinum Evaluation License Contains All Platinum Features *Except* Programming



Products & Services: Software Registration

Free Products

Click on the product you want to register:

A 45-day license for Libero Platinum excluding programming file generation. Select one license type:

○ Node-Locked ○ Floating

A FREE 1 year license for the complete Libero Gold product which supports all Actel devices up to and including 300K gates, or the smallest member of any family. This product is available on Windows OS platforms only and is node-locked.

A 45-day license for Designer Platinum excluding programming file generation. Select one license type:

○ Node-Locked ○ Floating

A FREE 1 year license for the complete Designer Gold product which supports all Actel devices up to and including 300K gates. This product is available on PC platforms only and is node-locked.

A 45-day license for Magma Design Automation PALACE Physical Synthesis software. Select one license type:

○ Node-Locked ○ Floating

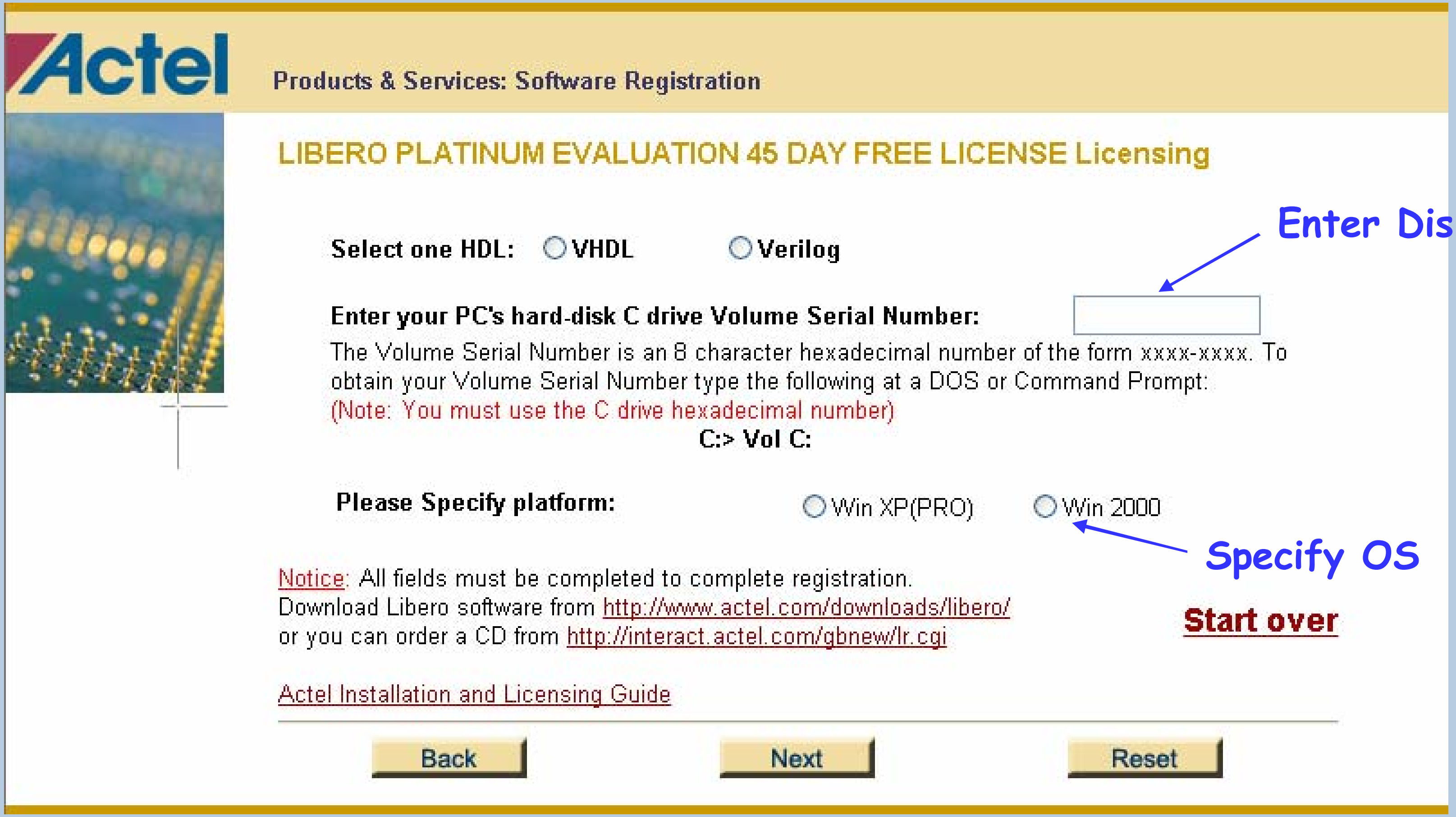
Link to the Tools Overview website

Specify Floating or Node-Locked

Click to request Libero Eval License

# Libero Platinum Evaluation License (cont.)

- Evaluation License Is Node-Locked to Disk ID
  - **Available from "About Your Installation"**



Products & Services: Software Registration

LIBERO PLATINUM EVALUATION 45 DAY FREE LICENSE Licensing

**Select one HDL:** ○ VHDL ○ Verilog

**Enter your PC's hard-disk C drive Volume Serial Number:**

The Volume Serial Number is an 8 character hexadecimal number of the form xxxx-xxxx. To obtain your Volume Serial Number type the following at a DOS or Command Prompt:
(Note: You must use the C drive hexadecimal number)

C:> Vol C:

**Please Specify platform:** ○ Win XP(PRO) ○ Win 2000

Notice: All fields must be completed to complete registration.
Download Libero software from http://www.actel.com/downloads/libero/
or you can order a CD from http://interact.actel.com/gbnew/lr.cgi

Actel Installation and Licensing Guide

Enter Disk Id

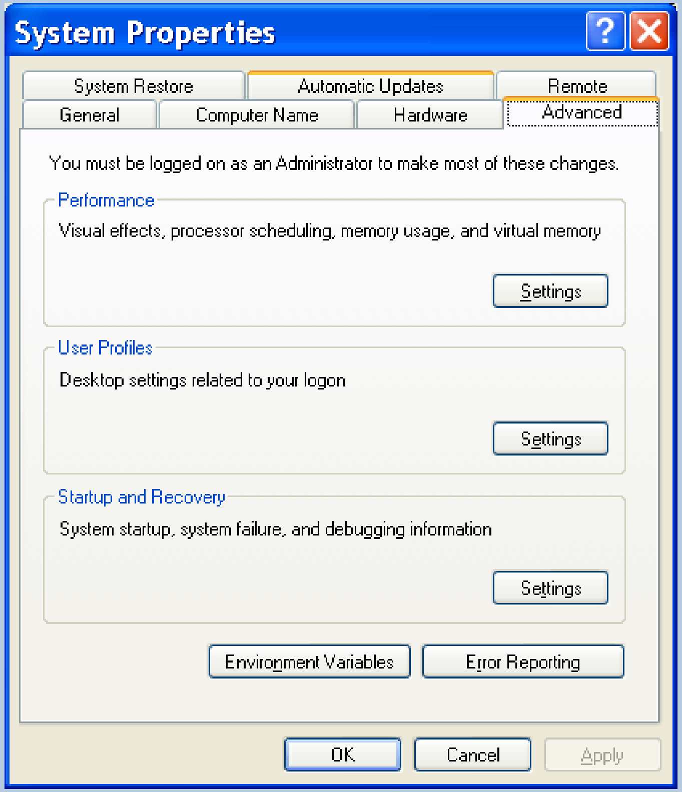
Specify OS

# Libero Licensing Summary

- Libero Gold License
  - Free!
  - Node-Locked to Disk ID
- Libero Platinum (Windows) License
  - Node-Locked or Locked to Hardware Keys
- Libero Platinum (Solaris or Linux) License
  - Floating License Locked to Host Id
    - Linux Requires Hardware Key for Synplify
- Libero Evaluation License
  - Node-Locked or Floating
  - Free 45 day License
- Synplicity License is included with Libero License

# License File:
## *Saving and Setting Variables*

- Store license.dat File in c:\flexlm Folder:
- Set Variables
  - **Windows NT**
    - **Control Panel -> System -> Environment Tab**
  - **Windows 2000**
    - **Control Panel -> System -> Advanced -> Environment Vars -> New**
  - **Windows XP**
    - **Control Panel -> System -> Advanced -> Environment Variables -> New**
  - **Set LM_LICENSE_FILE to c:\flexlm\license.dat**
  - **Set SYNPLICITY_LICENSE_FILE to c:\flexlm\license.dat**



System Properties

You must be logged on as an Administrator to make most of these changes.

Performance

Visual effects, processor scheduling, memory usage, and virtual memory

User Profiles

Desktop settings related to your logon

Startup and Recovery

System startup, system failure, and debugging information

# license.dat file

```
PACKAGE AEALL1 actlmgrd 1999.400 COMPONENTS="Viewdraw Actel \
     ActelACT-1Library ActelACT-2Library ActelACT-3Library Generic \
     GenericCAE EDIF_NetlistWriter ViewgenSchematicGenerator \
     Export1076 EDIF_NetlistReader GRAFLIB VERILNET ViewBASE WDIRDB \
     Altran Attdump Attmerge Attupdat Mega ViewGraf PARTSLIST" \
     SIGN=B56ED128C7D0
INCREMENT AEALL1 actlmgrd 1999.400 05-dec-2006 uncounted \
     VENDOR_STRING="Platform:NT exclusive:35" \
     HOSTID=DISK_SERIAL_NUM=a074afe9 ck=5 SIGN=4D2ACA78658C
FEATURE ACTEL_SUMMIT actlmgrd 6.3 05-dec-2006 uncounted \
     HOSTID=DISK_SERIAL_NUM=a074afe9 ck=172 SIGN=6E48D3D8E1709AA6
FEATURE wflite syncad 10.0 05-dec-2006 uncounted 0D826B8A5F9D \
     HOSTID=DISK_SERIAL_NUM=a074afe9 ck=157
FEATURE reactiveexport syncad 10.0 05-dec-2006 uncounted 5C6721A3F2E0 \
     HOSTID=DISK_SERIAL_NUM=a074afe9 ck=137
FEATURE basicvcdimport syncad 10.0 05-dec-2006 uncounted A1235A1BD49C \
     HOSTID=DISK_SERIAL_NUM=a074afe9 ck=130
FEATURE actelmtivlog mtioemd 2006.12 05-dec-2006 uncounted \
     489D4A494DAD HOSTID=DISK_SERIAL_NUM=a074afe9
FEATURE actelmtivhdl mtioemd 2006.12 05-dec-2006 uncounted \
     F2AF24411BCC HOSTID=DISK_SERIAL_NUM=a074afe9
FEATURE PALACE_ACTEL_APA_FULL aplus 4.000 05-dec-2006 uncounted \
     HOSTID=DISK_SERIAL_NUM=a074afe9 SIGN="03E4 2A9A F0DD 2AF7 D28E \
     31C3 229F 5481 924C C09D 6700 B368 0F71 CB42 D6C8 D52D 1C20 \
     65E4 4455 7A42 0137"
FEATURE synplify_pc synplctyd 2005.132 05-dec-2006 uncounted \
     1D43F615A72D9E5CBDCA VENDOR_STRING=actel_oem \
     HOSTID=DISK_SERIAL_NUM=a074afe9 \
     NOTICE=CUSTID=QASNT2155712607150 SIGN="0034 46A7 A572 1BE2 \
     313B 817D 6EA4 DB9F 8940 9188 9303 7D3D 10C5 B367 5E6E 03BA \
     3504 5FFB 4979 7381 6046"

# Your Software ID is : 14D-B05C-33D  #
```

ModelSim VHDL and Verilog

Synplicity License

Software id

Expiration date

# Libero Project Manager

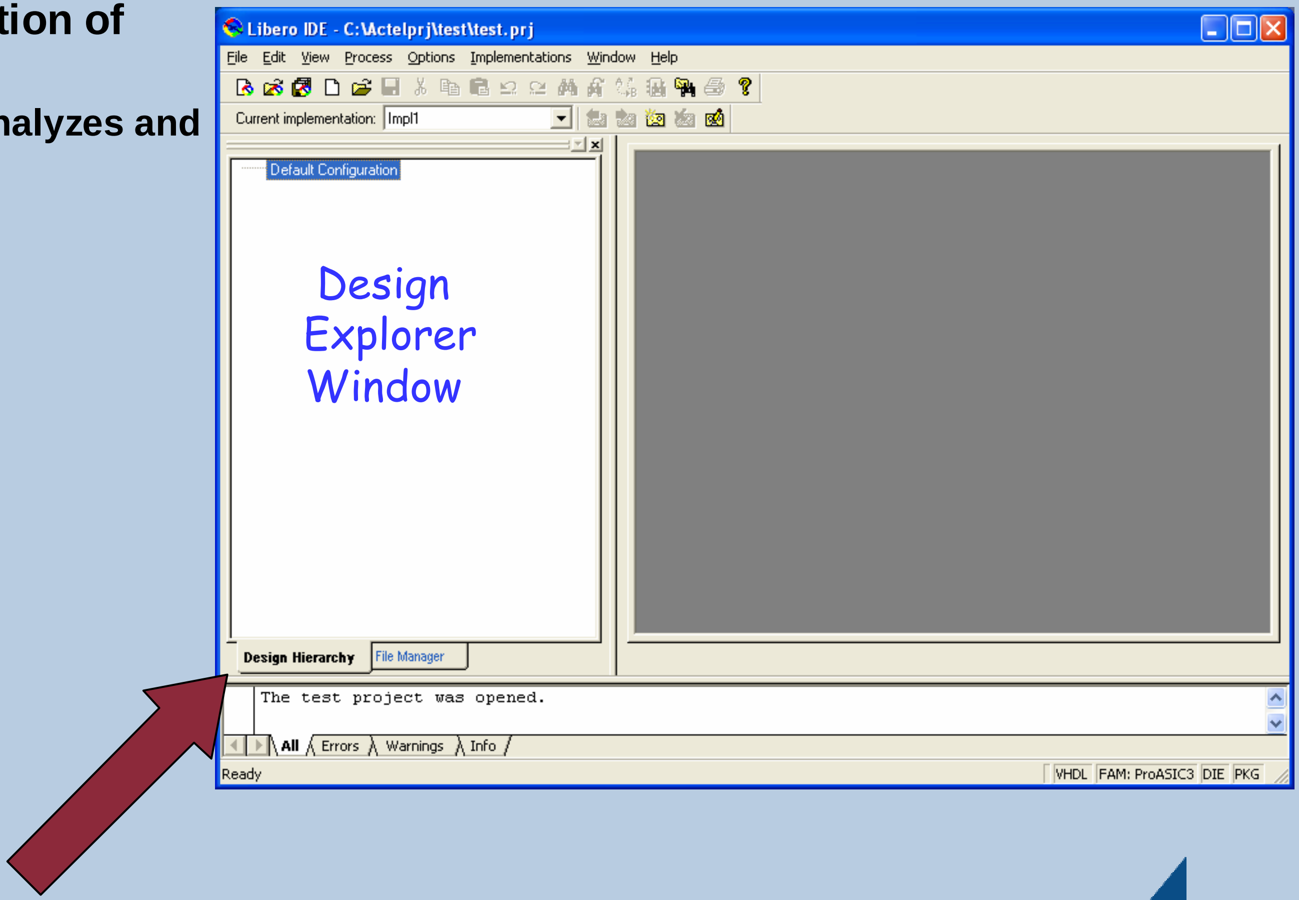
# Libero Project Manager Features

- Centrally Manages and Integrates Files and Tools
  - **Coordinates Project Information between Tools**
    - **e.g., Family Is Selected Once and Communicated to All Tools**
  - **Provides Seamless Piping of Internal Design Files among Tools**
  - **From within Libero's Project Manager, User Can Invoke Tools for:**
    - **Design Entry**
    - **Stimulus Generation**
    - **Simulation**
    - **Synthesis**
    - **Design Implementation and Static Timing Analysis**

# Libero IDE Project Manager

## Design Explorer Window

- Design Hierarchy Tab Displays Hierarchical Representation of Source Files in Project
  - Libero Continuously Analyzes and Updates Hierarchy

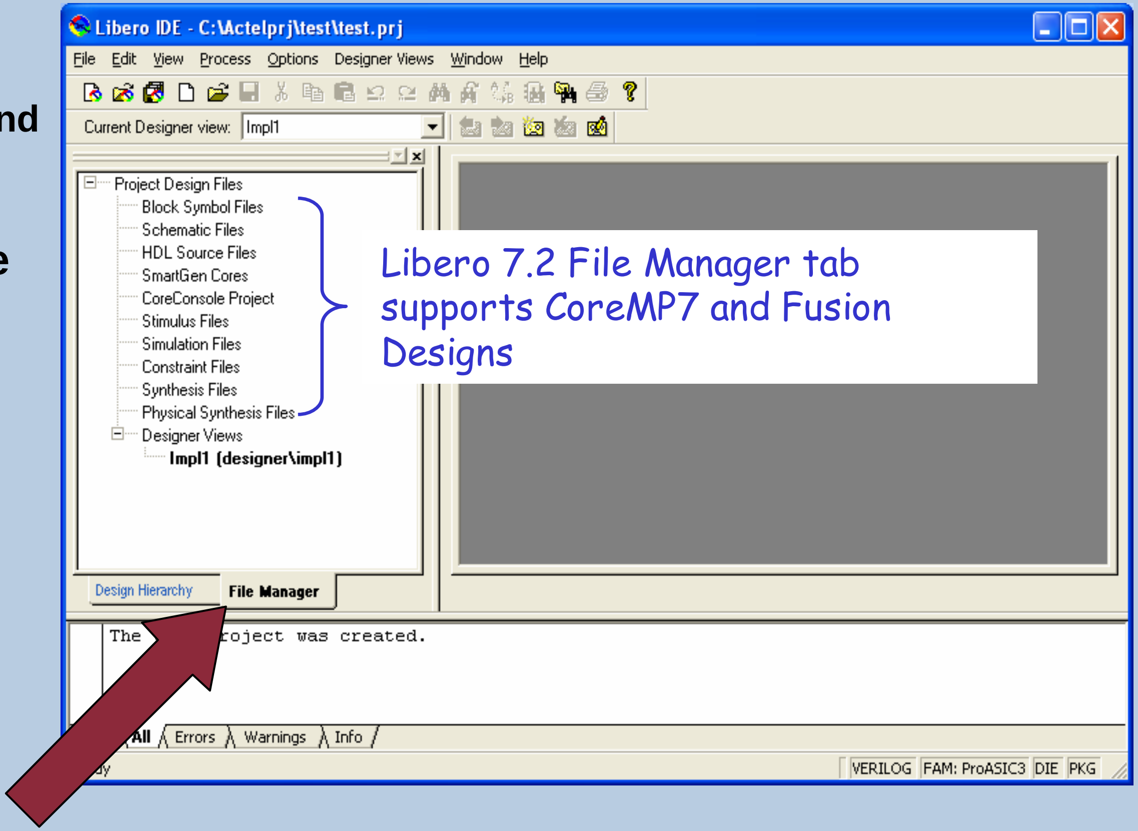

Libero IDE - C:\Actelprj\test\test.prj
File Edit View Process Options Implementations Window Help
Current implementation: Impl1
Default Configuration
Design Explorer Window
Design Hierarchy
File Manager
All
Errors
Warnings
Info
Ready
VHDL
FAM: ProASIC3
DIE
PKG

```
The test project was opened.
```

# Libero IDE Project Manager

## Design Explorer Window

- **Design Hierarchy Tab Displays Hierarchical Representation of Source Files in Project**
  - **Libero Continuously Analyzes and Updates Hierarchy**
- **File Manager Tab Displays All Files in Project Grouped by Type**



- Project Design Files
  - Block Symbol Files
  - Schematic Files
  - HDL Source Files
  - SmartGen Cores
  - CoreConsole Project
  - Stimulus Files
  - Simulation Files
  - Constraint Files
  - Synthesis Files
  - Physical Synthesis Files
  - Designer Views
    - **Impl1 (designer\impl1)**

```
The        roject was created.
```

dy

Libero 7.2 File Manager tab supports CoreMP7 and Fusion Designs

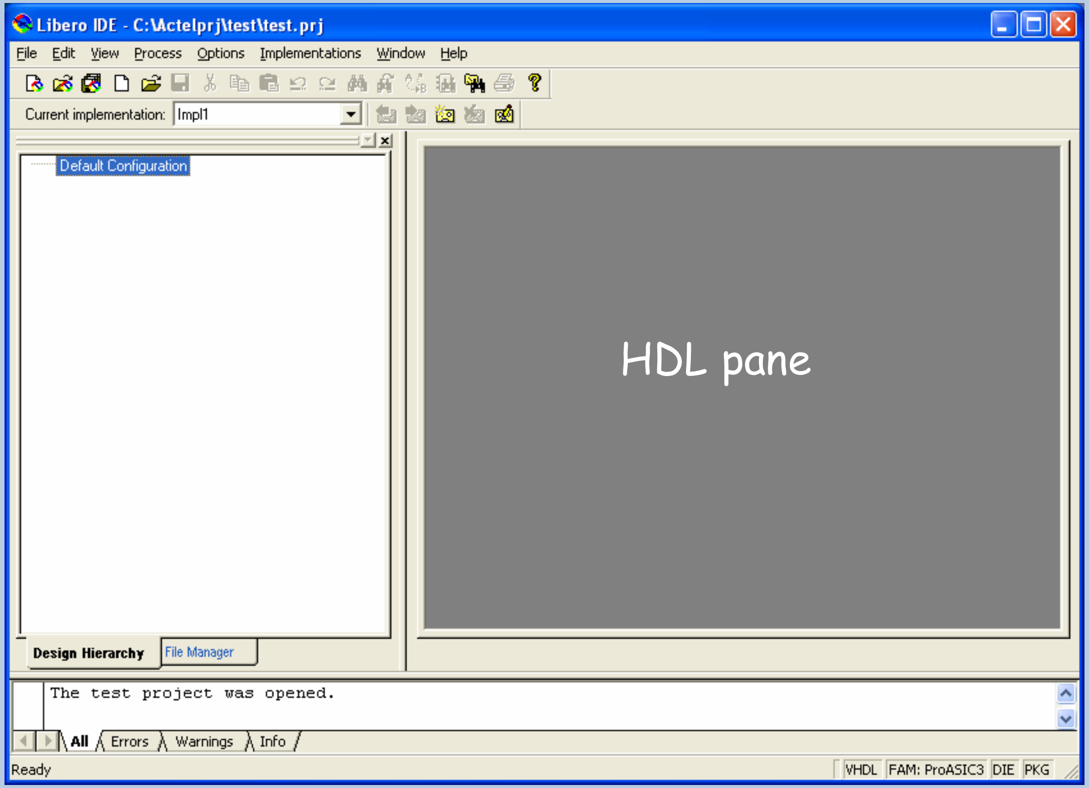
# Libero IDE Project Manager

## Design Explorer Window

- Design Hierarchy Tab Displays Hierarchical Representation of Source Files in Project
  - Libero Continuously Analyzes and Updates Hierarchy
- File Manager Tab Displays All Files in Project Grouped by Type

## Language-Sensitive HDL Editor

- Verilog 2001 or VHDL 93


Libero IDE - C:\Actelprj\test\test.prj
File Edit View Process Options Implementations Window Help
Current implementation: Impl1
Default Configuration
HDL pane
Design Hierarchy
File Manager
All Errors Warnings Info
Ready
VHDL FAM: ProASIC3 DIE PKG

```
The test project was opened.
```

# Libero IDE Project Manager

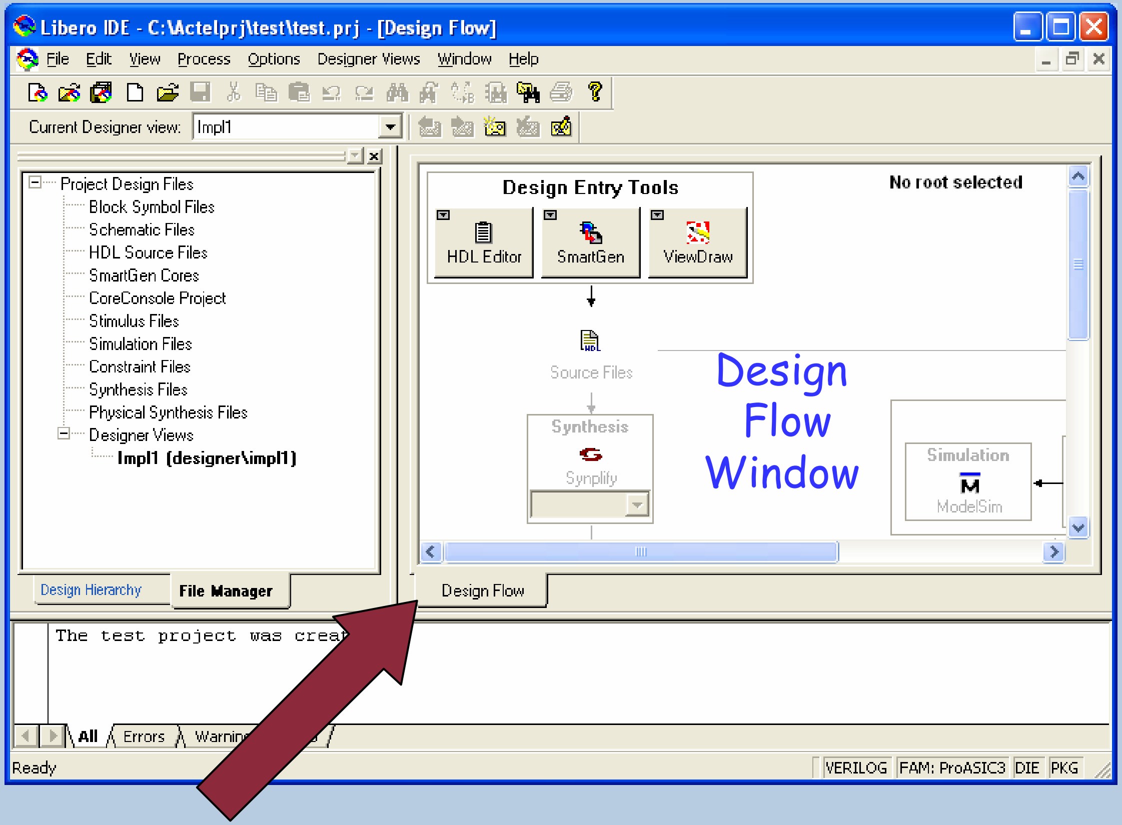
## ■ Design Explorer Window

- Design Hierarchy Tab Displays Hierarchical Representation of Source Files in Project
  - ◆ Libero Continuously Analyzes and Updates Hierarchy
- File Manager Tab Displays All Files in Project Grouped by Type

## ■ Language-Sensitive HDL Editor

- Verilog 2001 or VHDL 93

## ■ Tools Can Be Launched from Design Flow Window or Menus


Libero IDE - C:\Actelprj\test\test.prj - [Design Flow]

Current Designer view: Impl1

- Project Design Files
  - Block Symbol Files
  - Schematic Files
  - HDL Source Files
  - SmartGen Cores
  - CoreConsole Project
  - Stimulus Files
  - Simulation Files
  - Constraint Files
  - Synthesis Files
  - Physical Synthesis Files
  - Designer Views
    - **Impl1 (designer\impl1)**

```
The test project was creat
```

Ready

ONECHIP is all you need

# Libero IDE Project Manager

## Design Explorer Window

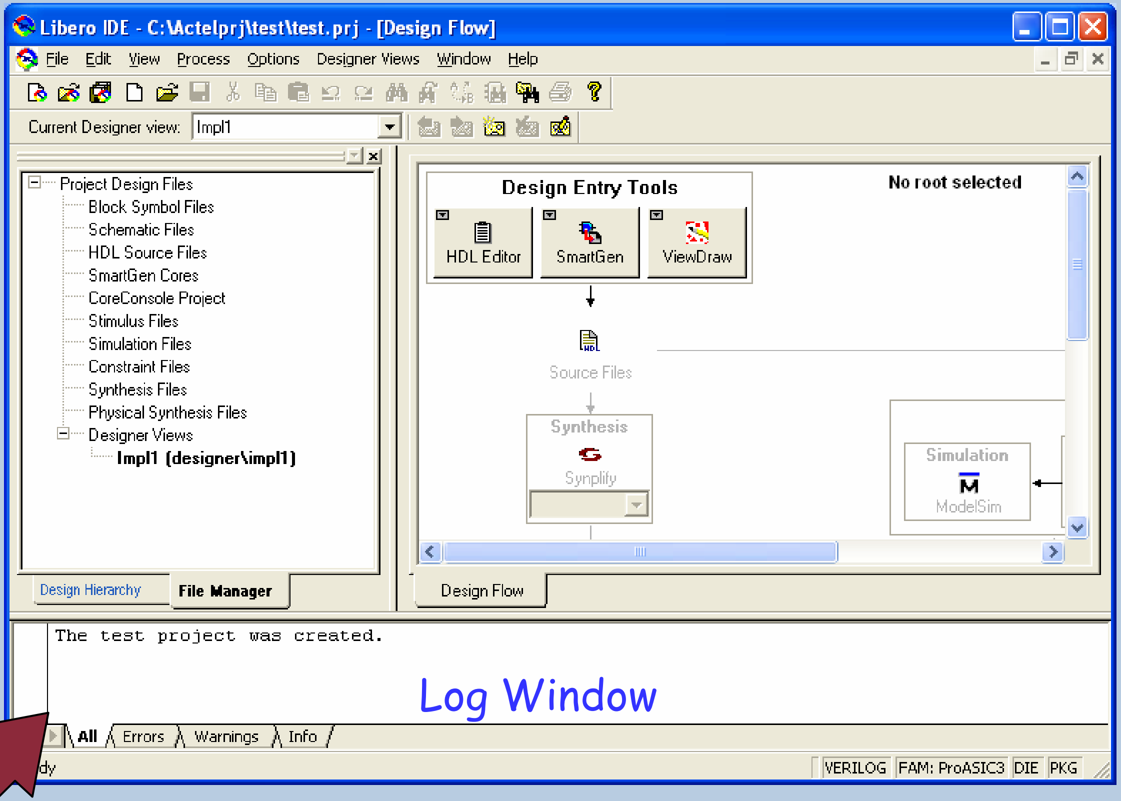
- Design Hierarchy Tab Displays Hierarchical Representation of Source Files in Project
  - Libero Continuously Analyzes and Updates Hierarchy
- File Manager Tab Displays All Files in Project Grouped by Type

## Language-Sensitive HDL Editor

- Verilog 2001 or VHDL 93

## Tools Can Be Launched from Design Flow Window or Menus

## Log Windows Provide Status and Error Messages

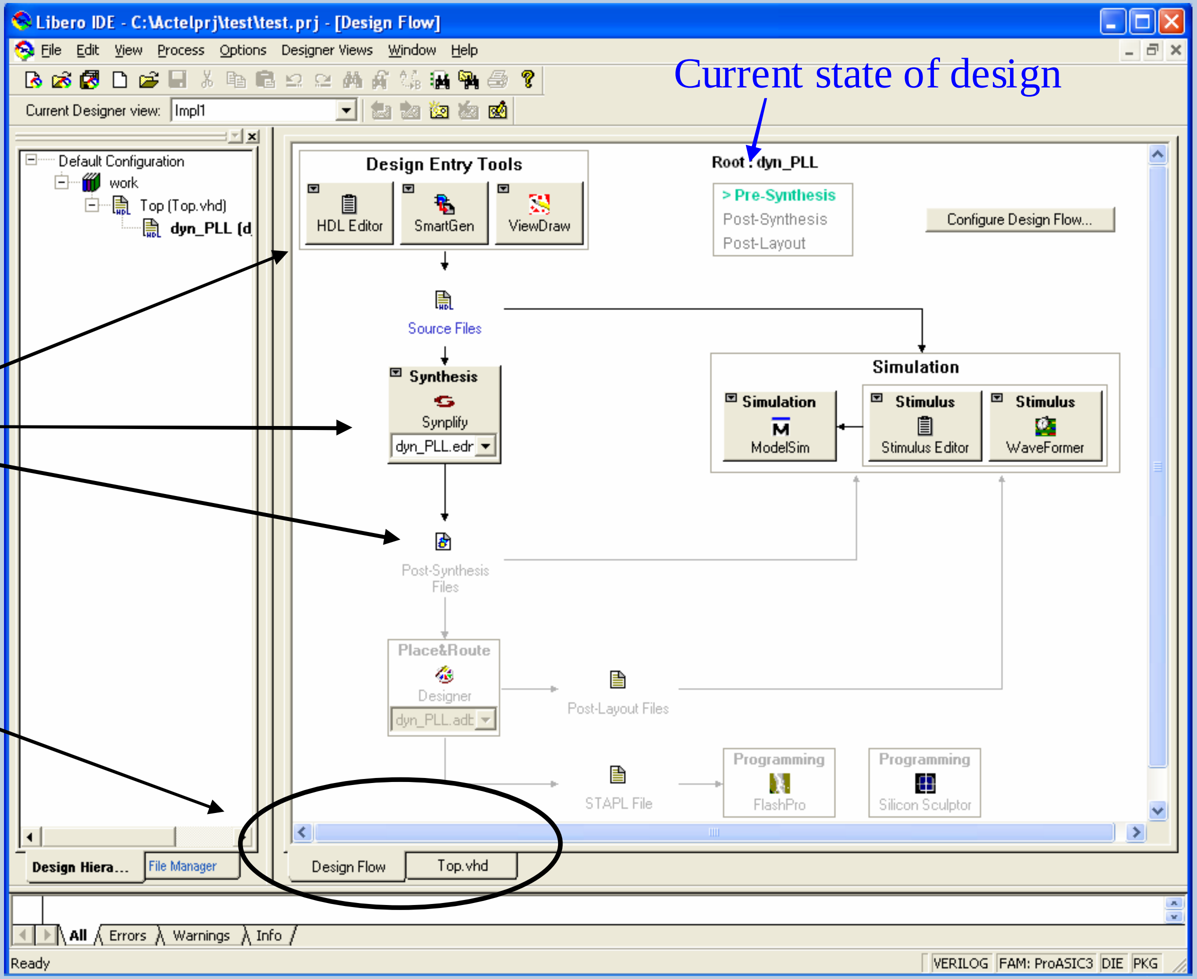


```
The test project was created.
```

# Libero IDE
# Design Flow Window

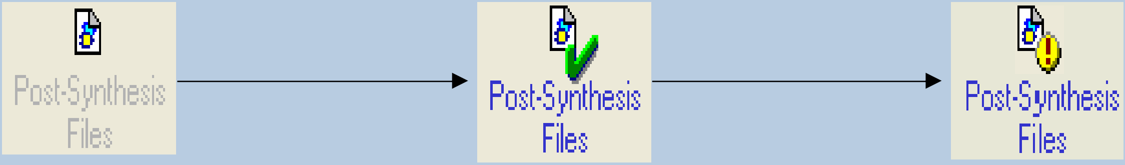
## Step-by-Step design flow decreases design development time

- Design Flow Window Displays:
  - **Tools**
  - **Files**
  - **Transitions**
  - **Current State**
  - **Tool Tips**
- Interactive Blocks
  - **Activates Tools**
  - **View Files**
- Display changes dynamically based on target family
- Tabs Switch between Flow Window and HDL Window



# Libero IDE Design Flow Window
## *File Status of Displayed Items*

- Group of Files Can Be …
- … Missing
  - If ANY Are Missing, Block Is Shadowed Out
- … Available and Current
  - Green Check Mark Is Shown ✓
- … Available, but Not Current ⚠
  - If at Least One is Not Current, Warning Icon Is Displayed



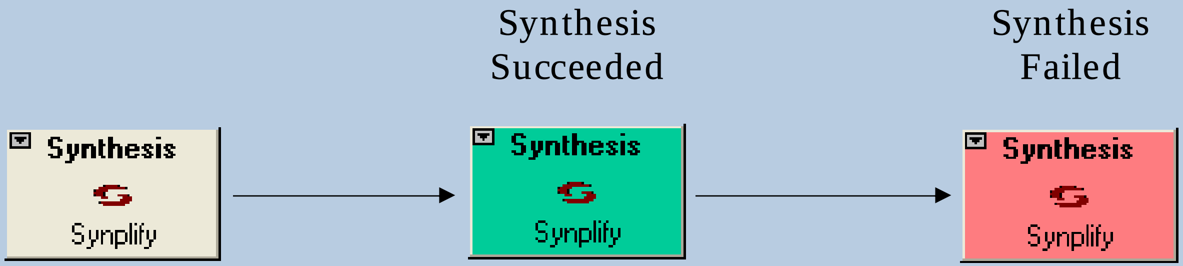
Synthesis Incomplete

Synthesis Complete

Source Modified – EDIF Netlist not current

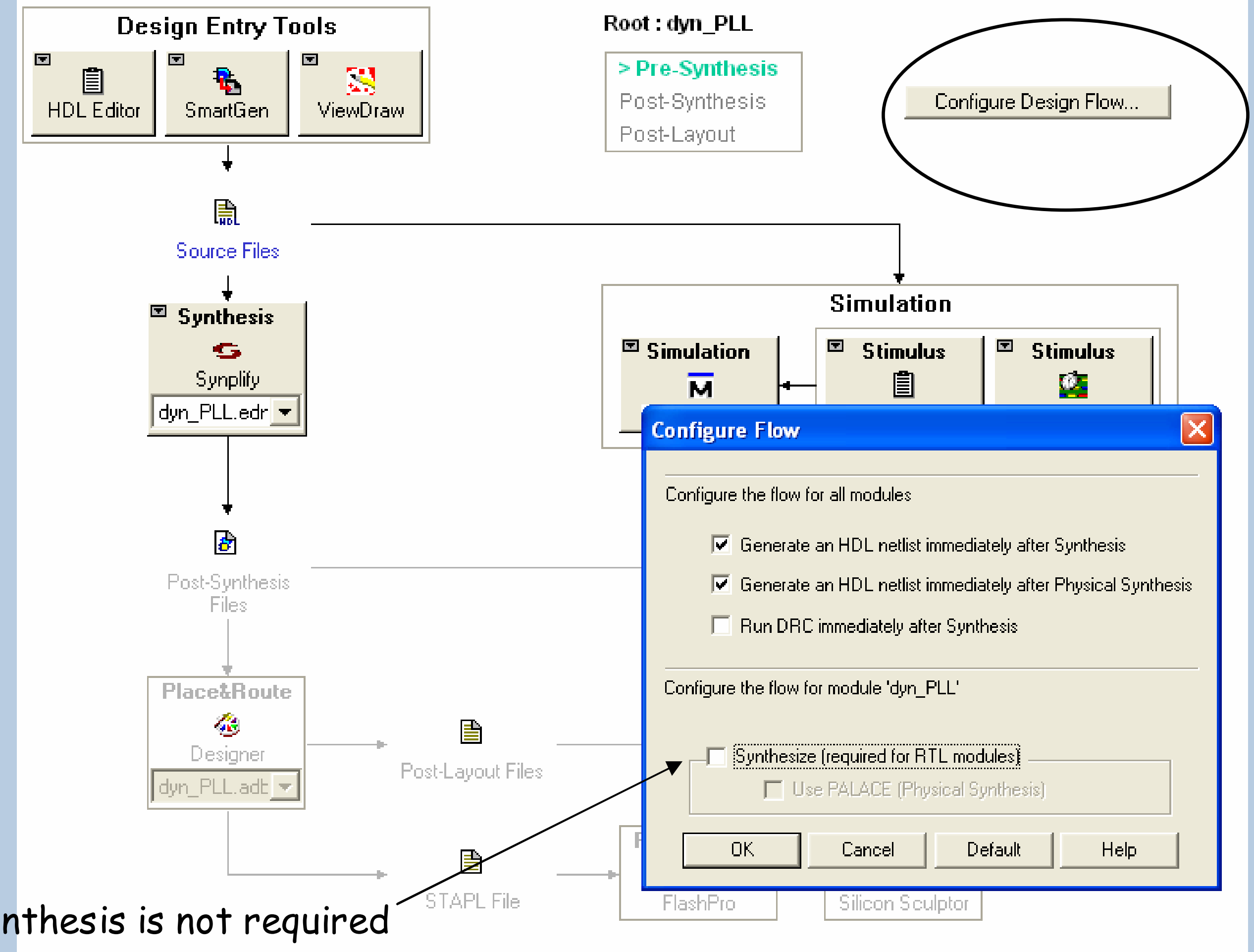
# Libero IDE Design Flow Window
## *Tool States*

- Disabled => Button Is Shadowed
- White => Available, but Not Yet Used
- Green => Completed Successfully
- Red => Error in Running Tool



# Libero IDE Design Flow Window
*Structural Designs*

- Design Flow Window Can Be Configured For Structural Designs That Do Not Require Synthesis



**Configure Flow**

Configure the flow for all modules

☑ Generate an HDL netlist immediately after Synthesis

☑ Generate an HDL netlist immediately after Physical Synthesis

□ Run DRC immediately after Synthesis

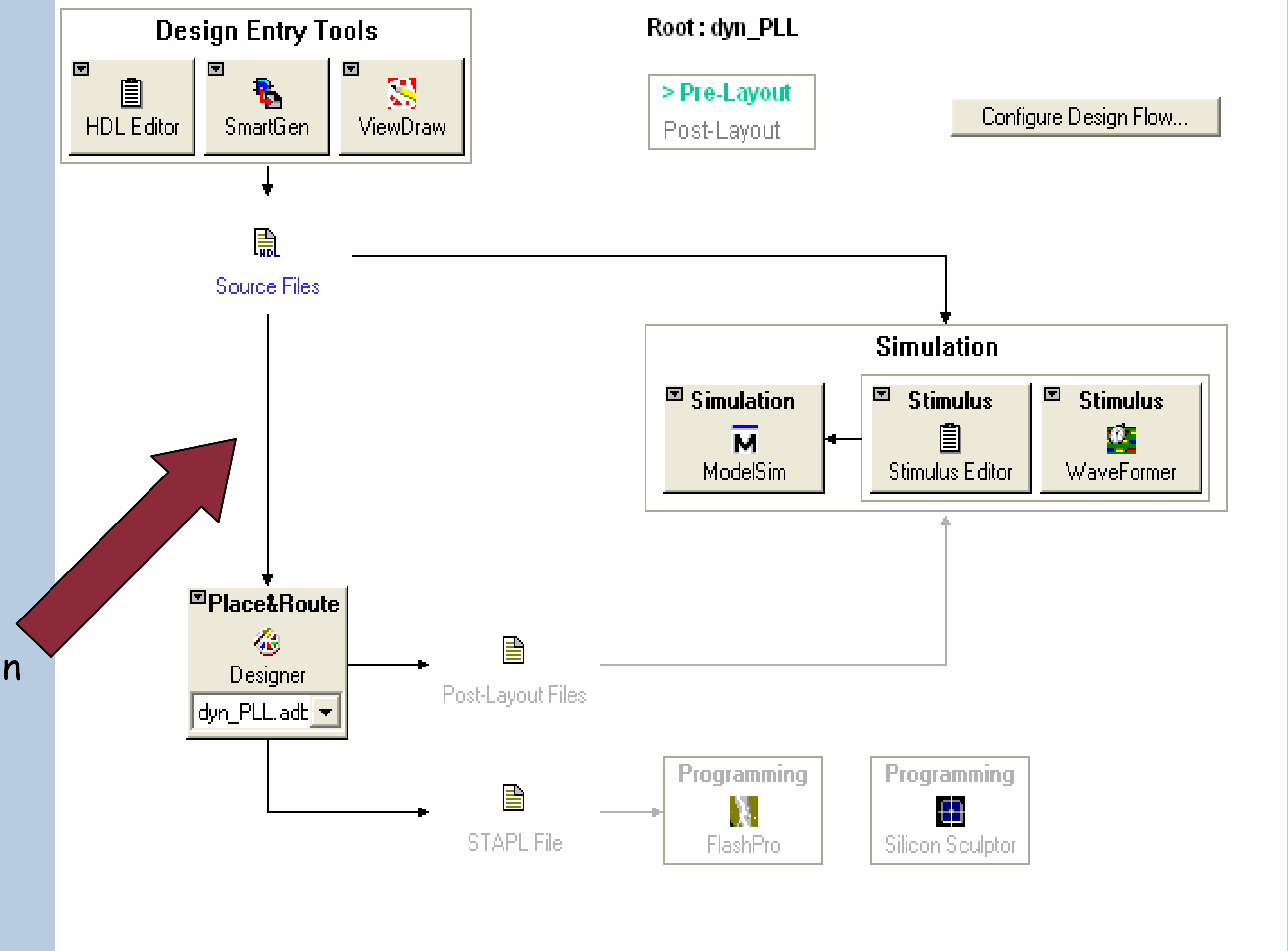
Configure the flow for module 'dyn_PLL'

□ Synthesize (required for RTL modules)

□ Use PALACE (Physical Synthesis)

Un-check if synthesis is not required

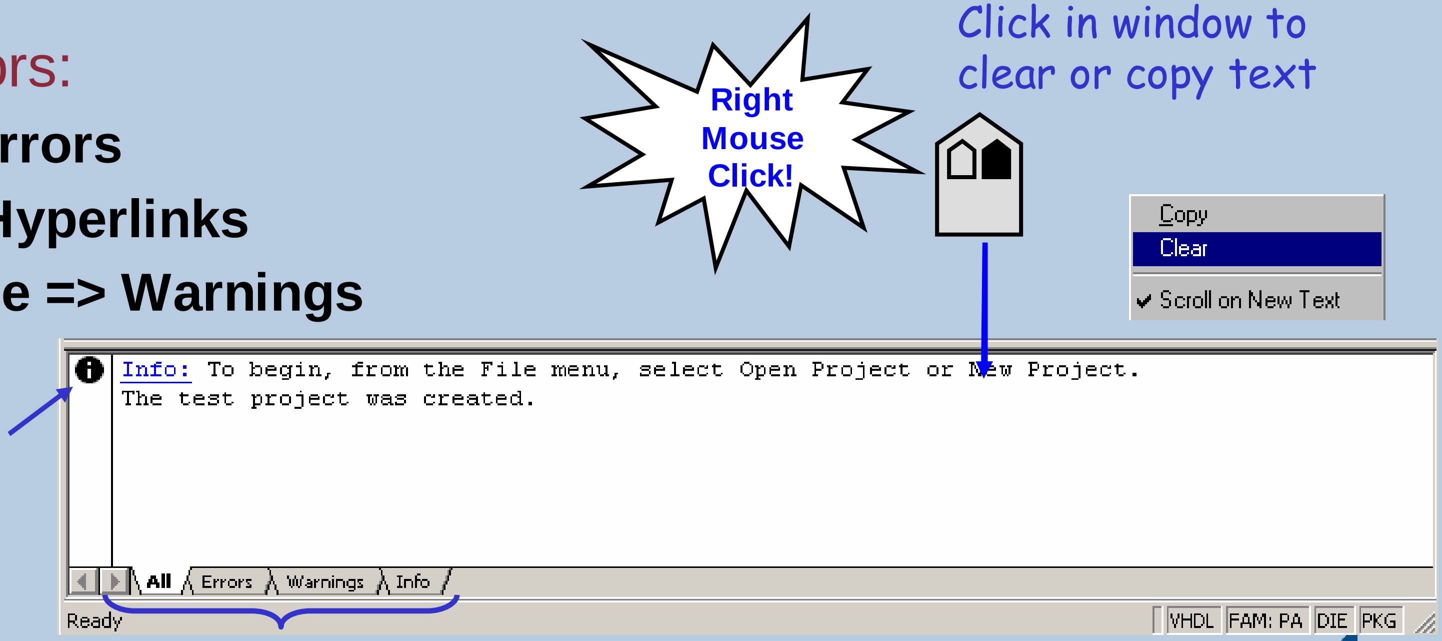
# Libero IDE Design Flow Window
*Synthesis Not Required*



Synthesis button disabled

# Libero Log Window Error Manager

- Error Manager Consists of 4 Tabs in Log Window:
  - **All: Displays All Messages**
  - **Errors: Displays Error Messages**
  - **Warnings: Displays Warning Messages**
  - **Info: Displays Information Messages**
- Default Colors:
  - **Red => Errors**
  - **Blue => Hyperlinks**
  - **Light Blue => Warnings**



```
Info: To begin, from the File menu, select Open Project or New Project.
The test project was created.
```

Click in window to clear or copy text

Icon appears next to each message

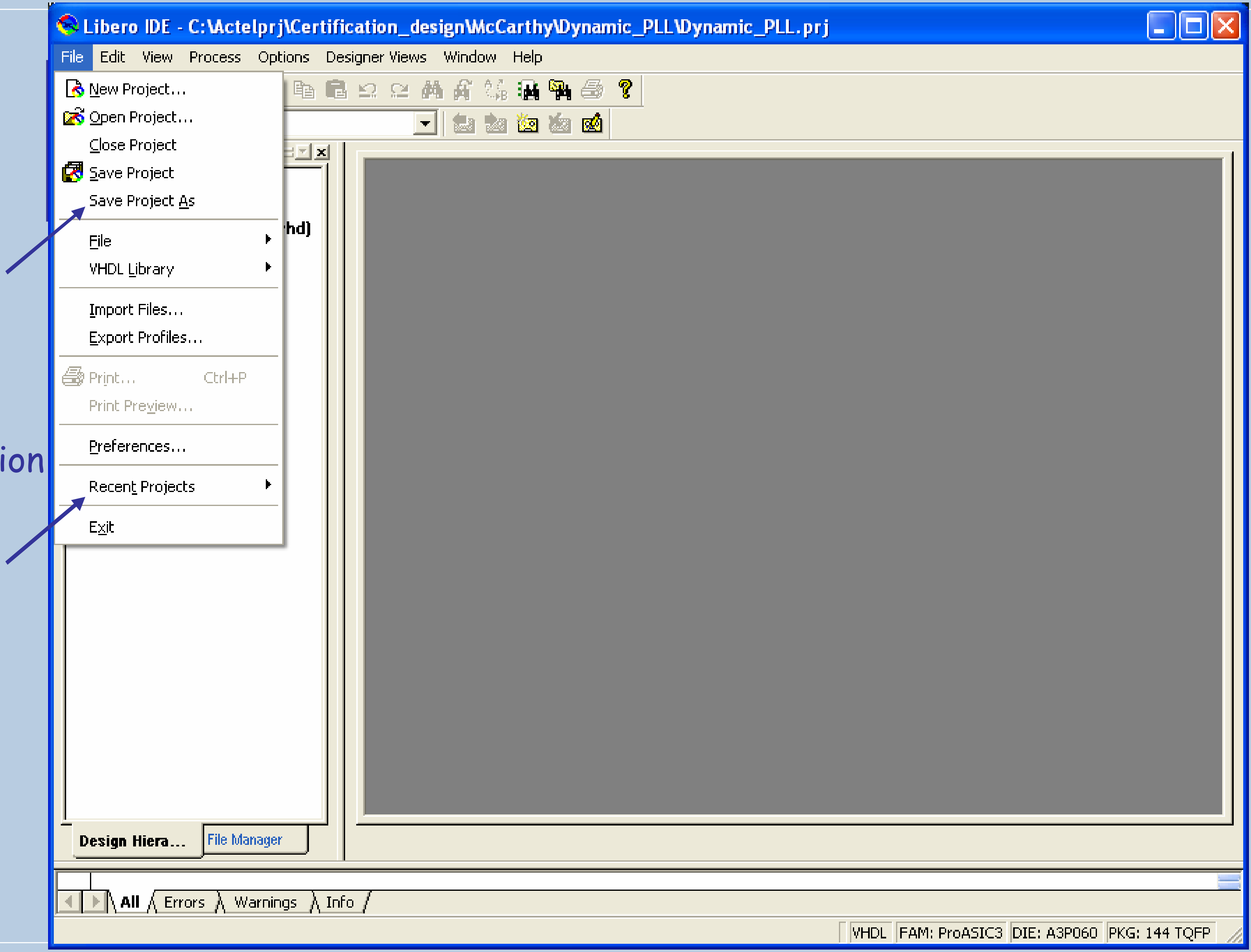
Libero error manager tabs

# Libero IDE File Menu Options

Create, open, close and save projects

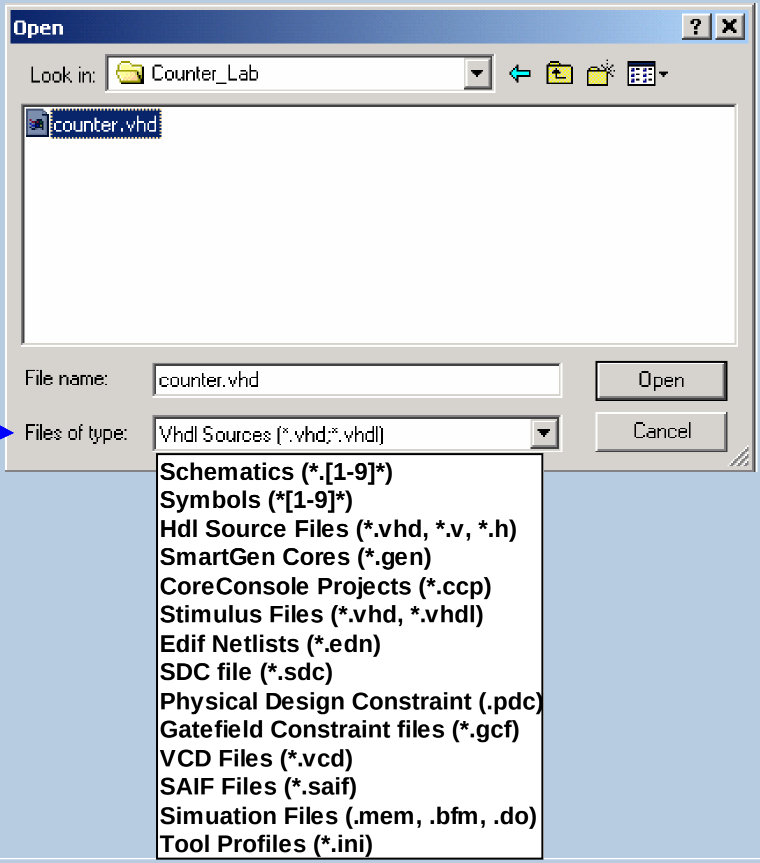
"Save-As": Save Project with Different Name and/or in Different Location

List of Recent Projects



# Importing Files

- File -> Import Files
- Existing Design Files Can Be Imported into Libero Project
  - Schematics, Symbols, HDL (VHDL or Verilog), Stimulus (VHDL or Verilog), SmartGen Cores, EDIF Netlists, SDC Files, Constraint Files, Tool Profiles



Open

Look in: Counter_Lab

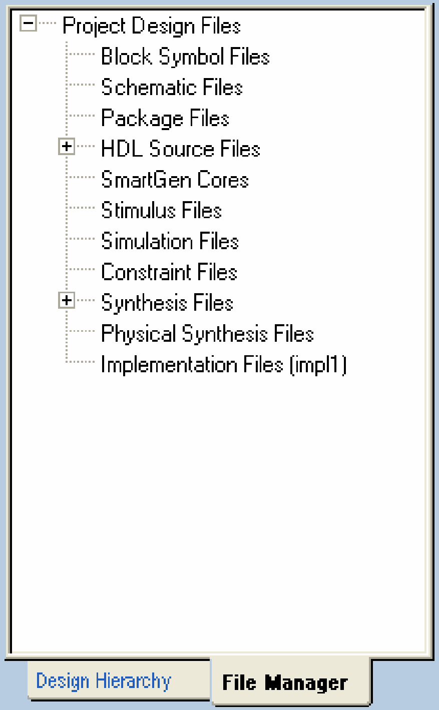
counter.vhd

File name: counter.vhd

Files of type: Vhdl Sources (*.vhd;*.vhdl)

Schematics (*.[1-9]*)
Symbols (*[1-9]*)
Hdl Source Files (*.vhd, *.v, *.h)
SmartGen Cores (*.gen)
CoreConsole Projects (*.ccp)
Stimulus Files (*.vhd, *.vhdl)
Edif Netlists (*.edn)
SDC file (*.sdc)
Physical Design Constraint (.pdc)
Gatefield Constraint files (*.gcf)
VCD Files (*.vcd)
SAIF Files (*.saif)
Simuation Files (.mem, .bfm, .do)
Tool Profiles (*.ini)

Select file type from pull-down menu

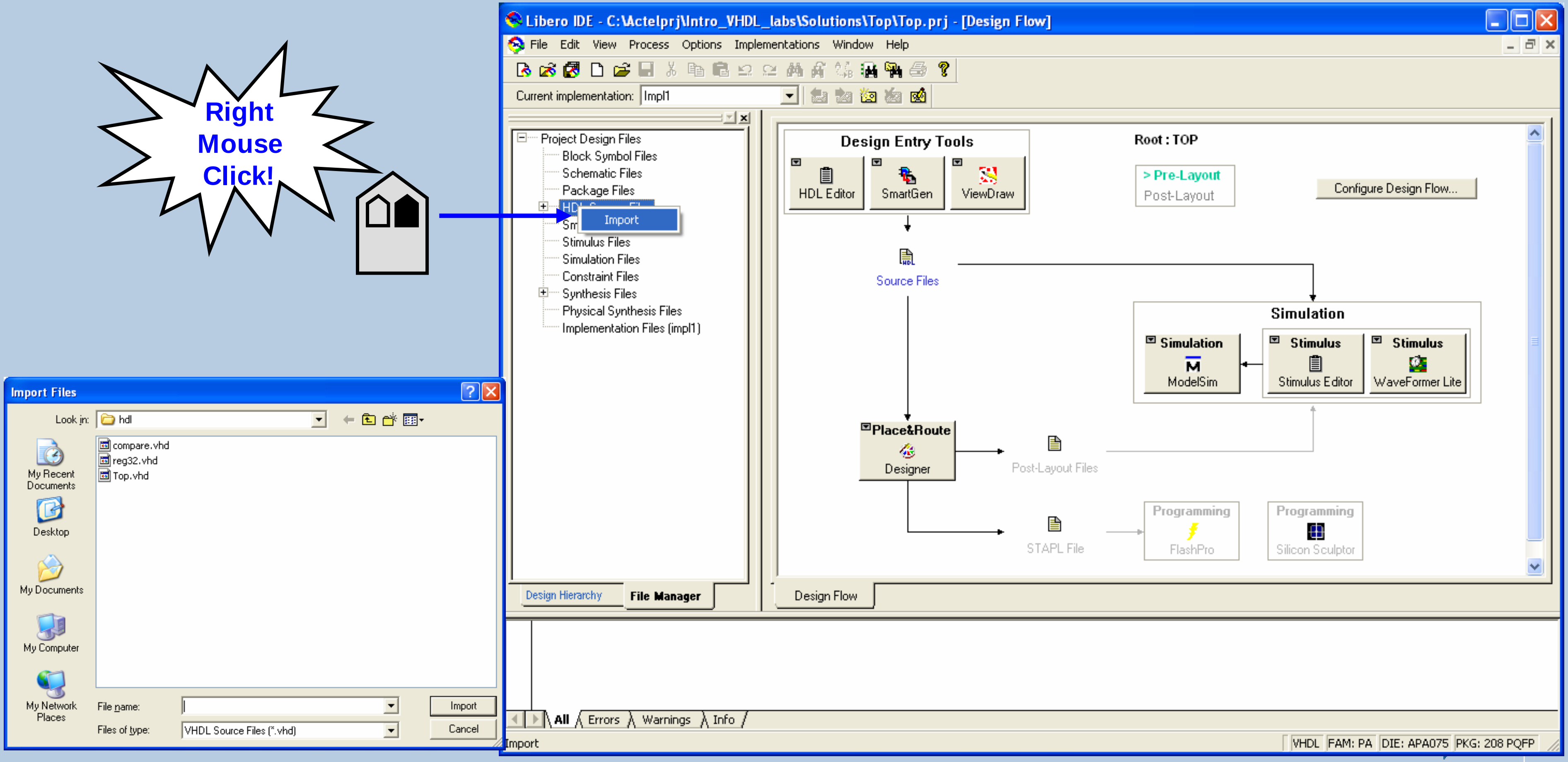


Project Design Files
- Block Symbol Files
- Schematic Files
- Package Files
- HDL Source Files
- SmartGen Cores
- Stimulus Files
- Simulation Files
- Constraint Files
- Synthesis Files
- Physical Synthesis Files
- Implementation Files (impl1)

u need

# Import Files
## *File Manager Tab*

- Files Can Also Be Imported from File Manager Tab
  - **Click on File Type and Select Import**



Right Mouse Click!

Libero IDE - C:\Actelprj\Intro_VHDL_labs\Solutions\Top\Top.prj - [Design Flow]

Current implementation: Impl1

Root : TOP

Import Files

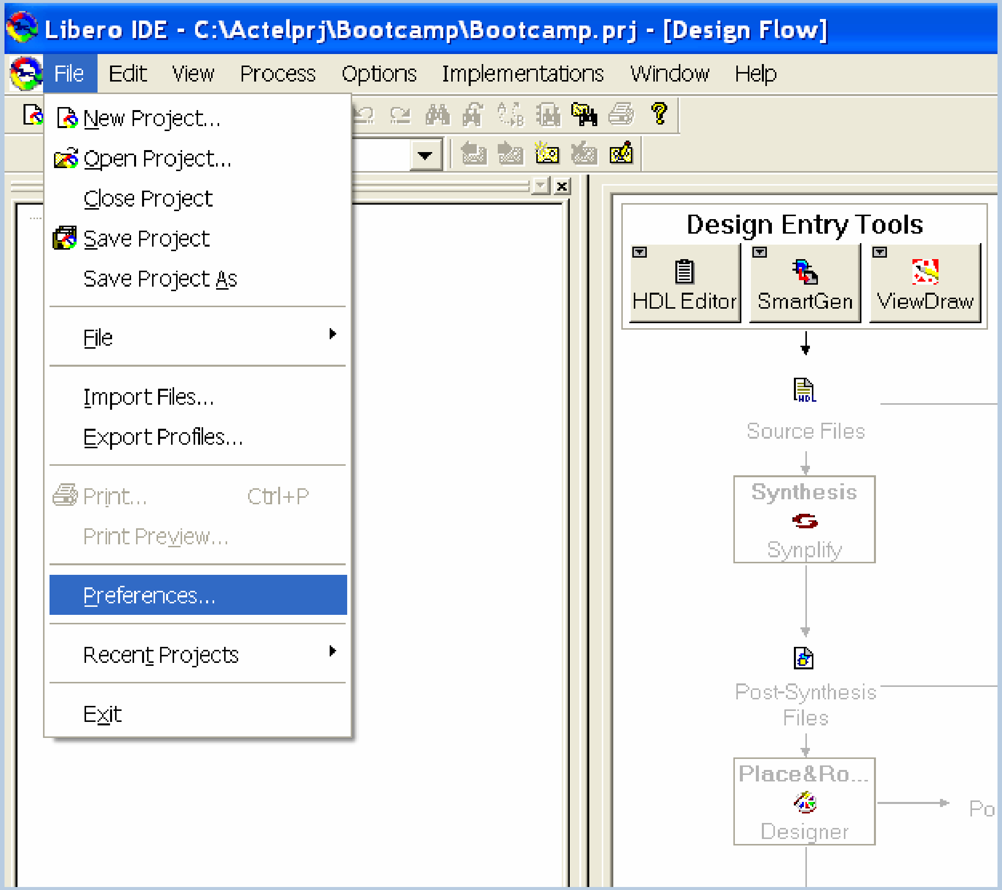
Look in: hdl

compare.vhd
reg32.vhd
Top.vhd

File name:

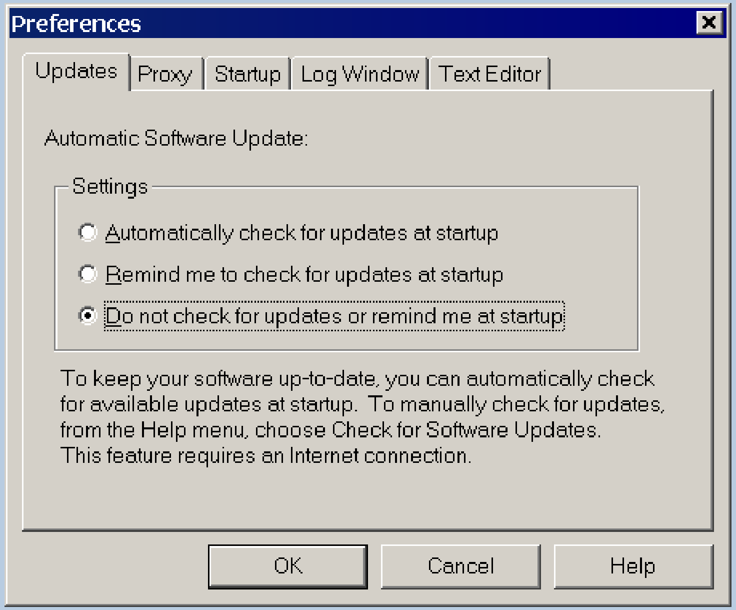
Files of type: VHDL Source Files (*.vhd)

# Libero IDE File Menu
## *User Preferences*



# Libero IDE User Preferences
## *Automatic Software Update Check*

- Enable or Disable Checking for Updates When Libero is Launched



Automatic Software Update:

Settings

○ Automatically check for updates at startup

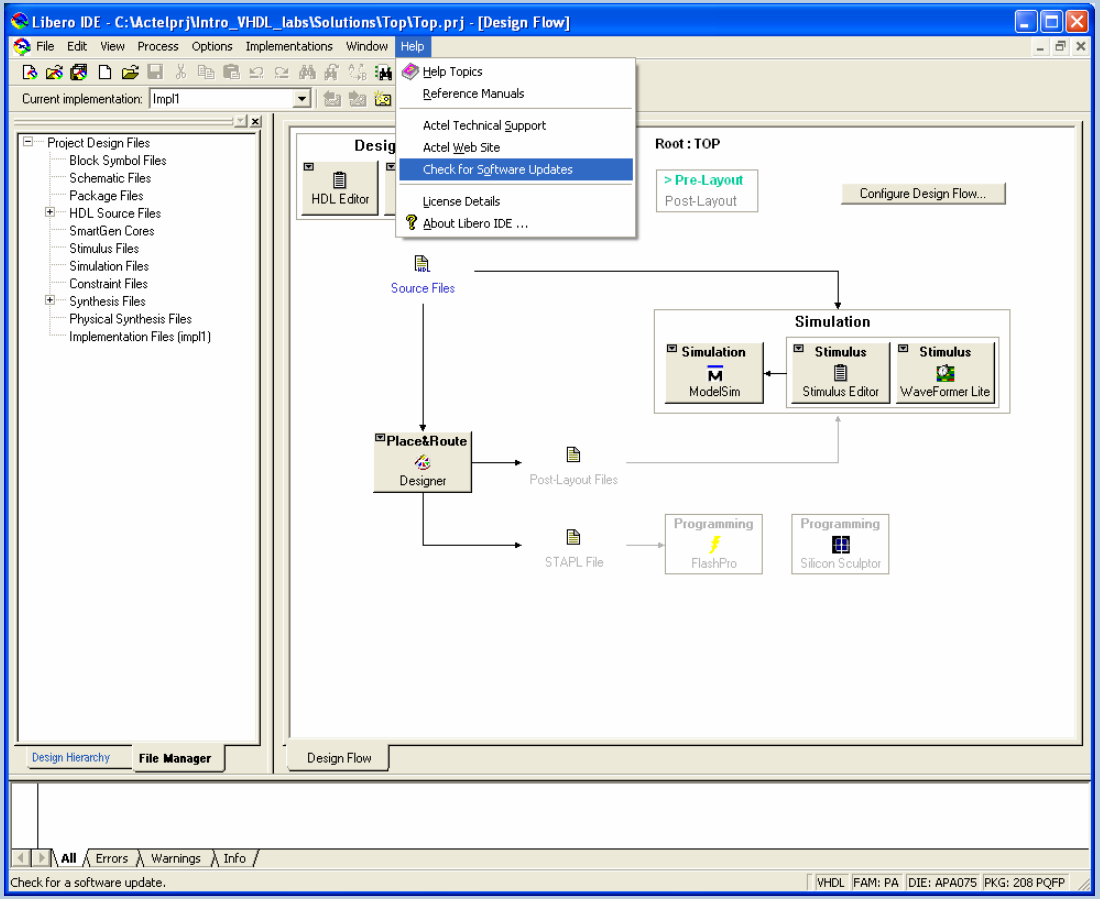
○ Remind me to check for updates at startup

● Do not check for updates or remind me at startup

To keep your software up-to-date, you can automatically check for available updates at startup. To manually check for updates, from the Help menu, choose Check for Software Updates. This feature requires an Internet connection.

# Libero IDE
## *Checking for Software Updates Manually*

- Manually Check for Software Updates from Help Menu



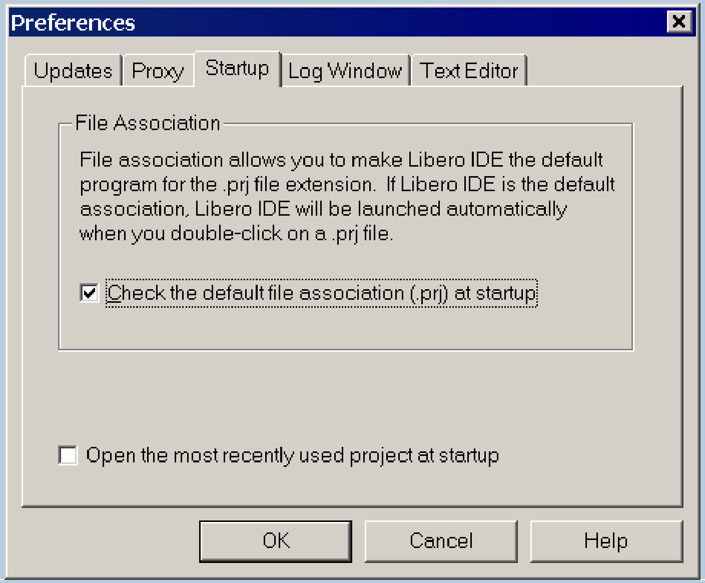
Libero IDE - C:\Actelprj\Intro_VHDL_labs\Solutions\Top\Top.prj - [Design Flow]

Check for a software update.

VHDL | FAM: PA | DIE: APA075 | PKG: 208 PQFP

# Libero IDE User Preferences
## *Project Startup Behavior*

- Specify How Libero Behaves When Opened
  - **Open with no project or open most recently used project**
- Default Startup
  - **Most Recent Project Is Opened When Libero is Launched**
  - **If None Exists, Libero Launches the New Project Wizard**
- Default Can be Modified in Libero Startup Properties
  - **Check or Uncheck "Open the most recently used project at startup"**



File Association

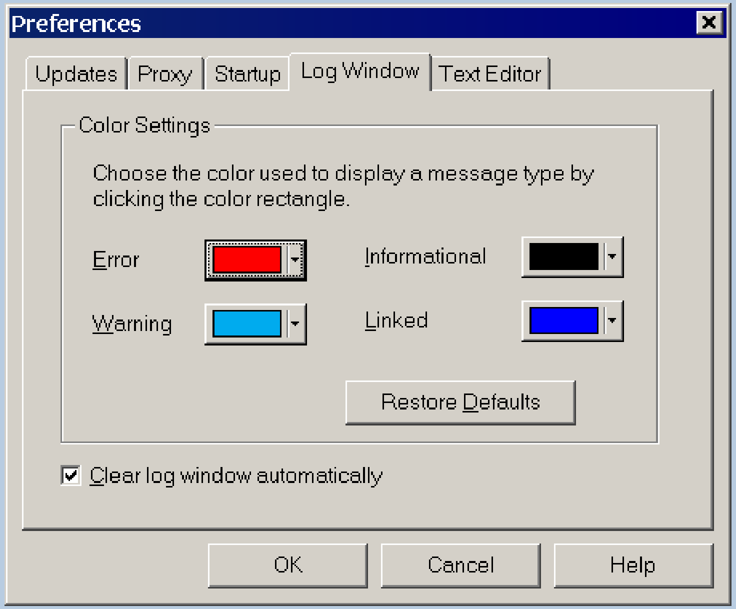
File association allows you to make Libero IDE the default program for the .prj file extension. If Libero IDE is the default association, Libero IDE will be launched automatically when you double-click on a .prj file.

☑ Check the default file association (.prj) at startup

□ Open the most recently used project at startup

# Libero IDE User Preferences
## *Log Window Colors*

- Specify Colors for Messages in the Libero Log Window



Preferences

Updates | Proxy | Startup | Log Window | Text Editor

Color Settings

Choose the color used to display a message type by clicking the color rectangle.

Error 🟥

Informational ⬛

Warning 🟦

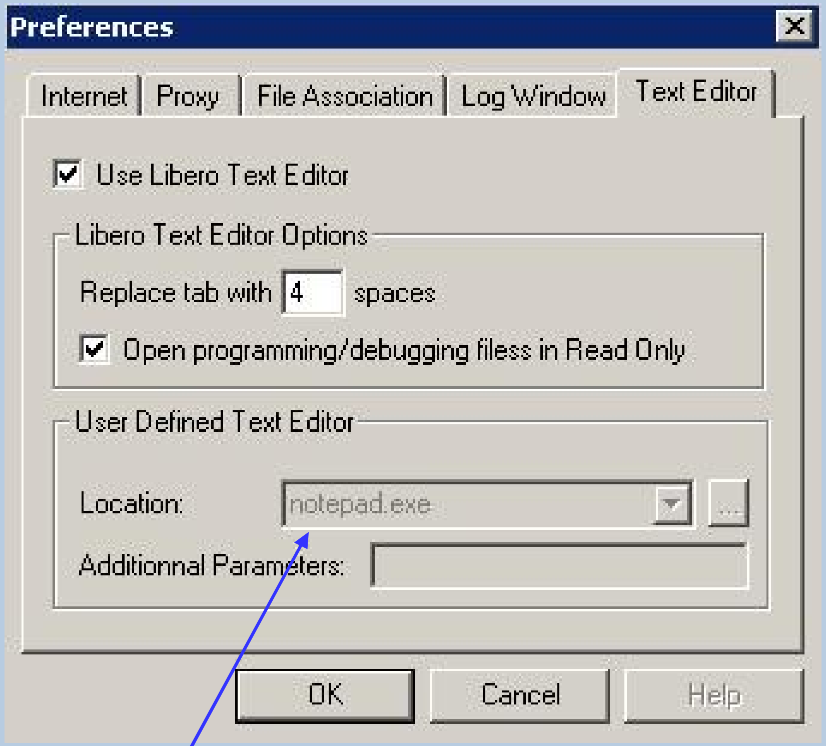
Linked 🟦

☑ Clear log window automatically

# Libero IDE User Preferences
*Text Editor*

## Text Editor Selection

- Use Libero IDE Text Editor or External Text Editor
  - File > Preferences  Text Editor Tab



Preferences

☑ Use Libero Text Editor

Libero Text Editor Options

Replace tab with 4 spaces

☑ Open programming/debugging filess in Read Only

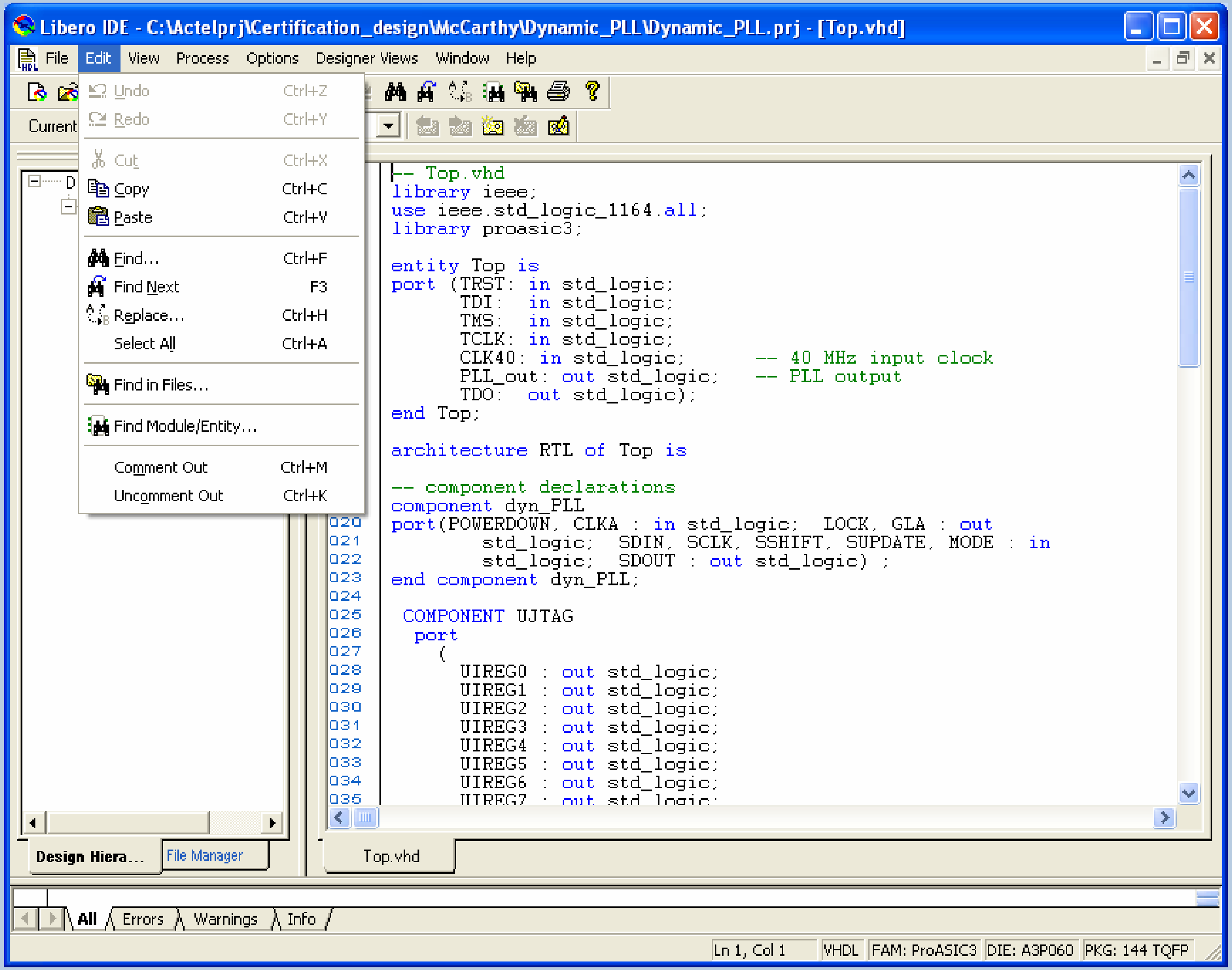
User Defined Text Editor

Location: notepad.exe

Additionnal Parameters:

Enter location of external text editor if selected

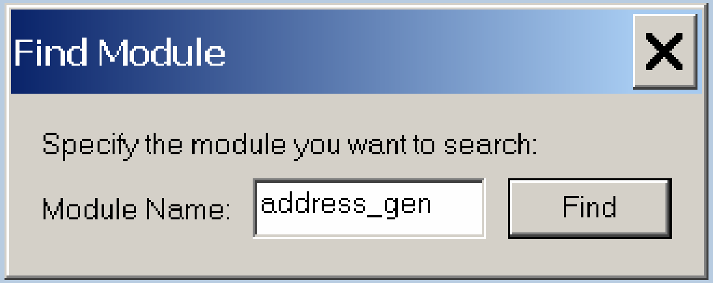
# Libero IDE
## *Edit Menu Options*



```
-- Top.vhd
library ieee;
use ieee.std_logic_1164.all;
library proasic3;

entity Top is
port (TRST:  in std_logic;
      TDI:   in std_logic;
      TMS:   in std_logic;
      TCLK:  in std_logic;
      CLK40: in std_logic;        -- 40 MHz input clock
      PLL_out: out std_logic;     -- PLL output
      TDO:   out std_logic);
end Top;

architecture RTL of Top is

-- component declarations
component dyn_PLL
port(POWERDOWN, CLKA : in std_logic;  LOCK, GLA : out
        std_logic;  SDIN, SCLK, SSHIFT, SUPDATE, MODE : in
        std_logic;  SDOUT : out std_logic) ;
end component dyn_PLL;

 COMPONENT UJTAG
  port
    (
      UIREG0  : out std_logic;
      UIREG1  : out std_logic;
      UIREG2  : out std_logic;
      UIREG3  : out std_logic;
      UIREG4  : out std_logic;
      UIREG5  : out std_logic;
      UIREG6  : out std_logic;
      UIREG7  : out std_logic;
```

# Libero Project Manager
## *Find Module / Entity*

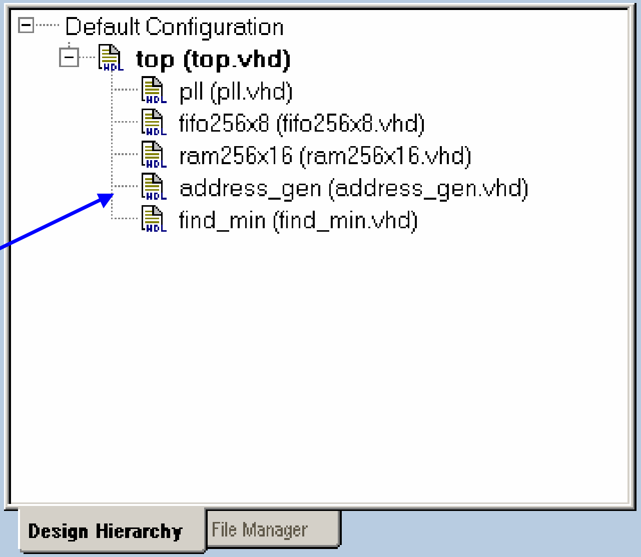
- To find Module in a Hierarchy, click Find Module Icon on Tool bar, or Click Edit/Find Module



Specify the module you want to search:

Module Name: address_gen

Libero selects and displays the found module

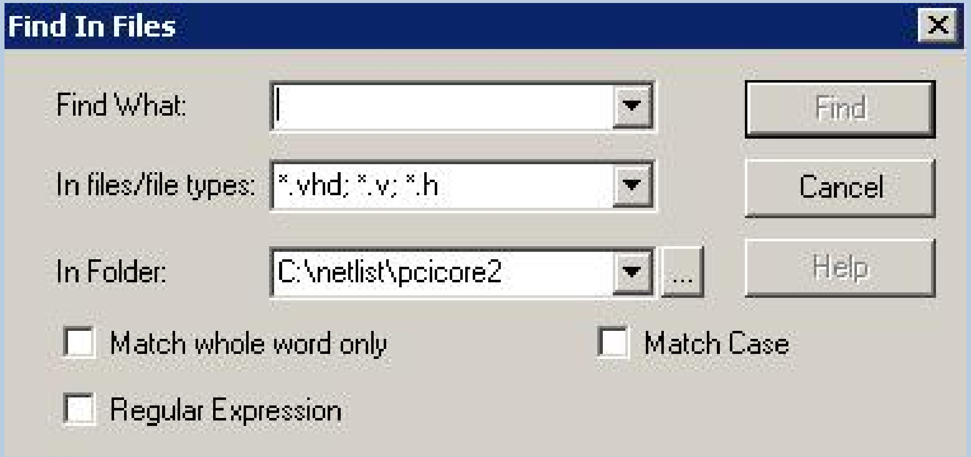


```
⊟ Default Configuration
   ⊟ top (top.vhd)
        pll (pll.vhd)
        fifo256x8 (fifo256x8.vhd)
        ram256x16 (ram256x16.vhd)
        address_gen (address_gen.vhd)
        find_min (find_min.vhd)
```

- “Find Next” in Design Hierarchy
  - **From the “Find Module” dialog you can select “Find Next”**
    - **Find by using regular expression e.g. *_cntrl => “mode_cntrl”**
    - **Find by matching exact case**

# Libero Project Manager
## *Find in Files*

- Edit => Find in Files, or Toolbar Icons
  - Search for Files, Words, etc
  - Specify by File Types
  - Specify where to Search
  - Match Whole Word
  - Match Case
  - Regular Expression



Find What:

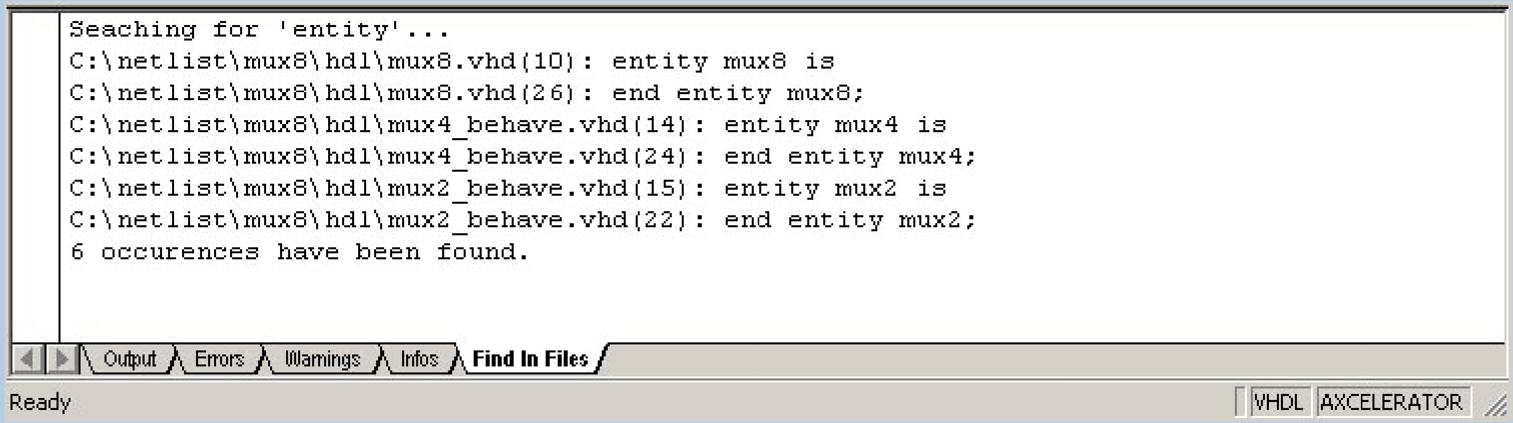
In files/file types: *.vhd; *.v; *.h

In Folder: C:\netlist\pcicore2

□ Match whole word only □ Match Case

□ Regular Expression

- Results Shown in "Find in Files" Tab in Log Window

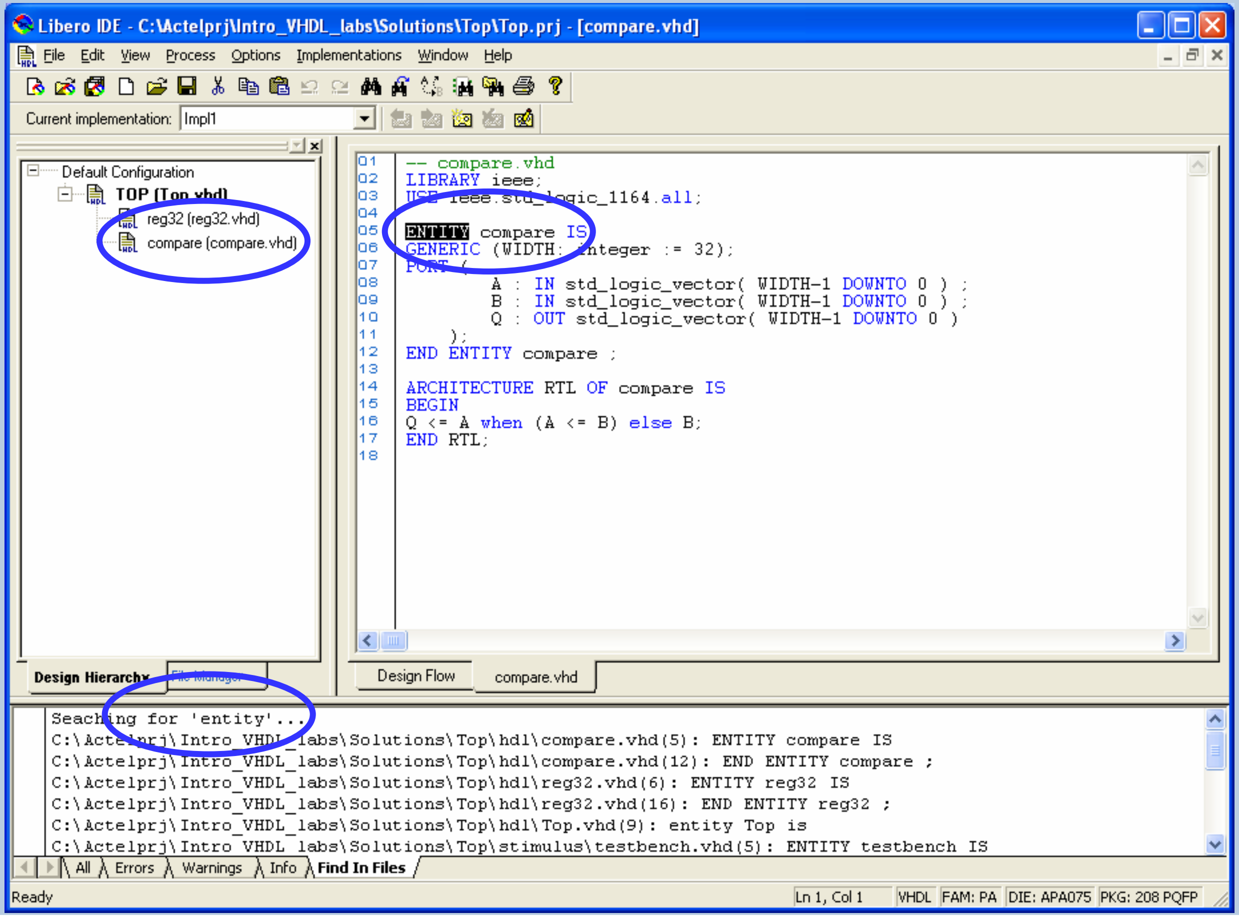


```
Seaching for 'entity'...
C:\netlist\mux8\hdl\mux8.vhd(10): entity mux8 is
C:\netlist\mux8\hdl\mux8.vhd(26): end entity mux8;
C:\netlist\mux8\hdl\mux4_behave.vhd(14): entity mux4 is
C:\netlist\mux8\hdl\mux4_behave.vhd(24): end entity mux4;
C:\netlist\mux8\hdl\mux2_behave.vhd(15): entity mux2 is
C:\netlist\mux8\hdl\mux2_behave.vhd(22): end entity mux2;
6 occurences have been found.
```

# Find in Files

*Cross Probing*

- Selecting File Name Presented in Find in Files Log Window …
  - … Opens Selected File in Libero Text Editor
  - … Highlights Match



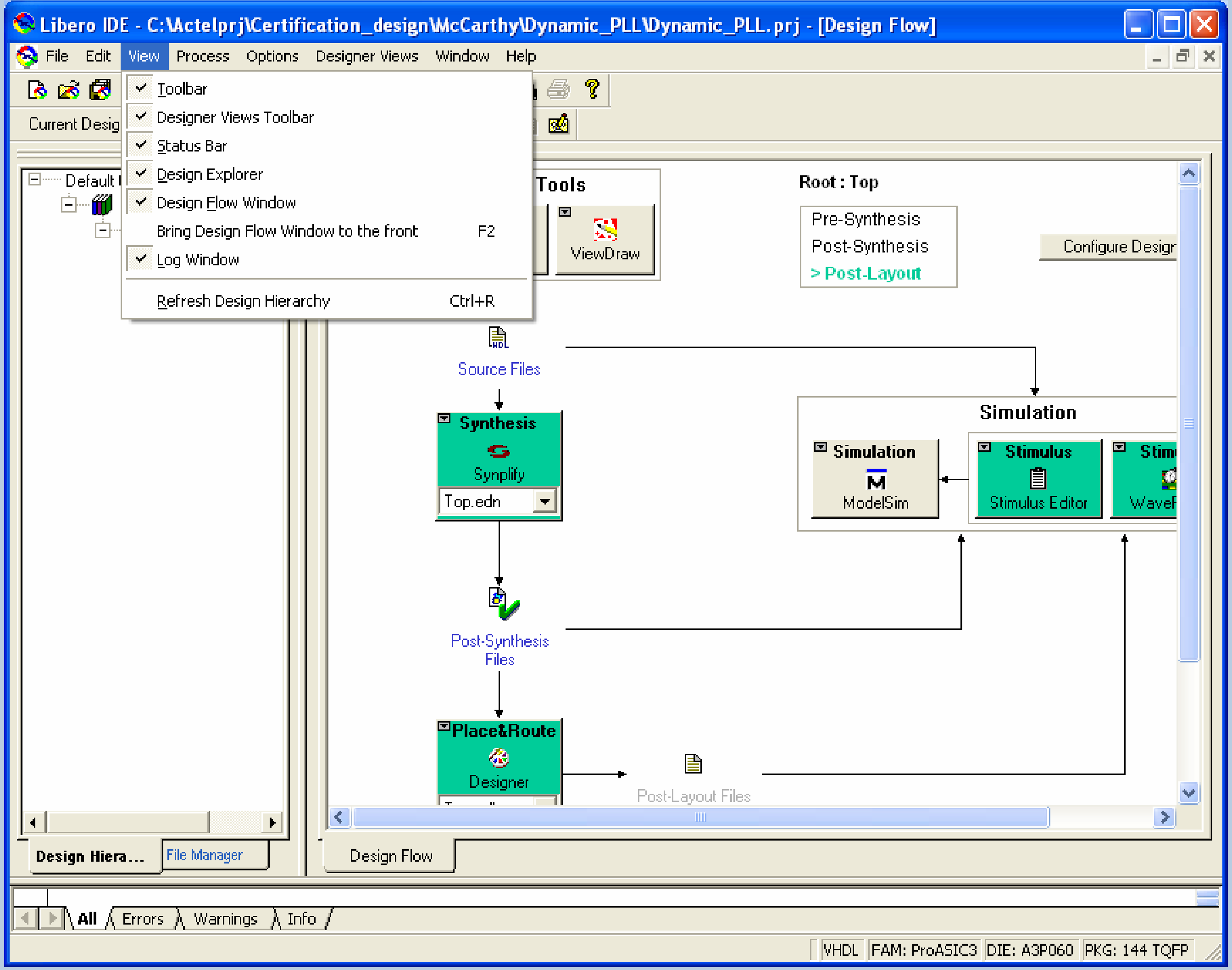
Libero IDE - C:\Actelprj\Intro_VHDL_labs\Solutions\Top\Top.prj - [compare.vhd]
File Edit View Process Options Implementations Window Help
Current implementation: Impl1
Default Configuration
TOP (Top.vhd)
reg32 (reg32.vhd)
compare (compare.vhd)
Design Hierarchy
File Manager
Design Flow
compare.vhd
All Errors Warnings Info Find In Files
Ready
Ln 1, Col 1
VHDL
FAM: PA
DIE: APA075
PKG: 208 PQFP

```
-- compare.vhd
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY compare IS
GENERIC (WIDTH: integer := 32);
PORT (
          A  :  IN std_logic_vector( WIDTH-1 DOWNTO 0 ) ;
          B  :  IN std_logic_vector( WIDTH-1 DOWNTO 0 ) ;
          Q  :  OUT std_logic_vector( WIDTH-1 DOWNTO 0 )
     );
END ENTITY compare ;

ARCHITECTURE RTL OF compare IS
BEGIN
Q <= A when (A <= B) else B;
END RTL;
```

```
Seaching for 'entity'...
C:\Actelprj\Intro_VHDL_labs\Solutions\Top\hdl\compare.vhd(5): ENTITY compare IS
C:\Actelprj\Intro_VHDL_labs\Solutions\Top\hdl\compare.vhd(12): END ENTITY compare ;
C:\Actelprj\Intro_VHDL_labs\Solutions\Top\hdl\reg32.vhd(6): ENTITY reg32 IS
C:\Actelprj\Intro_VHDL_labs\Solutions\Top\hdl\reg32.vhd(16): END ENTITY reg32 ;
C:\Actelprj\Intro_VHDL_labs\Solutions\Top\hdl\Top.vhd(9): entity Top is
C:\Actelprj\Intro_VHDL_labs\Solutions\Top\stimulus\testbench.vhd(5): ENTITY testbench IS
```

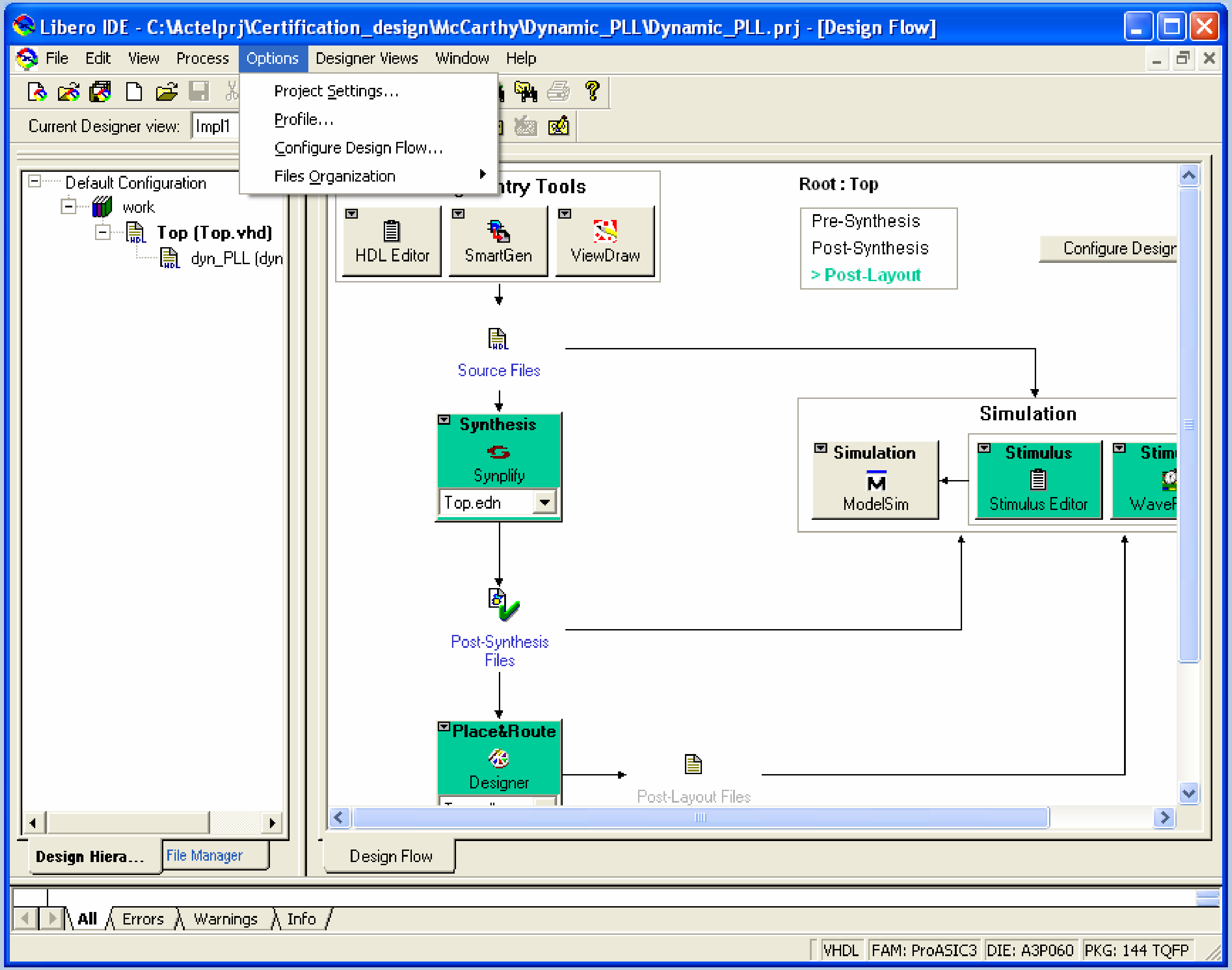
# Libero IDE View Options

- Displayed Windows Turned On or Off Using Libero “View” Menu



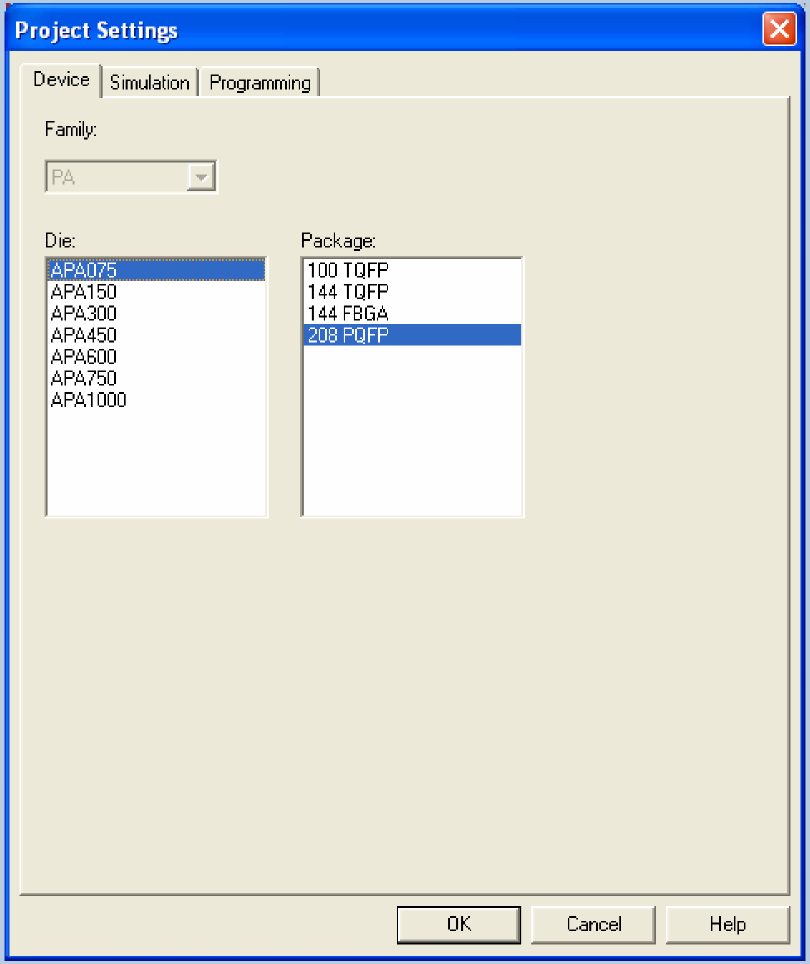
Libero IDE - C:\Actelprj\Certification_design\McCarthy\Dynamic_PLL\Dynamic_PLL.prj - [Design Flow]

# Libero IDE Options Menu



# Libero IDE Project Settings

- Device - change FPGA die or package
  - **Family cannot be changed**



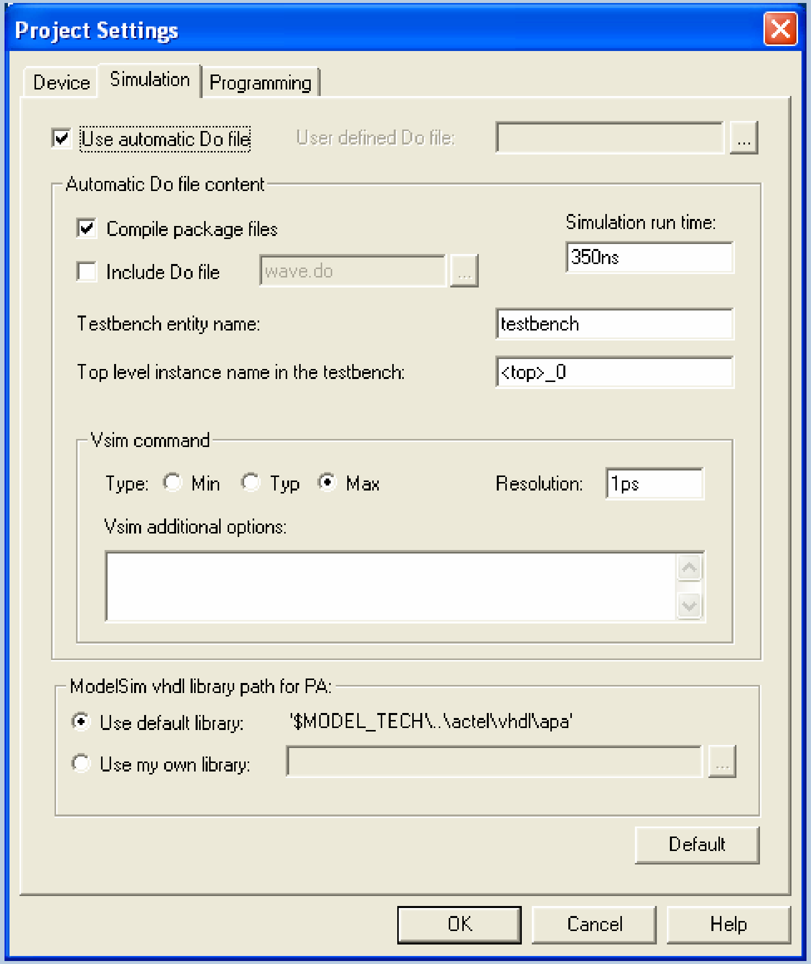
Family: PA

Die:
APA075
APA150
APA300
APA450
APA600
APA750
APA1000

Package:
100 TQFP
144 TQFP
144 FBGA
208 PQFP

# Libero IDE Project Settings

- Device - change FPGA die or package
  - **Family cannot be changed**
- Simulation – specify simulation options
  - **“Compile VHDL Package Files” option is on by default**



☑ Use automatic Do file

User defined Do file:

Automatic Do file content

☑ Compile package files

☐ Include Do file: wave.do

Simulation run time: 350ns

Testbench entity name: testbench

Top level instance name in the testbench: <top>_0

Vsim command

Type: ○ Min ○ Typ ● Max

Resolution: 1ps

Vsim additional options:

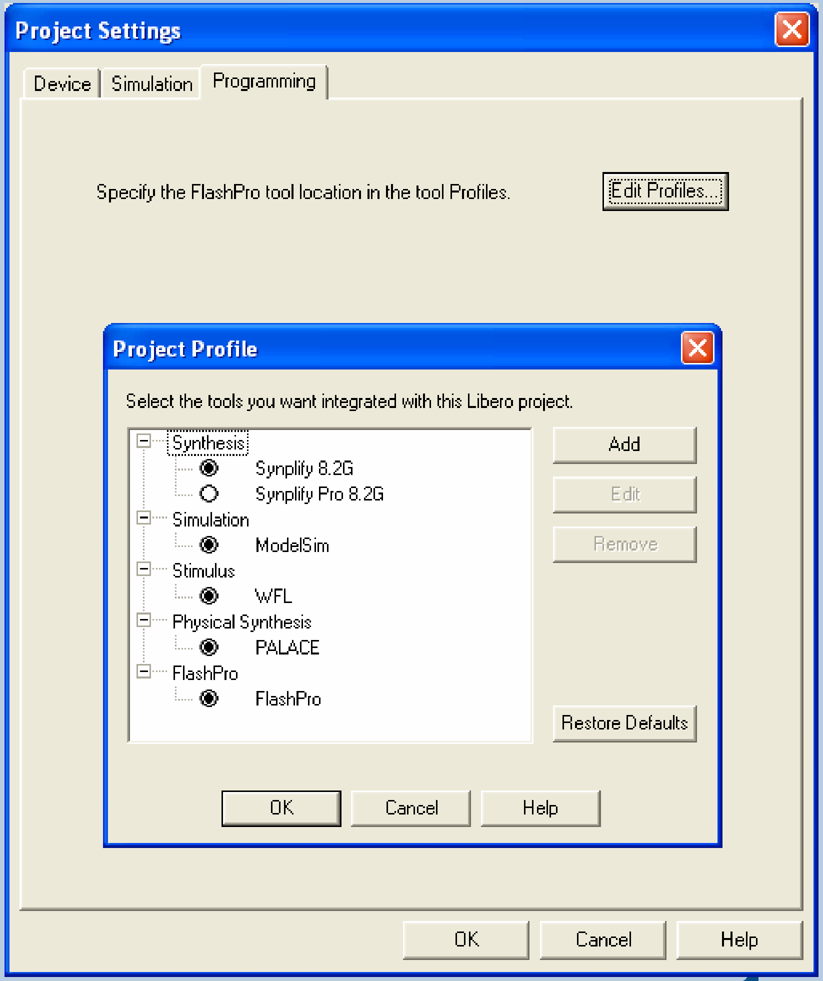
ModelSim vhdl library path for PA:

● Use default library: '$MODEL_TECH\..\actel\vhdl\apa'

○ Use my own library:

# Libero IDE Project Settings

- Device - change FPGA die or package
  - **Family cannot be changed**
- Simulation – specify simulation options
  - **“Compile VHDL Package Files” option is on by default**
- Programming – specify location of programming file and software



Project Settings

Specify the FlashPro tool location in the tool Profiles.

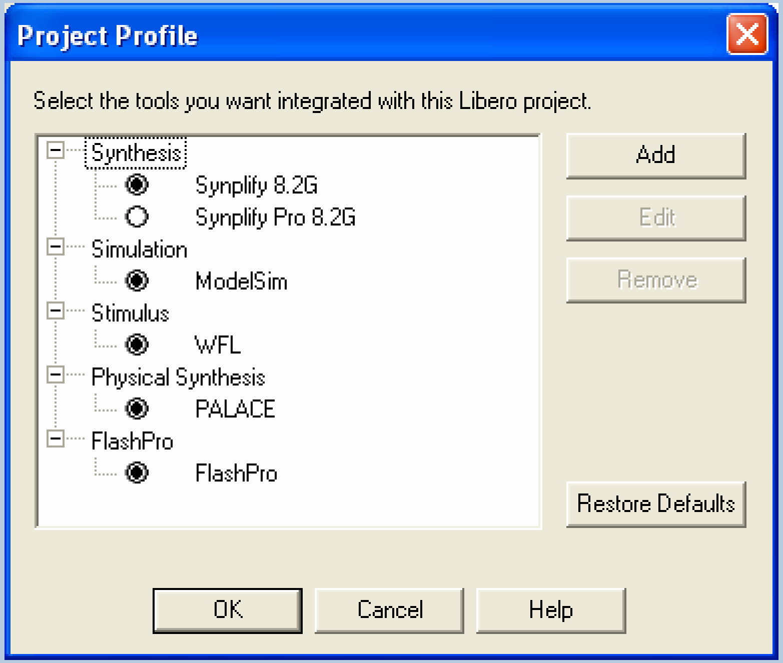
Project Profile

Select the tools you want integrated with this Libero project.

- Synthesis
  - ● Synplify 8.2G
  - ○ Synplify Pro 8.2G
- Simulation
  - ● ModelSim
- Stimulus
  - ● WFL
- Physical Synthesis
  - ● PALACE
- FlashPro
  - ● FlashPro

# OEM Tools Support
## *Tool Profiles*

- Create or Edit Tool Profile for Project
  - Options > Profiles
  - Select Third-Party Tools & Versions
    - Synthesis
      - *Vendor (e.g. Synplify)*
        - *Version*
    - Physical Synthesis
      - *PALACE*
        - *Version*
    - Simulation
      - *ModelSim*
        - *Select Version*
    - Testbench Generation
      - *WaveFormer Lite*
        - *Select Version*
  - Name Profile and Save
  - Edit or Add Profiles As Needed


Project Profile

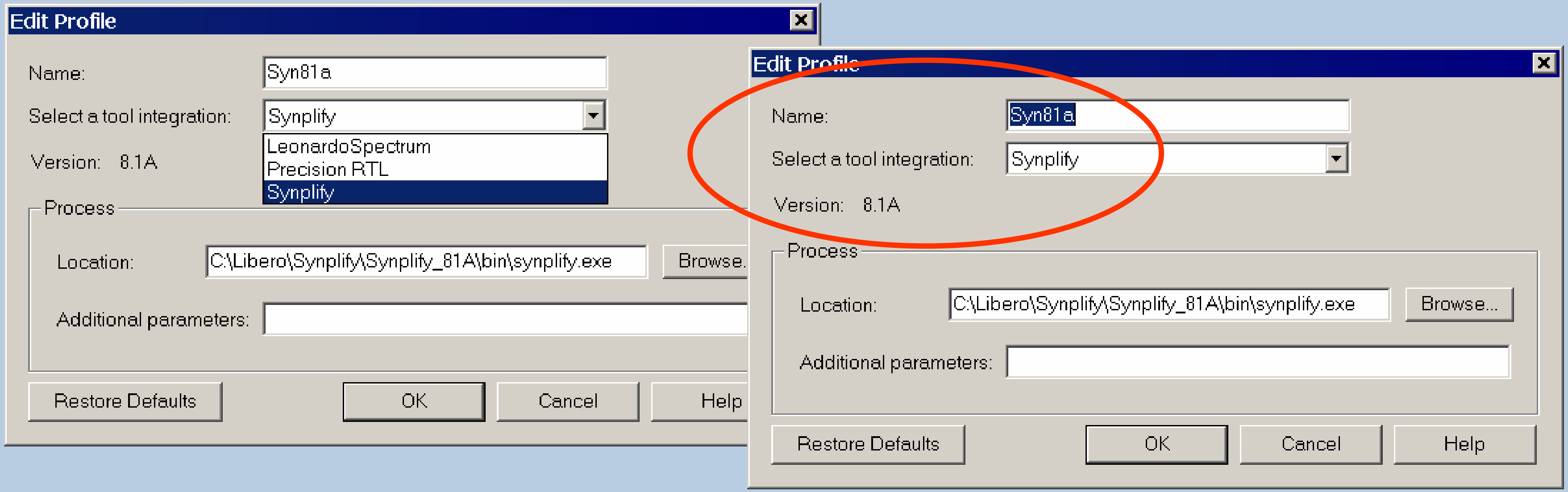
Select the tools you want integrated with this Libero project.

- Synthesis
  - ● Synplify 8.2G
  - ○ Synplify Pro 8.2G
- Simulation
  - ● ModelSim
- Stimulus
  - ● WFL
- Physical Synthesis
  - ● PALACE
- FlashPro
  - ● FlashPro

# OEM Tools Support
*Tool Versions*

## Tool Profiles

- **Now Automatically Finds Versions of Installed Tools**



Edit Profile

Name: Syn81a

Select a tool integration: Synplify

LeonardoSpectrum
Precision RTL
Synplify

Version: 8.1A

Process

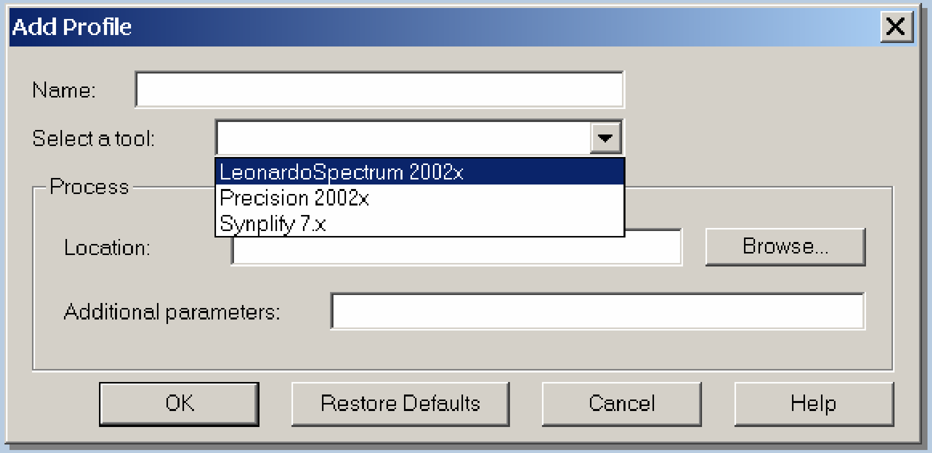
Location: C:\Libero\Synplify\Synplify_81A\bin\synplify.exe

Additional parameters:

- **Export/import Profiles**
  - **Allows saving & moving profiles to another project**
  - **Setting up a new project allows import from another project**

# Add / Edit Tool Profiles

- Add/Edit Profile Requires
  - **… Name of Profile**
  - **… Choosing Tool**
    - **From Drop-down Menu**
    - **Choose Version**
  - **… Choosing Tool Location**
    - **Browse for Location**
    - **Specify Location**



Add Profile

Name:

Select a tool:

LeonardoSpectrum 2002x

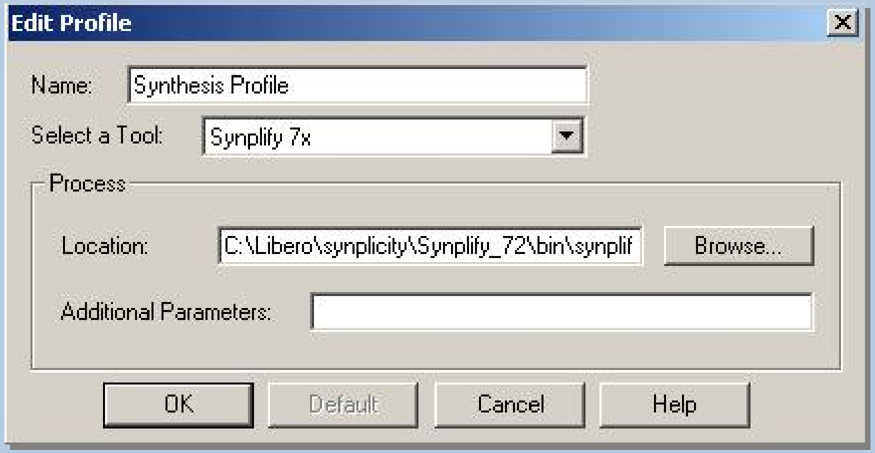
Precision 2002x

Synplify 7.x

Process

Location:

Additional parameters:



Edit Profile

Name: Synthesis Profile

Select a Tool: Synplify 7x

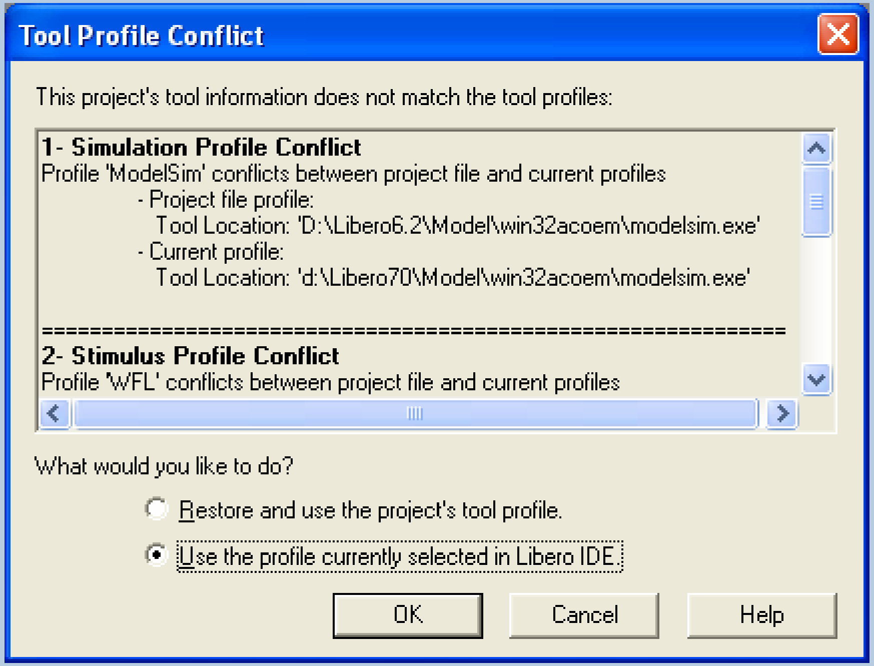
Process

Location: C:\Libero\synplicity\Synplify_72\bin\synplif

Additional Parameters:

# Profile Conflict

- Occurs when Current Profile Settings Are Different from those of Previous Project that is Opened
  - **May Have Newer Version Selected when Opening Project Created with an Older Version**



Tool Profile Conflict

This project's tool information does not match the tool profiles:

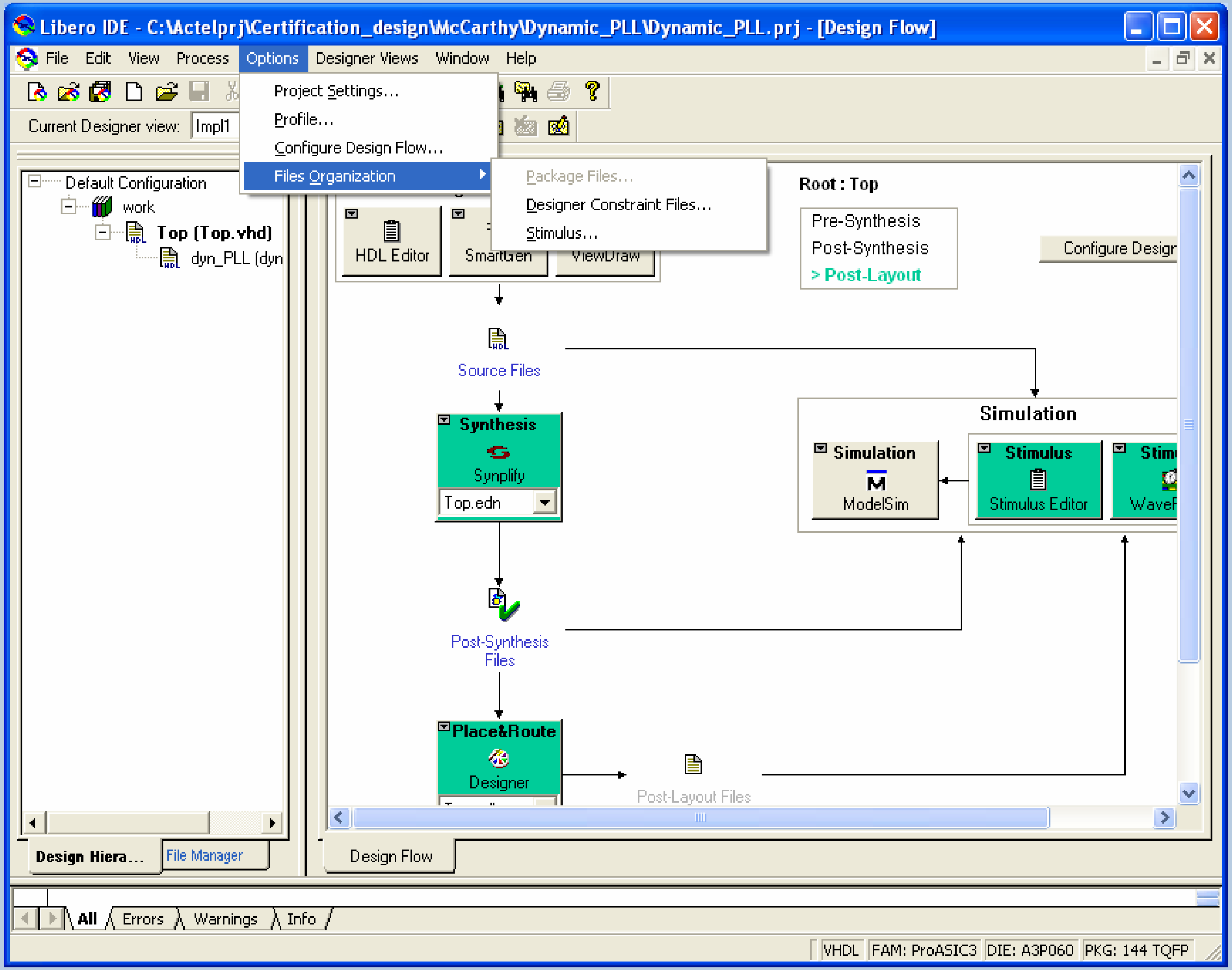
```
1- Simulation Profile Conflict
Profile 'ModelSim' conflicts between project file and current profiles
        - Project file profile:
          Tool Location: 'D:\Libero6.2\Model\win32acoem\modelsim.exe'
        - Current profile:
          Tool Location: 'd:\Libero70\Model\win32acoem\modelsim.exe'

=====================================================================
2- Stimulus Profile Conflict
Profile 'WFL' conflicts between project file and current profiles
```

What would you like to do?

○ Restore and use the project's tool profile.

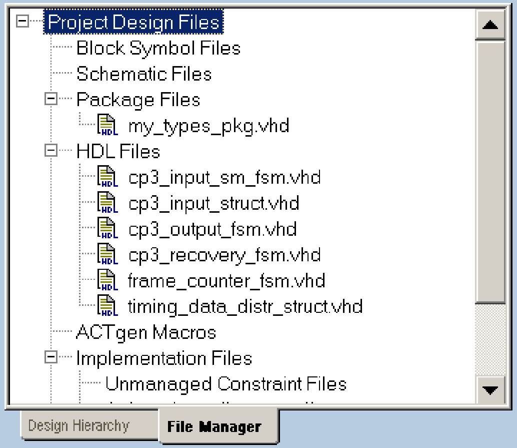
● Use the profile currently selected in Libero IDE.

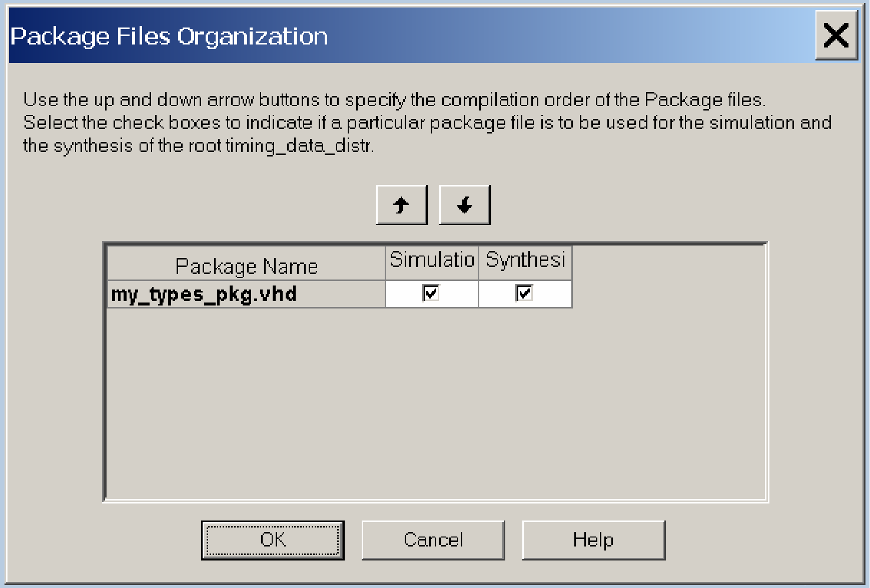
# Libero IDE Files Organization



# Package Files
## *Compile Order*

- Package Files Displayed on Libero IDE File Manager Tab
  - **VHDL Packages**
  - **Verilog Include Files**
- Use Package Files Order Window to Indicate if Packages Are for Simulation, Synthesis or Both and to Set Compile Order
  - **Use Up or Down Arrows to Change Compile Order**
  - **Check Boxes to Compile Packages for Simulation, Synthesis, or Both**
- Select Options => Package Files Organization, or Right Click in Design Hierarchy Window





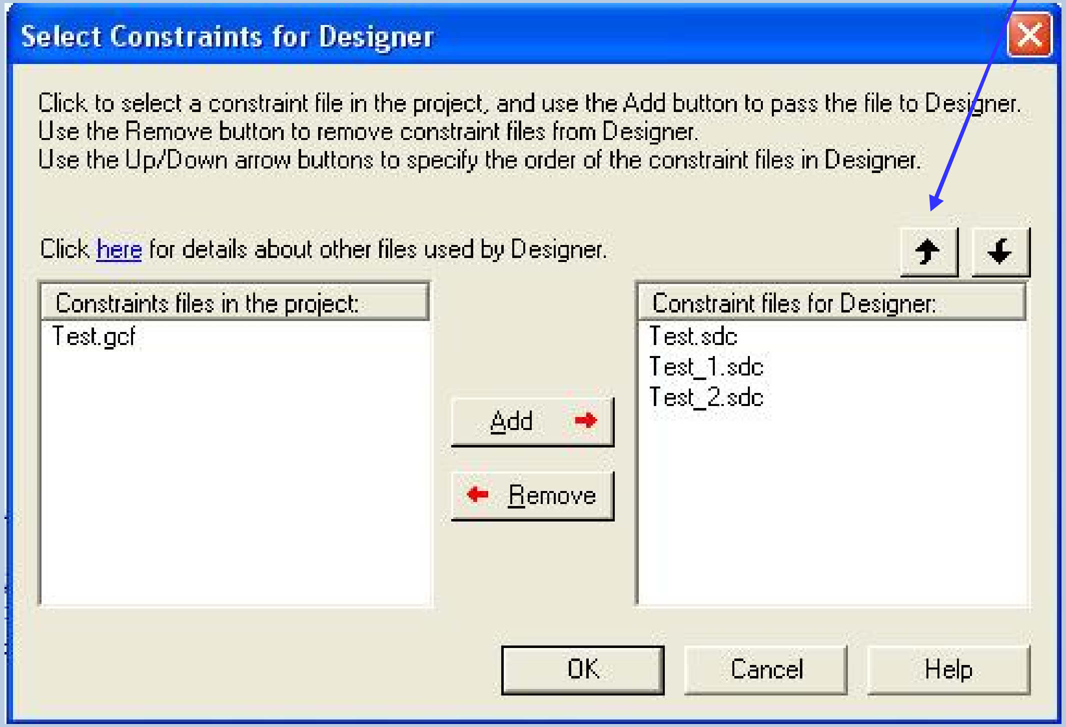
Use the up and down arrow buttons to specify the compilation order of the Package files. Select the check boxes to indicate if a particular package file is to be used for the simulation and the synthesis of the root timing_data_distr.

| Package Name | Simulatio | Synthesi |
|---|---|---|
| my_types_pkg.vhd | ☑ | ☑ |

# Libero Project Manager
## *Designer Constraint Files*

- User Can Specify Constraint Files To Send To Designer
  - **Timing Constraints (.sdc) or Physical Constraints (.pdc)**
    - **Files may come from Synthesis or PALACE or be generated by the engineer**

Specify order which files are imported



Select Constraints for Designer

Click to select a constraint file in the project, and use the Add button to pass the file to Designer.
Use the Remove button to remove constraint files from Designer.
Use the Up/Down arrow buttons to specify the order of the constraint files in Designer.

Click here for details about other files used by Designer.

| Constraints files in the project: |
|---|
| Test.gcf |

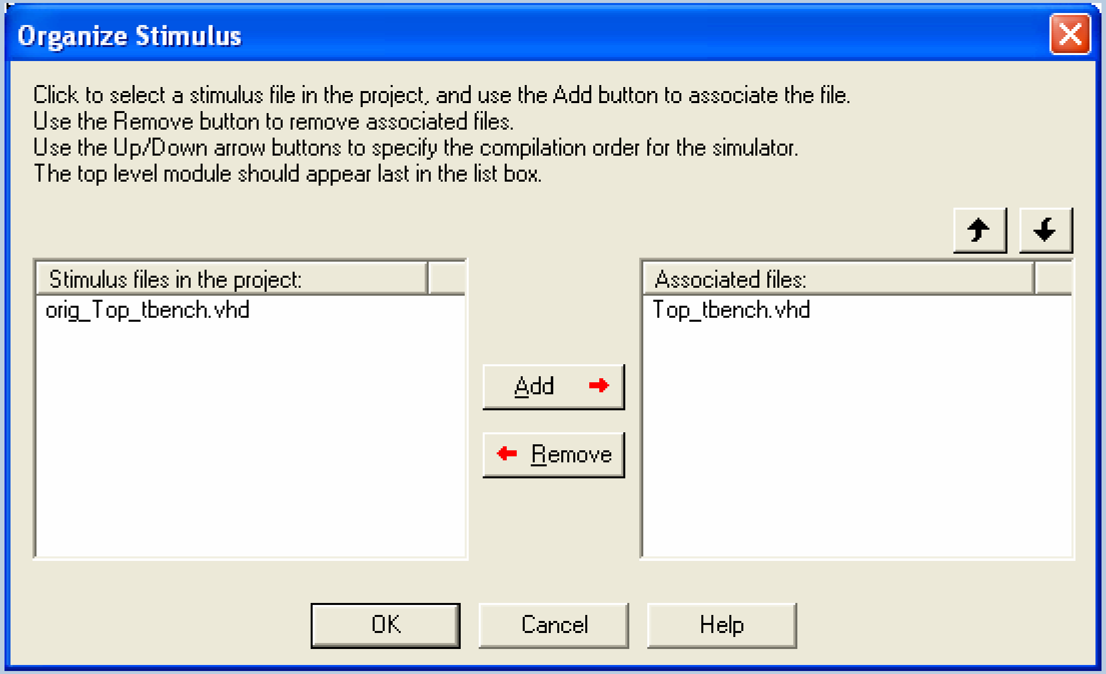
| Constraint files for Designer: |
|---|
| Test.sdc |
| Test_1.sdc |
| Test_2.sdc |

Constraint files in project

Constraint files sent to Designer

# Libero Project Manager
*Stimulus Files*

- Libero Allows Users to Specify List of Stimulus Files for Simulation
  - **No Stimulus File Selected by Default**
  - **Libero Remembers Stimulus Association for Any Block**



Organize Stimulus

Click to select a stimulus file in the project, and use the Add button to associate the file.
Use the Remove button to remove associated files.
Use the Up/Down arrow buttons to specify the compilation order for the simulator.
The top level module should appear last in the list box.

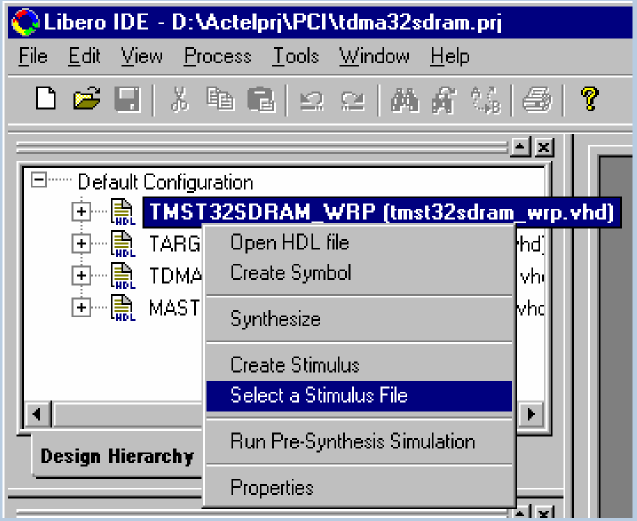
| Stimulus files in the project: |
|---|
| orig_Top_tbench.vhd |

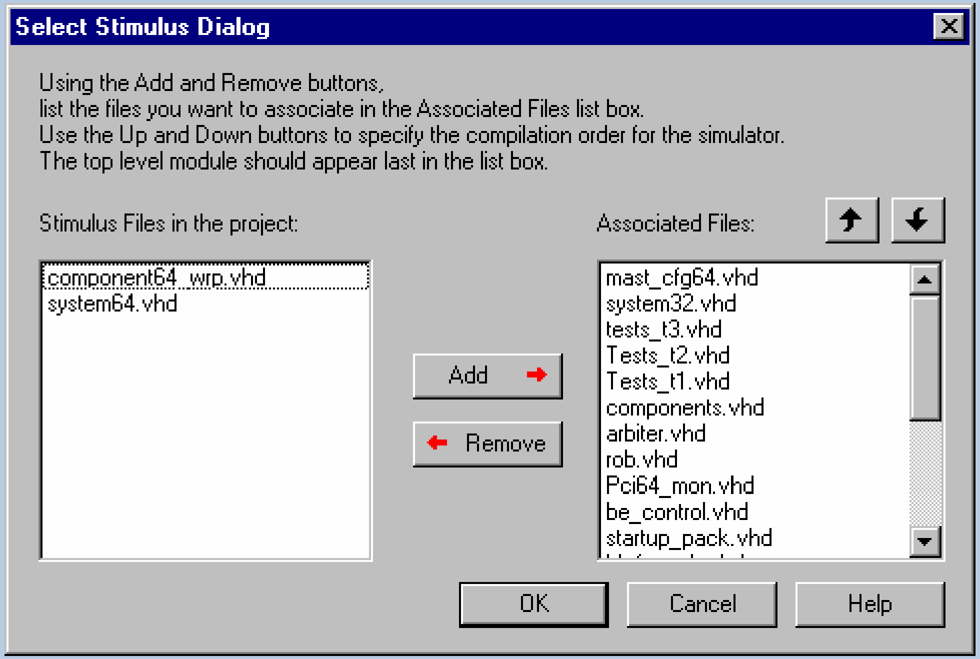
| Associated files: |
|---|
| Top_tbench.vhd |

# Hierarchical Testbench Support

## Libero Supports Hierarchical Testbenches

- **Select Multiple Files**
- **Libero does not automatically determine compile dependencies of stimulus files**


Libero IDE - D:\Actelprj\PCI\tdma32sdram.prj
File Edit View Process Tools Window Help
Default Configuration
TMST32SDRAM_WRP (tmst32sdram_wrp.vhd)
TARG
TDMA
MAST
Open HDL file
Create Symbol
Synthesize
Create Stimulus
Select a Stimulus File
Run Pre-Synthesis Simulation
Properties
Design Hierarchy



Using the Add and Remove buttons,
list the files you want to associate in the Associated Files list box.
Use the Up and Down buttons to specify the compilation order for the simulator.
The top level module should appear last in the list box.

Stimulus Files in the project:

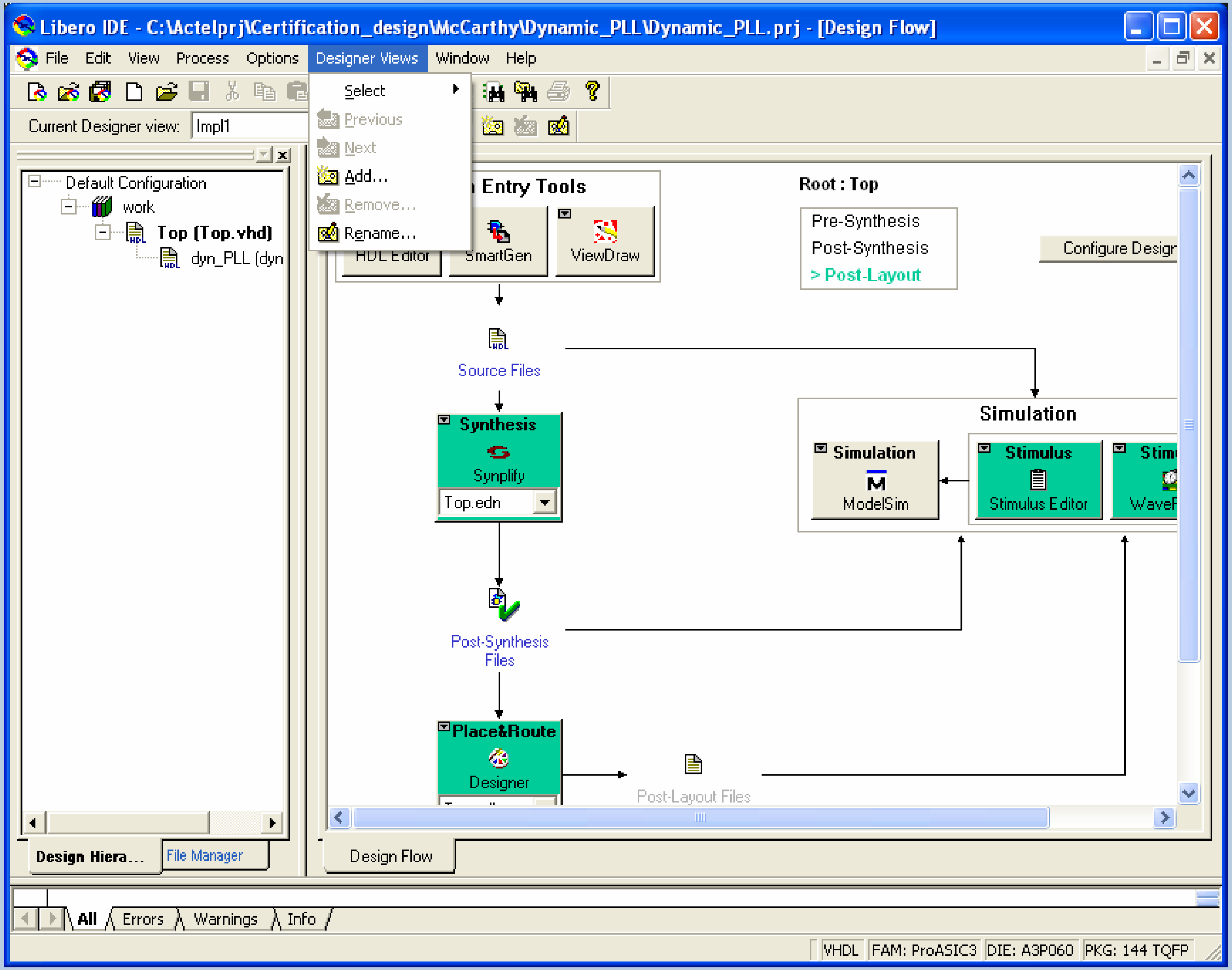
component64_wrp.vhd
system64.vhd

Associated Files:

mast_cfg64.vhd
system32.vhd
tests_t3.vhd
Tests_t2.vhd
Tests_t1.vhd
components.vhd
arbiter.vhd
rob.vhd
Pci64_mon.vhd
be_control.vhd
startup_pack.vhd

# Libero IDE

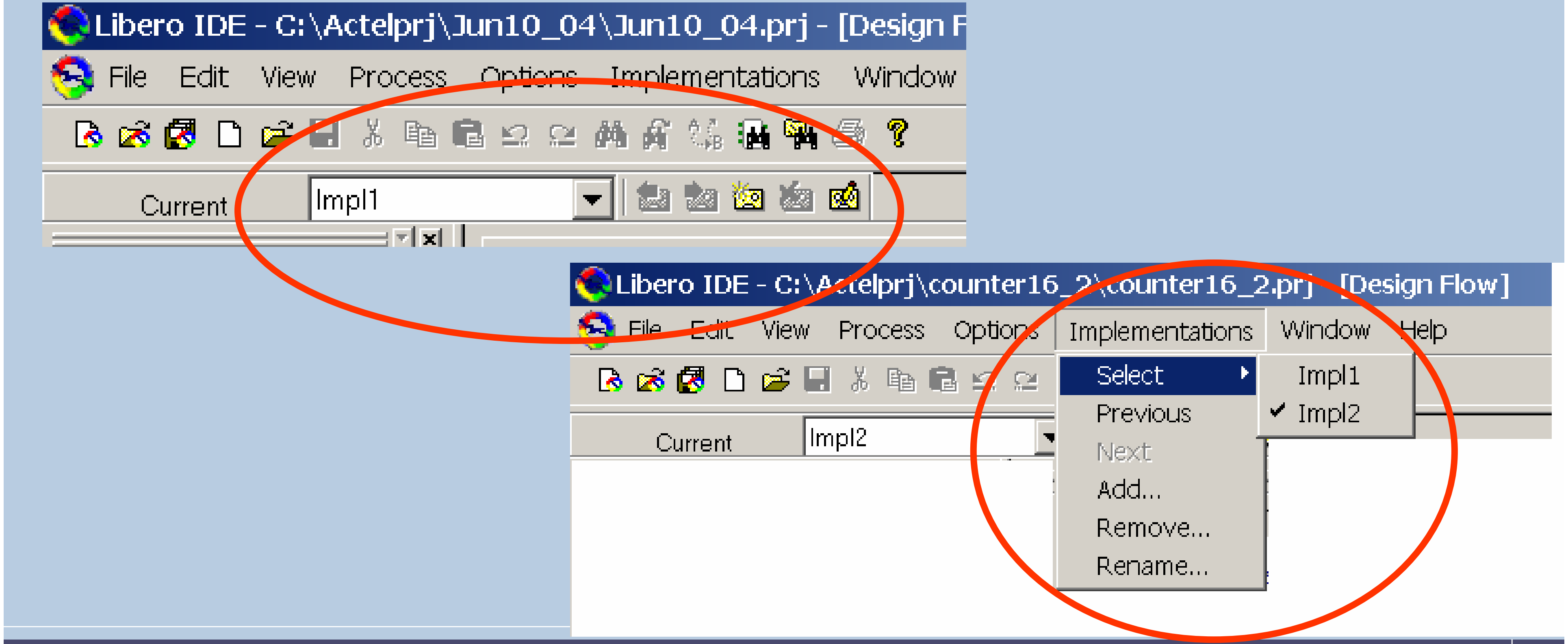
## *Designer Views Menu*



# Libero Project Manager
*Design Implementations*

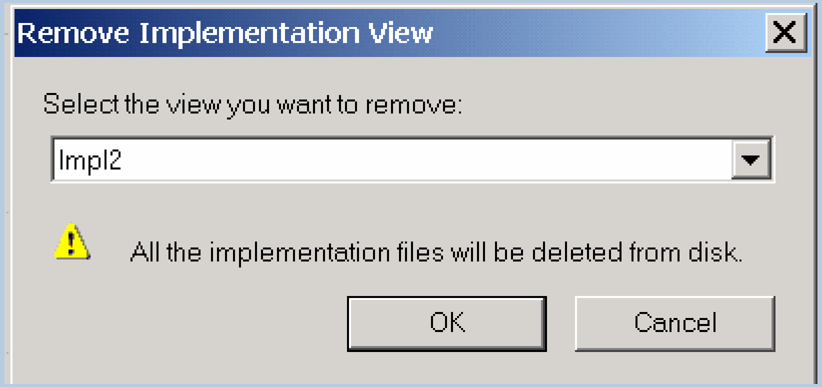
## Create Project Variations

- **Save Different Project Views for Comparison**
- **Requires .adb file, Back-annotated File, Programming/Debugging File, or Post-layout Simulation Folder**


Libero IDE - C:\Actelprj\Jun10_04\Jun10_04.prj - [Design F
File Edit View Process Options Implementations Window
Current
Impl1
Libero IDE - C:\Actelprj\counter16_2\counter16_2.prj - [Design Flow]
File Edit View Process Options Implementations Window Help
Current
Impl2
Select
Previous
Next
Add...
Remove...
Rename...
Impl1
✓ Impl2

# Libero Project Manager
*Design Implementations*

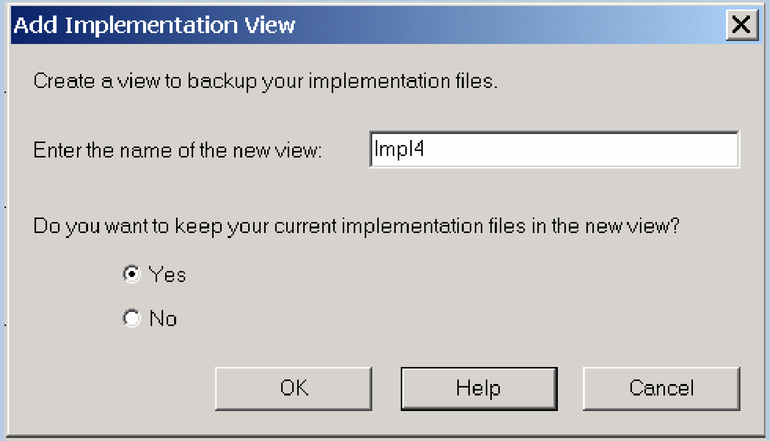
- Add, Rename or remove design implementations



Select the view you want to remove:

Impl2

⚠ All the implementation files will be deleted from disk.



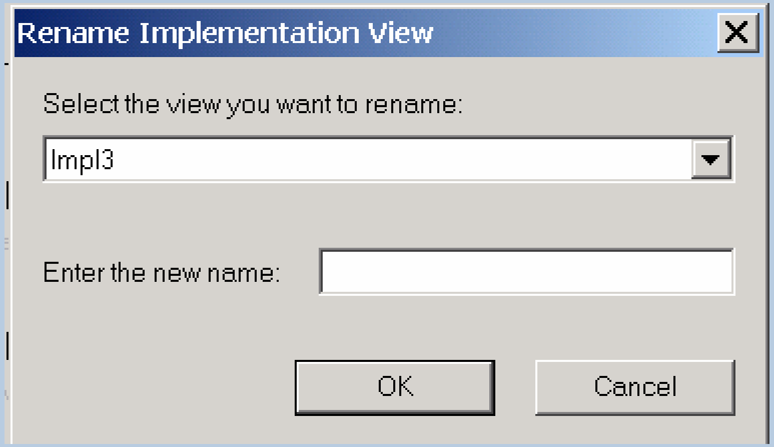
Create a view to backup your implementation files.

Enter the name of the new view: Impl4

Do you want to keep your current implementation files in the new view?

● Yes

○ No



Select the view you want to rename:

Impl3

Enter the new name:

# Libero Project Manager
*Design Implementations*

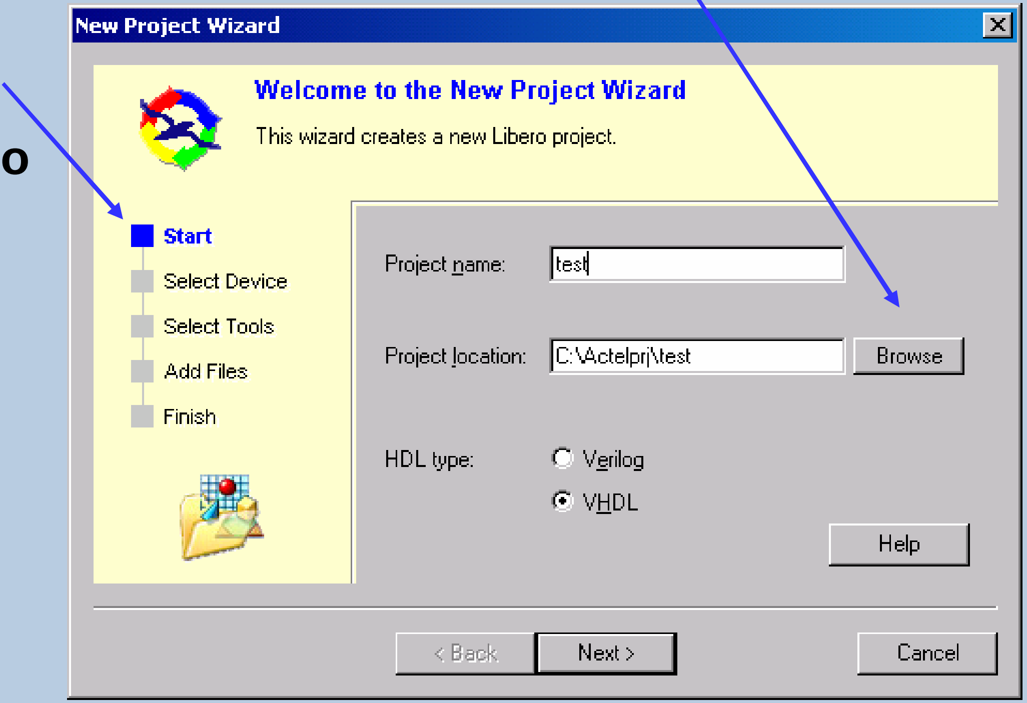
## Implementations

- **Making Changes in Current View Can Change State of Project**
  - **Pre-Synthesis**
  - **Post-Synthesis**
  - **Post-Physical Synthesis**
  - **Affects All Other Views**
- **Changing Implementation Files for Current View Does Not Affect Other Views**

# Libero IDE New Project Wizard

- Menu-Driven Wizard
  - **File > New Project**
- Status Guide Shows Current State
  - **All Fields Must Be Filled in to Continue**
- HDL Type Must Be Consistent with License
- Next Button Goes to Next Wizard Screen
- Finish Button Finishes/Closes Wizard after Making Changes. Saves All Selections.

Use Browse button to change project location



New Project Wizard

**Welcome to the New Project Wizard**

This wizard creates a new Libero project.

Project name: test

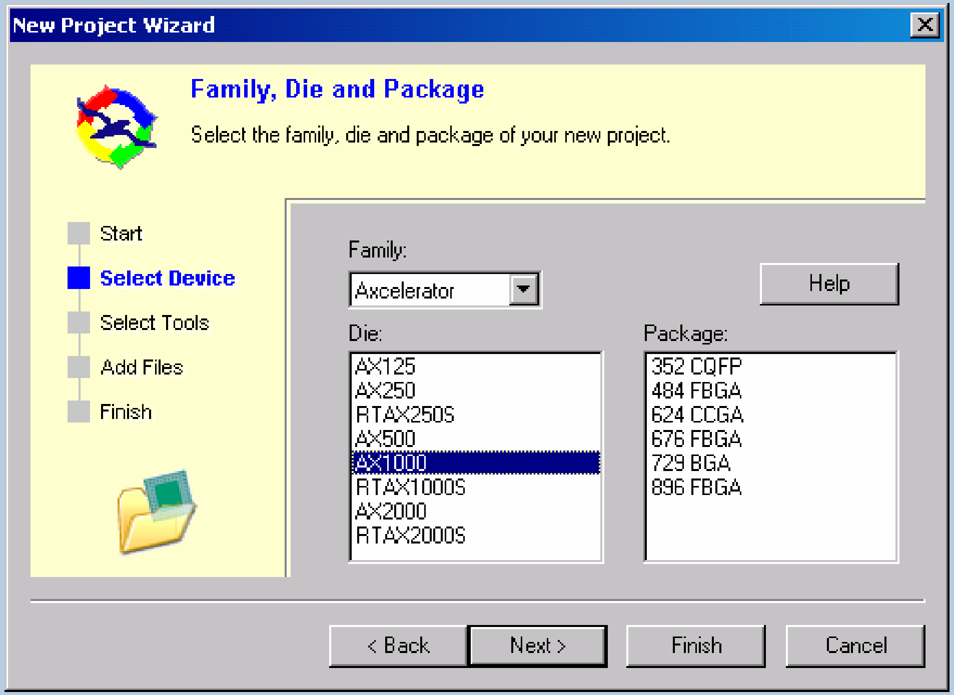
Project location: C:\Actelprj\test

HDL type: ○ Verilog ● VHDL

# Libero IDE New Project Wizard

## *Select Device*

- Select Family
- After Family Is Selected, Devices from that Family Are Displayed
- After Device Is Selected, Available Packages for that Device Are Displayed



New Project Wizard

**Family, Die and Package**

Select the family, die and package of your new project.

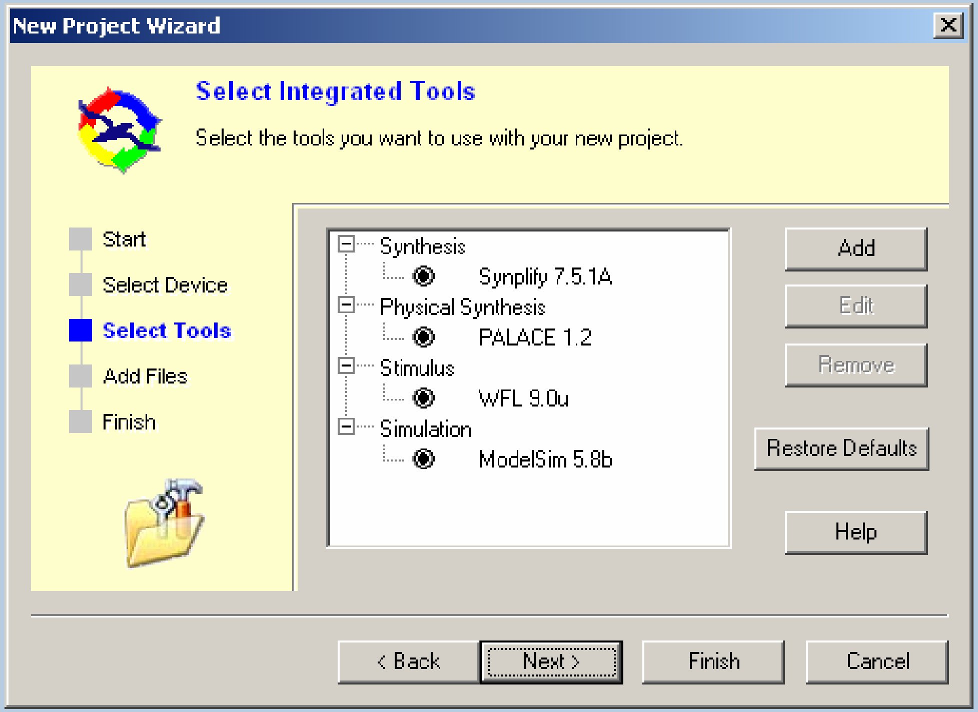
Family: Axcelerator

Die:
AX125
AX250
RTAX250S
AX500
AX1000
RTAX1000S
AX2000
RTAX2000S

Package:
352 CQFP
484 FBGA
624 CCGA
676 FBGA
729 BGA
896 FBGA

# Libero IDE New Project Wizard
## *Select Tools*

- **Synthesis**
  - **Vendor (e.g. Synplify)**
    - **Version**
- **Physical Synthesis**
  - **PALACE**
    - **Version**
- **Testbench Generation**
  - **WaveFormer Lite**
    - **Select Version**
- **Simulation**
  - **ModelSim**
    - **Select Version**
- **Support for Mentor Graphic's LeonardoSpectrum and Precision**
  - **Standard Tools Direct from Mentor**
    - **No Actel OEM Versions**


New Project Wizard

Select Integrated Tools

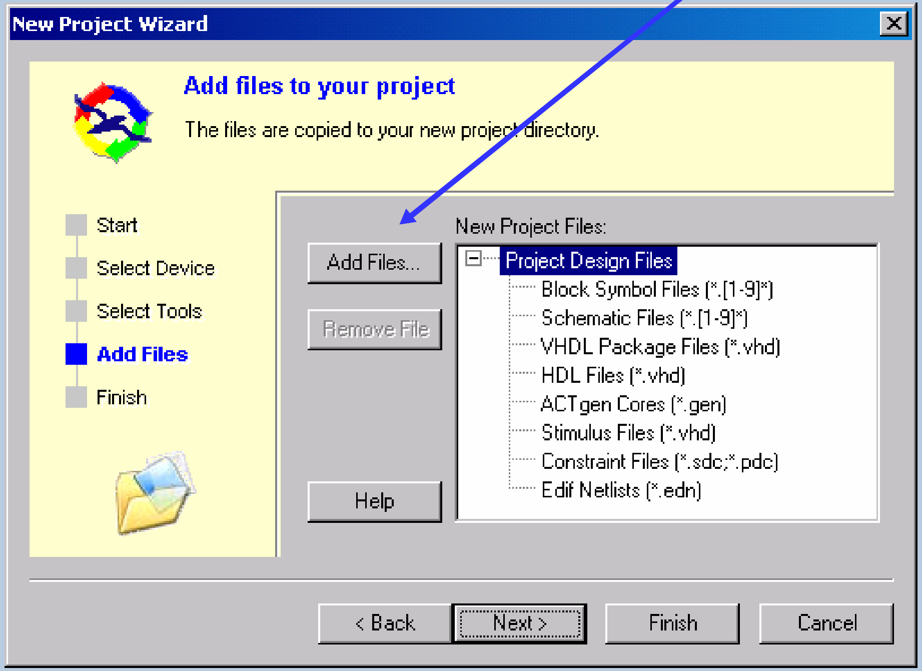
Select the tools you want to use with your new project.

- Synthesis
  - Synplify 7.5.1A
- Physical Synthesis
  - PALACE 1.2
- Stimulus
  - WFL 9.0u
- Simulation
  - ModelSim 5.8b

# Libero IDE New Project Wizard
## *Add Files*

## Add Existing Design Files to Project

- **Schematics, Symbols, HDL (VHDL or Verilog), Stimulus (VHDL or Verilog), SmartGen Macros or EDIF Netlists**



**Add files to your project**

The files are copied to your new project directory.

New Project Files:

- Project Design Files
  - Block Symbol Files (*.[1-9]*)
  - Schematic Files (*.[1-9]*)
  - VHDL Package Files (*.vhd)
  - HDL Files (*.vhd)
  - ACTgen Cores (*.gen)
  - Stimulus Files (*.vhd)
  - Constraint Files (*.sdc;*.pdc)
  - Edif Netlists (*.edn)

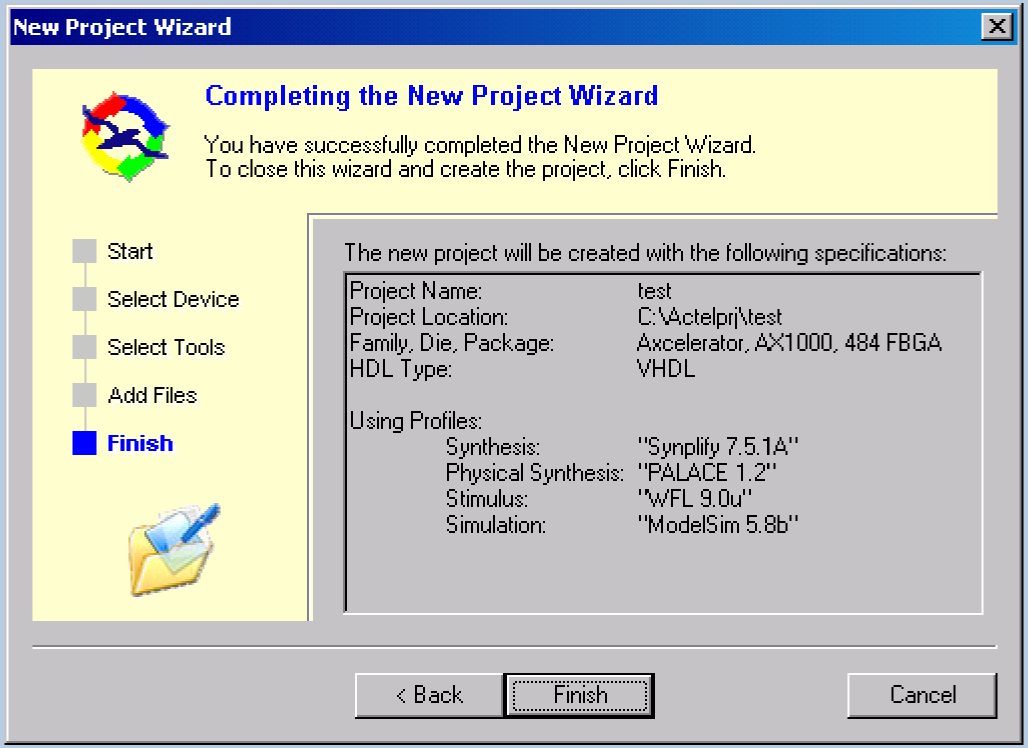
Browse to file location

Select file type

# Libero IDE New Project Wizard
*Finish*

## Project Information Listed in Dialog Box

- **Click "Finish" to Complete Project Creation or "Back" to Make Corrections or Additions**



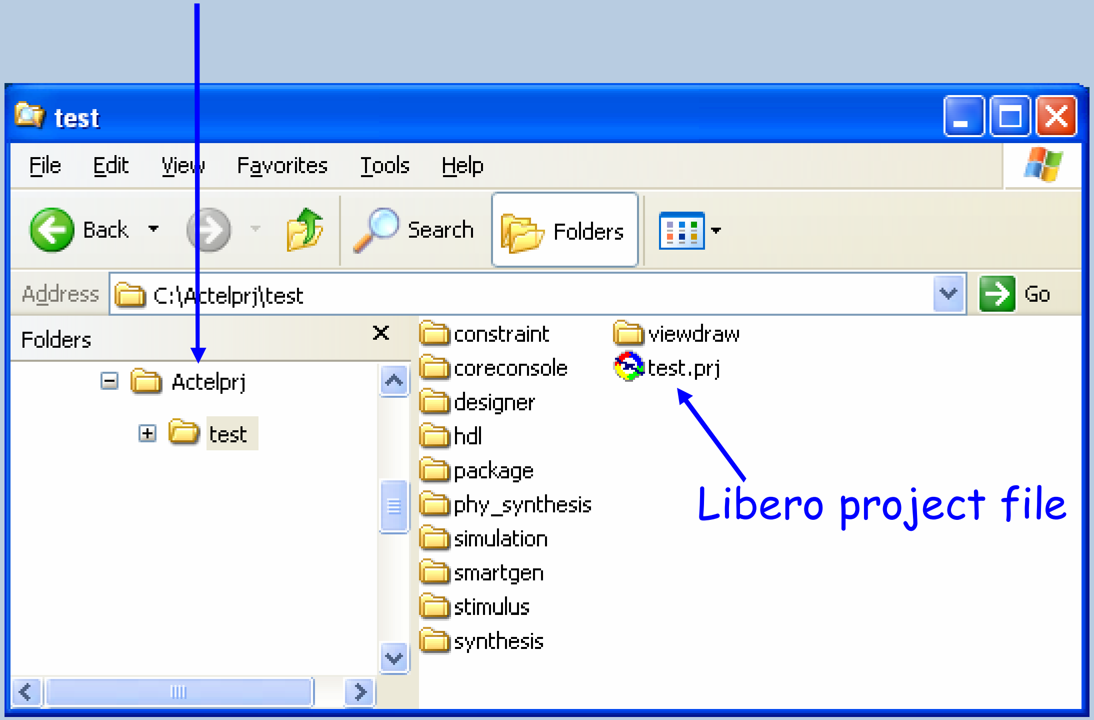
You have successfully completed the New Project Wizard.
To close this wizard and create the project, click Finish.

The new project will be created with the following specifications:

```
Project Name:            test
Project Location:        C:\Actelprj\test
Family, Die, Package:    Axcelerator, AX1000, 484 FBGA
HDL Type:                VHDL

Using Profiles:
        Synthesis:           "Synplify 7.5.1A"
        Physical Synthesis:  "PALACE 1.2"
        Stimulus:            "WFL 9.0u"
        Simulation:          "ModelSim 5.8b"
```

Project summary shown in window

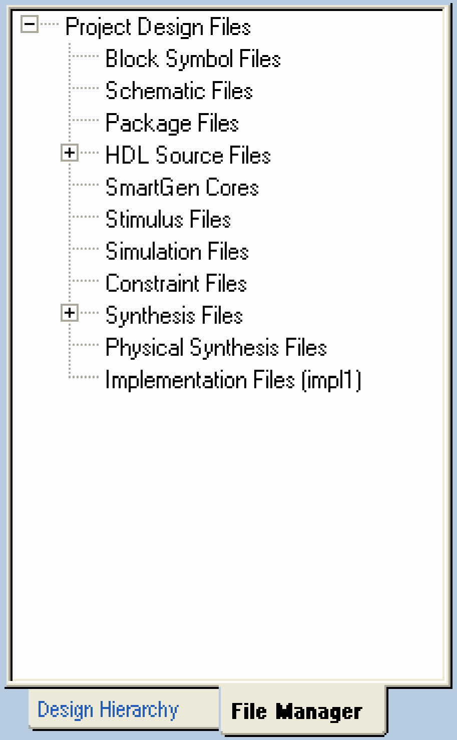
# Organization of Libero Project Files



constraint
coreconsole
designer
hdl
package
phy_synthesis
simulation
smartgen
stimulus
synthesis
viewdraw
test.prj

Default folder for Libero projects

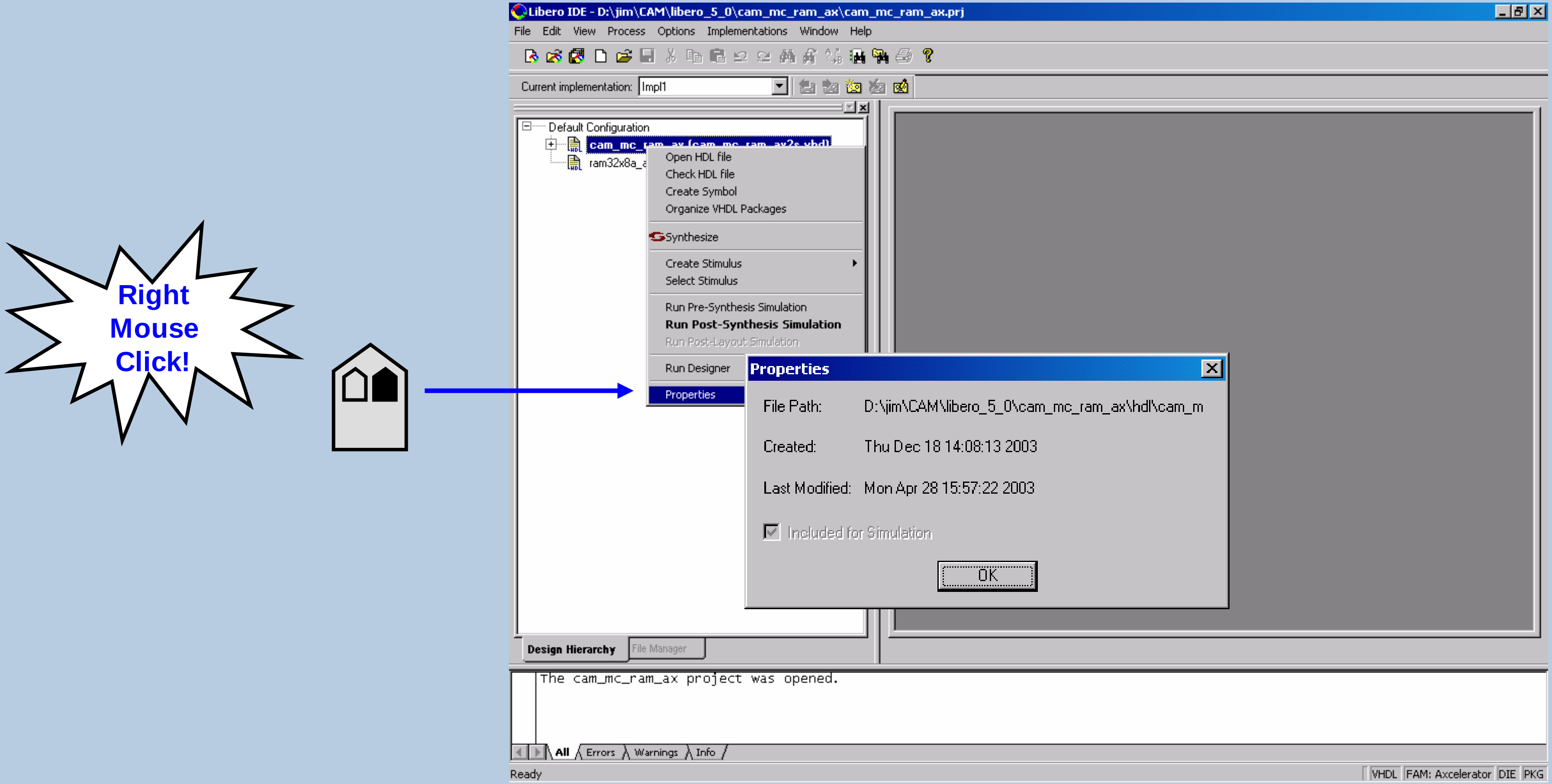
Libero project file



- Project Design Files
  - Block Symbol Files
  - Schematic Files
  - Package Files
  - HDL Source Files
  - SmartGen Cores
  - Stimulus Files
  - Simulation Files
  - Constraint Files
  - Synthesis Files
  - Physical Synthesis Files
  - Implementation Files (impl1)

# Design Hierarchy Tab
## *Block Properties*

- Block Properties Dialog Box Displays File Path, Date Created and Last Modified Date



**Properties**

File Path: D:\jim\CAM\libero_5_0\cam_mc_ram_ax\hdl\cam_m

Created: Thu Dec 18 14:08:13 2003

Last Modified: Mon Apr 28 15:57:22 2003

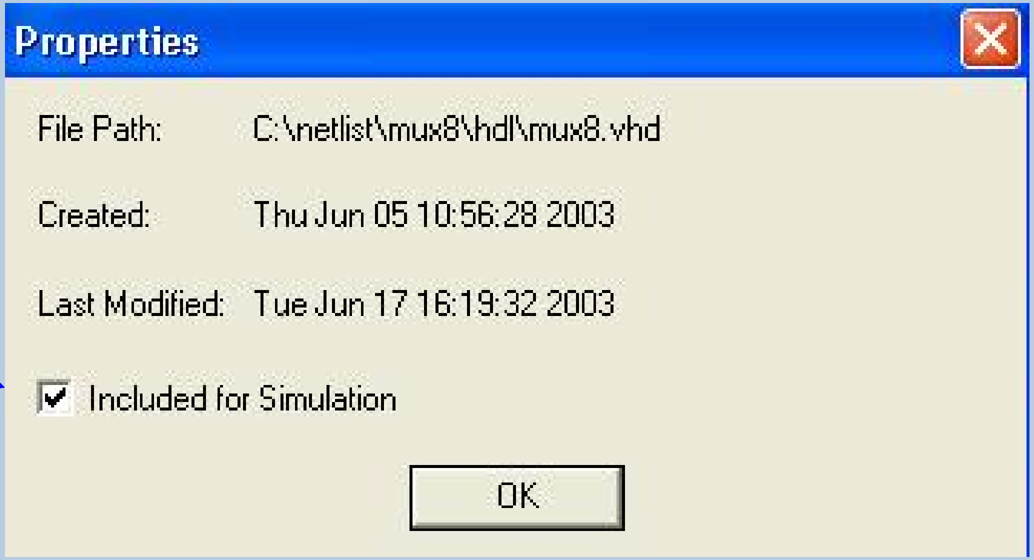
☑ Included for Simulation

OK

```
The cam_mc_ram_ax project was opened.
```

# Libero Project Manager
## *Include Modules for Simulation*

- Libero Only Passes Top-level Source-related Modules to Simulation
- If Other Source Modules Are Required for Simulation, Check Box on File Properties



File Path: C:\netlist\mux8\hdl\mux8.vhd

Created: Thu Jun 05 10:56:28 2003

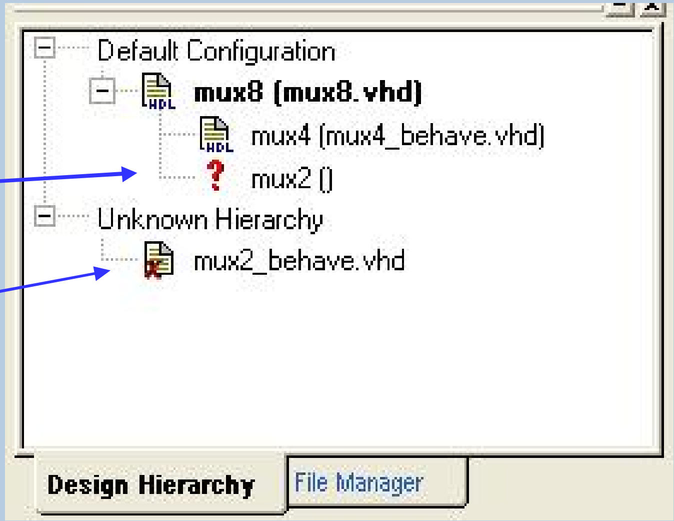
Last Modified: Tue Jun 17 16:19:32 2003

☑ Included for Simulation

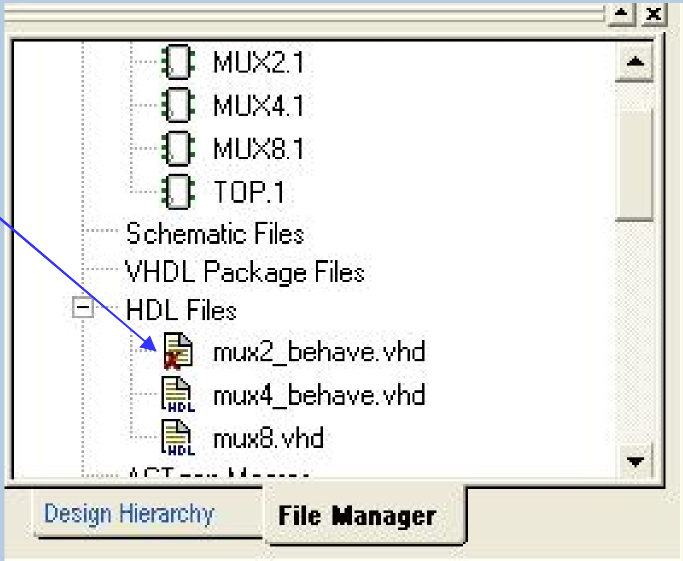
Check to include file in simulation

# Unknown Hierarchy

- Libero Displays Files in “Default Configuration” Tree
- Missing Files Indicated with “?”
- When Libero Cannot Determine Hierarchy, Files Are Shown with “X” under Unknown Hierarchy on Design Hierarchy Tab
  - **Files also Shown with “X” on File Manager Tab**
  - **Examine these Files to Correct Problem or Remove File from Project**



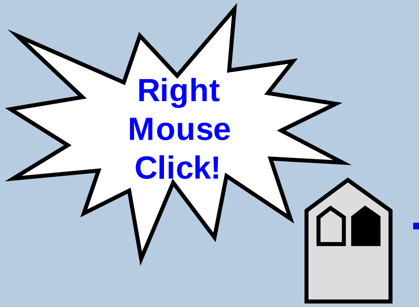
Default Configuration
mux8 (mux8.vhd)
mux4 (mux4_behave.vhd)
mux2 ()
Unknown Hierarchy
mux2_behave.vhd

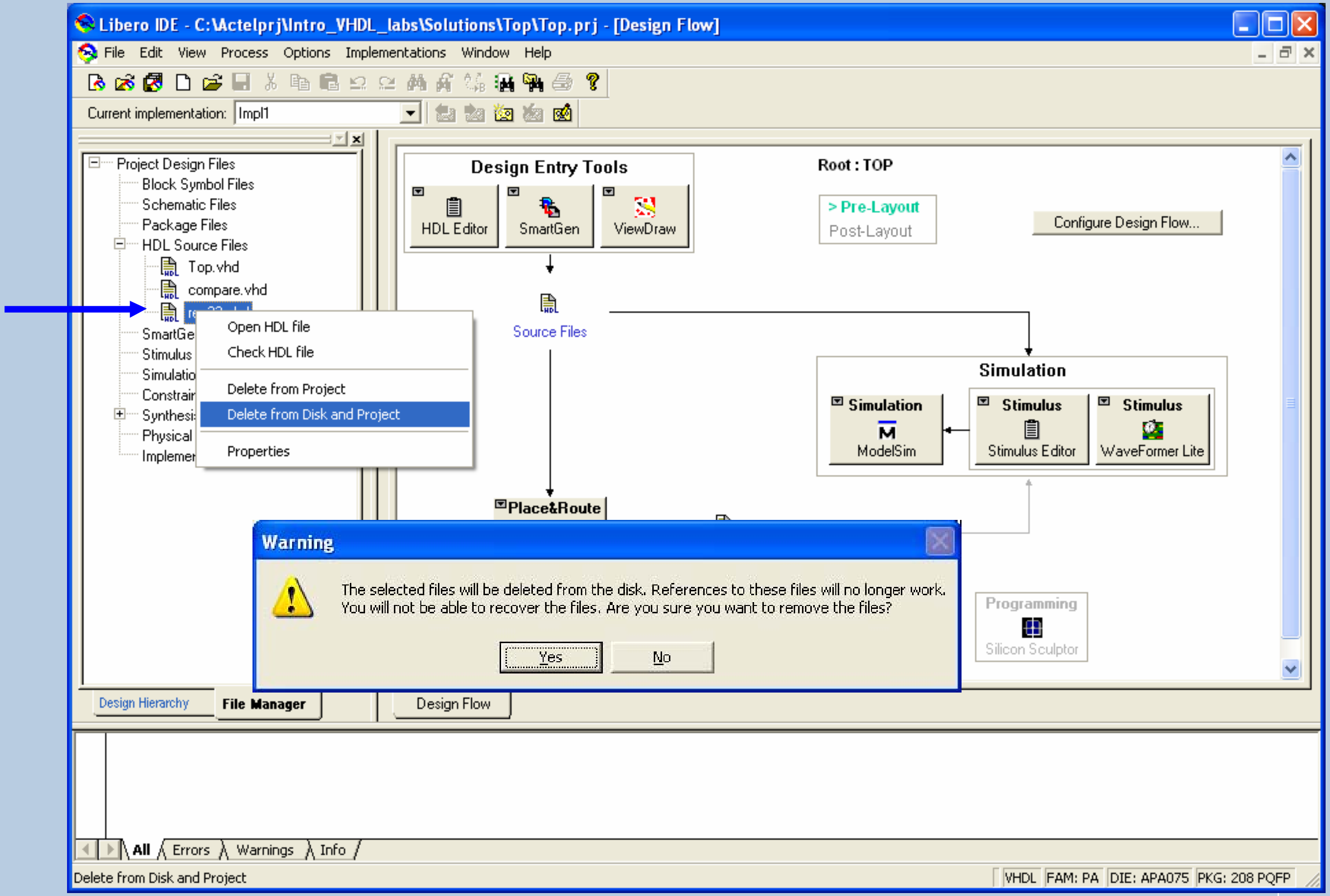


MUX2.1
MUX4.1
MUX8.1
TOP.1
Schematic Files
VHDL Package Files
HDL Files
mux2_behave.vhd
mux4_behave.vhd
mux8.vhd

# Deleting Files from Libero Project

- Files Can Be Deleted from Project and from HDD
  - **Files Deleted from HDD *Cannot* Be Recovered!**





Warning

The selected files will be deleted from the disk. References to these files will no longer work. You will not be able to recover the files. Are you sure you want to remove the files?

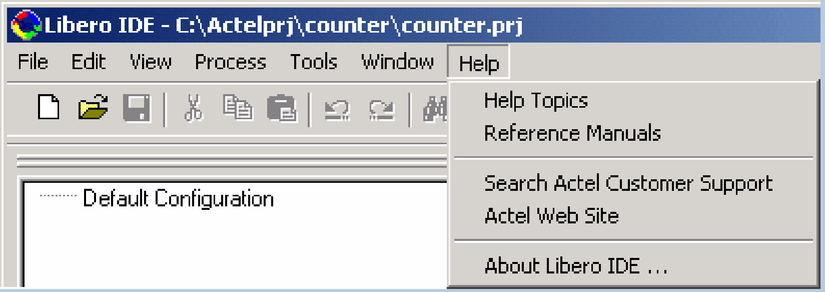
Yes No

Delete from Disk and Project

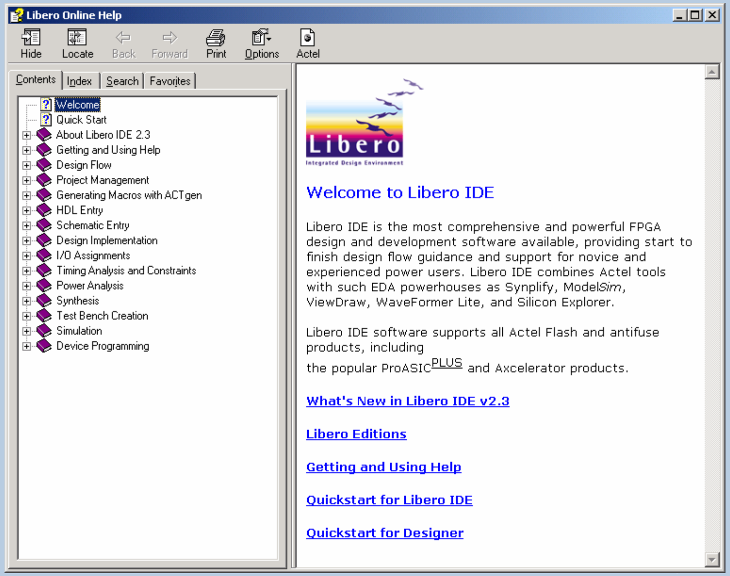
# Libero IDE Online Help

## HTML-based Help System

- Help Available for Error Messages, Specific Screens and Menus
- Expanded Content



- Hyperlinks to Application Notes and Actel Web Pages
- Help Menu Provides Direct Access to All Libero PDF Reference Manuals



Welcome to Libero IDE

Libero IDE is the most comprehensive and powerful FPGA design and development software available, providing start to finish design flow guidance and support for novice and experienced power users. Libero IDE combines Actel tools with such EDA powerhouses as Synplify, Model*Sim*, ViewDraw, WaveFormer Lite, and Silicon Explorer.

Libero IDE software supports all Actel Flash and antifuse products, including
the popular ProASIC$^{\text{PLUS}}$ and Axcelerator products.

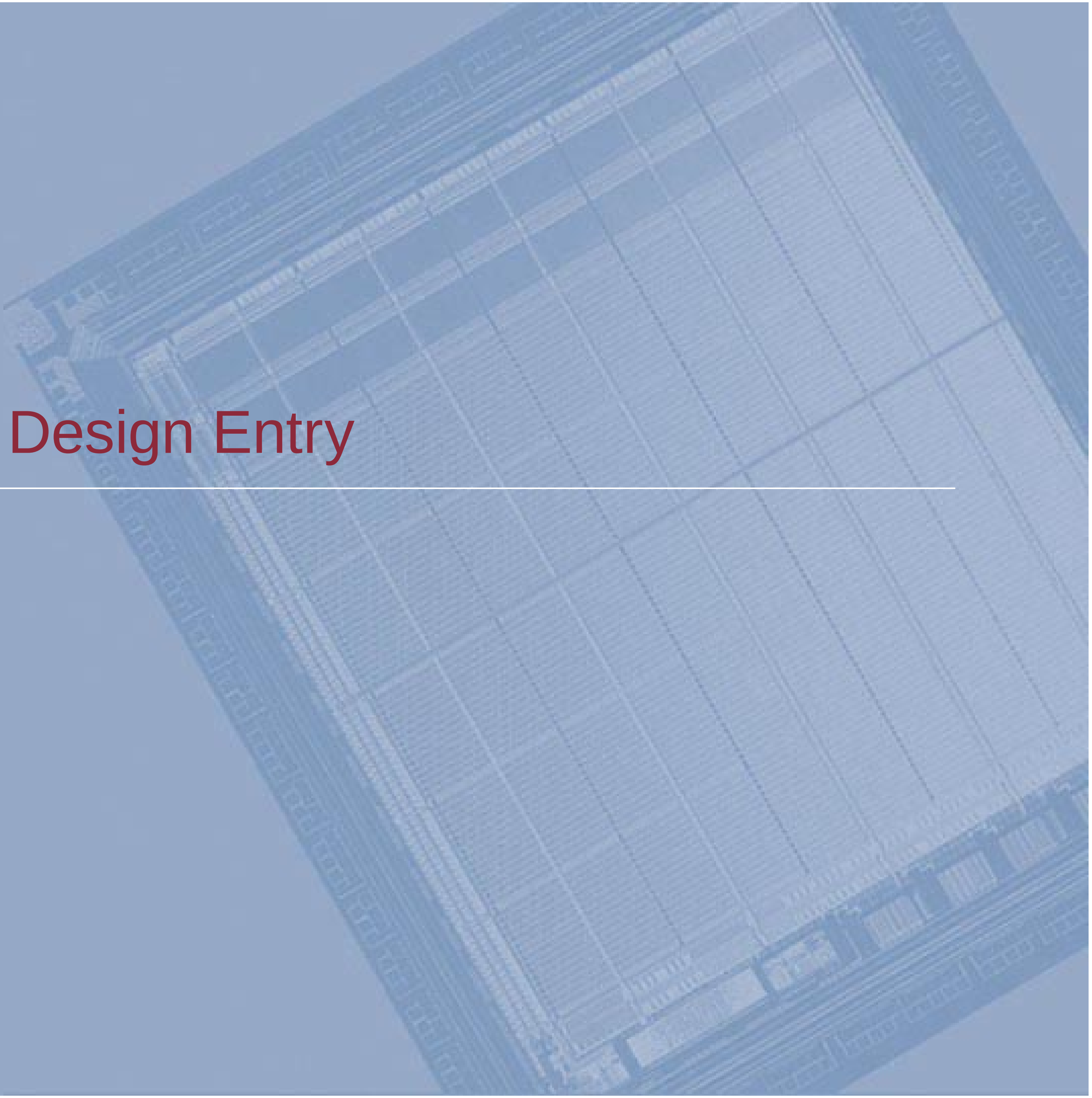
What's New in Libero IDE v2.3

Libero Editions

Getting and Using Help

Quickstart for Libero IDE

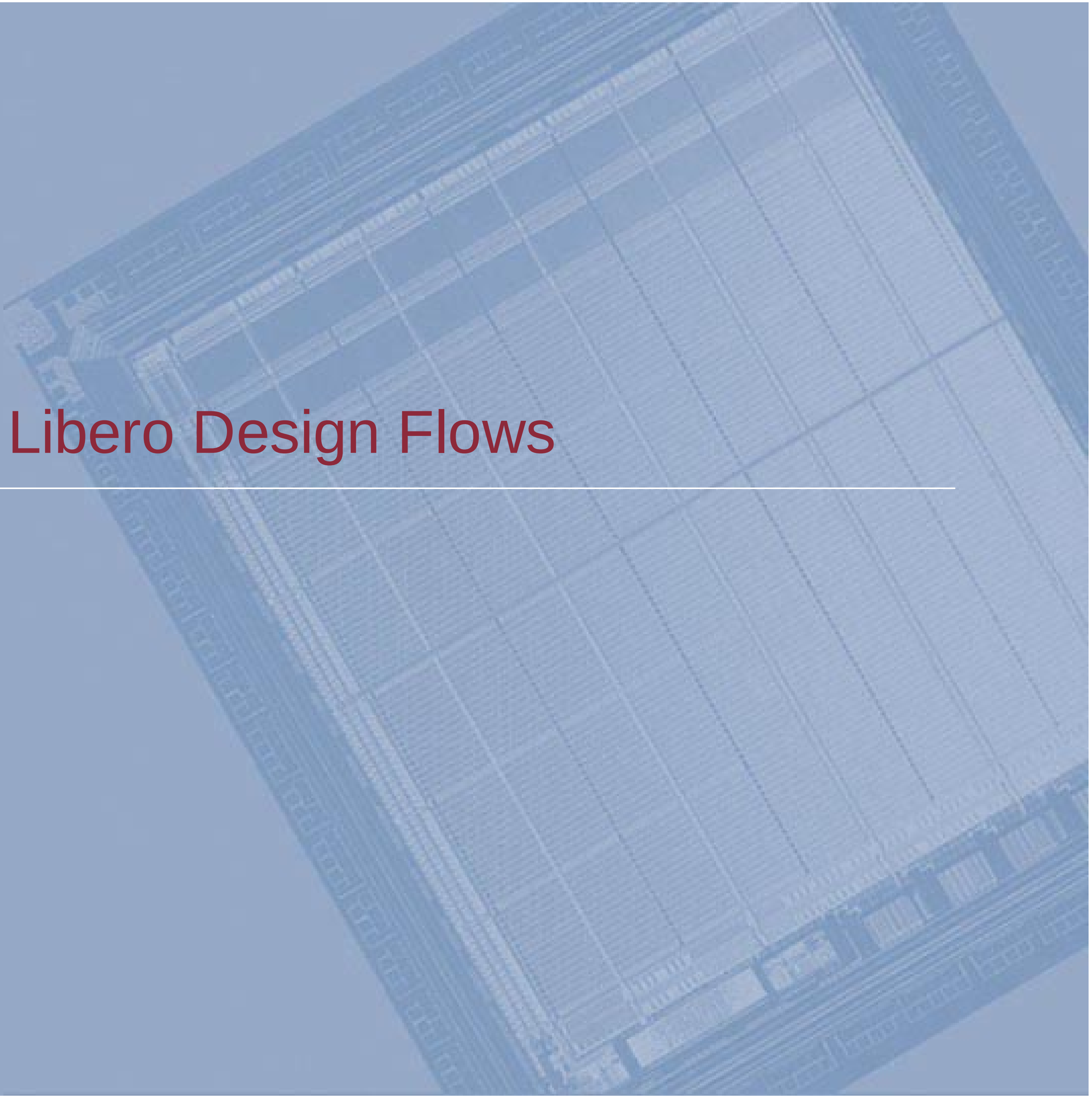
Quickstart for Designer



# Design Entry

# Design Entry

- Libero Supported Design Flows
  - Structural Schematic Flow
  - Mixed-Mode Flow
  - HDL Flow
- SmartGen Macro Builder
- ViewDraw Overview
  - Schematic Design Entry Tool



# Libero Design Flows

Actel

# Libero Design Flows

## Structural Schematic Flow

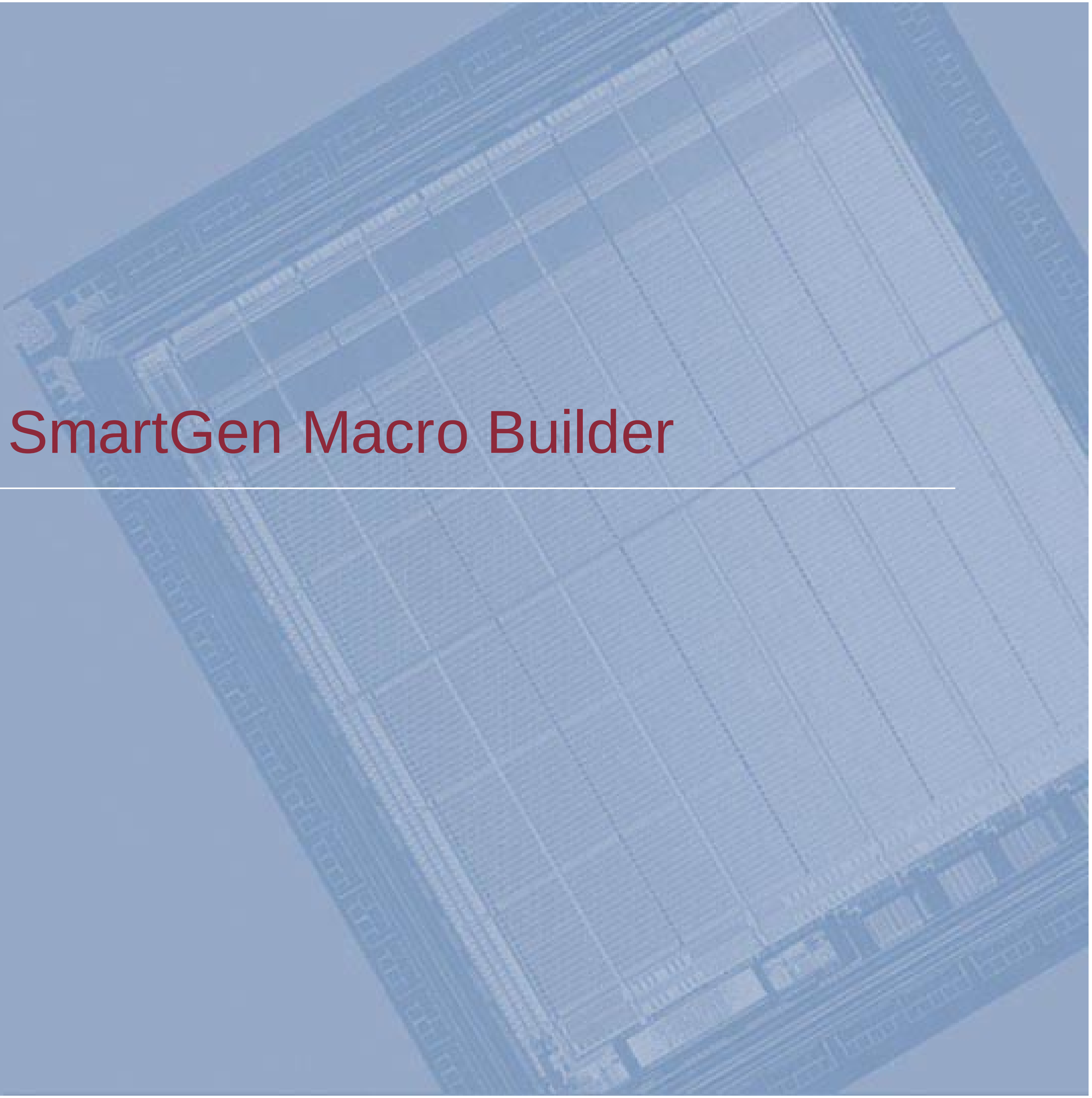
- **Contains only Actel ViewDraw Library Components or Mix of Actel ViewDraw Library Components and Structural HDL**
- **Top Level *Must* Be Schematic!**
- **Synthesis *Optional* before Layout**

## Mixed-Mode Flow

- **Schematic and RTL Blocks**
  - **May also Contain Structural HDL Blocks**
- **Top Level *Must* Be Schematic!**
- **Synthesis *Required* before Layout**

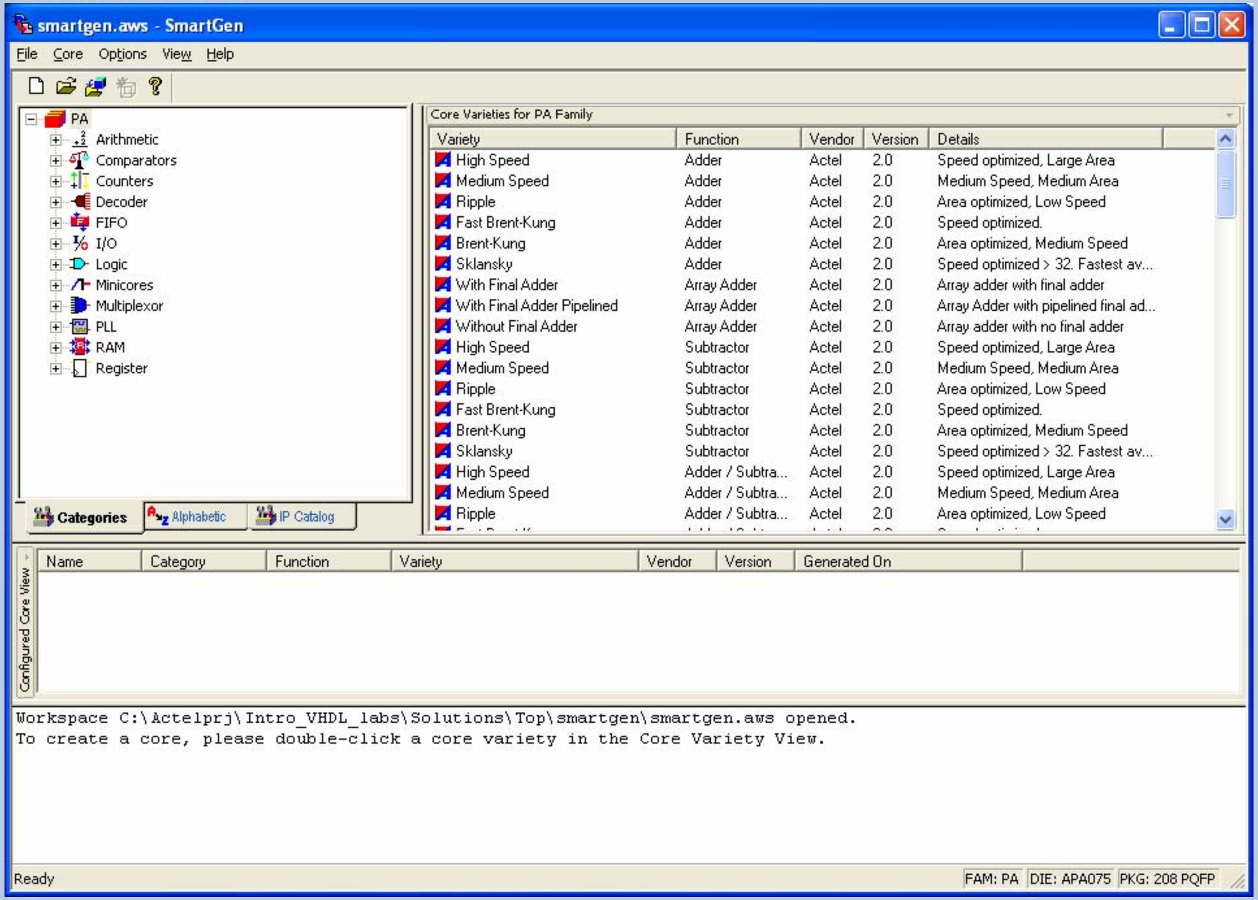
## HDL Flow

- **VHDL or Verilog (not both)**
- **May Contain Structural Blocks**



# SmartGen Macro Builder

# SmartGen Macro Builder



Core Varieties for PA Family

| Variety | Function | Vendor | Version | Details |
|---|---|---|---|---|
| High Speed | Adder | Actel | 2.0 | Speed optimized, Large Area |
| Medium Speed | Adder | Actel | 2.0 | Medium Speed, Medium Area |
| Ripple | Adder | Actel | 2.0 | Area optimized, Low Speed |
| Fast Brent-Kung | Adder | Actel | 2.0 | Speed optimized. |
| Brent-Kung | Adder | Actel | 2.0 | Area optimized, Medium Speed |
| Sklansky | Adder | Actel | 2.0 | Speed optimized > 32. Fastest av... |
| With Final Adder | Array Adder | Actel | 2.0 | Array adder with final adder |
| With Final Adder Pipelined | Array Adder | Actel | 2.0 | Array Adder with pipelined final ad... |
| Without Final Adder | Array Adder | Actel | 2.0 | Array adder with no final adder |
| High Speed | Subtractor | Actel | 2.0 | Speed optimized, Large Area |
| Medium Speed | Subtractor | Actel | 2.0 | Medium Speed, Medium Area |
| Ripple | Subtractor | Actel | 2.0 | Area optimized, Low Speed |
| Fast Brent-Kung | Subtractor | Actel | 2.0 | Speed optimized. |
| Brent-Kung | Subtractor | Actel | 2.0 | Area optimized, Medium Speed |
| Sklansky | Subtractor | Actel | 2.0 | Speed optimized > 32. Fastest av... |
| High Speed | Adder / Subtra... | Actel | 2.0 | Speed optimized, Large Area |
| Medium Speed | Adder / Subtra... | Actel | 2.0 | Medium Speed, Medium Area |
| Ripple | Adder / Subtra... | Actel | 2.0 | Area optimized, Low Speed |

| Name | Category | Function | Variety | Vendor | Version | Generated On |
|---|---|---|---|---|---|---|

```
Workspace C:\Actelprj\Intro_VHDL_labs\Solutions\Top\smartgen\smartgen.aws opened.
To create a core, please double-click a core variety in the Core Variety View.
```

Ready FAM: PA DIE: APA075 PKG: 208 PQFP

- Create Macro Functions from User's Parameters
- Optimized for Actel Architecture
  - **High Speed**
  - **Small Area**
- Rule-based Generation Guarantees Functional Accuracy
- Outputs:
  - **VHDL - Behavioral and Structural**
  - **Verilog - Behavioral and Structural**

# Using SmartGen within Libero

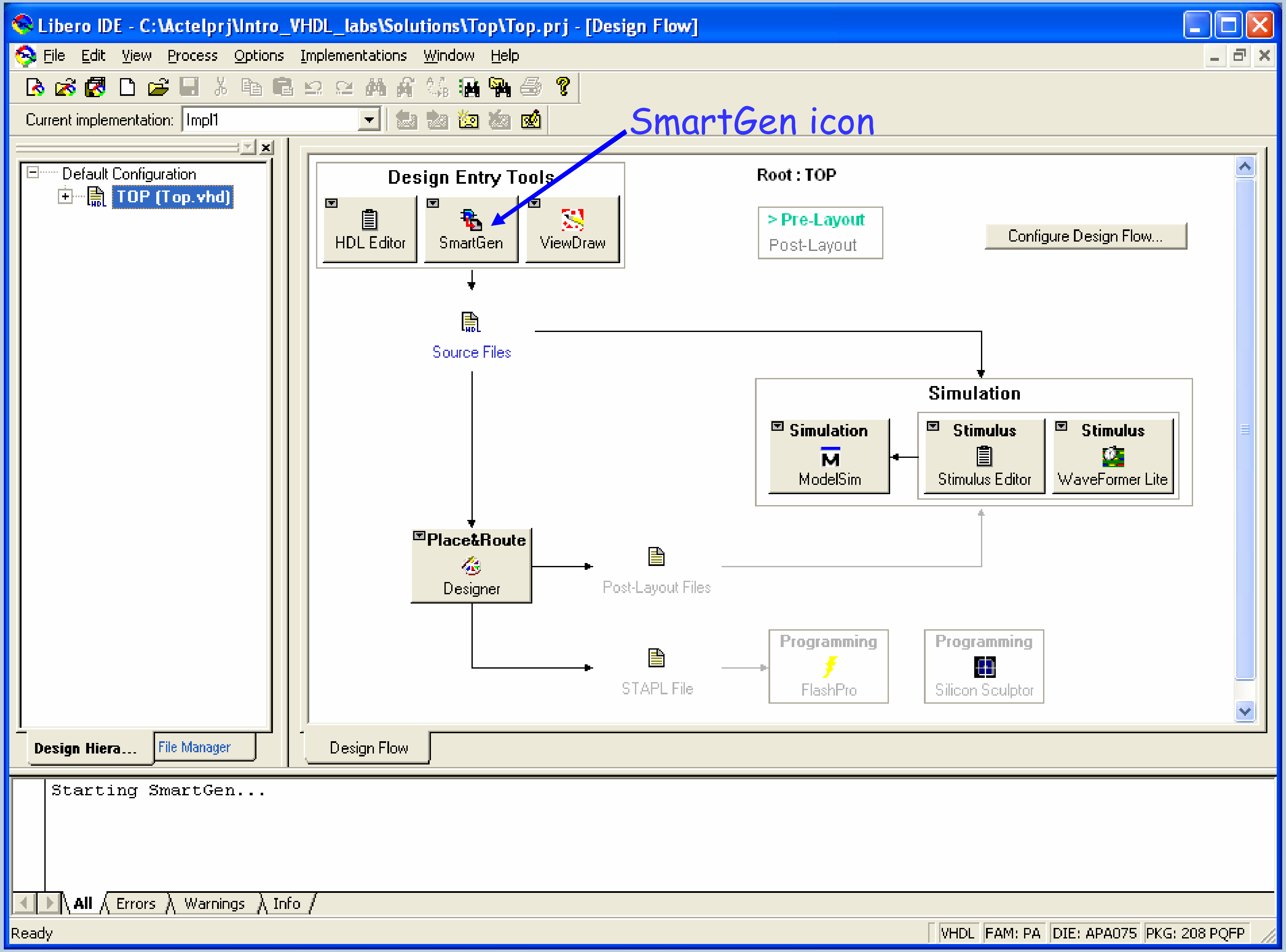
## SmartGen Macros Can Be Used in …

- … Structural Schematic flow
- … Mixed-mode Flow
- … HDL Flow

## Steps:

- Launch SmartGen from Libero IDE Project Manager
- Create HDL Structural Implementation
  - VHDL or Verilog
- HDL Flow
  - Instantiate Macro in Top-level RTL
- Structural Schematic and Mixed-mode Flows
  - Create ViewDraw Symbol from Libero
  - instantiate Symbol in Schematic

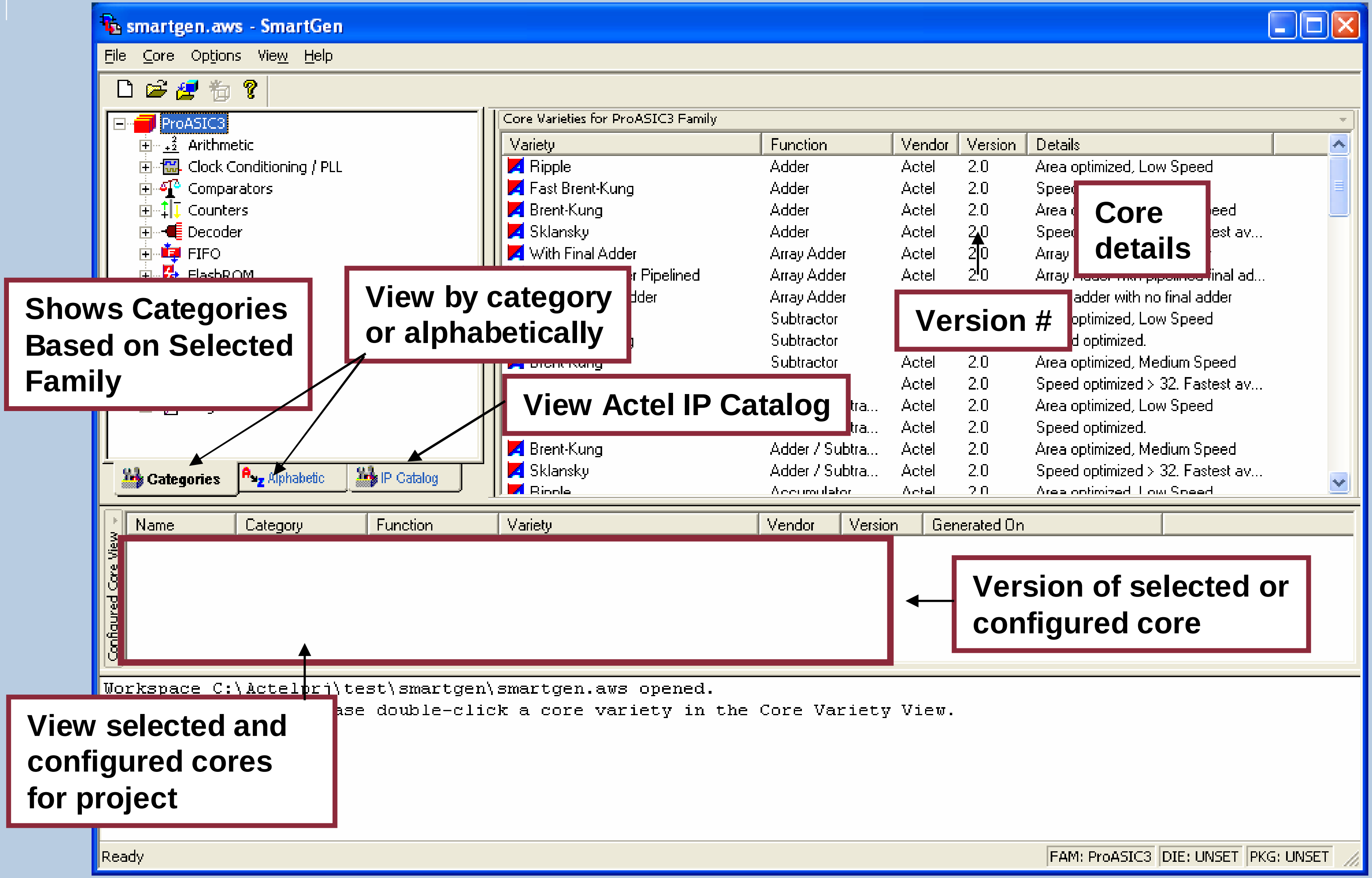
# Launching SmartGen from Libero



SmartGen icon

```
Starting SmartGen...
```

# SmartGen User Interface



| Variety | Function | Vendor | Version | Details |
|---|---|---|---|---|
| Ripple | Adder | Actel | 2.0 | Area optimized, Low Speed |
| Fast Brent-Kung | Adder | Actel | 2.0 | Speed |
| Brent-Kung | Adder | Actel | 2.0 | Area eed |
| Sklansky | Adder | Actel | 2.0 | Speed est av... |
| With Final Adder | Array Adder | Actel | 2.0 | Array |
| Pipelined | Array Adder | Actel | 2.0 | Array inal ad... |
| dder | Array Adder | | | adder with no final adder |
| | Subtractor | | | optimized, Low Speed |
| | Subtractor | | | d optimized. |
| | Subtractor | Actel | 2.0 | Area optimized, Medium Speed |
| | | Actel | 2.0 | Speed optimized > 32. Fastest av... |
| | tra... | Actel | 2.0 | Area optimized, Low Speed |
| | tra... | Actel | 2.0 | Speed optimized. |
| Brent-Kung | Adder / Subtra... | Actel | 2.0 | Area optimized, Medium Speed |
| Sklansky | Adder / Subtra... | Actel | 2.0 | Speed optimized > 32. Fastest av... |
| Ripple | Accumulator | Actel | 2.0 | Area optimized, Low Speed |

| Name | Category | Function | Variety | Vendor | Version | Generated On |
|---|---|---|---|---|---|---|

```
Workspace C:\Actelprj\test\smartgen\smartgen.aws opened.
          ase double-click a core variety in the Core Variety View.
```

Ready    FAM: ProASIC3    DIE: UNSET    PKG: UNSET

Shows Categories Based on Selected Family

View by category or alphabetically

View Actel IP Catalog

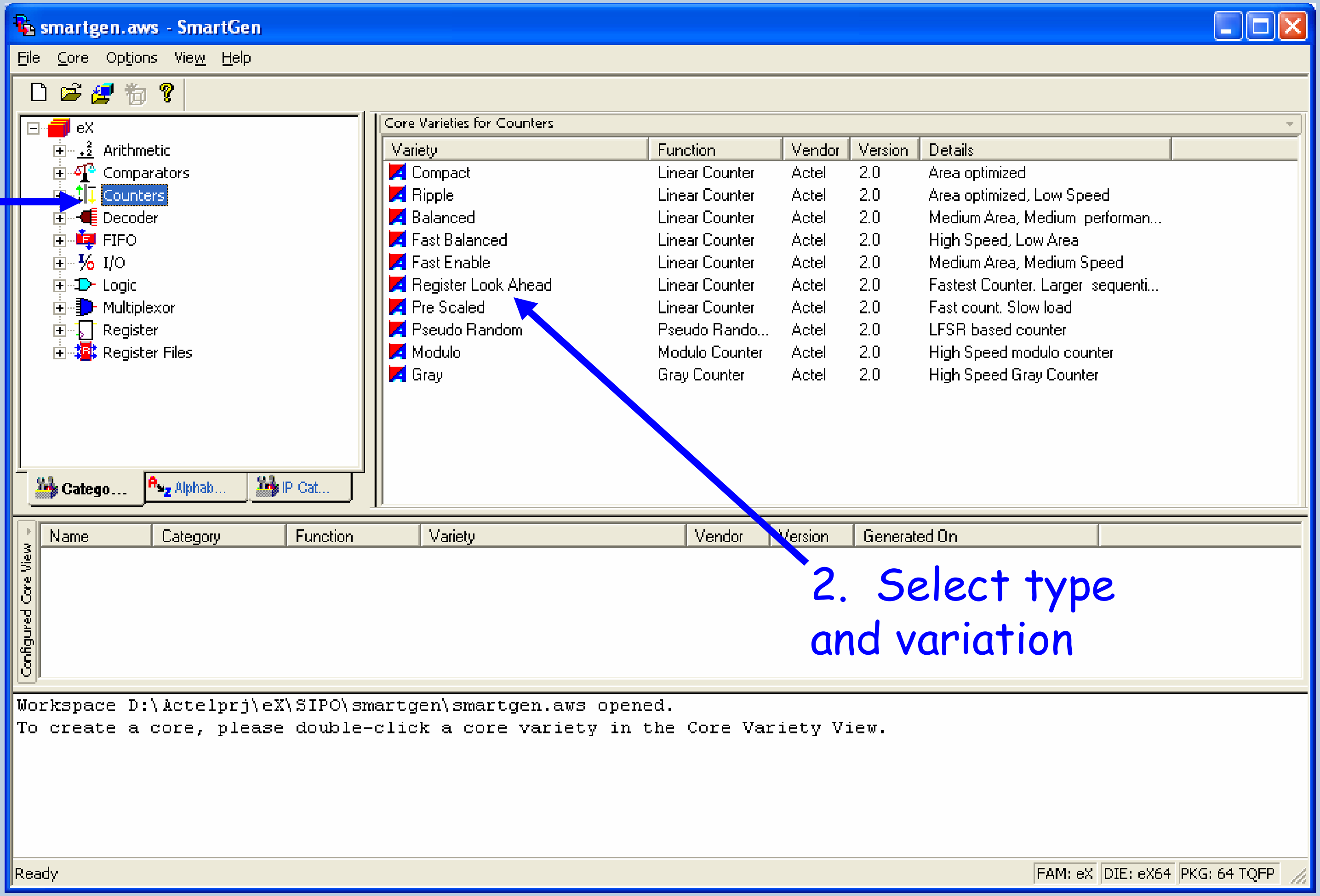
Core details

Version #

Version of selected or configured core

View selected and configured cores for project

# SmartGen
## *Counter Example*



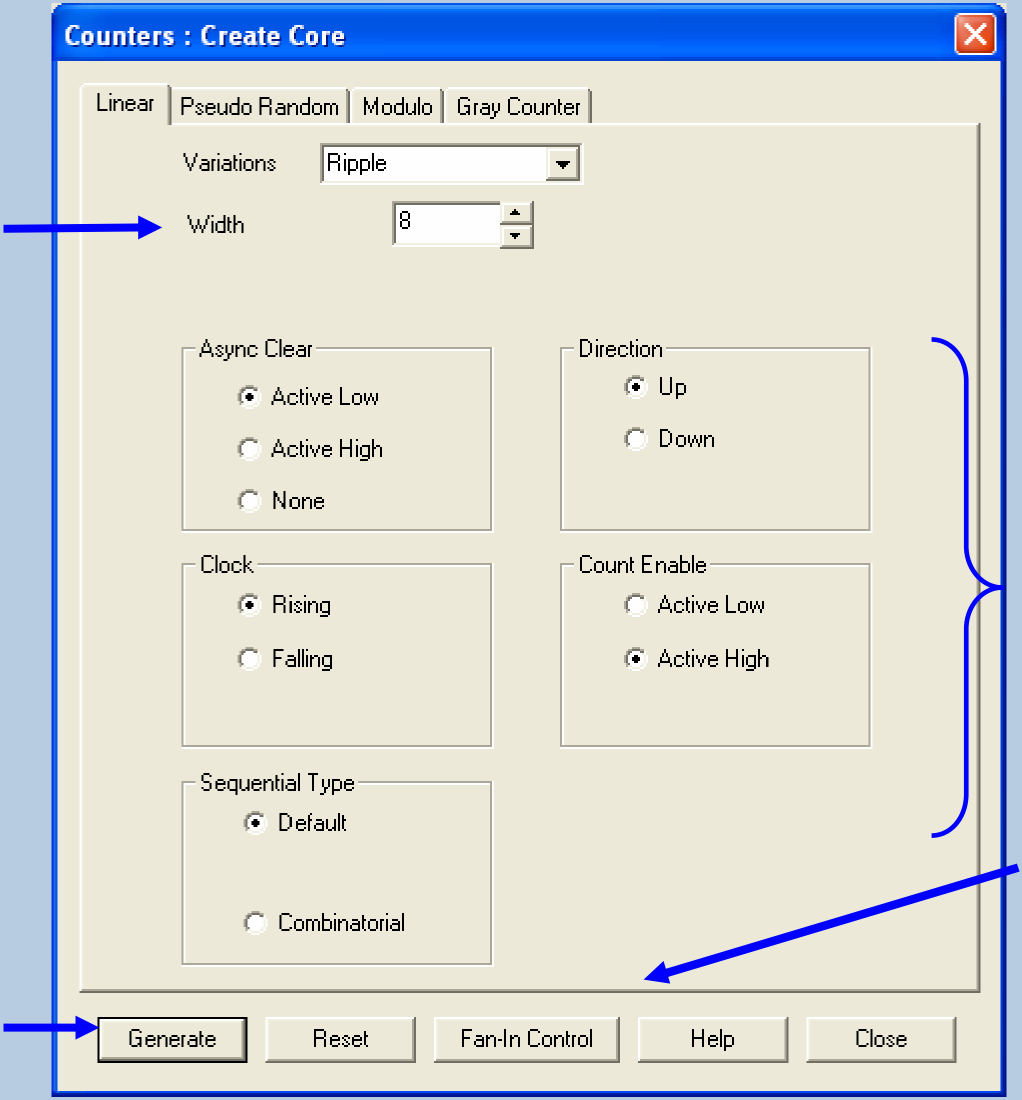
| Variety | Function | Vendor | Version | Details |
|---|---|---|---|---|
| Compact | Linear Counter | Actel | 2.0 | Area optimized |
| Ripple | Linear Counter | Actel | 2.0 | Area optimized, Low Speed |
| Balanced | Linear Counter | Actel | 2.0 | Medium Area, Medium performan... |
| Fast Balanced | Linear Counter | Actel | 2.0 | High Speed, Low Area |
| Fast Enable | Linear Counter | Actel | 2.0 | Medium Area, Medium Speed |
| Register Look Ahead | Linear Counter | Actel | 2.0 | Fastest Counter. Larger sequenti... |
| Pre Scaled | Linear Counter | Actel | 2.0 | Fast count. Slow load |
| Pseudo Random | Pseudo Rando... | Actel | 2.0 | LFSR based counter |
| Modulo | Modulo Counter | Actel | 2.0 | High Speed modulo counter |
| Gray | Gray Counter | Actel | 2.0 | High Speed Gray Counter |

```
Workspace D:\Actelprj\eX\SIPO\smartgen\smartgen.aws opened.
To create a core, please double-click a core variety in the Core Variety View.
```

1. Choose Function

2. Select type and variation

# SmartGen
## *Counter Example*



Counters : Create Core

Linear | Pseudo Random | Modulo | Gray Counter

Variations: Ripple

Width: 8

Async Clear
- ● Active Low
- ○ Active High
- ○ None

Direction
- ● Up
- ○ Down

Clock
- ● Rising
- ○ Falling

Count Enable
- ○ Active Low
- ● Active High

Sequential Type
- ● Default
- ○ Combinatorial

3. Enter width

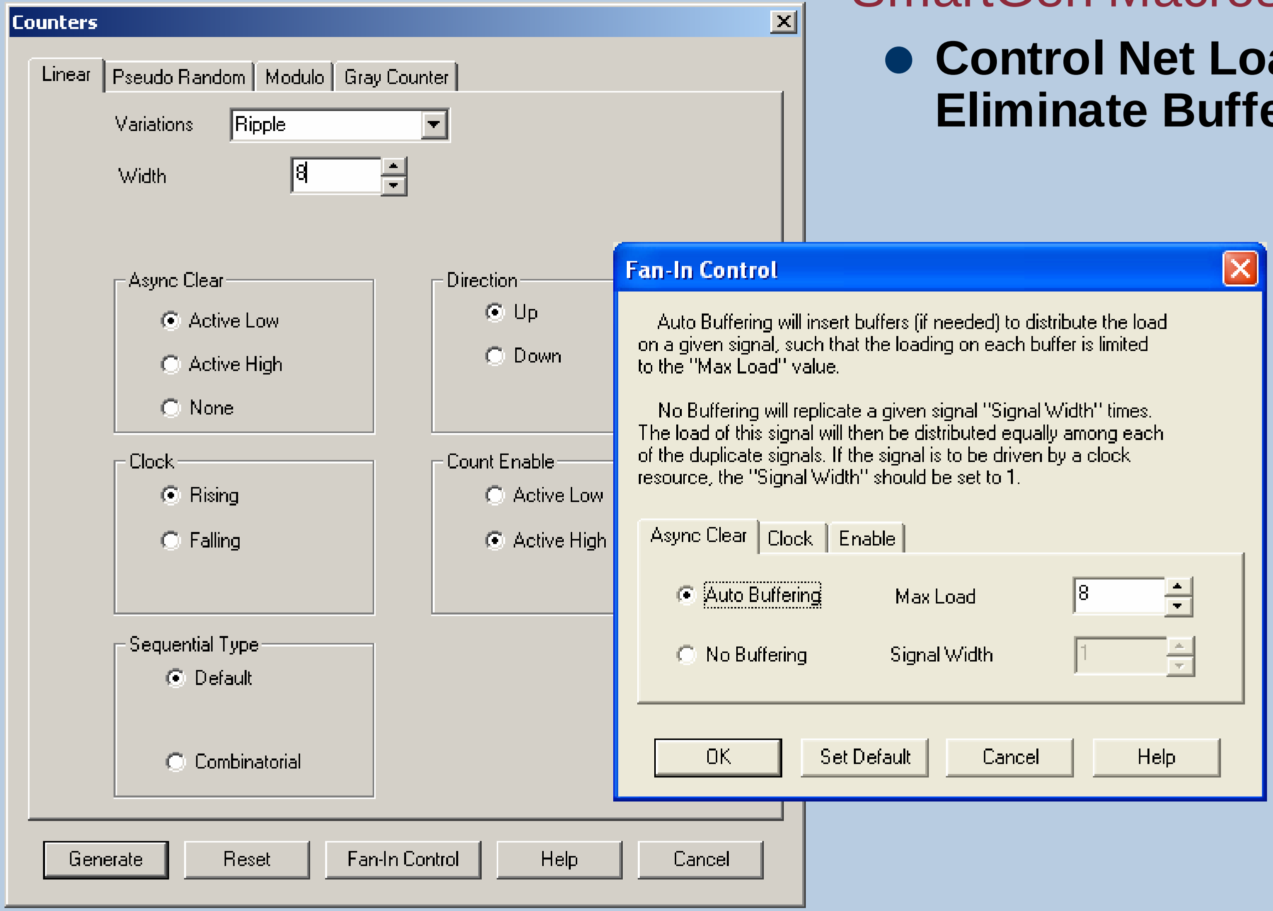
4. Complete the rest of the description

Optional Fan-In Control

5. Click Generate

# SmartGen Buffering Control

- Users Can Control Buffering in SmartGen Macros
  - **Control Net Loading or Eliminate Buffering**



Variations: Ripple

Width: 8

Async Clear: ● Active Low ○ Active High ○ None

Direction: ● Up ○ Down

Clock: ● Rising ○ Falling

Count Enable: ○ Active Low ● Active High

Sequential Type: ● Default ○ Combinatorial

Auto Buffering will insert buffers (if needed) to distribute the load on a given signal, such that the loading on each buffer is limited to the "Max Load" value.

No Buffering will replicate a given signal "Signal Width" times. The load of this signal will then be distributed equally among each of the duplicate signals. If the signal is to be driven by a clock resource, the "Signal Width" should be set to 1.

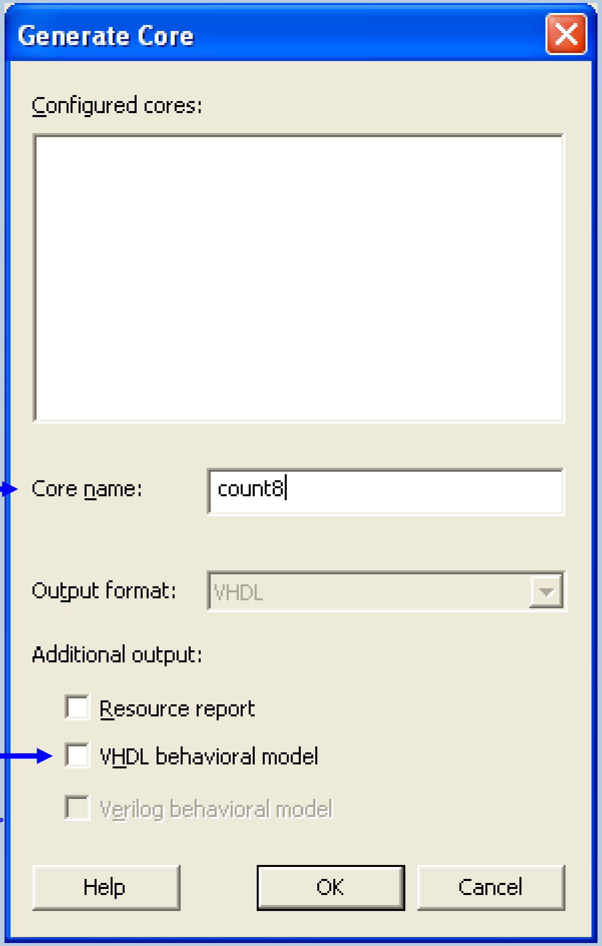
● Auto Buffering — Max Load: 8

○ No Buffering — Signal Width: 1

# SmartGen Component Generation

Core name

Generate behavioral VHDL or Verilog



Generate Core

Configured cores:

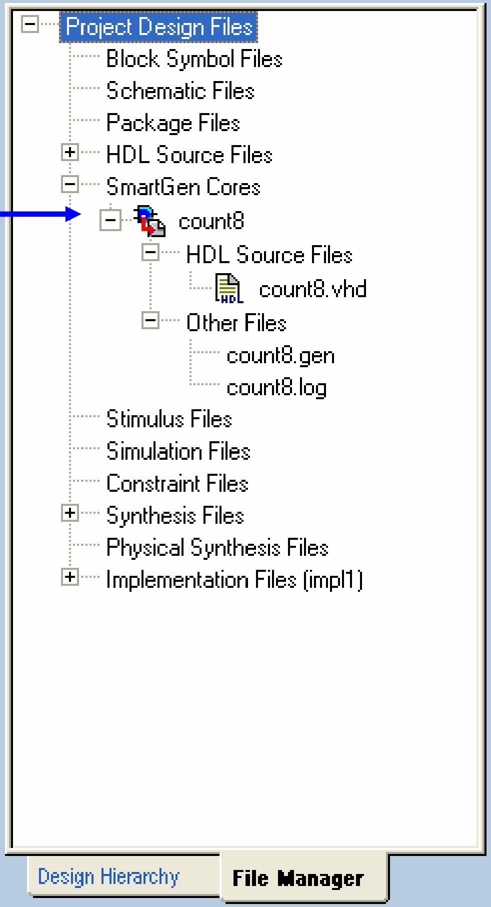
Core name: count8

Output format: VHDL

Additional output:

- □ Resource report
- □ VHDL behavioral model
- □ Verilog behavioral model

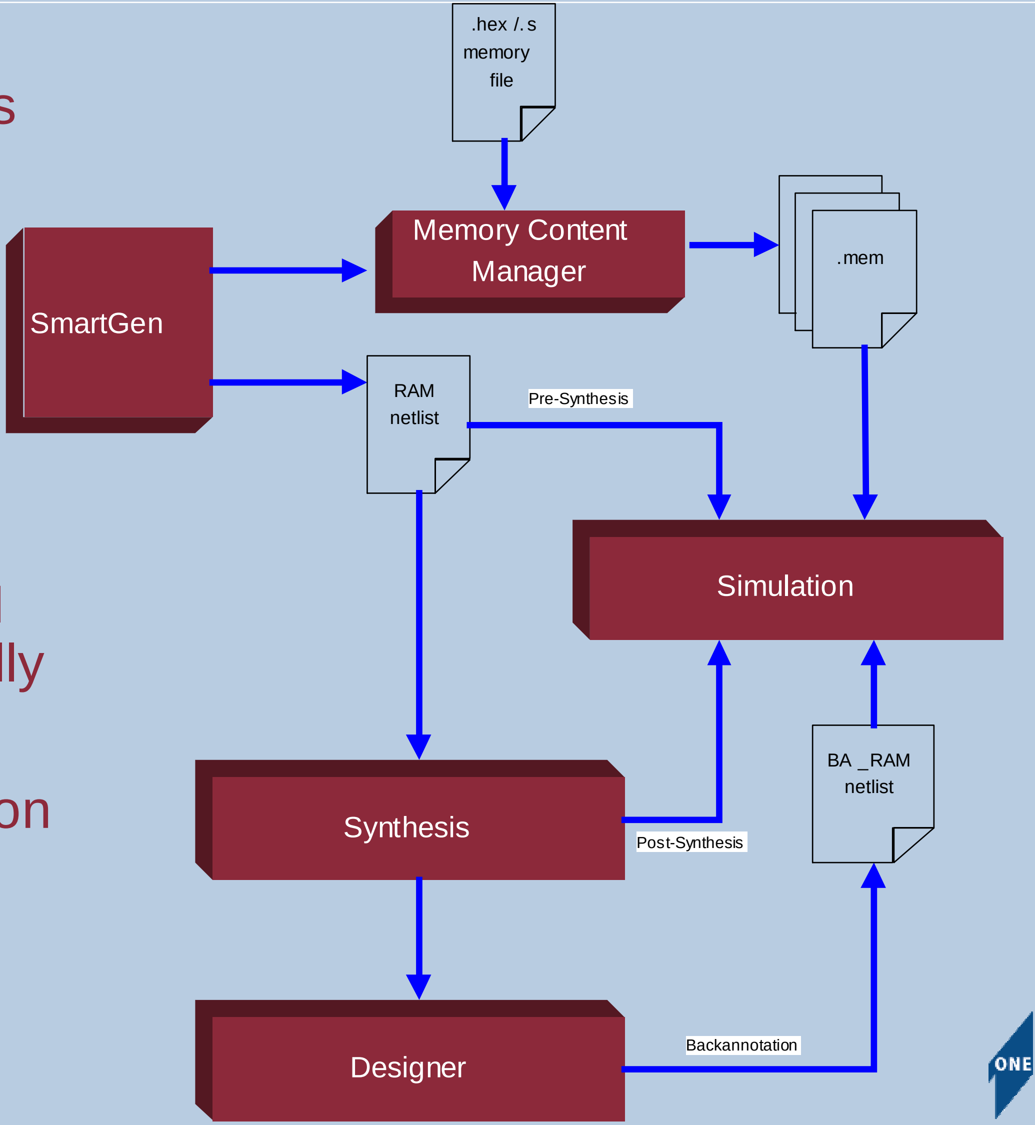
Files appear on Libero File Manager tab



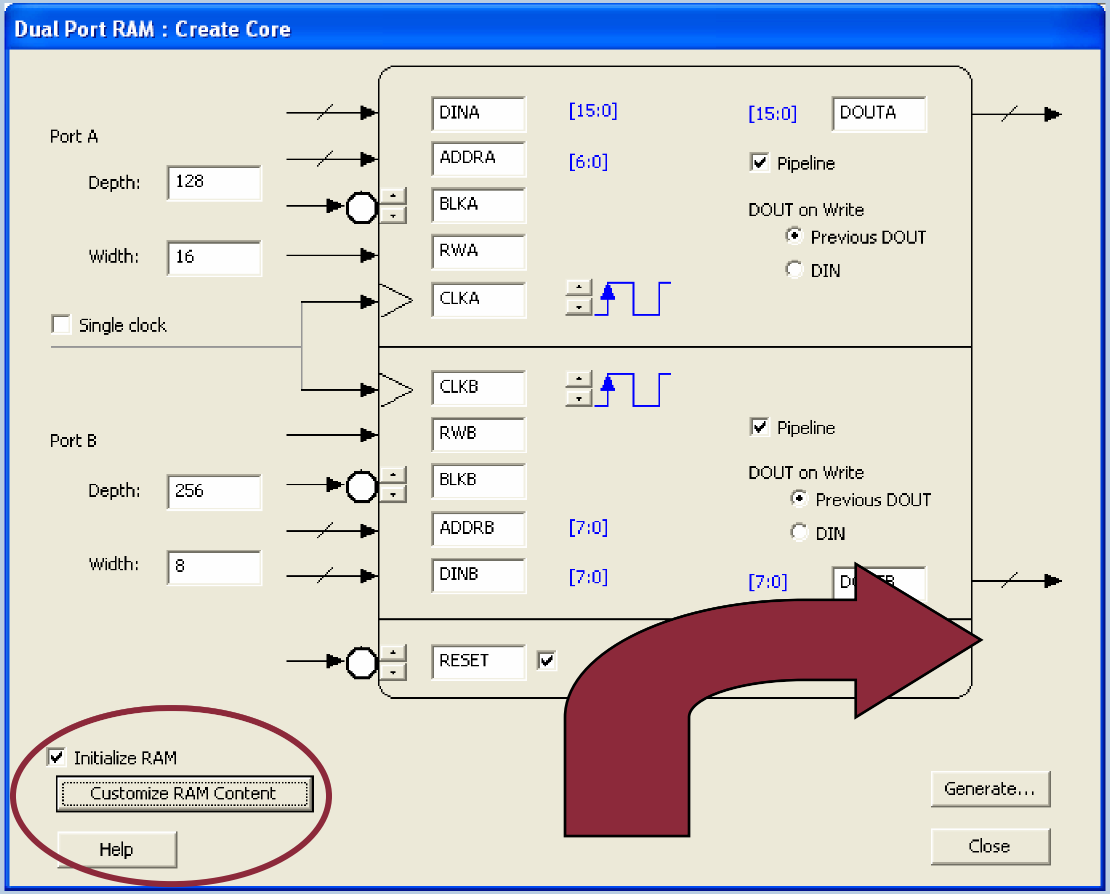
- Project Design Files
  - Block Symbol Files
  - Schematic Files
  - Package Files
  - HDL Source Files
  - SmartGen Cores
    - count8
      - HDL Source Files
        - count8.vhd
      - Other Files
        - count8.gen
        - count8.log
  - Stimulus Files
  - Simulation Files
  - Constraint Files
  - Synthesis Files
  - Physical Synthesis Files
  - Implementation Files (impl1)

# SmartGen RAM Initialization

- Speeds up simulation time by reducing the initial writes to setup the memory
- Completely automated simulation flow
- MEMORYFILE property preserved throughout the flow
- Cascading of multiple RAM blocks handled automatically
- Supports industry standard memory content specification files



# SmartGen RAM Initialization *(cont.)*



Dual Port RAM : Create Core

Port A

Depth: 128

Width: 16

☐ Single clock

Port B

Depth: 256

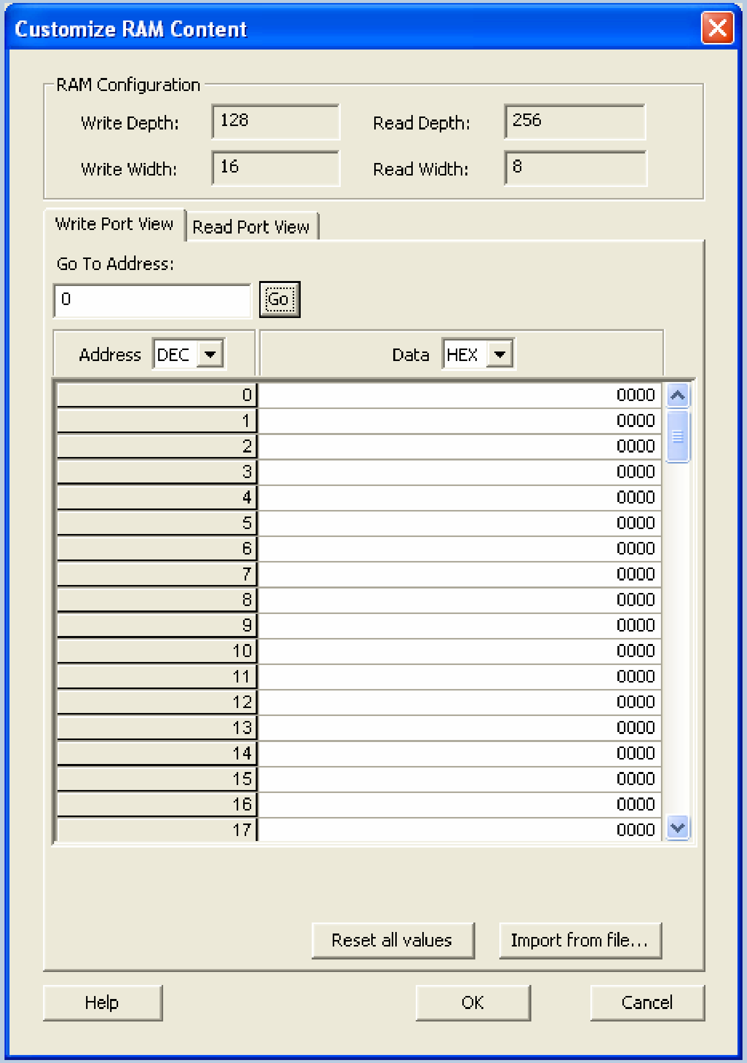
Width: 8

Port A: ☑ Pipeline; DOUT on Write: ● Previous DOUT ○ DIN

Port B: ☑ Pipeline; DOUT on Write: ● Previous DOUT ○ DIN

RESET ☑

☑ Initialize RAM



Customize RAM Content

RAM Configuration

| | | | |
|---|---|---|---|
| Write Depth: | 128 | Read Depth: | 256 |
| Write Width: | 16 | Read Width: | 8 |

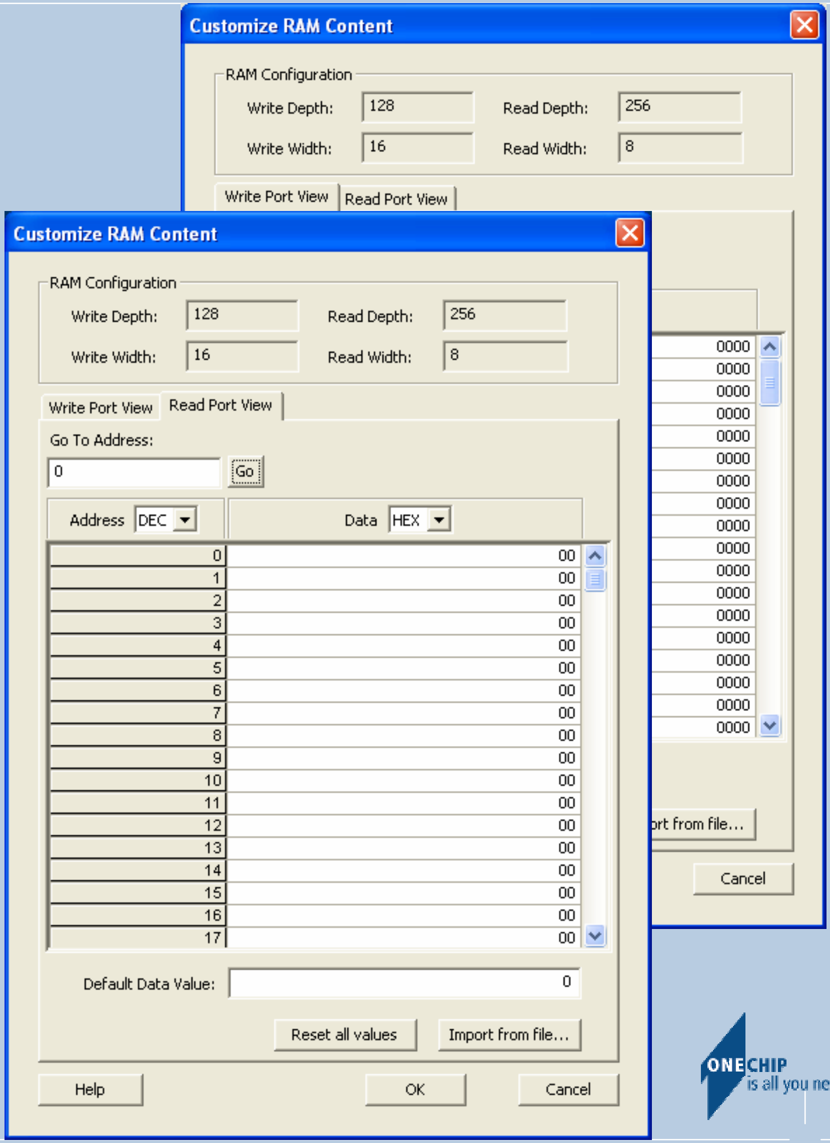
Write Port View | Read Port View

Go To Address: 0

| Address DEC | Data HEX |
|---|---|
| 0 | 0000 |
| 1 | 0000 |
| 2 | 0000 |
| 3 | 0000 |
| 4 | 0000 |
| 5 | 0000 |
| 6 | 0000 |
| 7 | 0000 |
| 8 | 0000 |
| 9 | 0000 |
| 10 | 0000 |
| 11 | 0000 |
| 12 | 0000 |
| 13 | 0000 |
| 14 | 0000 |
| 15 | 0000 |
| 16 | 0000 |
| 17 | 0000 |

# Memory Content Manager *Features*

- Variable aspect ratio support
  - **Read View & Write View**
- Import of User Memory File
  - **Intel hex format**
  - **Motorola- S format**
- Multiple Radix for data and address display
  - **Hex**
  - **Bin**
  - **Decimal**



Customize RAM Content

RAM Configuration

Write Depth: 128 Read Depth: 256

Write Width: 16 Read Width: 8

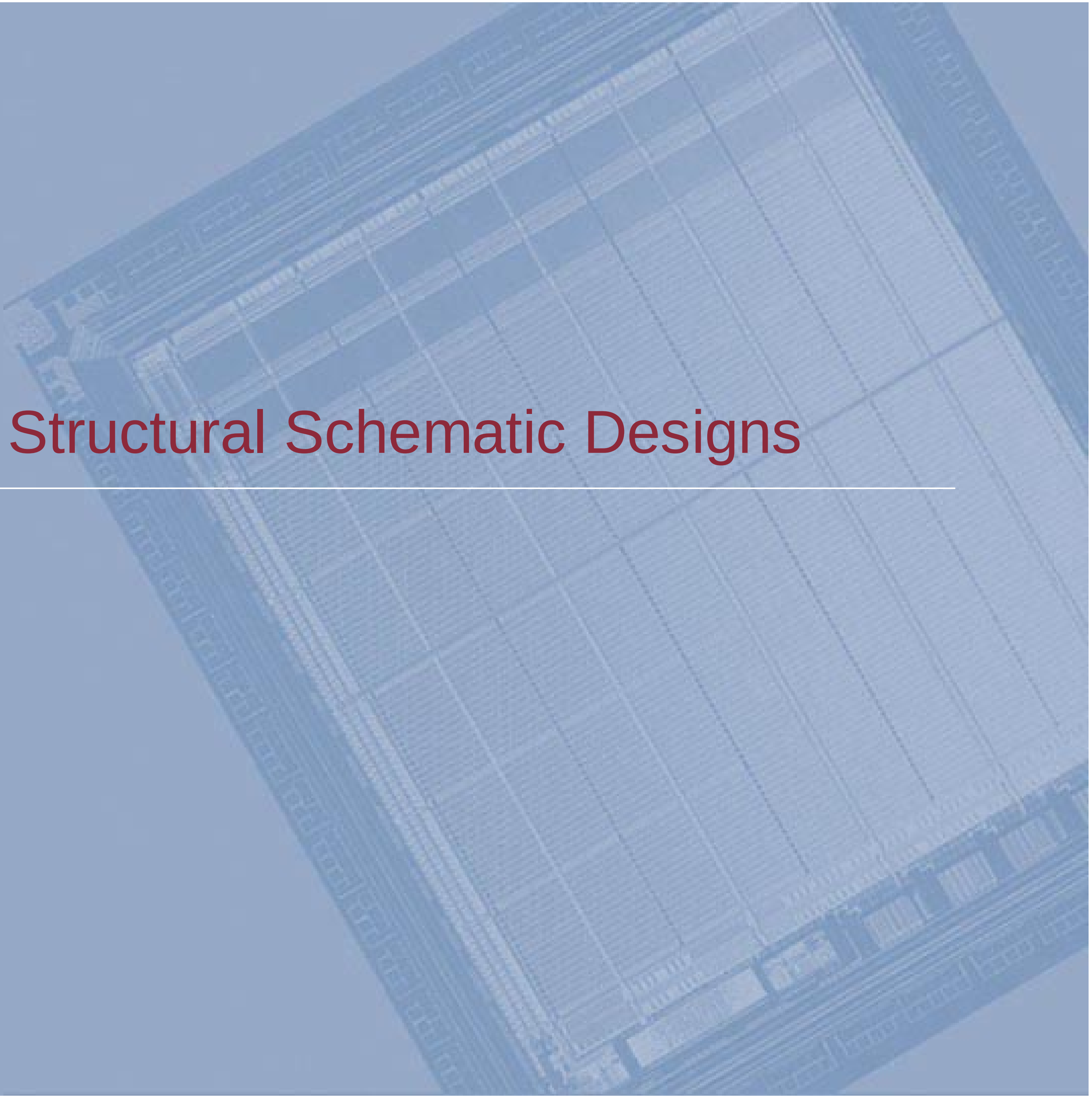
Write Port View | Read Port View

Go To Address: 0 Go

Address: DEC Data: HEX

| Address | Data |
|---|---|
| 0 | 00 |
| 1 | 00 |
| 2 | 00 |
| 3 | 00 |
| 4 | 00 |
| 5 | 00 |
| 6 | 00 |
| 7 | 00 |
| 8 | 00 |
| 9 | 00 |
| 10 | 00 |
| 11 | 00 |
| 12 | 00 |
| 13 | 00 |
| 14 | 00 |
| 15 | 00 |
| 16 | 00 |
| 17 | 00 |

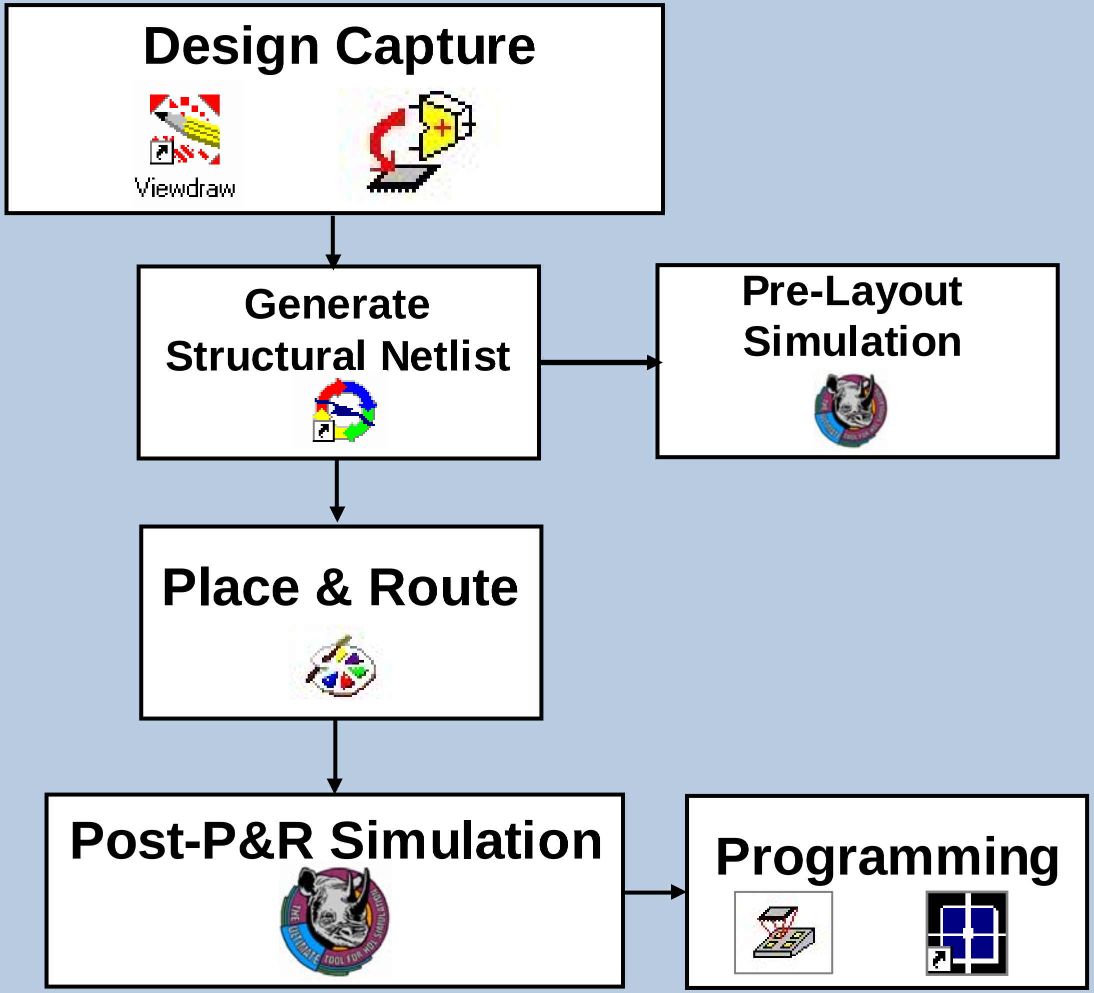
Default Data Value: 0



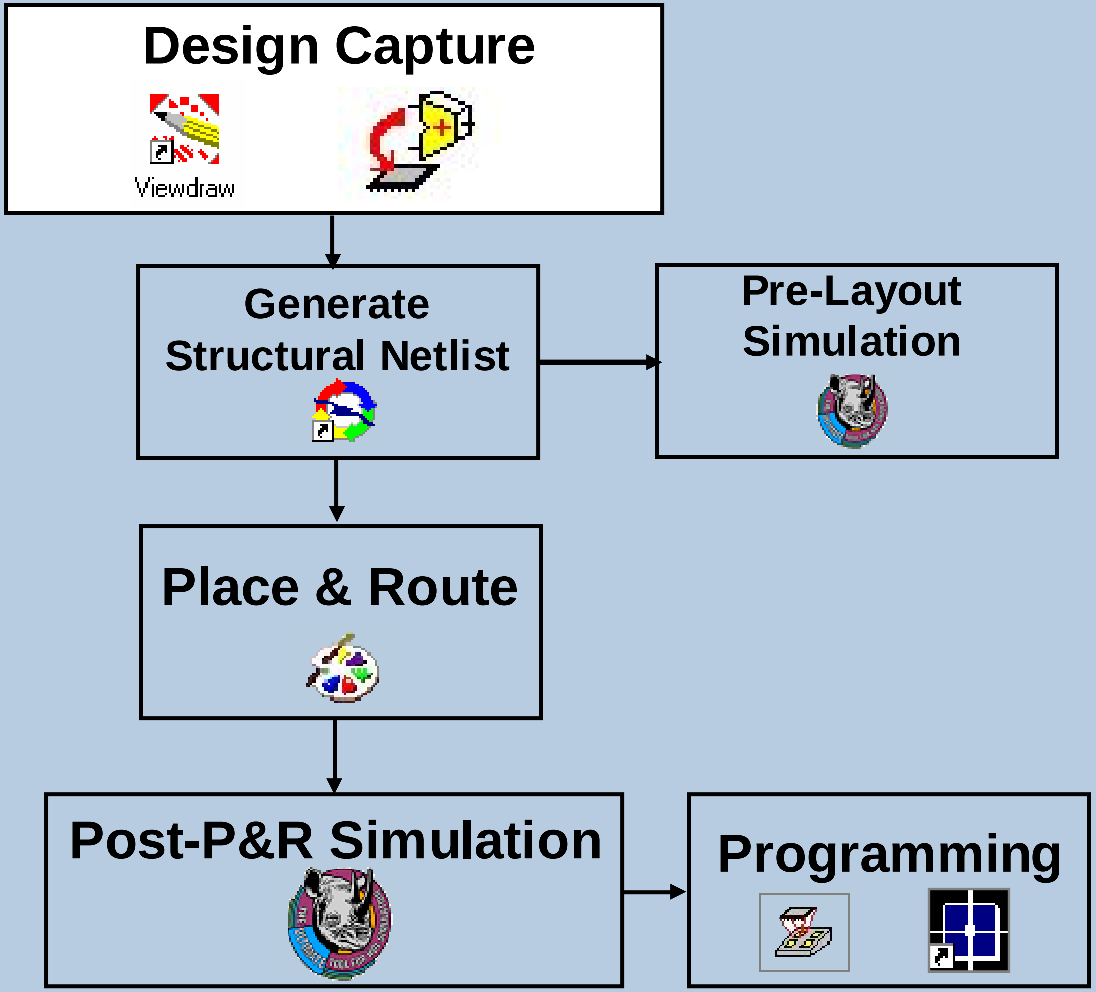
# Structural Schematic Designs

Actel

# Structural Schematic Design Flow



# Design Capture



# ViewDraw Overview

Schematic Design Entry Tool

# ViewDraw
*Features*

## Powerful Editing Capabilities

- Simple, Push-Button GUI Enables Rapid Design Input
- Infinite Undo/Redo
- Dynamic Pan and Autoscroll
- Automatic Connection of Abutting Pins
- Rubber Banding of Connected Nets with Dynamic Redraw

## Flexible and Customizable

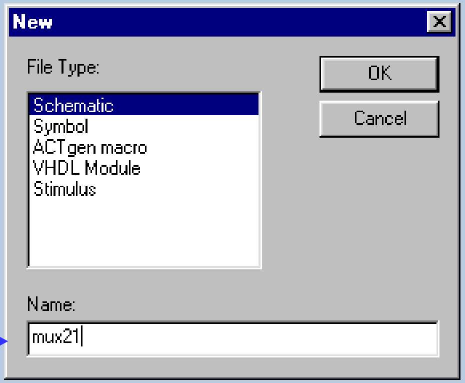
- Designers can Add, Delete, or Reorder Items in Menu System
- Commands Can Also Be Entered via Function Keys or CLI
- Selectable Display Styles for Lines, Fill Patterns, Bus Widths

# ViewDraw
## *Additional Features*

- ViewDraw AE can read
  - EPD 2.0 and 3.0
    - Generated schematics
    - Schematic files
    - Outputs in ViewDraw format
- ViewDraw can co-exist/co-install with ePD
  - Customers can switch back and forth between ViewDraw and ePD tools

# Invoking ViewDraw

- Launch ViewDraw from Libero.
- Create Schematic
- Save and Check



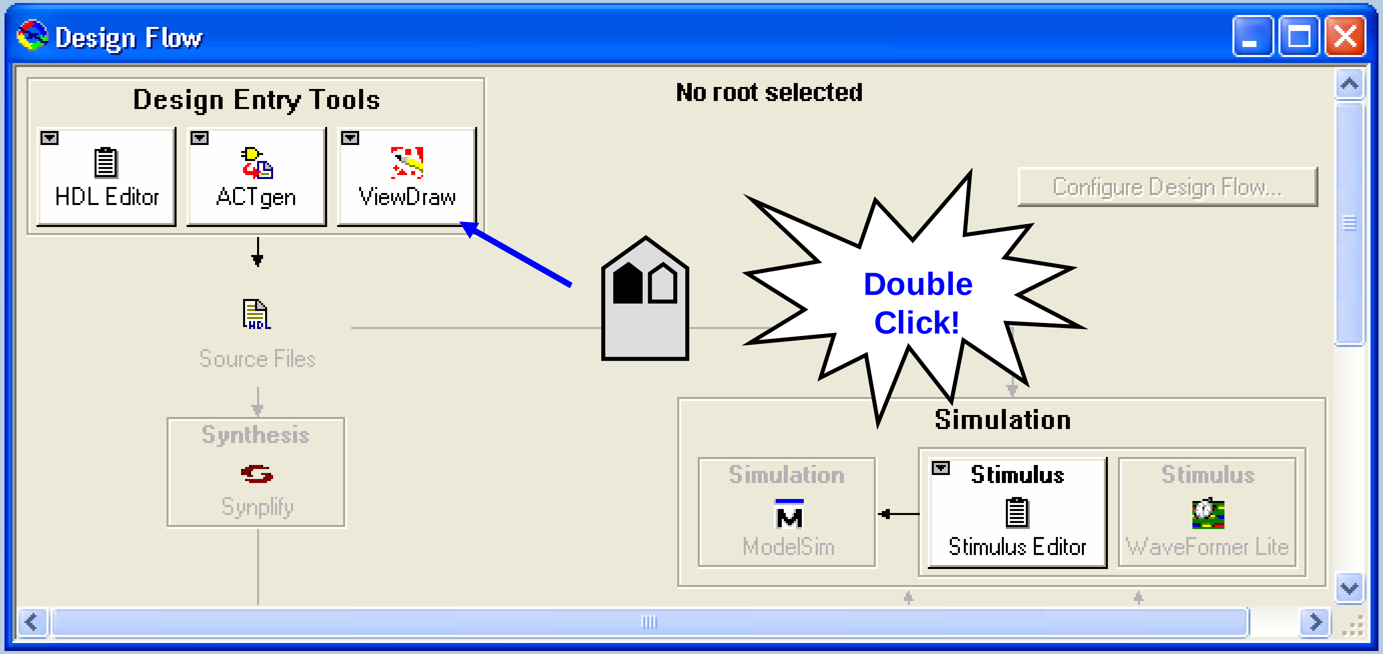
New

File Type:

Schematic
Symbol
ACTgen macro
VHDL Module
Stimulus

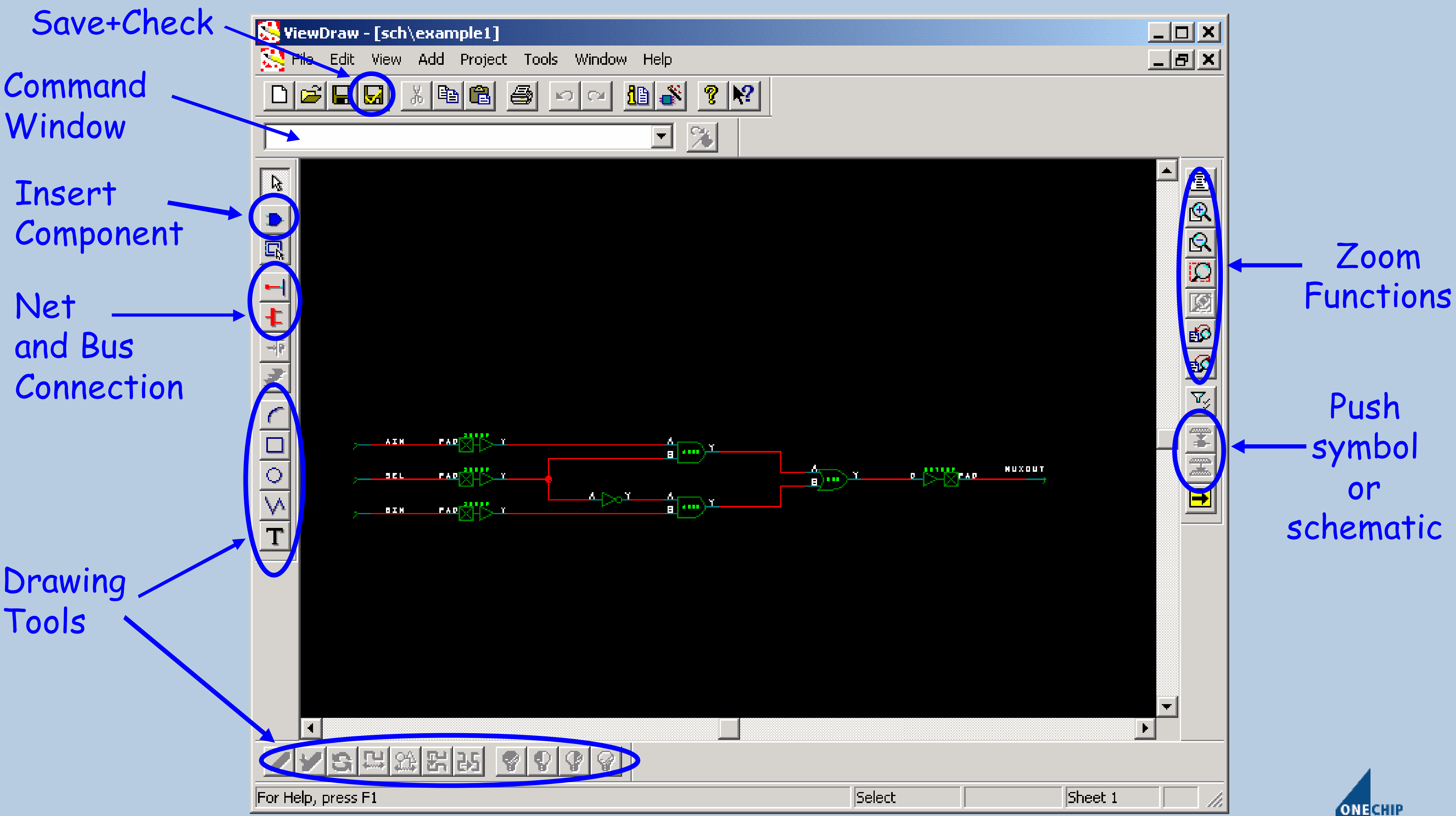
Name: mux21

Enter schematic name



Double Click!

# ViewDraw



Save+Check

Command Window

Insert Component

Net and Bus Connection

Drawing Tools

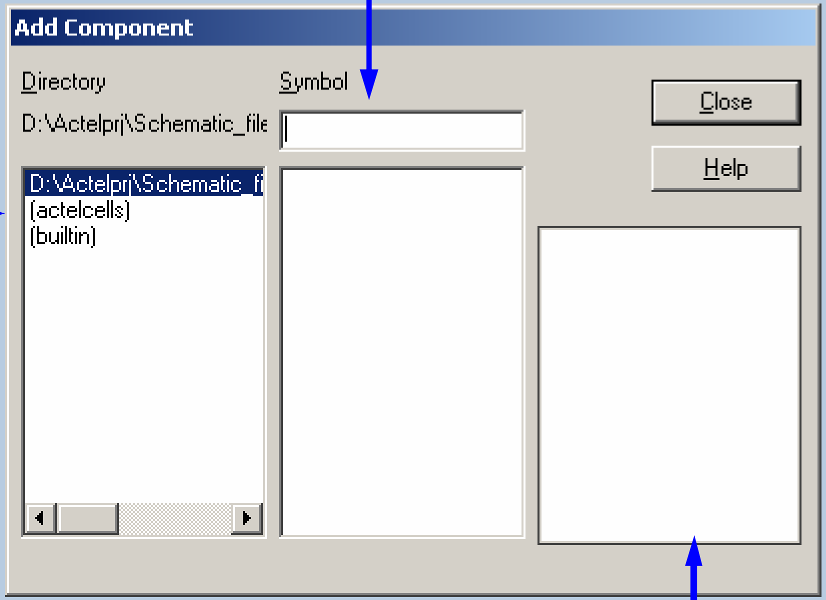
Zoom Functions

Push symbol or schematic

ViewDraw - [sch\example1]
File Edit View Add Project Tools Window Help
AIN
SEL
BIN
PAD
MUXOUT
For Help, press F1
Select
Sheet 1

# Inserting ViewDraw Components

- Add -> Component



Enter component name

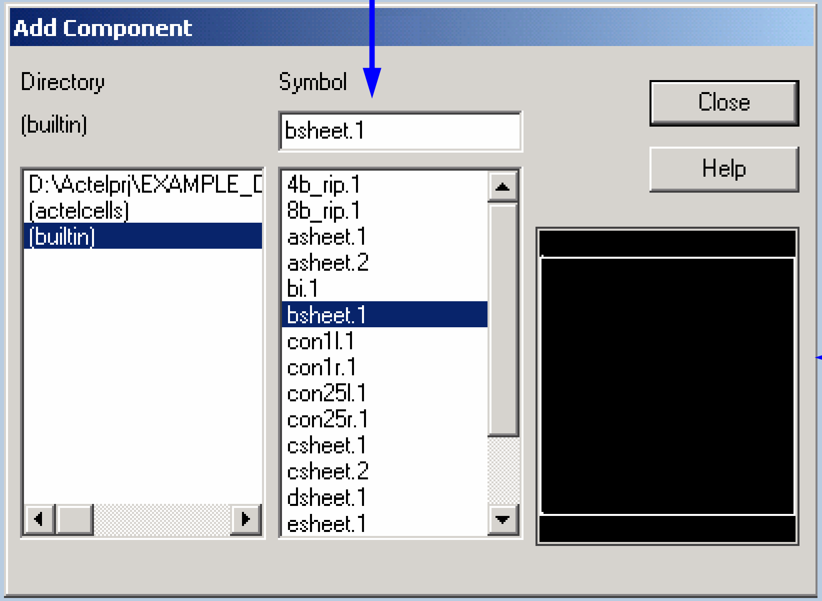
Select Directory
- Project directory
- Actel cells
- ViewDraw builtin

Component appears here
- Drag and drop into schematic

# Adding Schematic Border

- Built-in Library Contains Several Sheet Border Templates
  - Templates Can Be Modified

Enter sheet name (asheet, bsheet, etc.)



Add Component

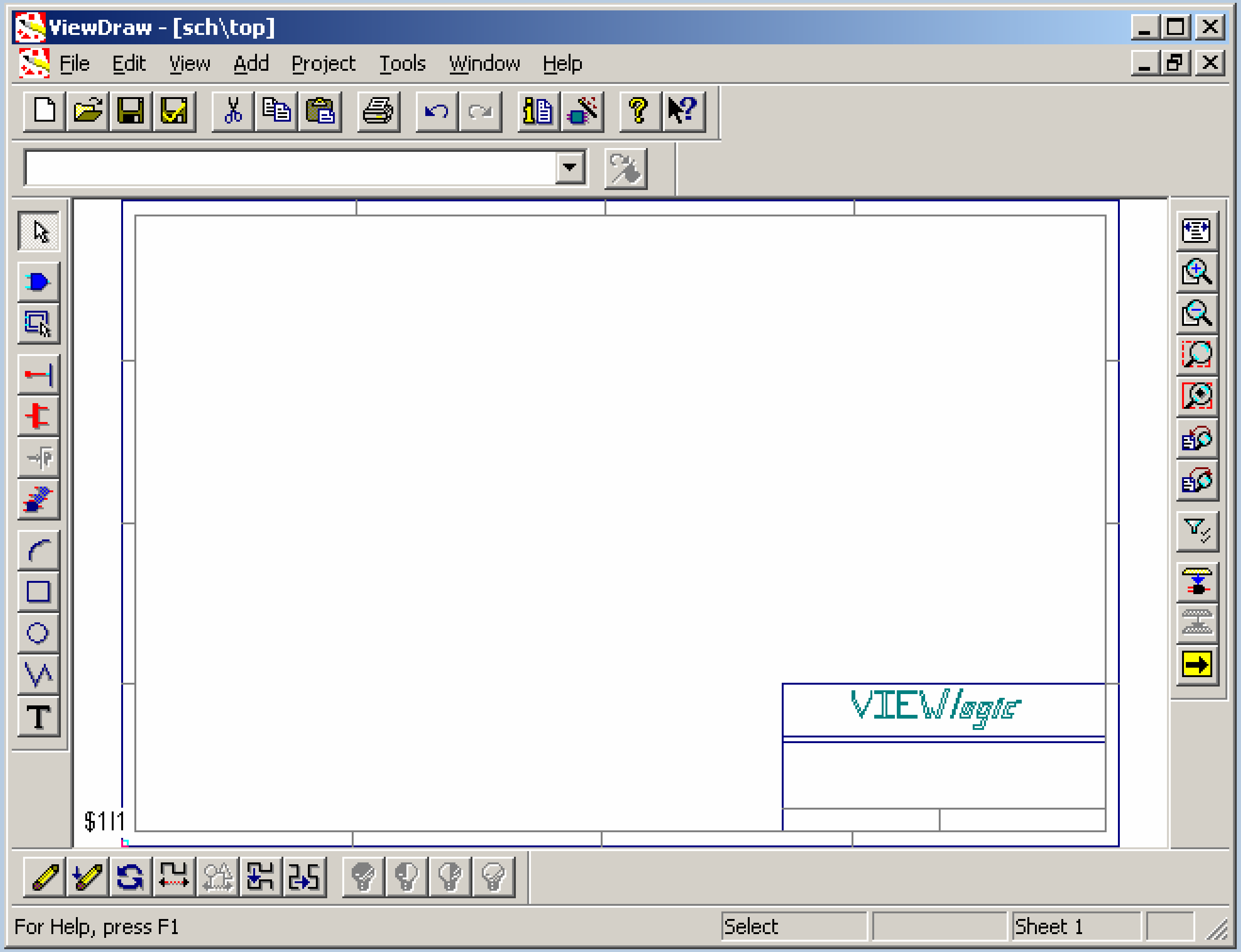
Directory: (builtin)

Symbol: bsheet.1

Select built-in library

Drag and drop into schematic

# ViewDraw Border in Schematic

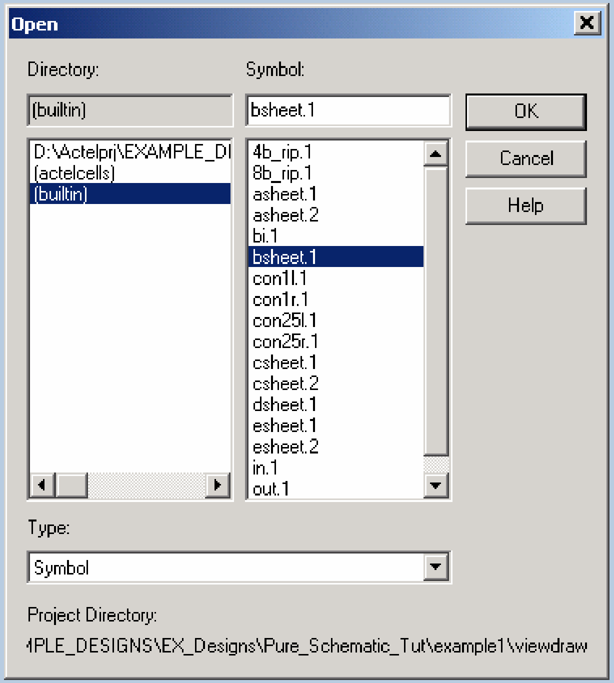


# Customizing a Schematic Border

- Border Template Can Be Customized
- Open Border (File > Open)
  - **Select Symbol from “Type” Menu**

Select built-in library

Select Symbol



Directory: (builtin)

D:\Actelprj\EXAMPLE_DI
(actelcells)
(builtin)

Symbol: bsheet.1

4b_rip.1
8b_rip.1
asheet.1
asheet.2
bi.1
bsheet.1
con1l.1
con1r.1
con25l.1
con25r.1
csheet.1
csheet.2
dsheet.1
esheet.1
esheet.2
in.1
out.1

Type: Symbol

Project Directory:
¬PLE_DESIGNS\EX_Designs\Pure_Schematic_Tut\example1\viewdraw

# Customizing a Schematic Border (cont.)

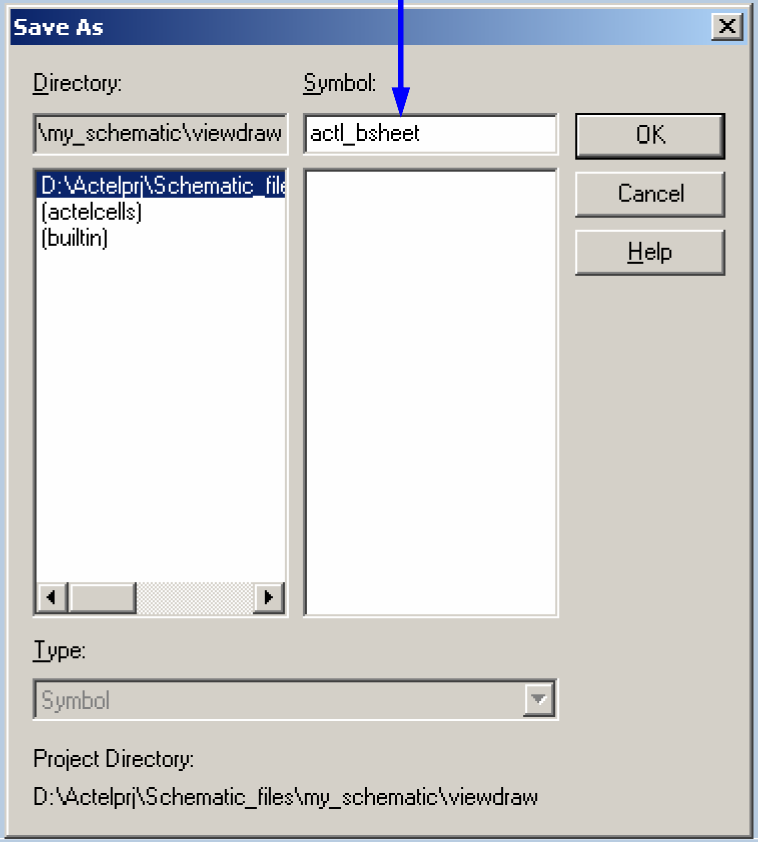
## Save File to New Name

- (File > Save Copy As <name>)
- Border Saved in Project Library
  - Visible on Libero File Manager Tab

Enter new sheet name

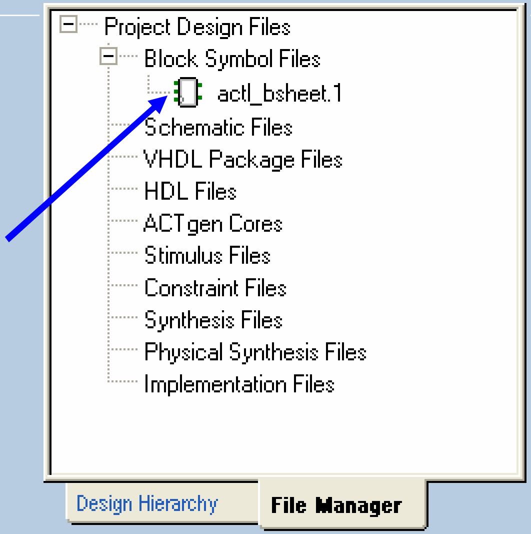
Select project library

Select Symbol



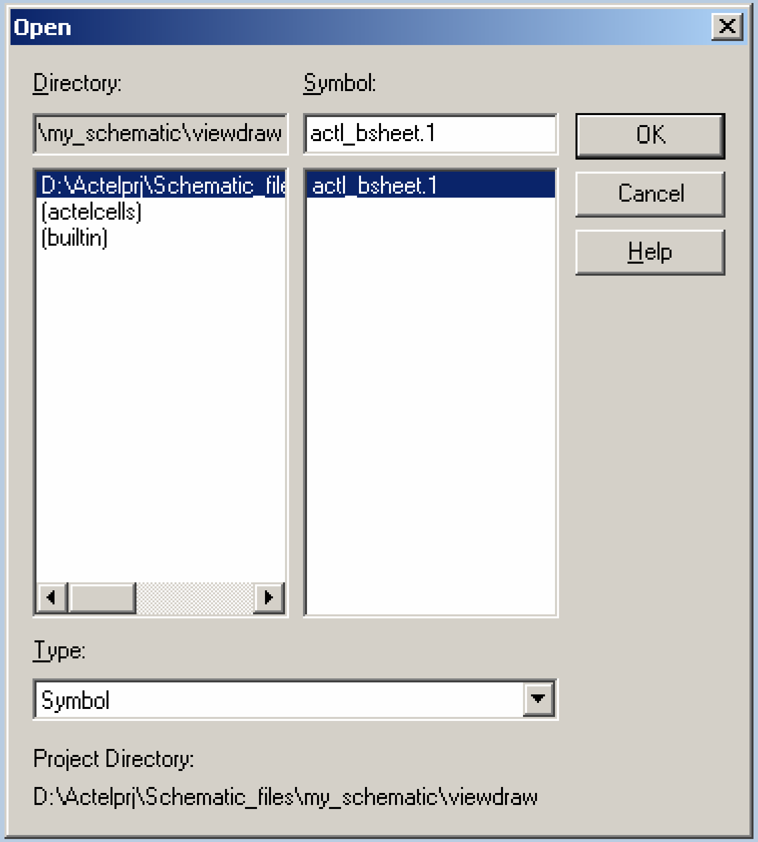
# Customizing a Schematic Border (cont.)

- Open Saved Border and Edit (File > Open)
  - **Add Lines, Arcs, Text, etc. as Necessary**



Project Design Files
Block Symbol Files
actl_bsheet.1
Schematic Files
VHDL Package Files
HDL Files
ACTgen Cores
Stimulus Files
Constraint Files
Synthesis Files
Physical Synthesis Files
Implementation Files

Modified border visible on File Manager tab



Open

Directory: \my_schematic\viewdraw

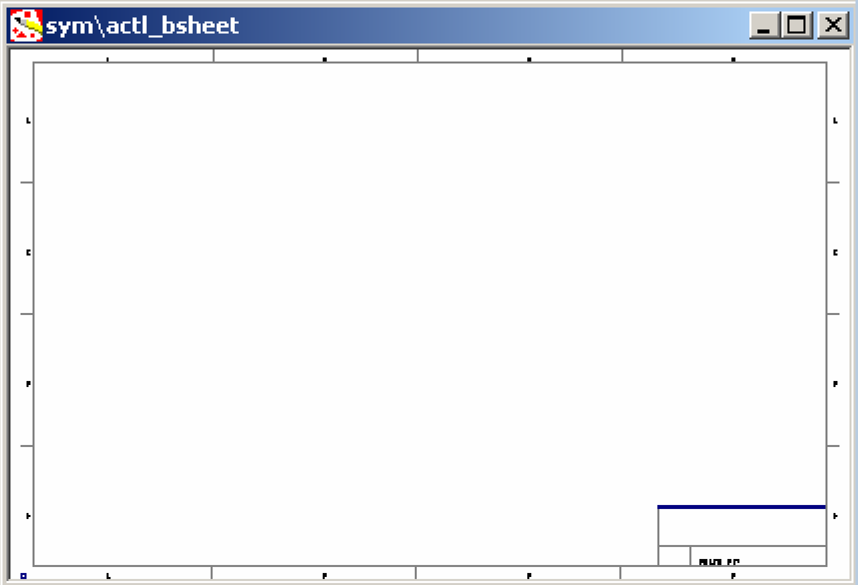
Symbol: actl_bsheet.1

D:\Actelprj\Schematic_file
(actelcells)
(builtin)

actl_bsheet.1

Type: Symbol

Project Directory:
D:\Actelprj\Schematic_files\my_schematic\viewdraw

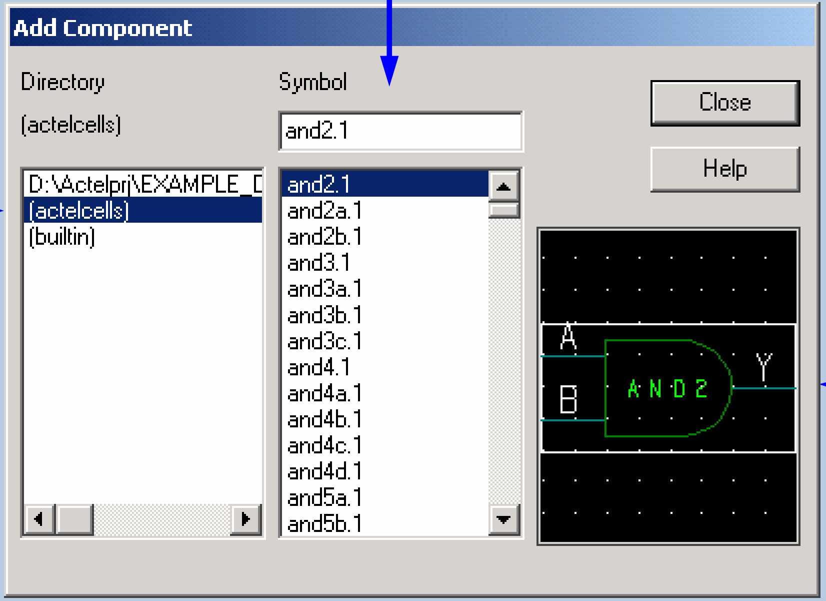


sym\actl_bsheet

# Adding Schematic Components

## Add > Component from ViewDraw Menu

- **Add SmartGen Macros, Custom Macros or Actel Basic Cells**
  - **Select VCC or GND from 'actelcells'**



Add Component

Directory: (actelcells)

Symbol: and2.1

Enter cell name

Select cell library

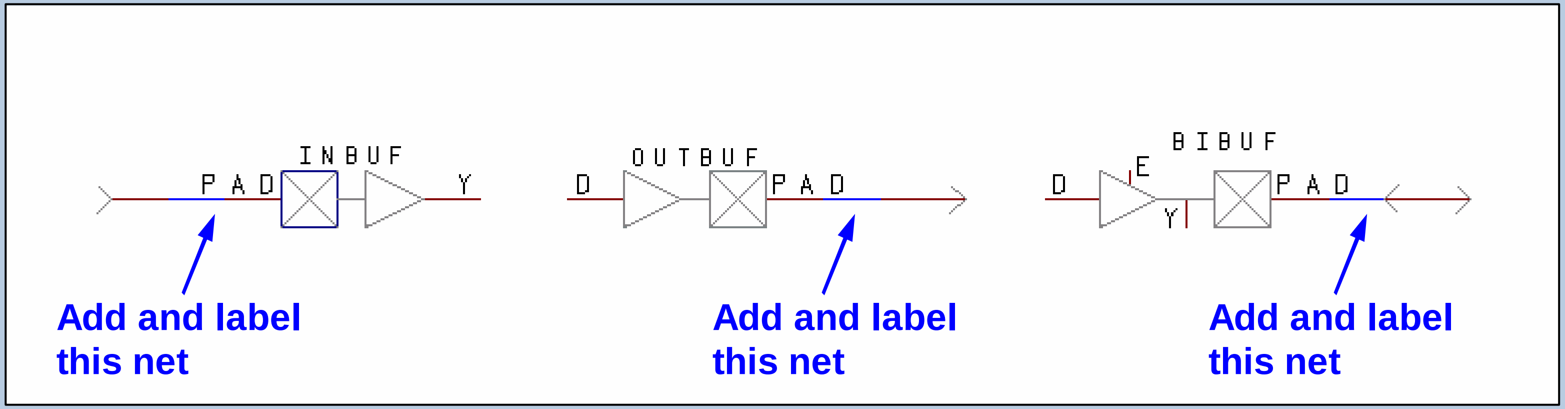
Drag and drop into schematic

# Drawing Wires and Busses
## *Adding a Net*

- To Add Net:
  - **Choose Add > Net (or Add > Bus)**
    - **Alternate: Click Wire ( ) or Bus ( ) Icon on Toolbar**
  - **Specify Net Origination Point and Depress Left Mouse Button**
  - **Drag Mouse to Form Net (or Bus), specifying Points along Net by Clicking Right Mouse Button**
  - **Click Right Mouse Button to Insert Vertex in Net**
  - **Release Left Mouse Button to Specify Ending Point for Net**

# Adding I/O Cells

- Add I/O Cells to Top-level Design Schematic
  - **Schematic-only Designs or Structural Schematic Designs**
  - **Macros Contained in "actelcells" Component Library**
- I/O Cells Must Have Dangling Hierarchical Connector Attached to Pad Side
  - **Label Dangling Connector**
- I/O Macros Can Be Buried in Hierarchy



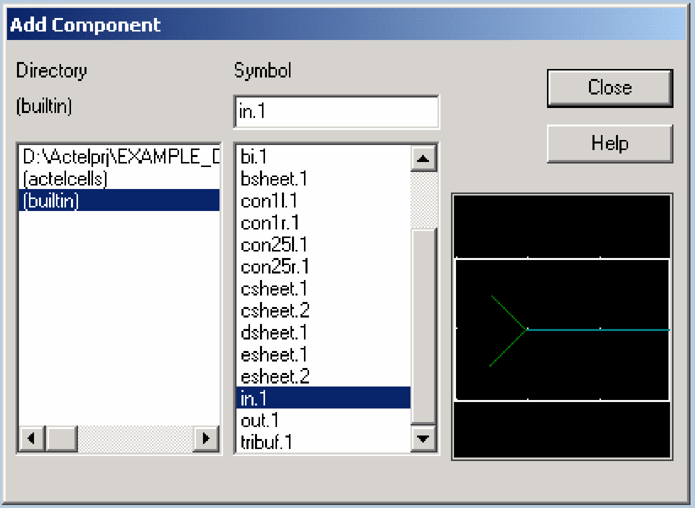
**Add and label this net**

**Add and label this net**

**Add and label this net**

# Hierarchical Connectors

- Use Hierarchical Connectors from ViewDraw Built-in Library for All Designs
  - **Add just like Any Other Component**
  - **Same Connector for Wire or Bus**
  - **Called ‘in’, ‘out’, or ‘bi’ in *Built-in* Libr**
- Label Net or Bus Next to Connector

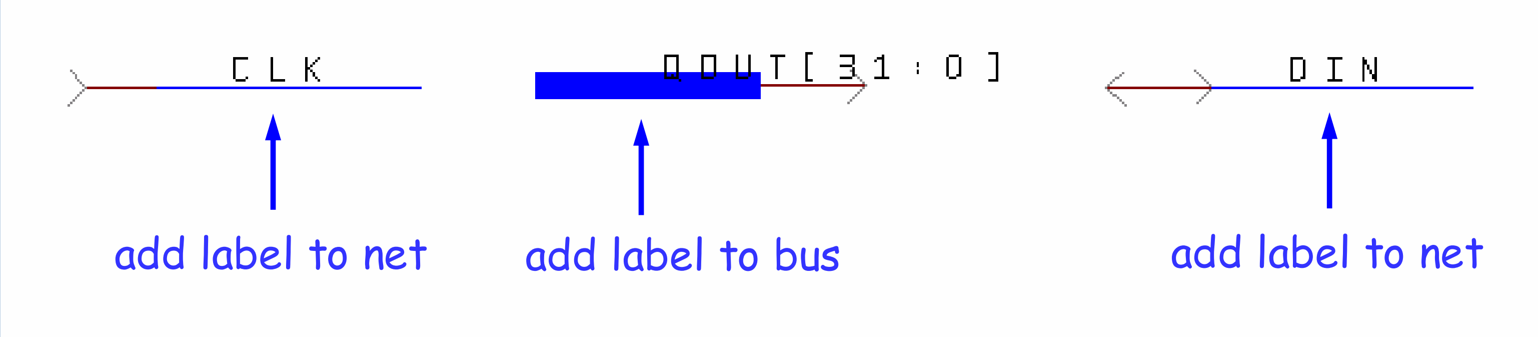

Add Component

Directory: (builtin)

Symbol: in.1

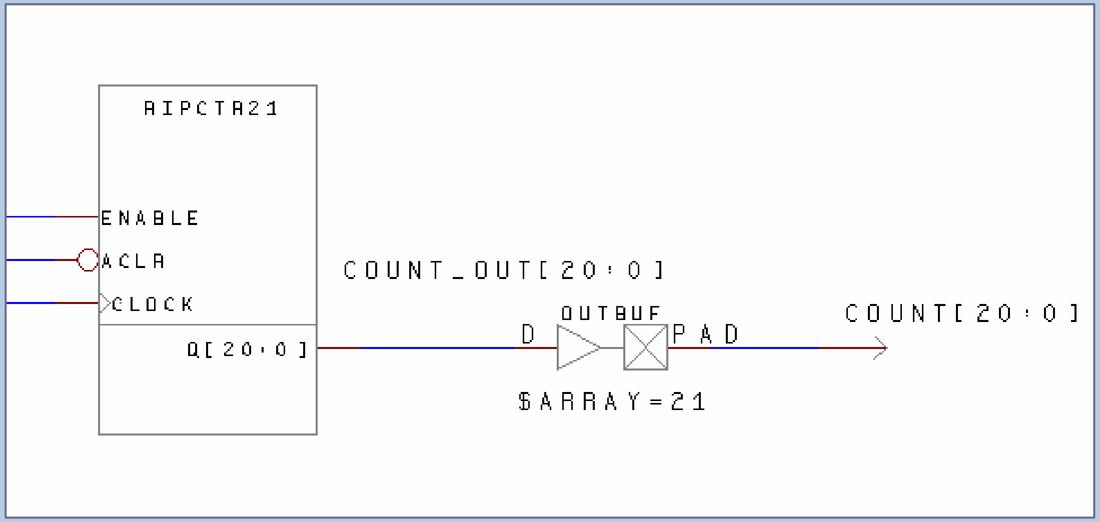
D:\Actelprj\EXAMPLE_D
(actelcells)
(builtin)

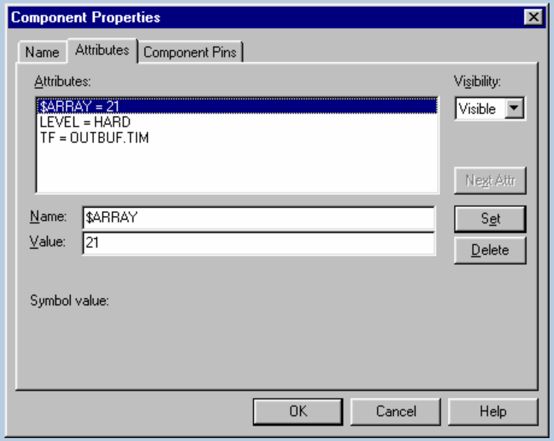
bi.1
bsheet.1
con1l.1
con1r.1
con25l.1
con25r.1
csheet.1
csheet.2
dsheet.1
esheet.1
esheet.2
in.1
out.1
tribuf.1



# ViewDraw Attributes

- A *Limited* Number of Attributes Can Be Entered into Schematic and Passed to Designer
- $Array Attribute
  - **Creates Arrays of Cells in Schematic**
    - **Useful for I/O Buffers**
  - **Double-click Cell, Enter on Attribute Tab**





Attributes:

```
$ARRAY = 21
LEVEL = HARD
TF = OUTBUF.TIM
```

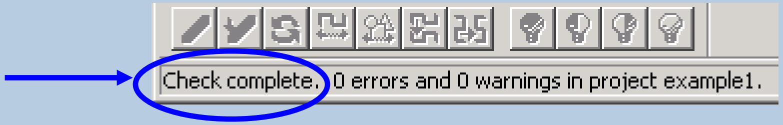
Name: $ARRAY

Value: 21

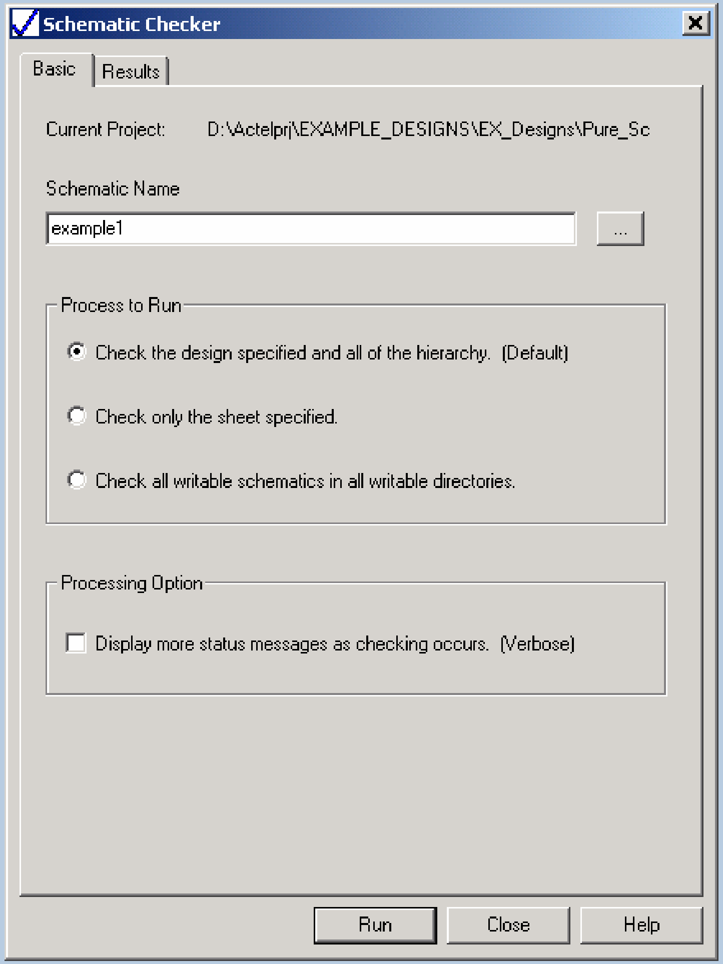
# Design Rule Checking

- At Design Entry Completion , Save and Check Design
  - Click Save Check Icon
  - Use Tools > Schematic Checker

**Viewdraw Status Bar:**



Check complete. 0 errors and 0 warnings in project example1.



Schematic Checker

Basic | Results

Current Project: D:\Actelprj\EXAMPLE_DESIGNS\EX_Designs\Pure_Sc

Schematic Name

example1

Process to Run

● Check the design specified and all of the hierarchy. (Default)

○ Check only the sheet specified.

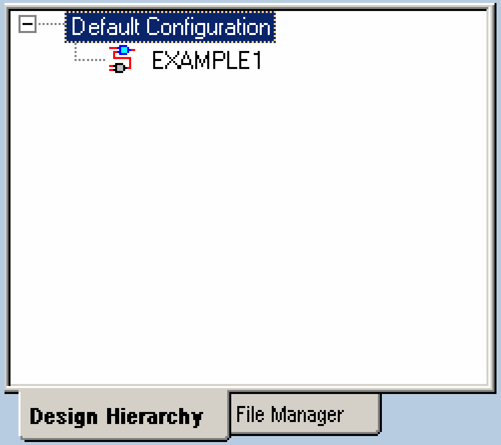
○ Check all writable schematics in all writable directories.

Processing Option

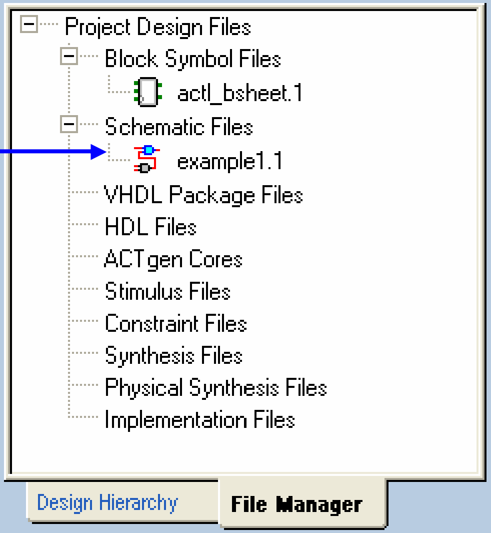
□ Display more status messages as checking occurs. (Verbose)

# Design Entry Completion

- Files in Implementation Are Displayed on Libero Design Hierarchy and File Manager Tabs

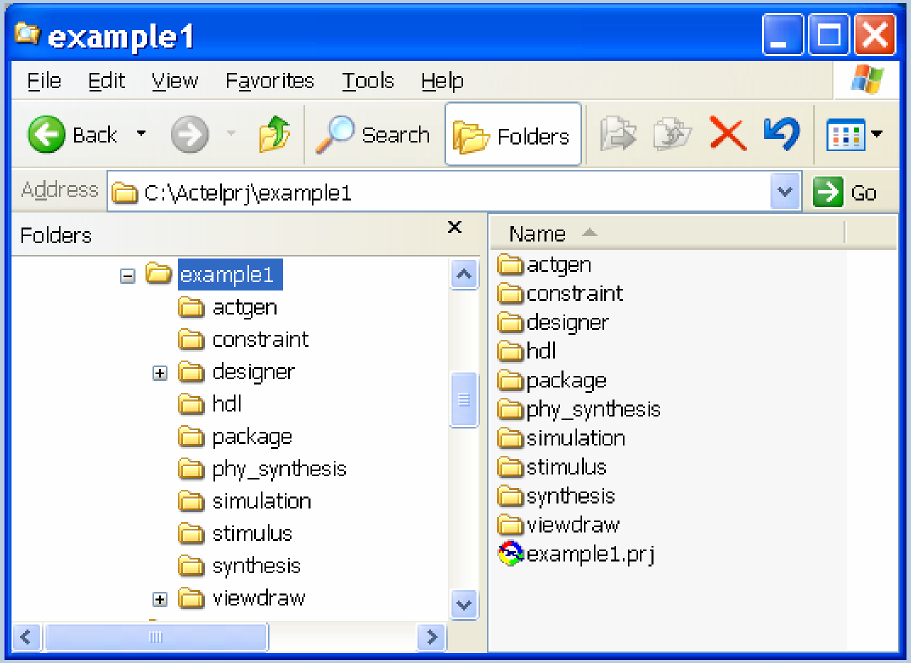


Schematic



# ViewDraw File Structure on HDD

- Schematic Files Saved in “sch” Folder
- Symbol Files Saved in “sym” Folder
- Wire Files Saved in “wir” Folder
- Files Visible on Libero File Manager Tab

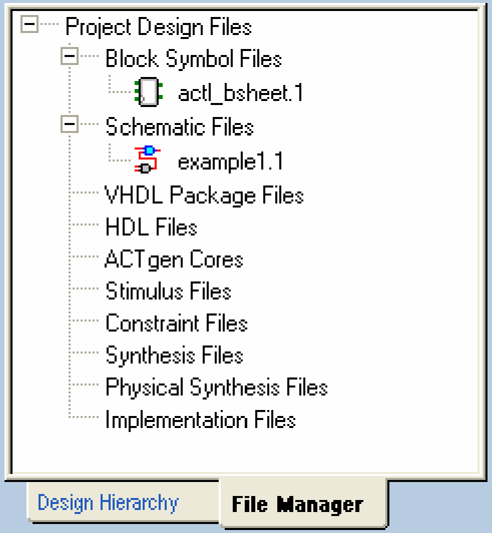


example1

Address C:\Actelprj\example1

Folders: example1, actgen, constraint, designer, hdl, package, phy_synthesis, simulation, stimulus, synthesis, viewdraw

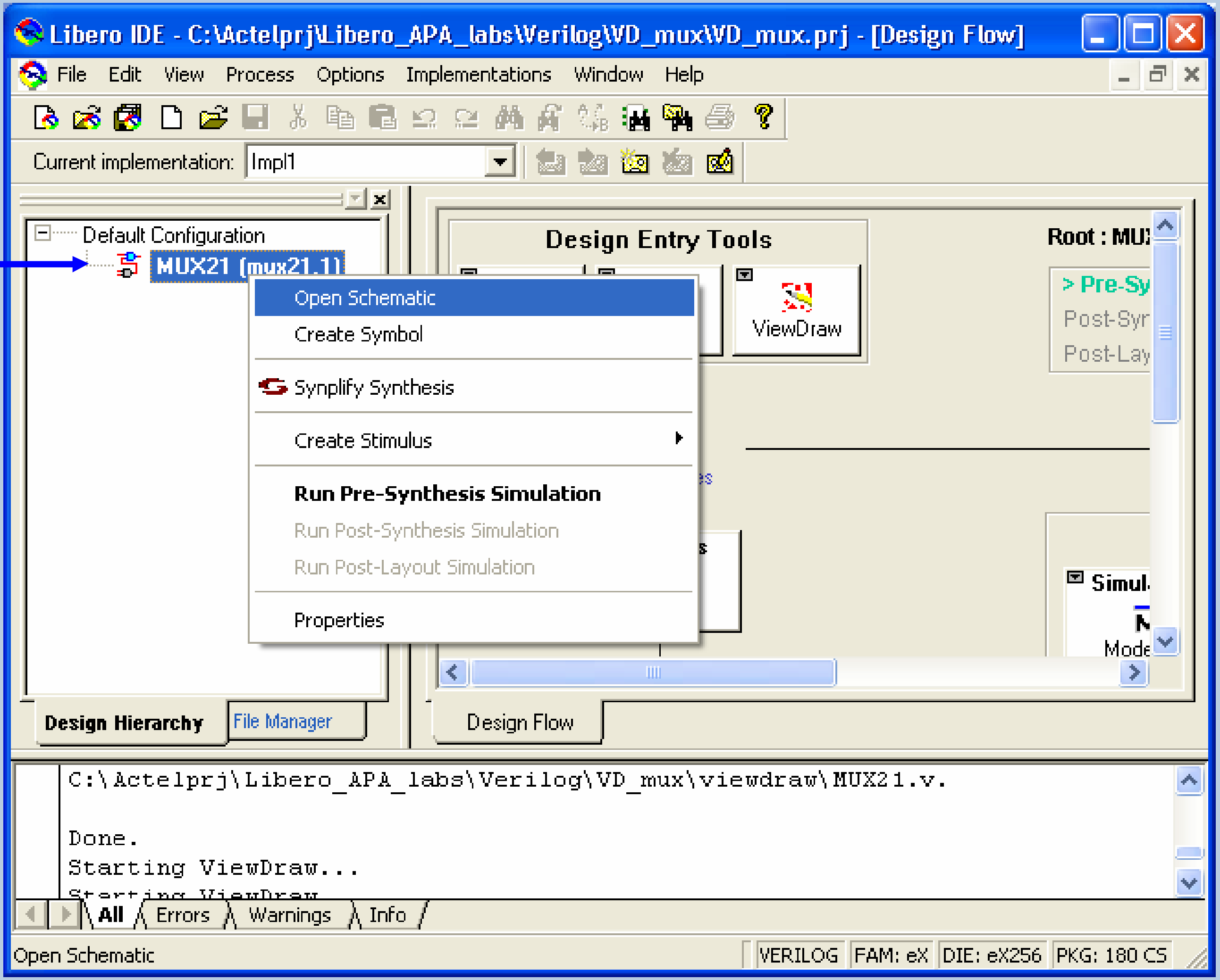
Name: actgen, constraint, designer, hdl, package, phy_synthesis, simulation, stimulus, synthesis, viewdraw, example1.prj



- Project Design Files
  - Block Symbol Files
    - actl_bsheet.1
  - Schematic Files
    - example1.1
  - VHDL Package Files
  - HDL Files
  - ACTgen Cores
  - Stimulus Files
  - Constraint Files
  - Synthesis Files
  - Physical Synthesis Files
  - Implementation Files

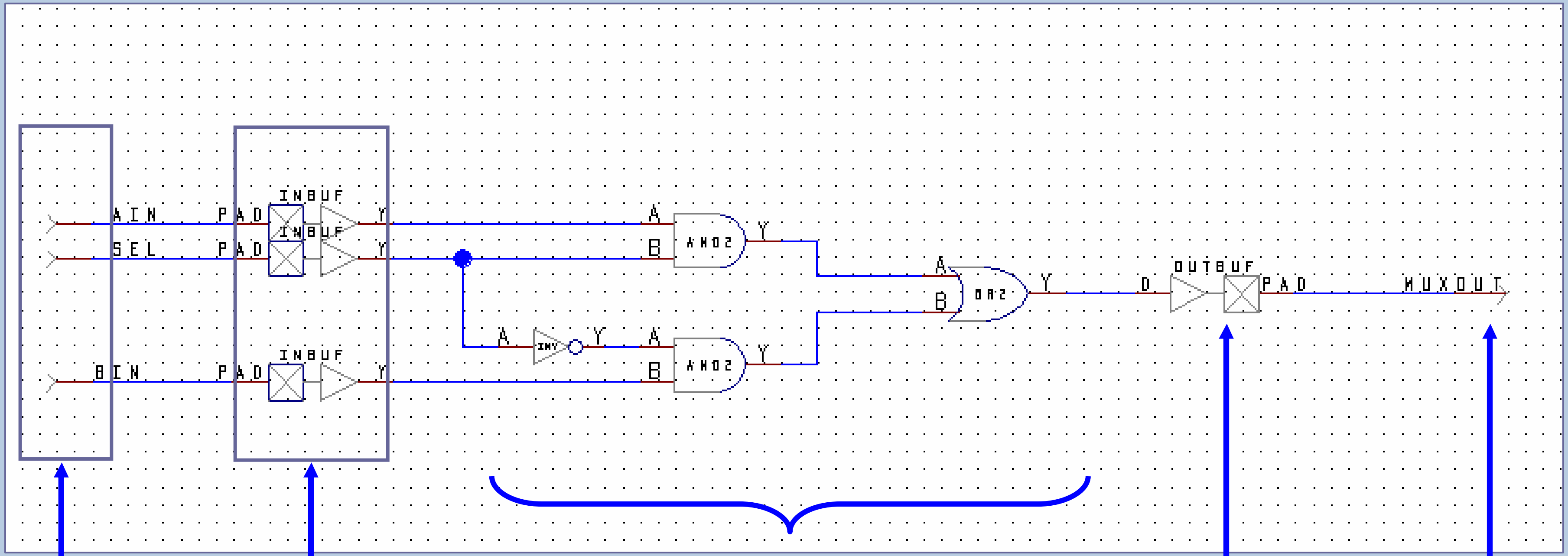
# Opening Existing Schematics

Right Mouse Click!



```
C:\Actelprj\Libero_APA_labs\Verilog\VD_mux\viewdraw\MUX21.v.

Done.
Starting ViewDraw...
Starting ViewDraw
```

# Completed Schematic



Input buffers

Actel library components

Output buffer

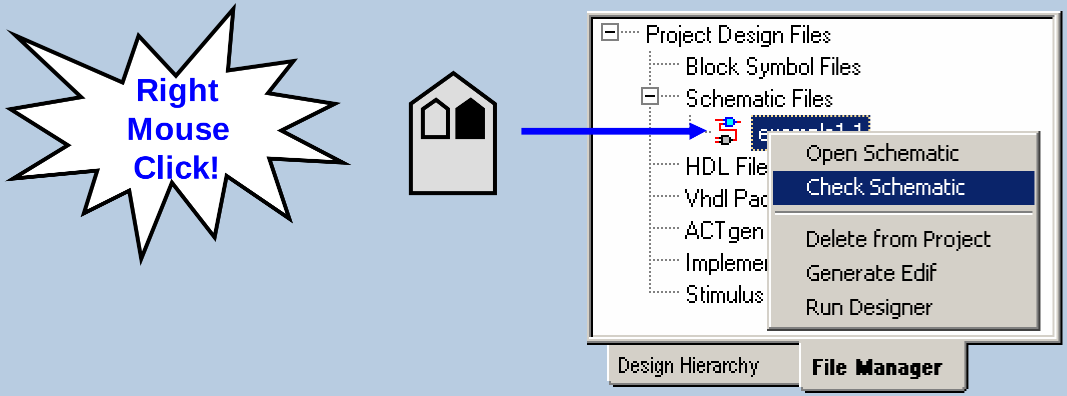
Hierarchical connectors

Hierarchical connector

# Libero Schematic Checker (Optional)

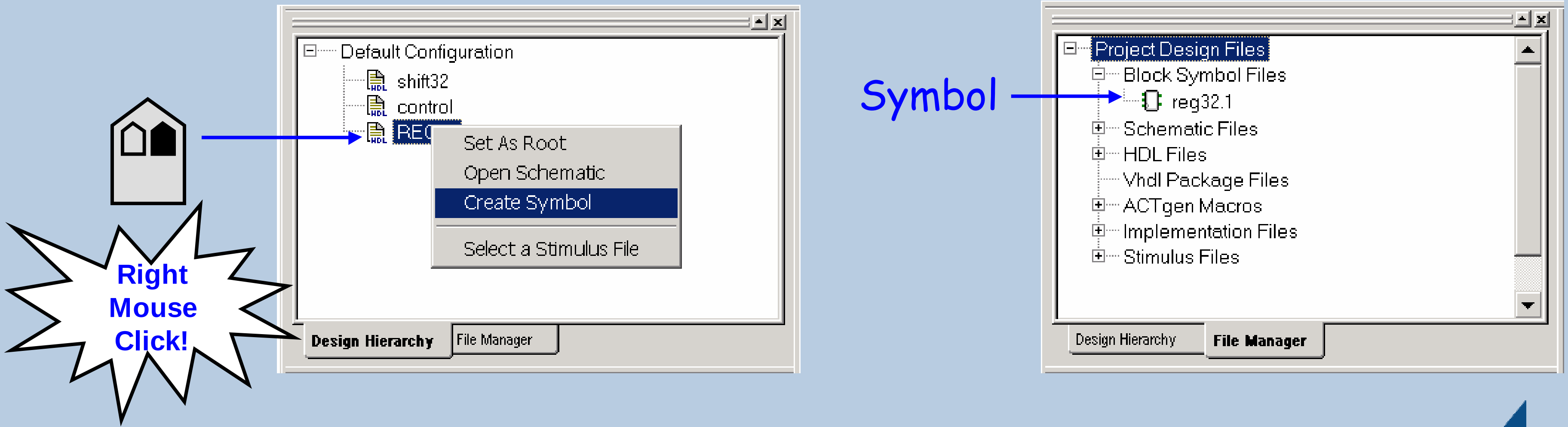
## Schematic Connectivity Checker in Libero

- **Checks for Errors Not Included in ViewDraw Save + Check**
- **Optional Step Available from File Manager Tab**

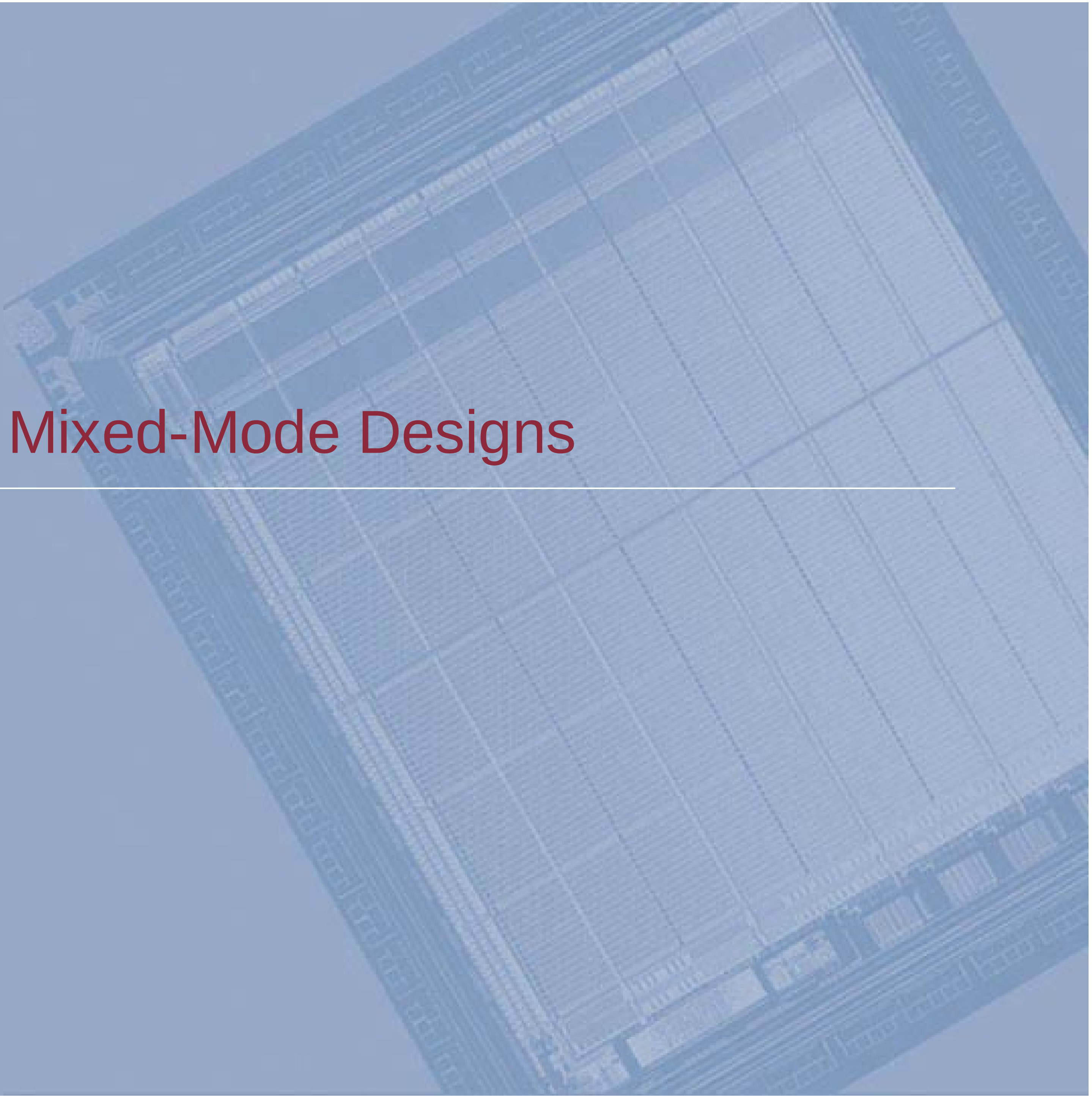


# Structural Schematic Flow
## *Using SmartGen Macros*

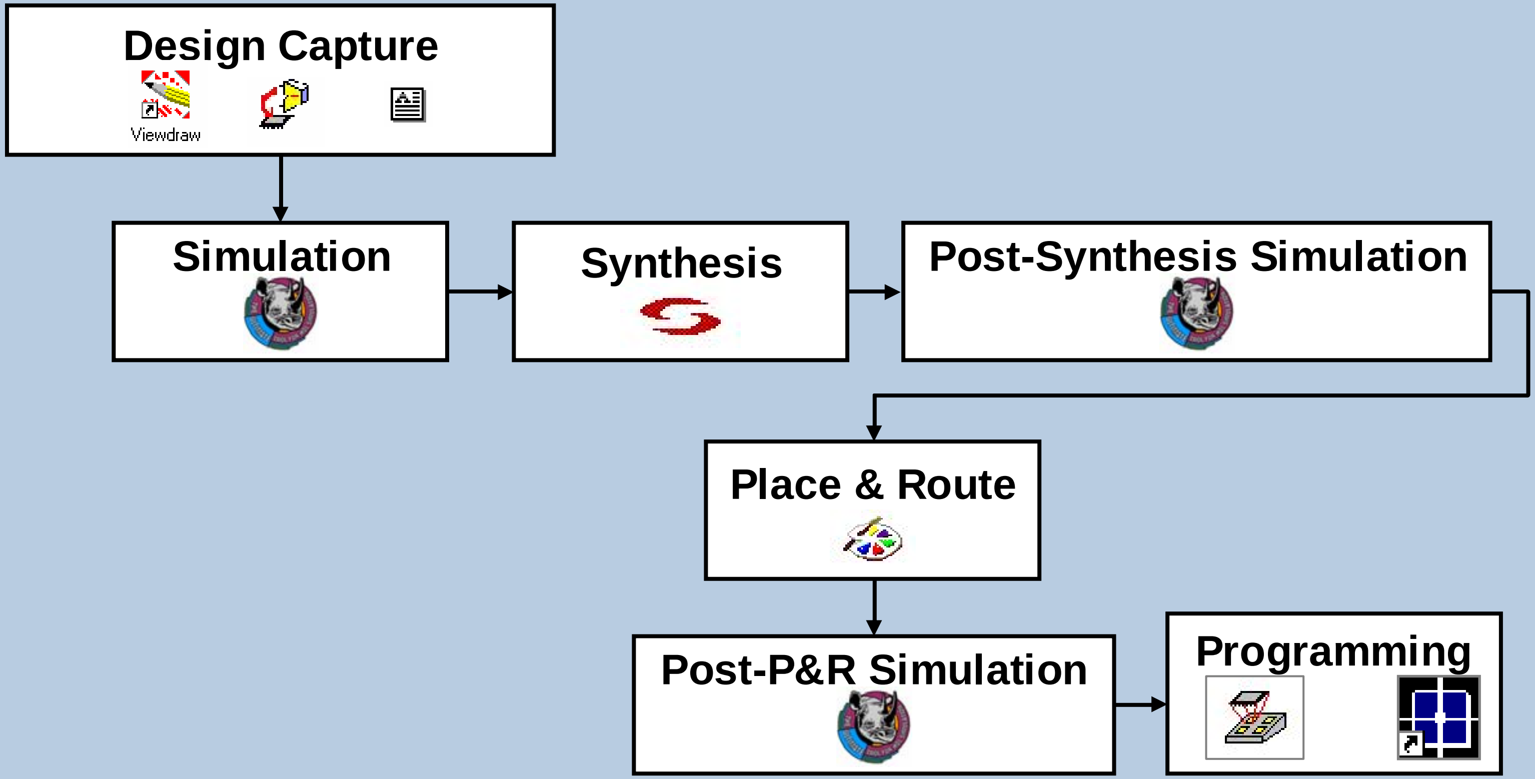
- **Launch SmartGen from Libero Project Manager**
- **Create HDL Structural Implementation**
  - **VHDL or Verilog**
- **Create ViewDraw Symbol from Libero and Instantiate Symbol in Schematic**
  - **Symbol Visible on File Manager Tab**



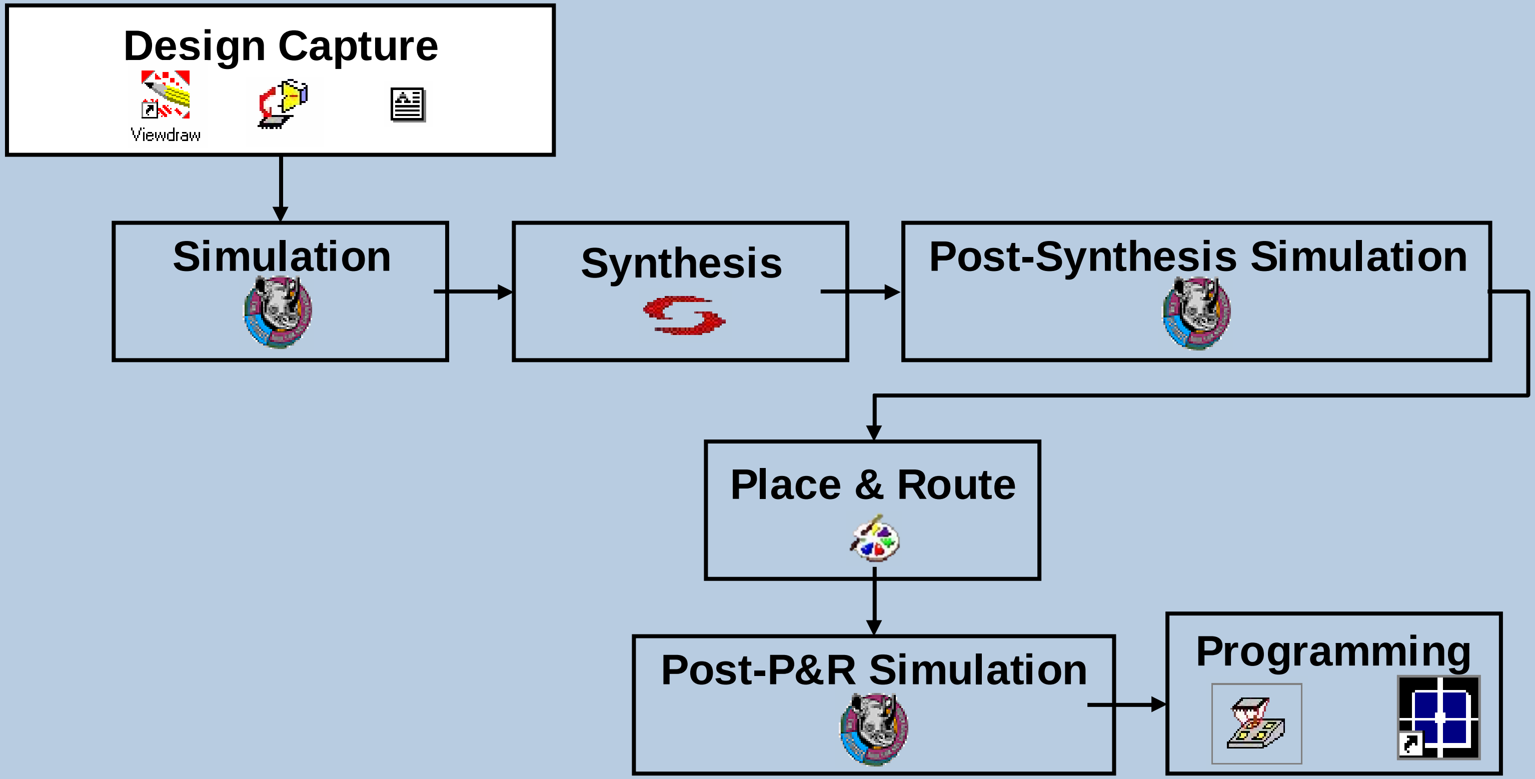
# Mixed-Mode Designs



# Mixed-Mode Design Flow

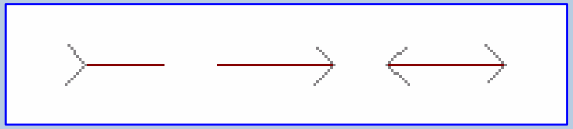


# Design Capture



# Mixed Mode Design Entry

- Mixed Mode => RTL Blocks within Schematic
  - **HDL Blocks Can Be Structural or Behavioral RTL**
    - **RTL Blocks Can Be VHDL or Verilog (But Not Both)**
  - **Top Level *Must* Be Schematic**
- Procedure
  - **Create HDL Blocks**
    - **RTL Blocks - Use HDL Editor or Import Existing Design Files**
    - **Structural Blocks - Use HDL Editor or SmartGen**
  - **Create ViewDraw Symbols for HDL Blocks**
    - **Done Automatically from Libero Design Flow Manager**
  - **Instantiate Blocks in Schematics and Make Interconnects**
    - **Use Hierarchical Connectors from ViewDraw “built-in” Library for HDL Ports in Schematic**

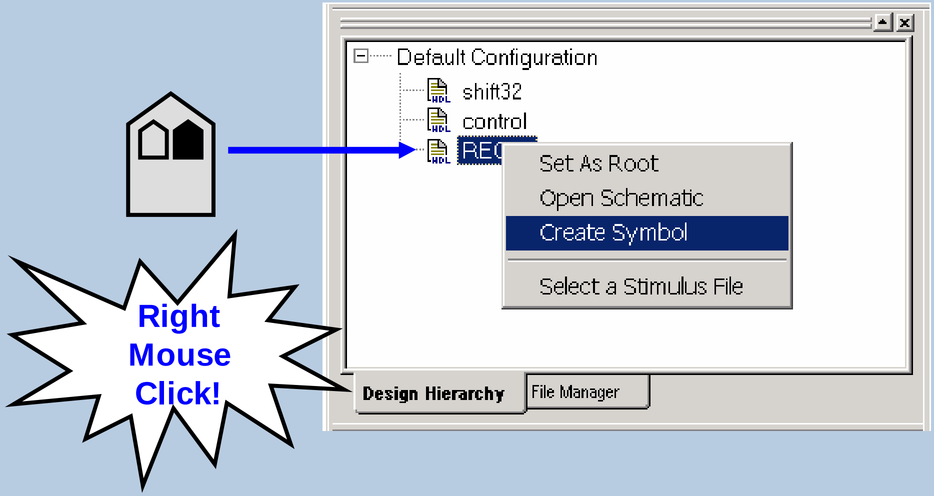


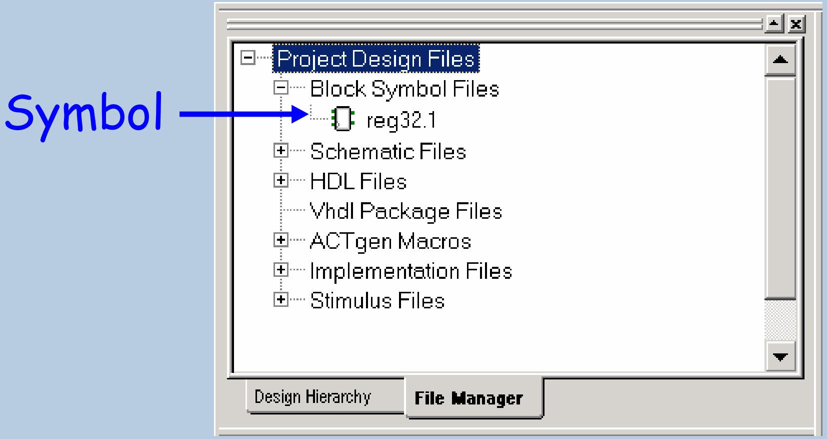
# RTL in Mixed-Mode Flow

- Create RTL from Libero HDL Editor or Import File

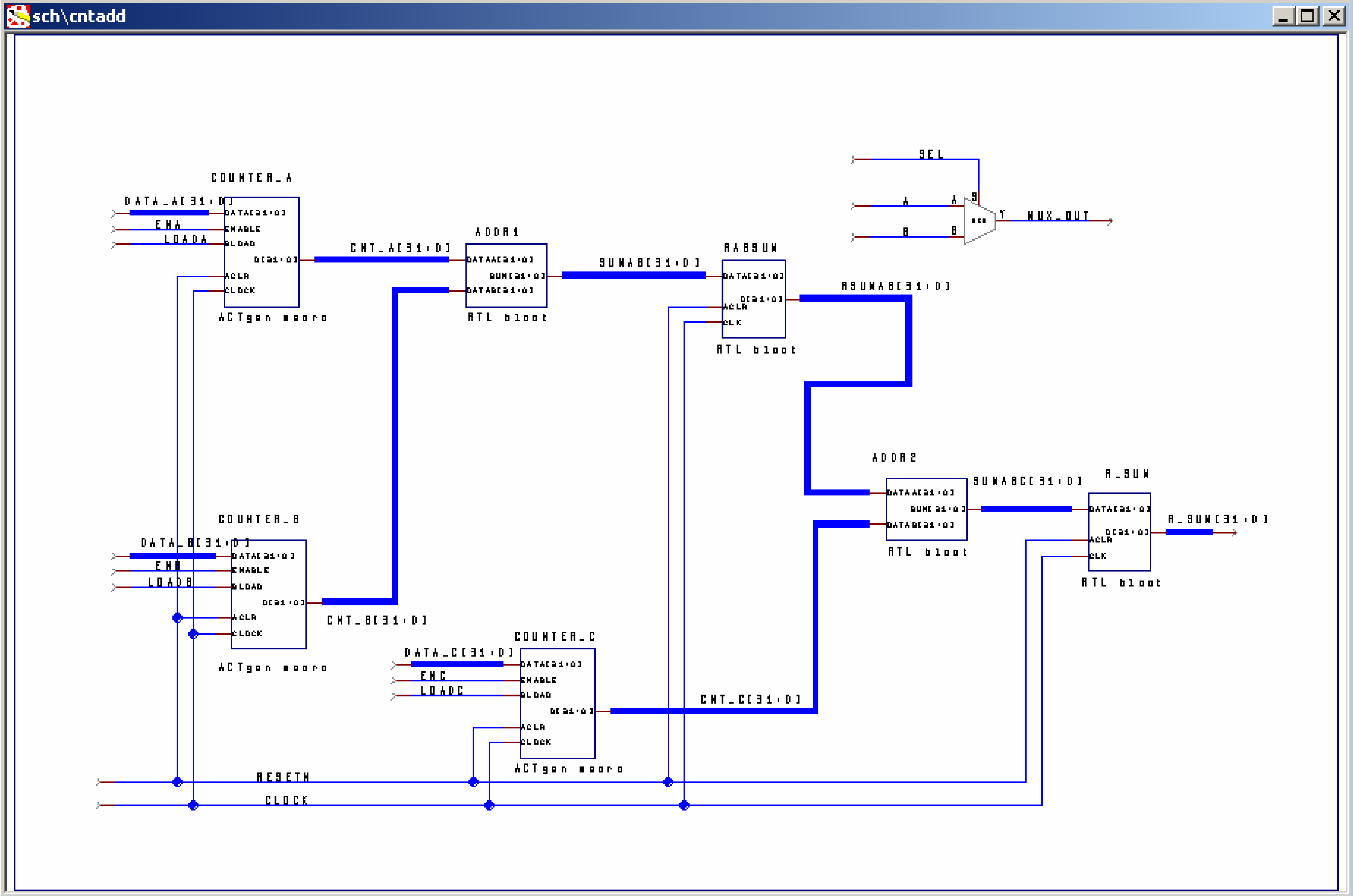
OR

- Create HDL Structural Implementation using SmartGen
  - VHDL or Verilog
- Create ViewDraw Symbol from Libero Instantiate Symbol in Schematic
  - Symbol Appears on File Manager Tab



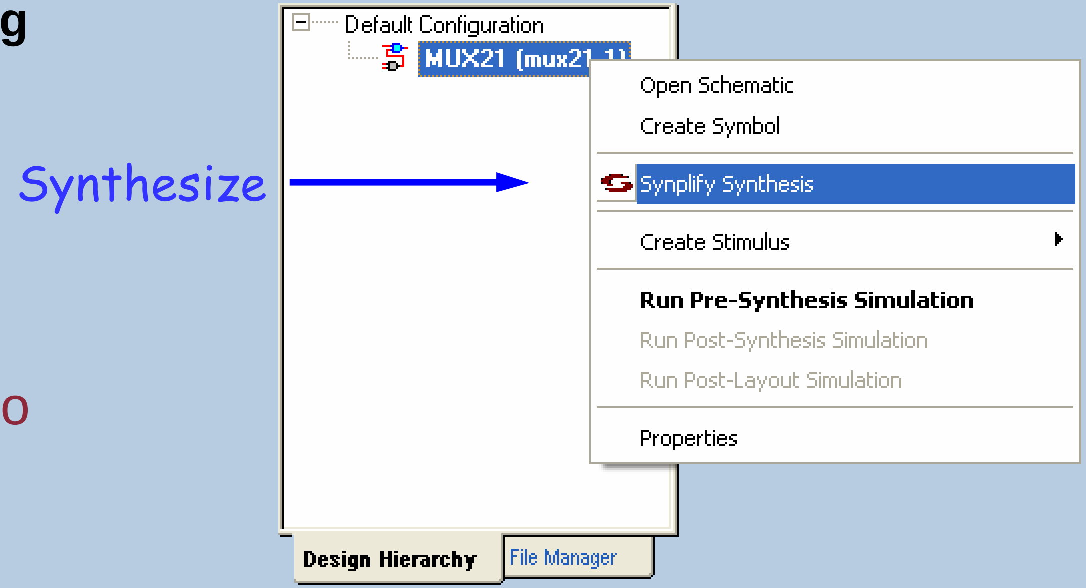


# Mixed Mode Schematic

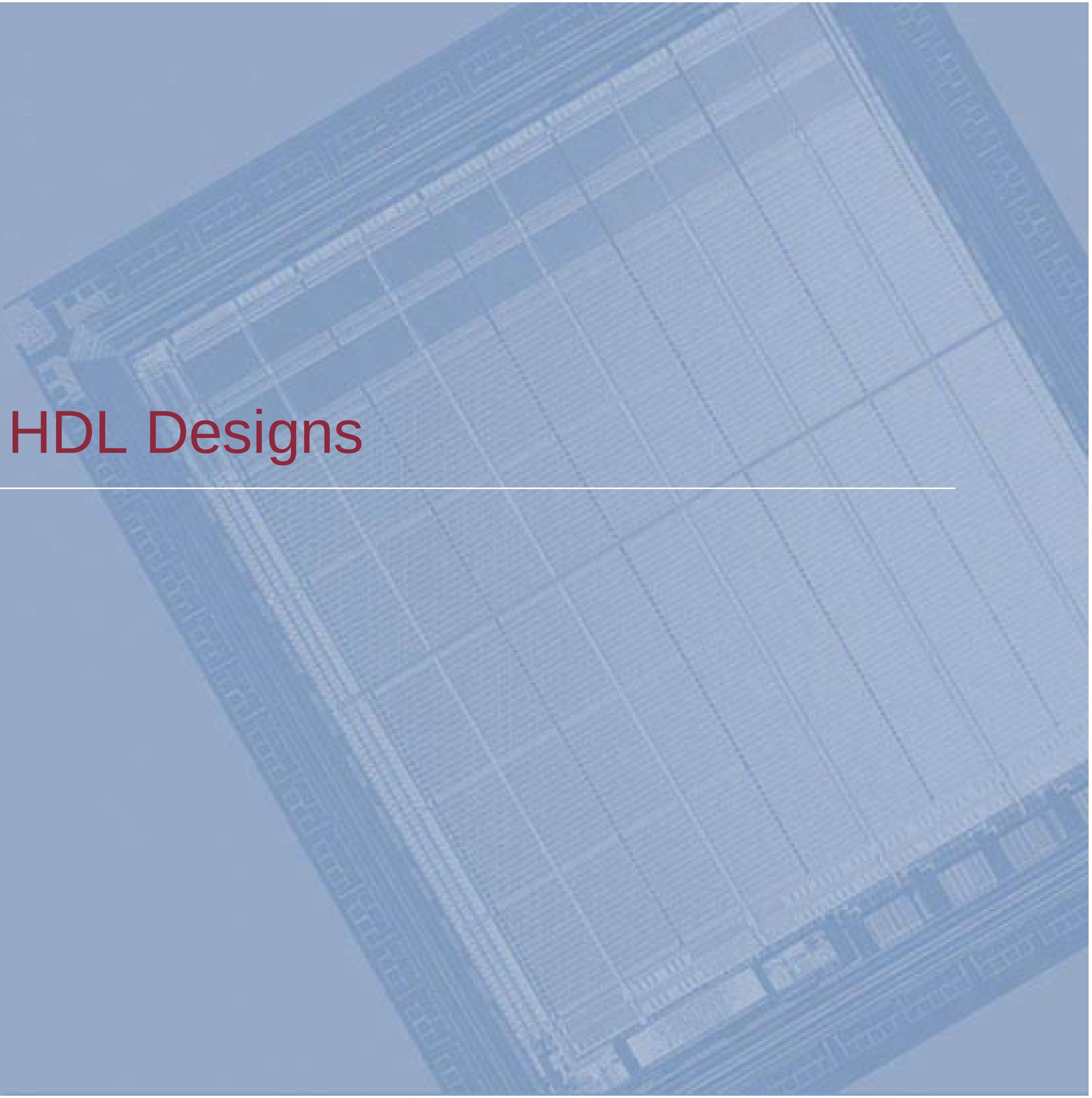


# Synthesize

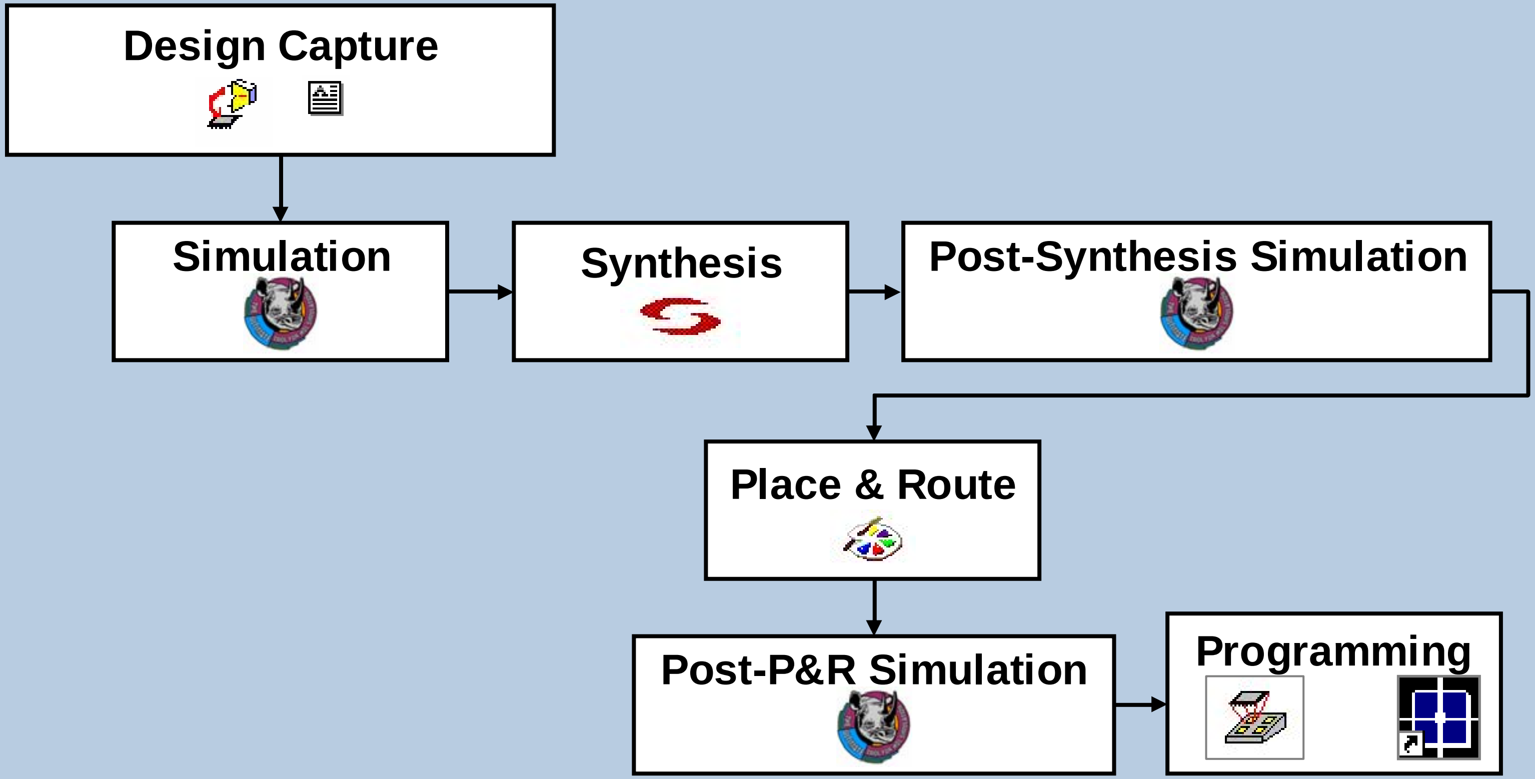
- Optional for Pure Schematic or Structural Schematic Flows
  - *All* HDL Blocks Are Structural VHDL or Verilog (e.g., SmartGen Blocks)
- Required for Mixed-mode Designs
  - Designs Containing RTL Blocks
- Libero Launches Synplicity to Insert Pads and Optimize Design
  - Hierarchical Connectors Must Be Used
  - Structural Schematics with All Pads Instantiated Can Go Directly to Designer Tool



# HDL Designs



# HDL Design Flow



Design Capture

Simulation

Synthesis

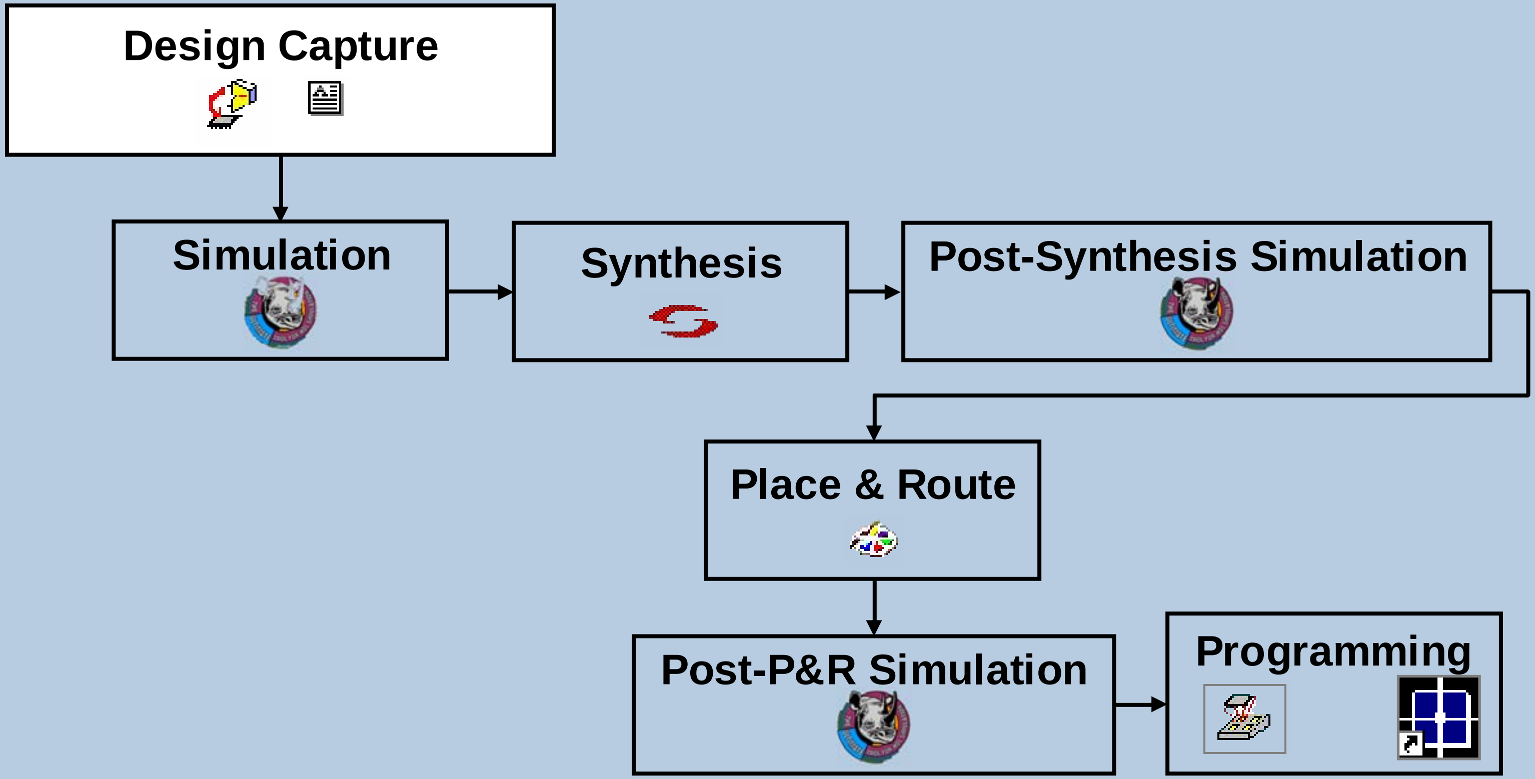
Post-Synthesis Simulation

Place & Route

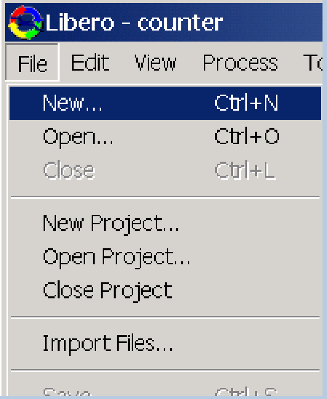
Post-P&R Simulation

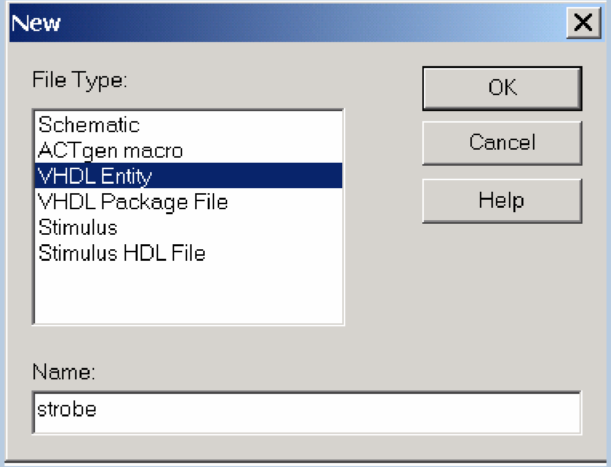
Programming

# Design Capture



# Creating New HDL Macros

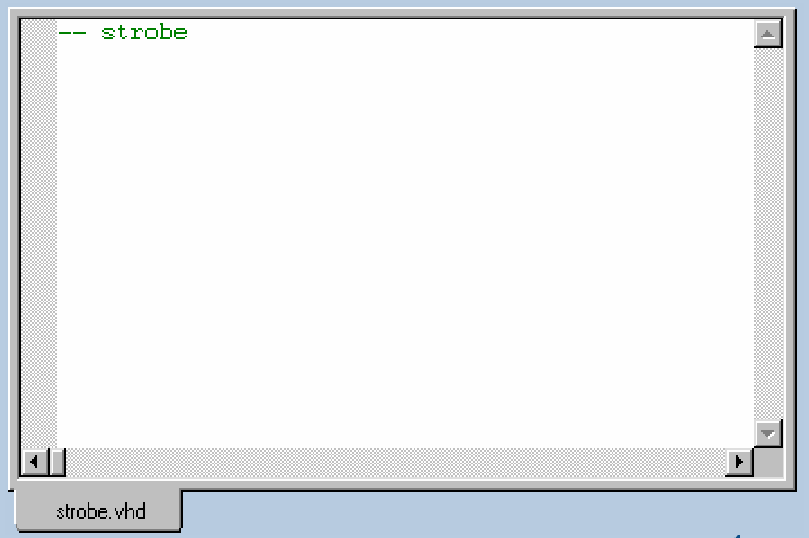




File Type:

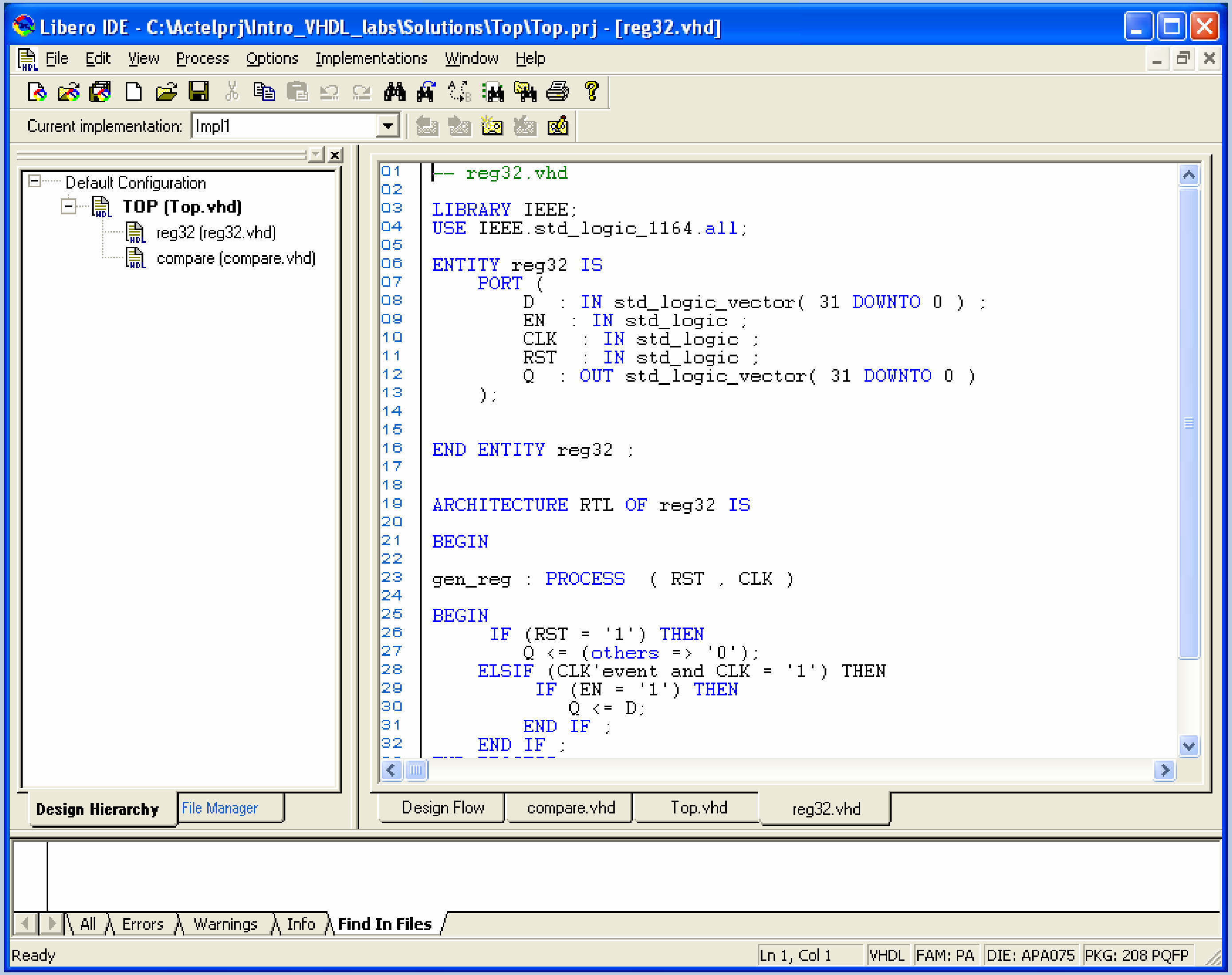
- Schematic
- ACTgen macro
- VHDL Entity
- VHDL Package File
- Stimulus
- Stimulus HDL File

Name: strobe



```
-- strobe
```

# HDL Editor



```vhdl
-- reg32.vhd

LIBRARY IEEE;
USE IEEE.std_logic_1164.all;

ENTITY reg32 IS
    PORT (
        D   : IN std_logic_vector( 31 DOWNTO 0 ) ;
        EN   : IN std_logic ;
        CLK   : IN std_logic ;
        RST   : IN std_logic ;
        Q   : OUT std_logic_vector( 31 DOWNTO 0 )
    );


END ENTITY reg32 ;


ARCHITECTURE RTL OF reg32 IS

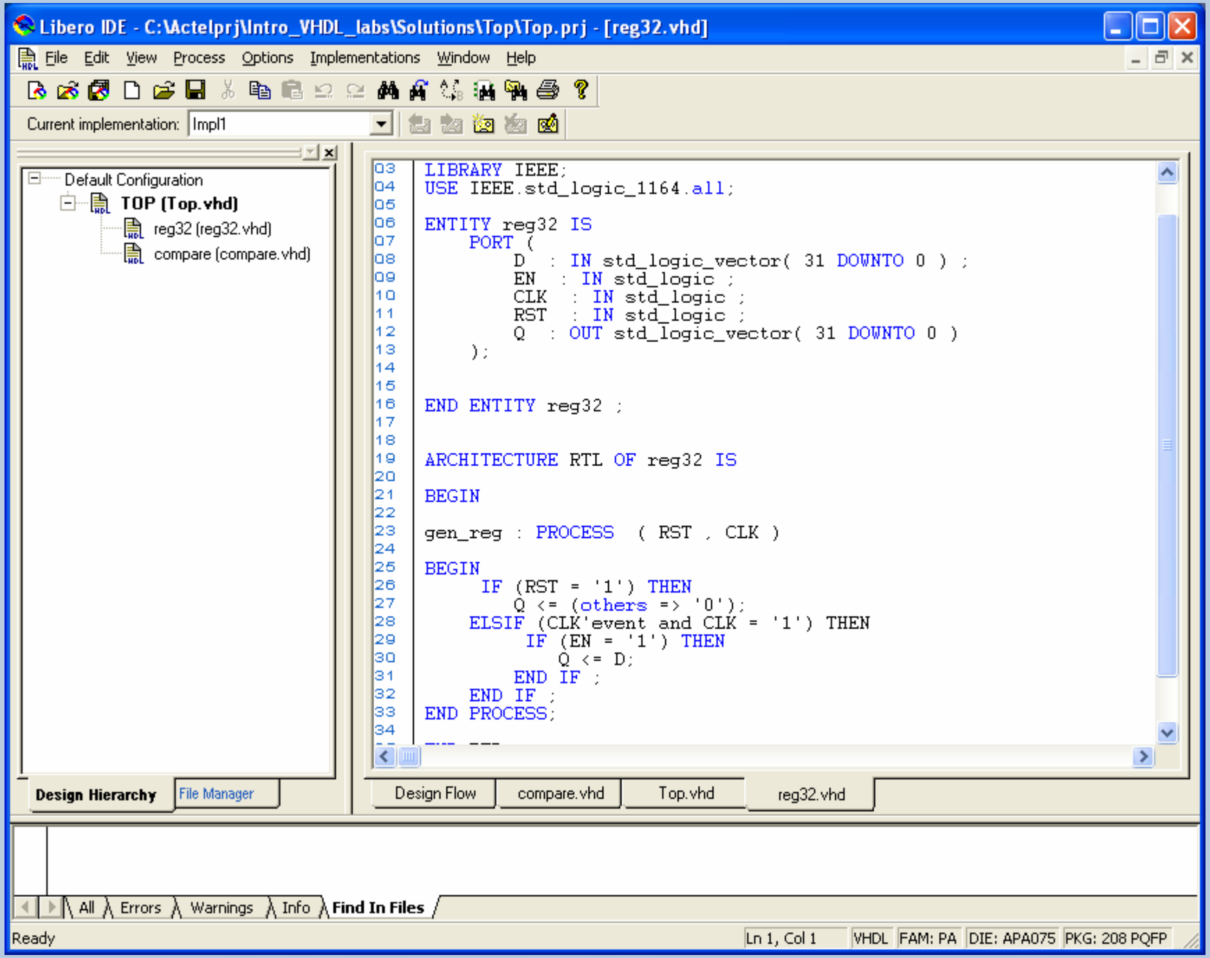
BEGIN

gen_reg : PROCESS  ( RST , CLK )

BEGIN
     IF (RST = '1') THEN
        Q <= (others => '0');
    ELSIF (CLK'event and CLK = '1') THEN
         IF (EN = '1') THEN
            Q <= D;
        END IF ;
    END IF ;
```

# HDL Editor
## *Block Comments*

- Comment Command Allows Users to Comment Sections of VHDL or Verilog Code



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        EN   : IN std_logic ;
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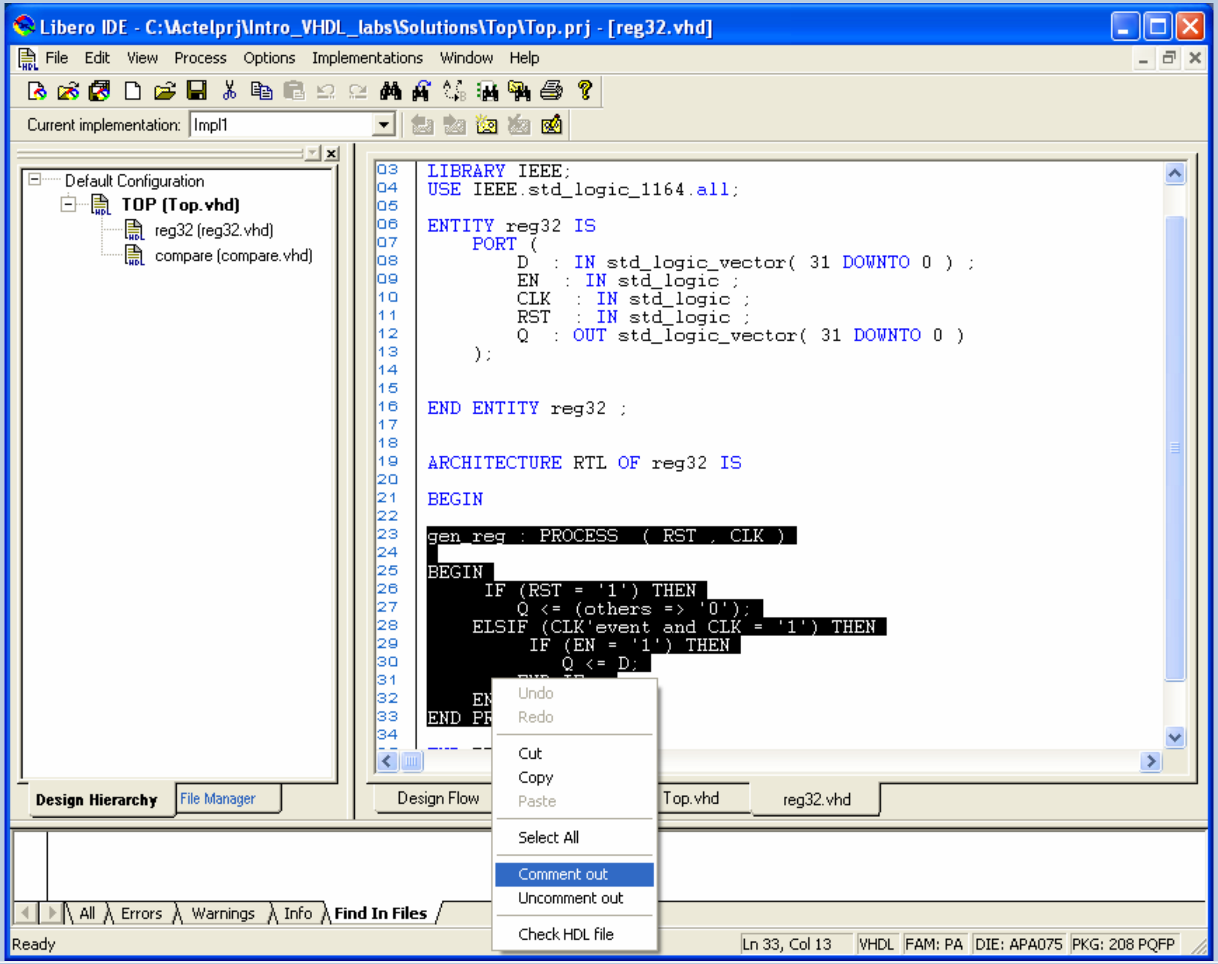
         IF (EN = '1') THEN
            Q <= D;
        END IF ;
    END IF ;
END PROCESS;
```

# HDL Editor
*Block Comments*

- Comment Command Allows Users to Comment Sections of VHDL or Verilog Code



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LIBRARY IEEE;
USE IEEE.std_logic_1164.all;

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    PORT (
        D   : IN std_logic_vector( 31 DOWNTO 0 ) ;
        EN   : IN std_logic ;
        CLK   : IN std_logic ;
        RST   : IN std_logic ;
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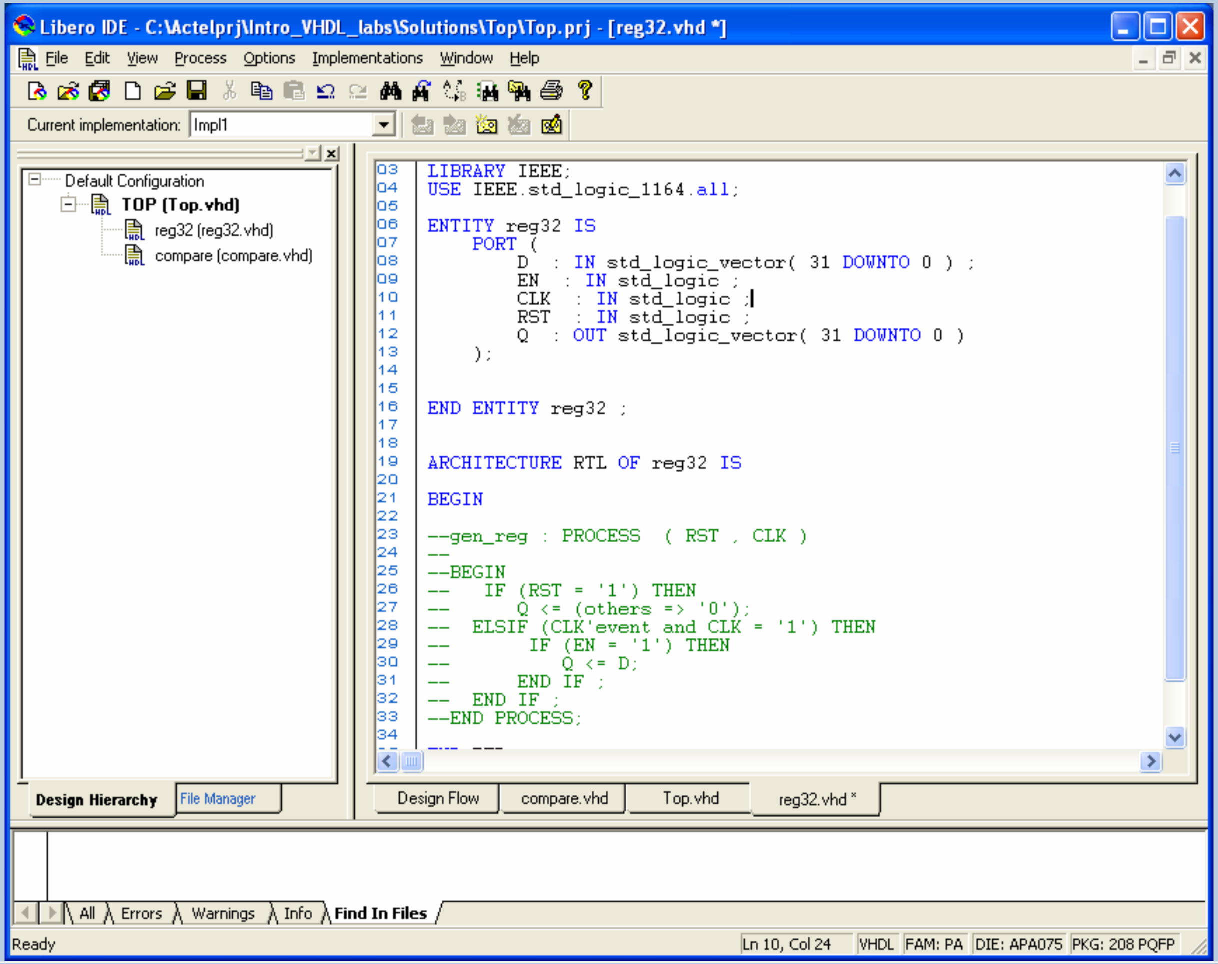
    ELSIF (CLK'event and CLK = '1') THEN
         IF (EN = '1') THEN
            Q <= D;
        END IF

    EN
END PR
```

# HDL Editor
## *Block Comments*

- Comment Command Allows Users to Comment Sections of VHDL or Verilog Code



Libero IDE - C:\Actelprj\Intro_VHDL_labs\Solutions\Top\Top.prj - [reg32.vhd *]

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.all;

ENTITY reg32 IS
    PORT (
        D   : IN std_logic_vector( 31 DOWNTO 0 ) ;
        EN   : IN std_logic ;
        CLK   : IN std_logic ;
        RST   : IN std_logic ;
        Q   : OUT std_logic_vector( 31 DOWNTO 0 )
    );


END ENTITY reg32 ;


ARCHITECTURE RTL OF reg32 IS

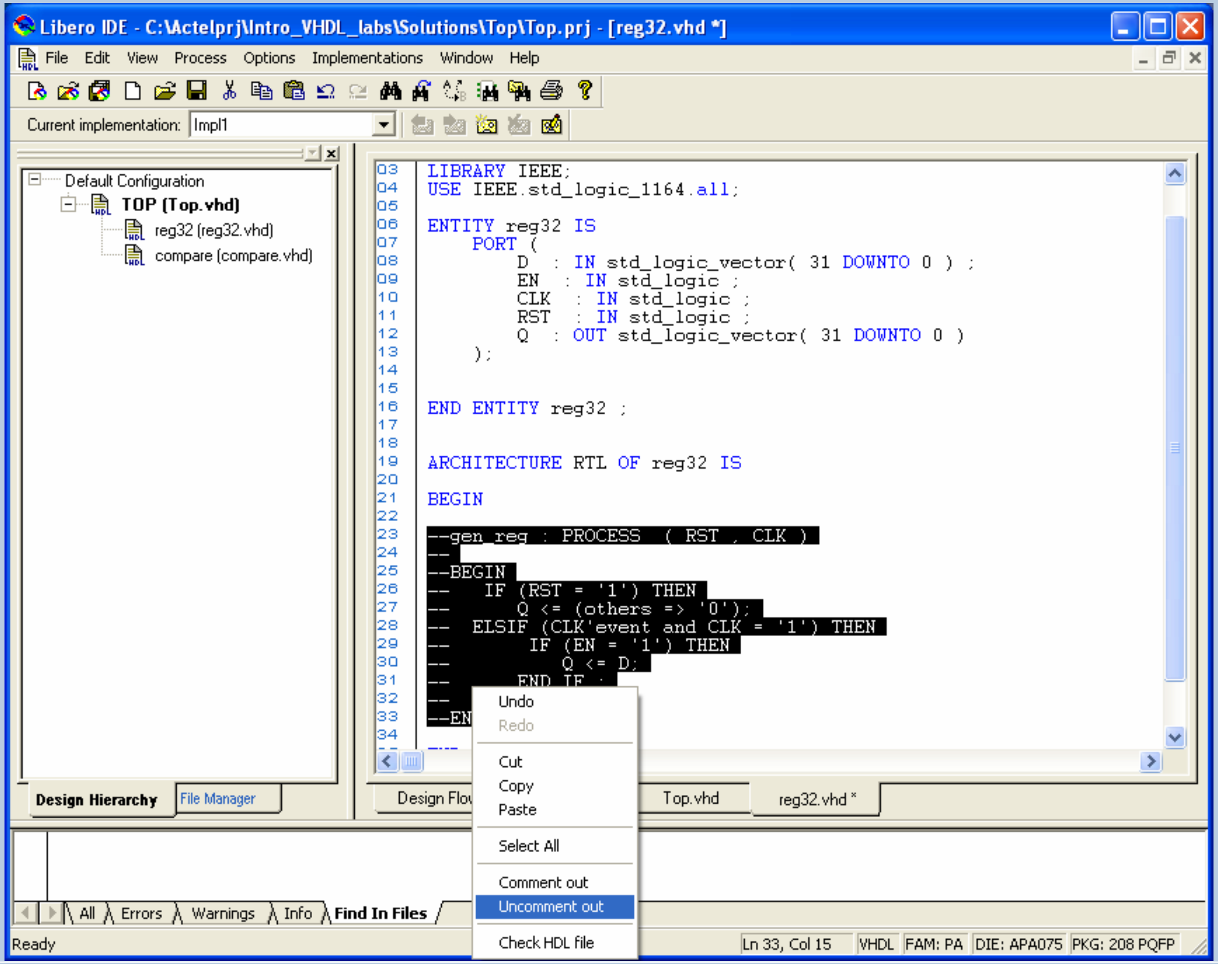
BEGIN

--gen_reg : PROCESS  ( RST , CLK )
--
--BEGIN
--    IF (RST = '1') THEN
--        Q <= (others => '0');
--  ELSIF (CLK'event and CLK = '1') THEN
--         IF (EN = '1') THEN
--             Q <= D;
--        END IF ;
--  END IF ;
--END PROCESS;
```

Ready | Ln 10, Col 24 | VHDL | FAM: PA | DIE: APA075 | PKG: 208 PQFP

# HDL Editor
## *Block Comments*

- Uncomment Command Allows Users to Uncomment Sections of VHDL or Verilog Code



```
LIBRARY IEEE;
USE IEEE.std_logic_1164.all;

ENTITY reg32 IS
    PORT (
        D   : IN std_logic_vector( 31 DOWNTO 0 ) ;
        EN   : IN std_logic ;
        CLK   : IN std_logic ;
        RST   : IN std_logic ;
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    );


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ARCHITECTURE RTL OF reg32 IS

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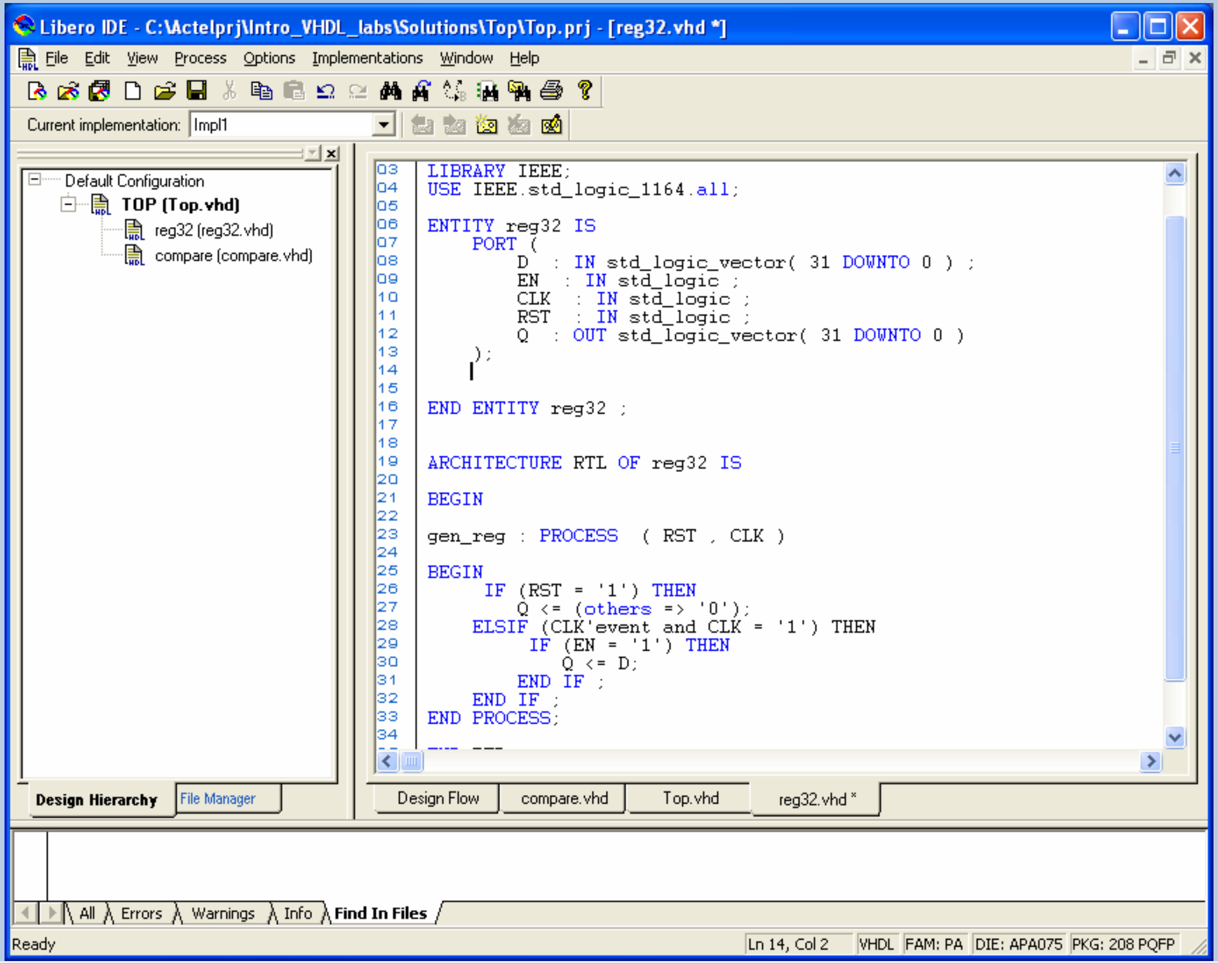
--BEGIN
--    IF (RST = '1') THEN
--       Q <= (others => '0');
--   ELSIF (CLK'event and CLK = '1') THEN
--        IF (EN = '1') THEN
--           Q <= D;
--       END IF ;
--
--EN
```

# HDL Editor
## *Block Comments*

- Uncomment Command Allows Users to Uncomment Sections of VHDL or Verilog Code



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LIBRARY IEEE;
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BEGIN
     IF (RST = '1') THEN
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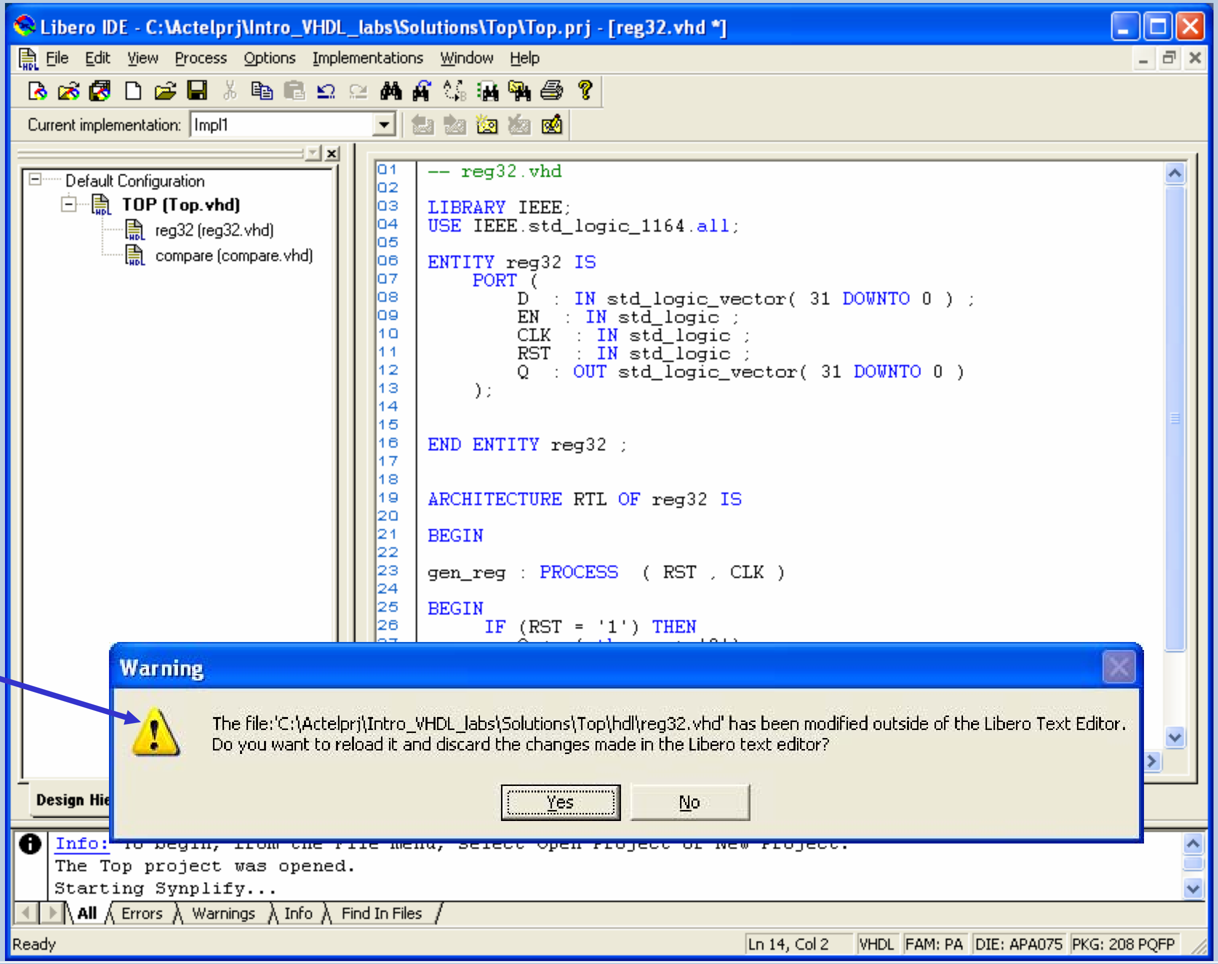
    ELSIF (CLK'event and CLK = '1') THEN
         IF (EN = '1') THEN
           Q <= D;
        END IF ;
    END IF ;
END PROCESS;
```

# HDL Editor
*Detect Changes*

- If File Is Open in Libero HDL Editor and Modified by another Text Editor, Warning Is Issued


Libero IDE - C:\Actelprj\Intro_VHDL_labs\Solutions\Top\Top.prj - [reg32.vhd *]
File Edit View Process Options Implementations Window Help
Current implementation: Impl1
Default Configuration
TOP (Top.vhd)
reg32 (reg32.vhd)
compare (compare.vhd)
Design Hie
All Errors Warnings Info Find In Files

```
-- reg32.vhd

LIBRARY IEEE;
USE IEEE.std_logic_1164.all;

ENTITY reg32 IS
    PORT (
        D   : IN std_logic_vector( 31 DOWNTO 0 ) ;
        EN  : IN std_logic ;
        CLK  : IN std_logic ;
        RST  : IN std_logic ;
        Q  : OUT std_logic_vector( 31 DOWNTO 0 )
    );


END ENTITY reg32 ;


ARCHITECTURE RTL OF reg32 IS

BEGIN

gen_reg : PROCESS  ( RST , CLK )

BEGIN
     IF (RST = '1') THEN
```

**Warning**

The file:'C:\Actelprj\Intro_VHDL_labs\Solutions\Top\hdl\reg32.vhd' has been modified outside of the Libero Text Editor.
Do you want to reload it and discard the changes made in the Libero text editor?

Yes No

```
Info: To begin, from the File menu, select Open Project or New Project.
The Top project was opened.
Starting Synplify...
```

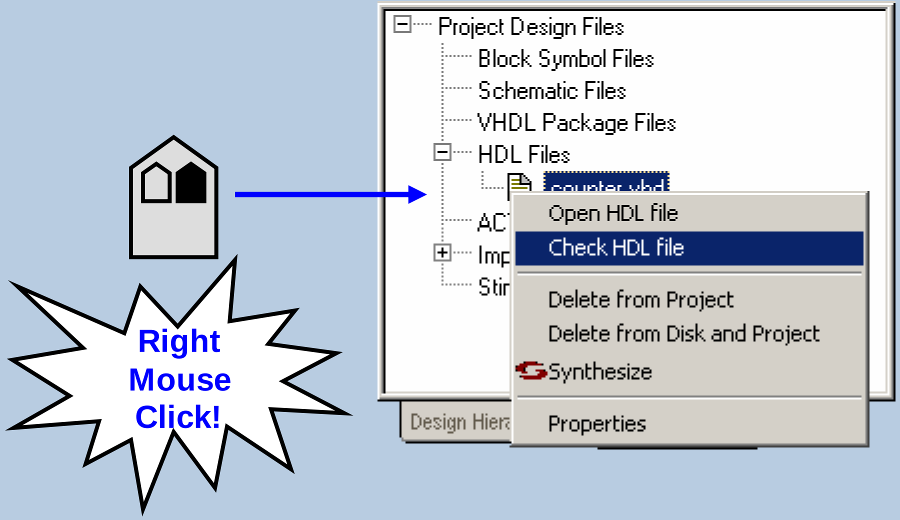
Ready | Ln 14, Col 2 | VHDL | FAM: PA | DIE: APA075 | PKG: 208 PQFP

Warning message in Libero

# Libero HDL Syntax Checker

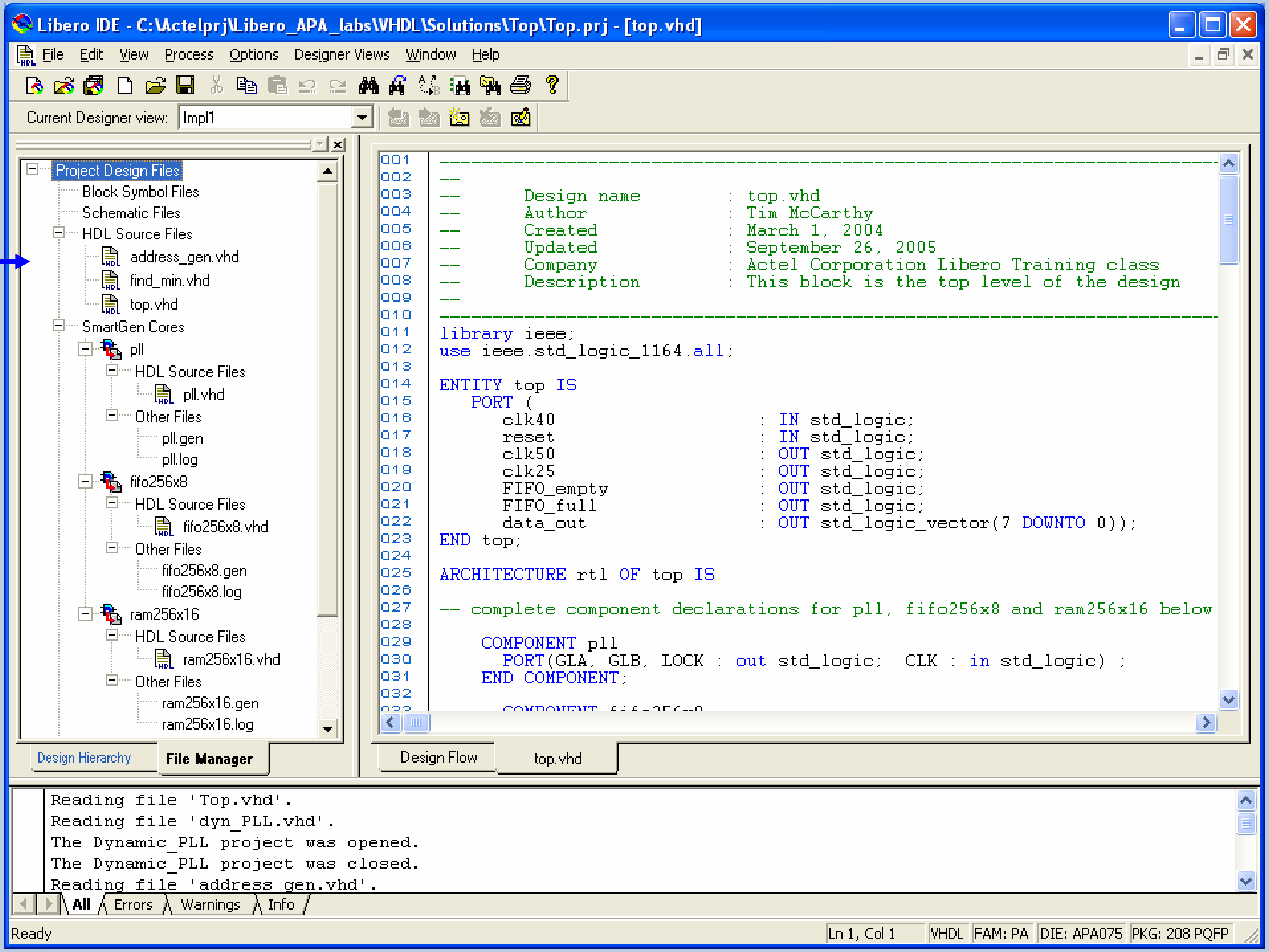
## HDL Syntax Checker Available from File Manager Tab

- Checks for Errors in HDL Blocks
- Errors Indicated in Libero Log Window
- Optional Step



# Project Manager with Saved Files...

VHDL files



```
-----------------------------------------------------------------------------
--
--      Design name         : top.vhd
--      Author              : Tim McCarthy
--      Created             : March 1, 2004
--      Updated             : September 26, 2005
--      Company             : Actel Corporation Libero Training class
--      Description         : This block is the top level of the design
--
-----------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;

ENTITY top IS
   PORT (
      clk40                       : IN std_logic;
      reset                       : IN std_logic;
      clk50                       : OUT std_logic;
      clk25                       : OUT std_logic;
      FIFO_empty                  : OUT std_logic;
      FIFO_full                   : OUT std_logic;
      data_out                    : OUT std_logic_vector(7 DOWNTO 0));
END top;

ARCHITECTURE rtl OF top IS

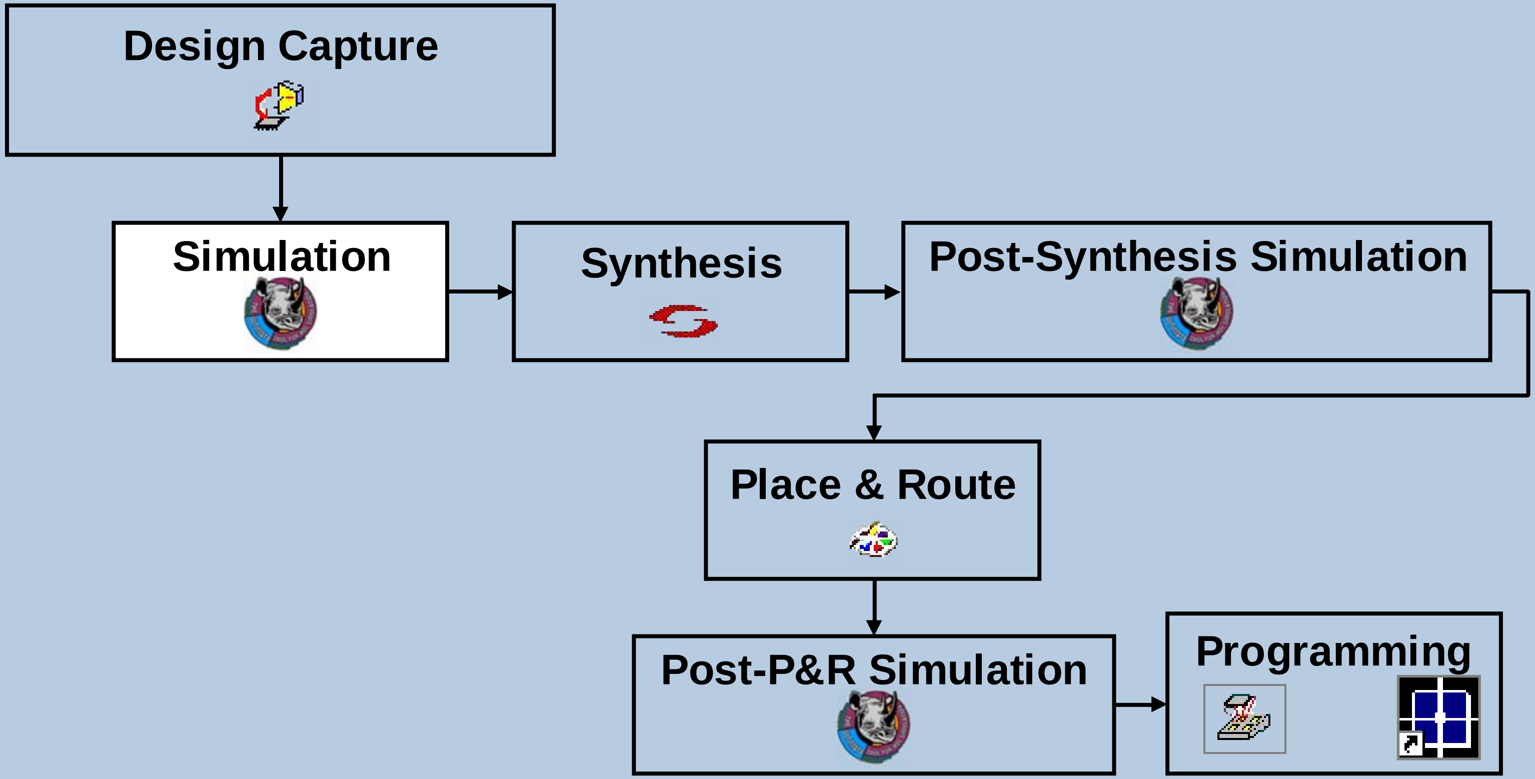
-- complete component declarations for pll, fifo256x8 and ram256x16 below

    COMPONENT pll
      PORT(GLA, GLB, LOCK : out std_logic;  CLK : in std_logic) ;
    END COMPONENT;

      COMPONENT fifo256x8
```

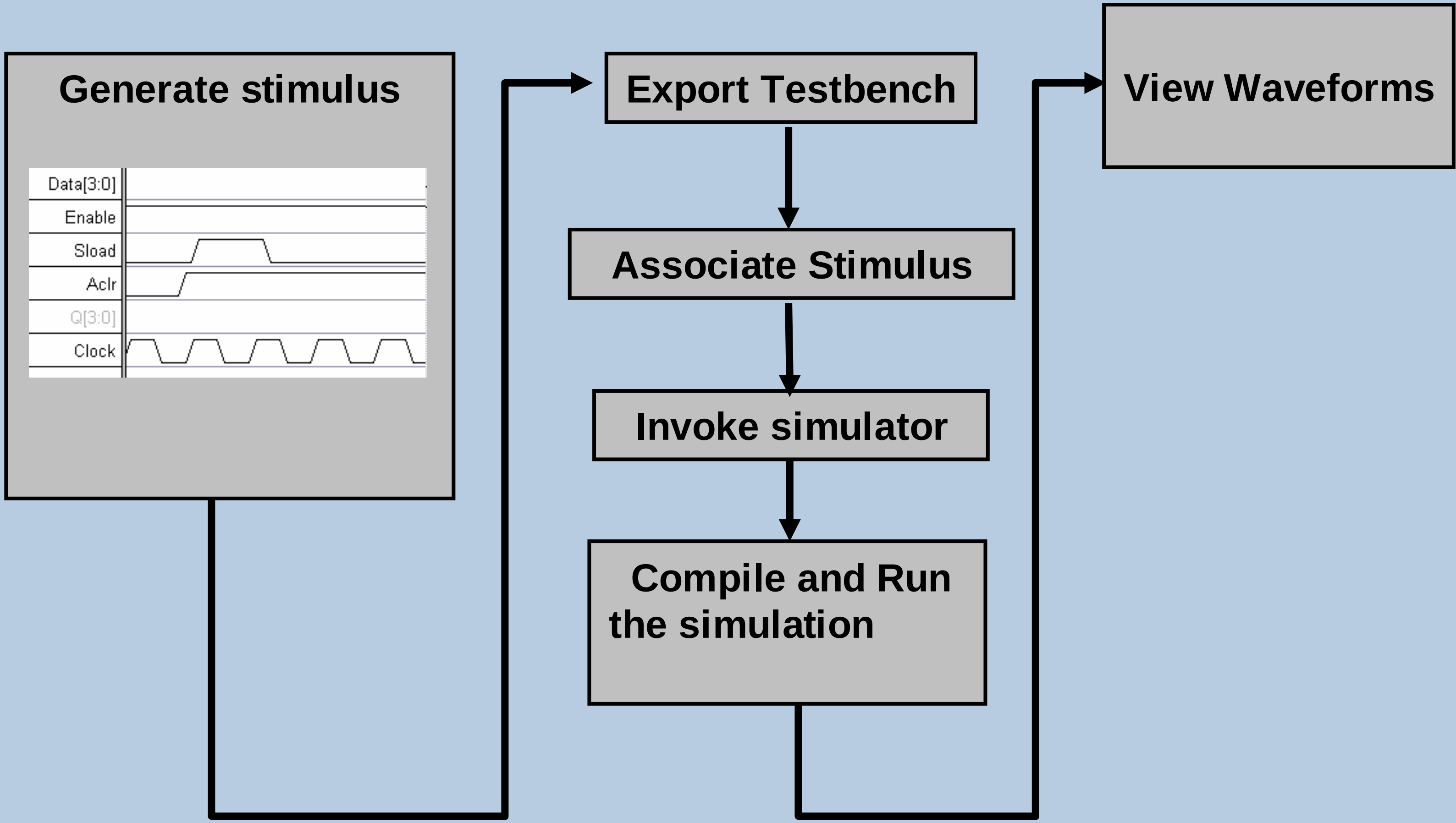
```
Reading file 'Top.vhd'.
Reading file 'dyn_PLL.vhd'.
The Dynamic_PLL project was opened.
The Dynamic_PLL project was closed.
Reading file 'address_gen.vhd'.
```

# Functional Simulation



# Simulation Flow

- For Each Block You Want to Simulate . . .



Generate stimulus

Export Testbench

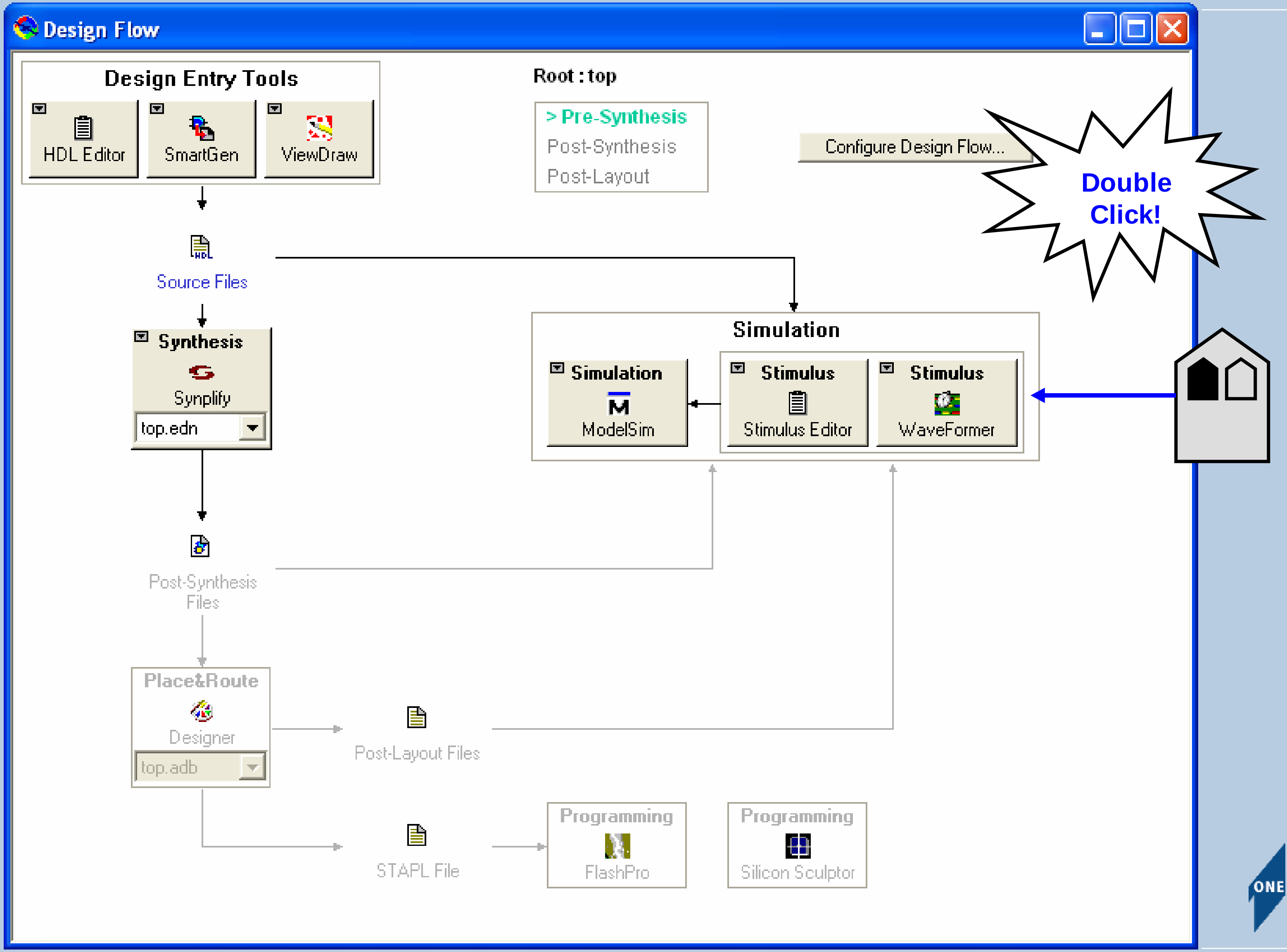
Associate Stimulus

Invoke simulator

Compile and Run the simulation

View Waveforms

# Invoking WaveFormer Lite



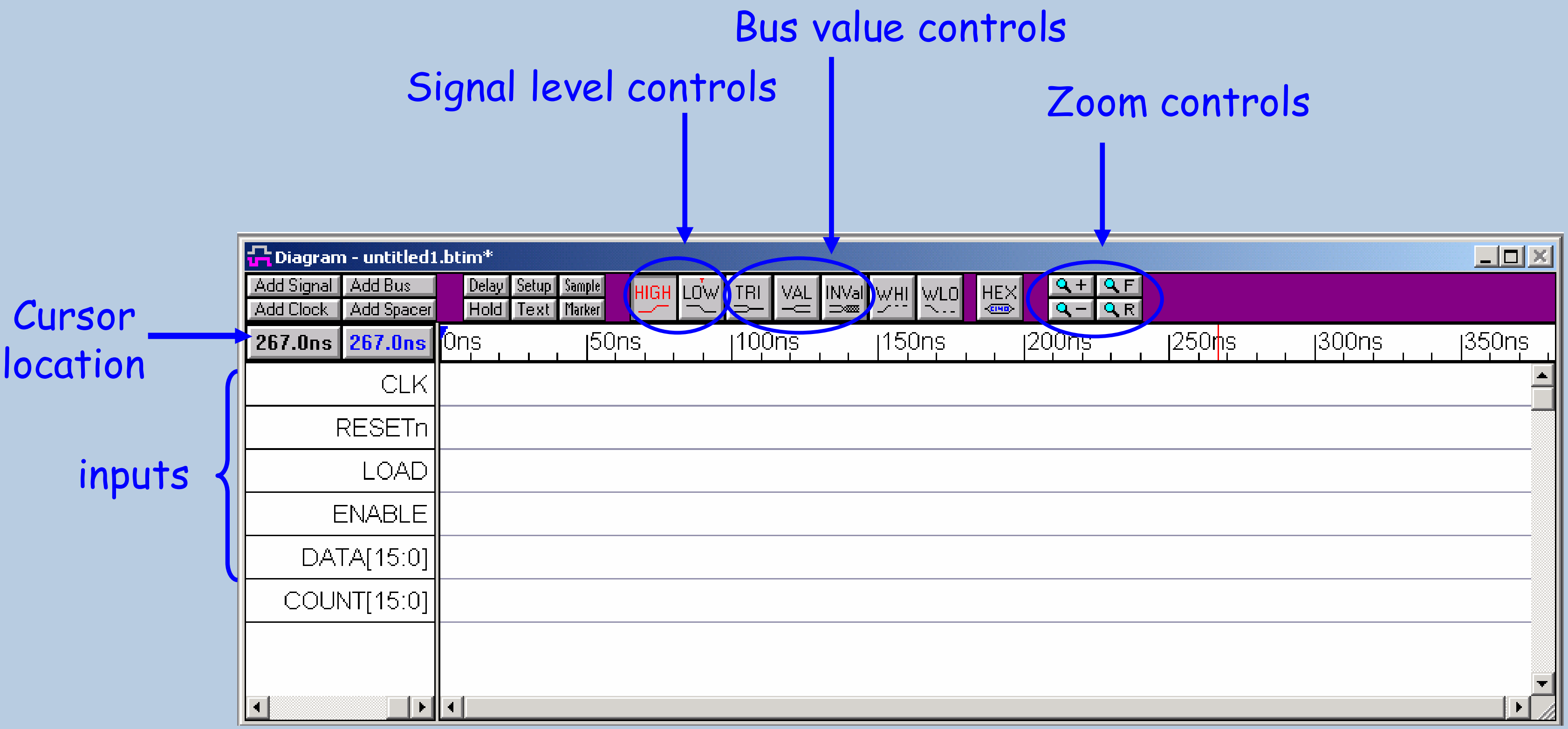
Double Click!

# WaveFormer Lite Features

- Allows Convenient Test Stimulus Specification via GUI
  - User Specifies Stimulus by Drawing Waveforms
    - Supports Copy / Paste / Append Operations
  - Significantly Reduces Testbench Creation Time
  - Automatically Converts Graphical Stimulus Files into HDL TestBenches
  - Can Generate:
    - VHDL Testbench (*.vhd)
    - Verilog Testbench (*.v)
- Users Can Annotate Waveform For Design Documentation

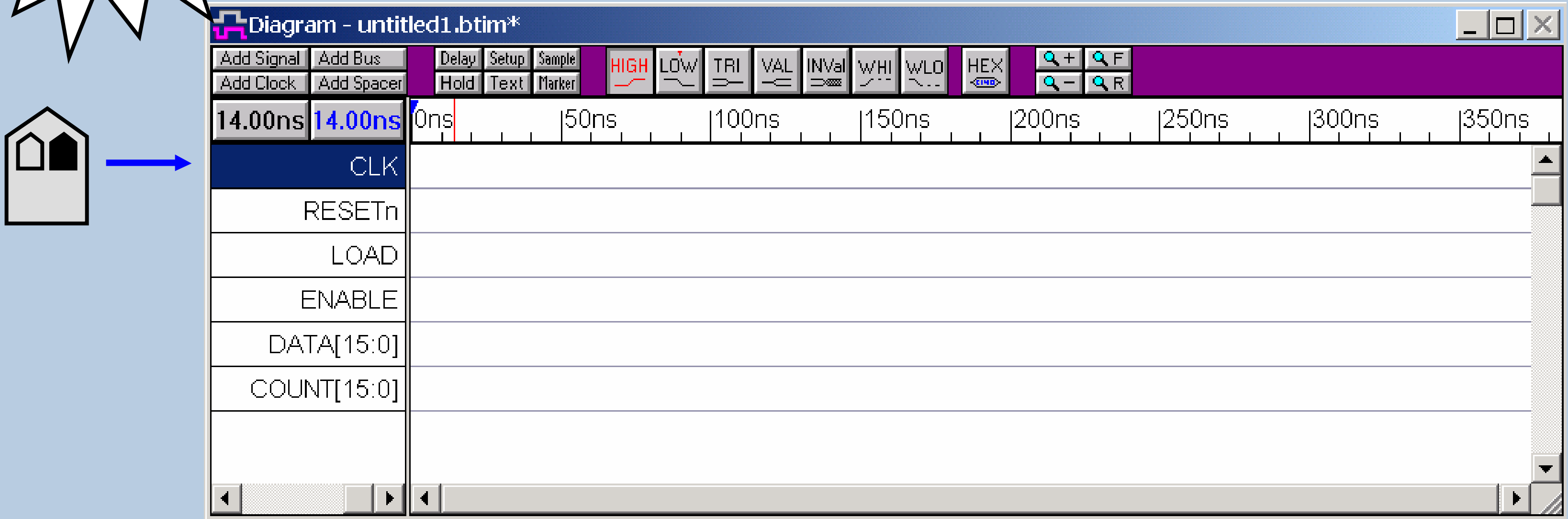
# Drawing Stimulus

## ■ WaveFormer Lite Diagram Window

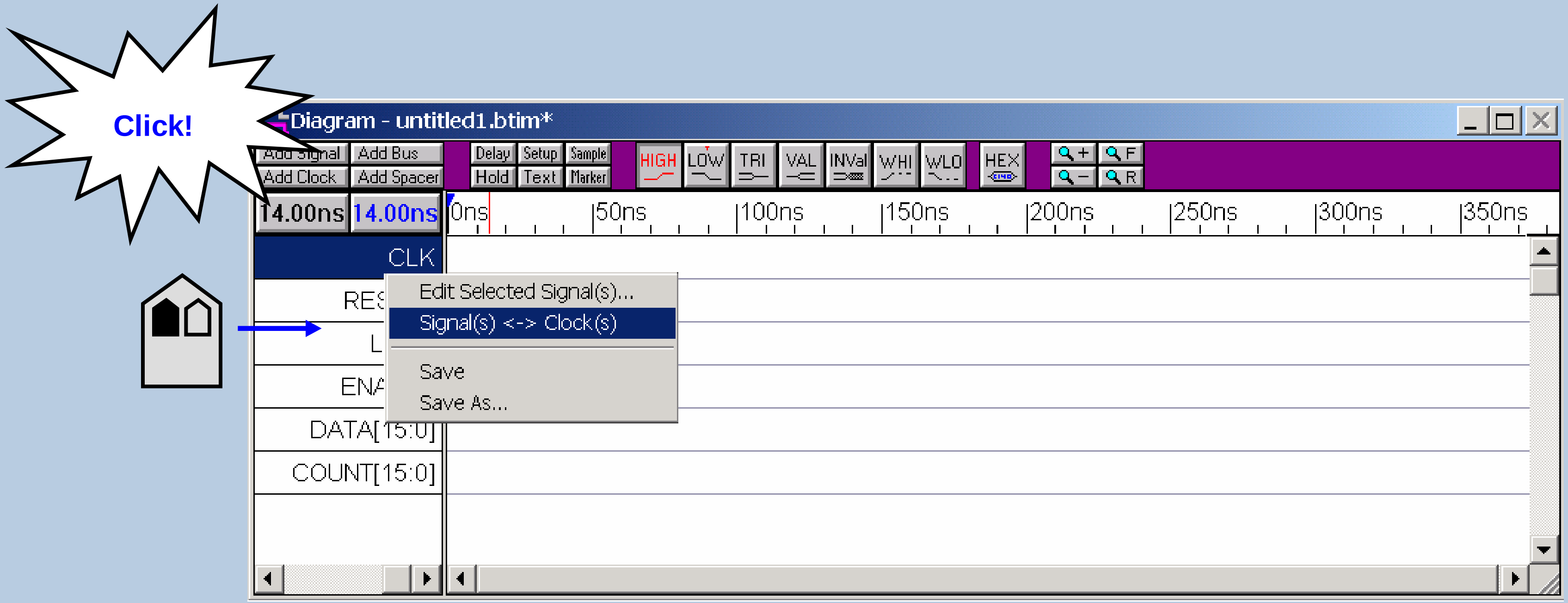


# Creating Clocks

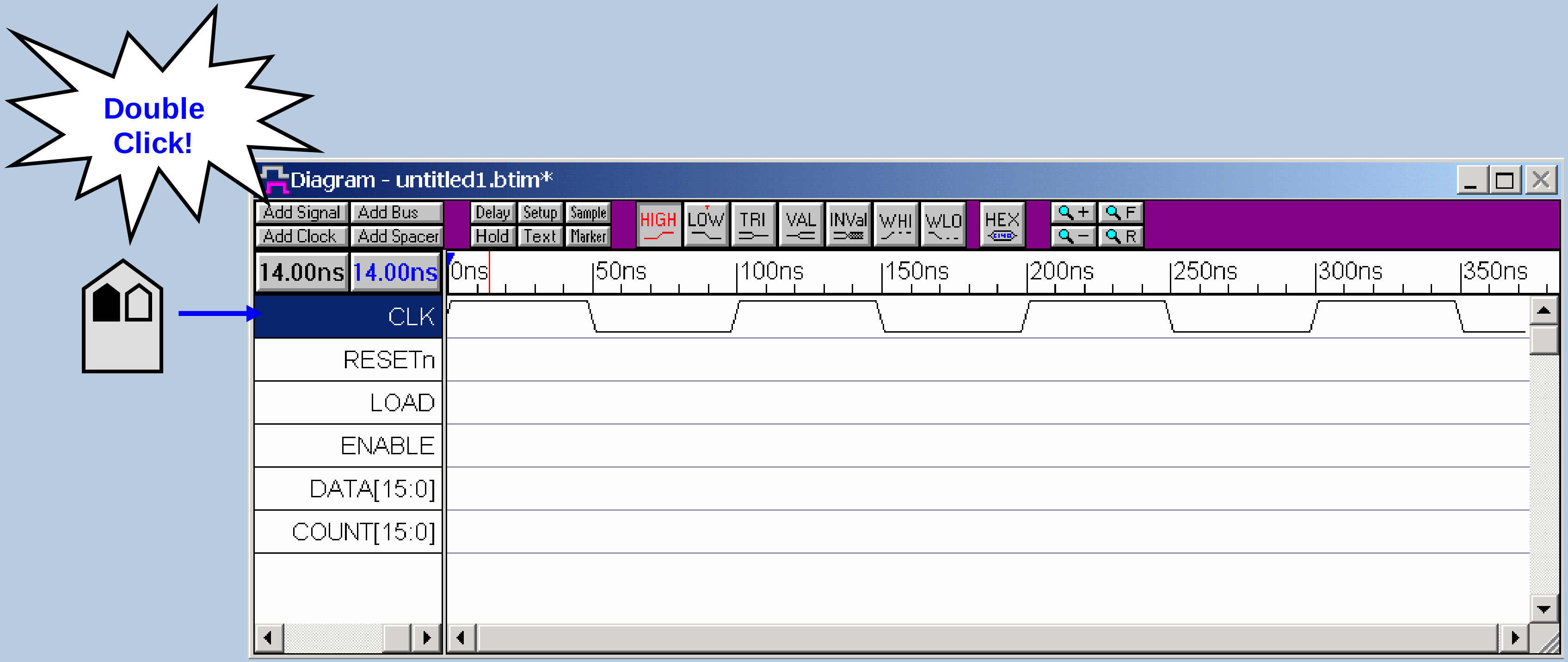
Right Mouse Click!



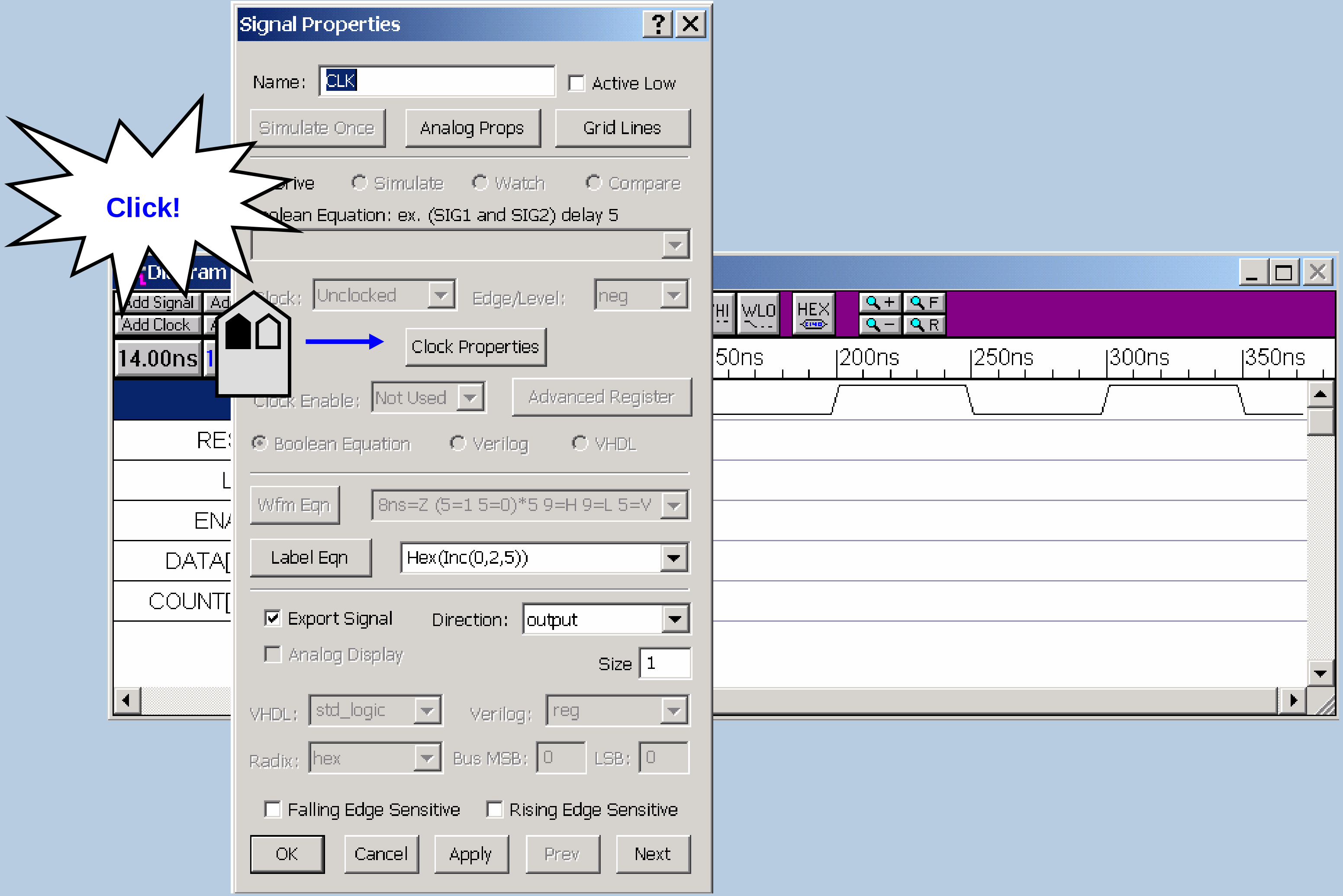
# Creating Clocks



# Creating Clocks



# Creating Clocks



Signal Properties

Name: CLK □ Active Low

rive ○ Simulate ○ Watch ○ Compare

olean Equation: ex. (SIG1 and SIG2) delay 5

lock: Unclocked Edge/Level: neg

Clock Enable: Not Used

● Boolean Equation ○ Verilog ○ VHDL

Wfm Eqn: 8ns=Z (5=1 5=0)*5 9=H 9=L 5=V

Label Eqn: Hex(Inc(0,2,5))

☑ Export Signal Direction: output

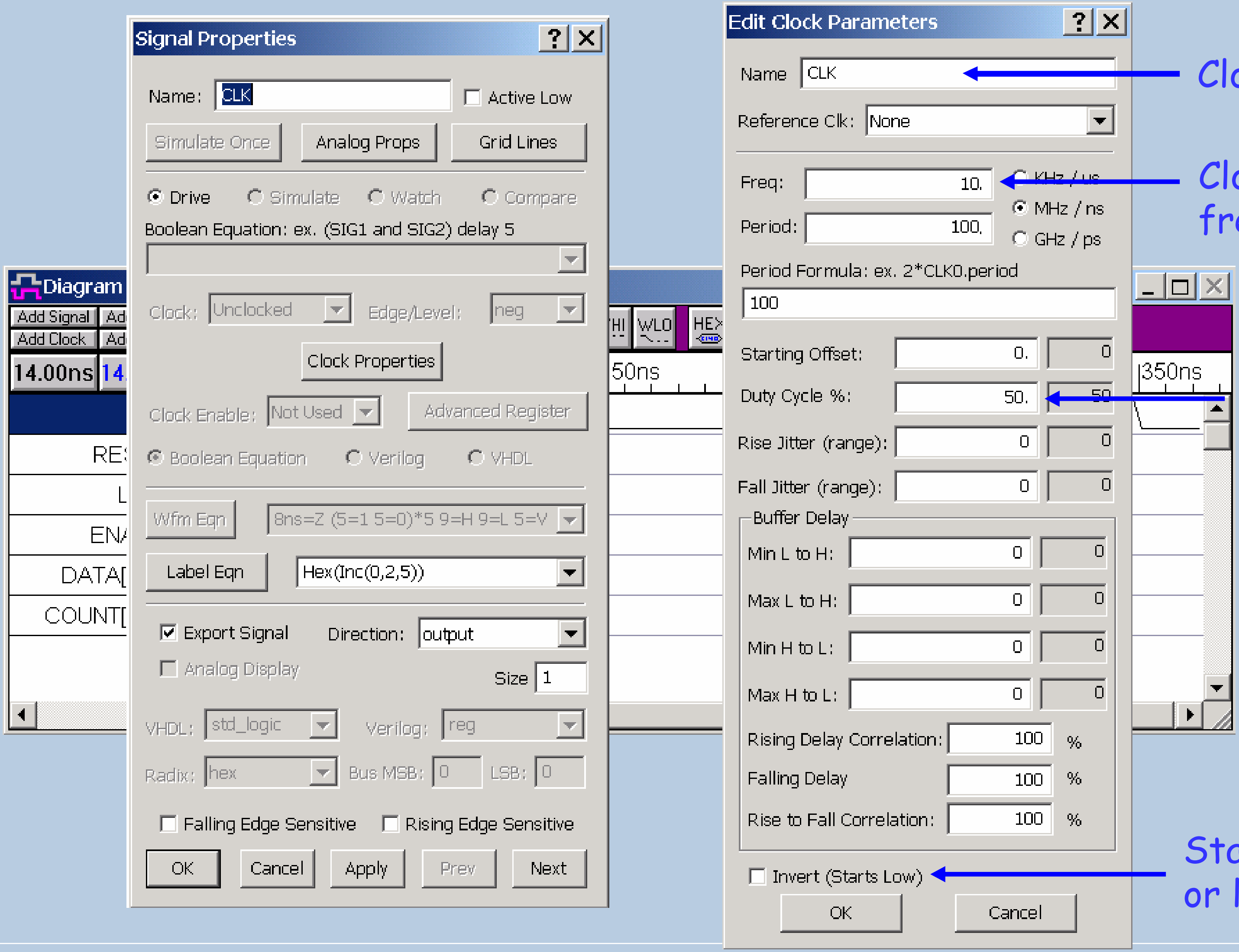
□ Analog Display Size 1

VHDL: std_logic Verilog: reg

Radix: hex Bus MSB: 0 LSB: 0

□ Falling Edge Sensitive □ Rising Edge Sensitive

# Creating Clocks



**Signal Properties**

Name: CLK □ Active Low

Simulate Once | Analog Props | Grid Lines

● Drive ○ Simulate ○ Watch ○ Compare

Boolean Equation: ex. (SIG1 and SIG2) delay 5

Clock: Unclocked Edge/Level: neg

Clock Properties

Clock Enable: Not Used | Advanced Register

● Boolean Equation ○ Verilog ○ VHDL

Wfm Eqn: 8ns=Z (5=1 5=0)*5 9=H 9=L 5=V

Label Eqn: Hex(Inc(0,2,5))

☑ Export Signal Direction: output

□ Analog Display Size 1

VHDL: std_logic Verilog: reg

Radix: hex Bus MSB: 0 LSB: 0

□ Falling Edge Sensitive □ Rising Edge Sensitive

OK | Cancel | Apply | Prev | Next

**Edit Clock Parameters**

Name: CLK

Reference Clk: None

Freq: 10. ○ KHz / us

Period: 100. ● MHz / ns ○ GHz / ps

Period Formula: ex. 2*CLK0.period

100

| | | |
|---|---|---|
| Starting Offset: | 0. | 0 |
| Duty Cycle %: | 50. | 50 |
| Rise Jitter (range): | 0 | 0 |
| Fall Jitter (range): | 0 | 0 |

Buffer Delay

| | | |
|---|---|---|
| Min L to H: | 0 | 0 |
| Max L to H: | 0 | 0 |
| Min H to L: | 0 | 0 |
| Max H to L: | 0 | 0 |

| | | |
|---|---|---|
| Rising Delay Correlation: | 100 | % |
| Falling Delay | 100 | % |
| Rise to Fall Correlation: | 100 | % |

□ Invert (Starts Low)

OK | Cancel

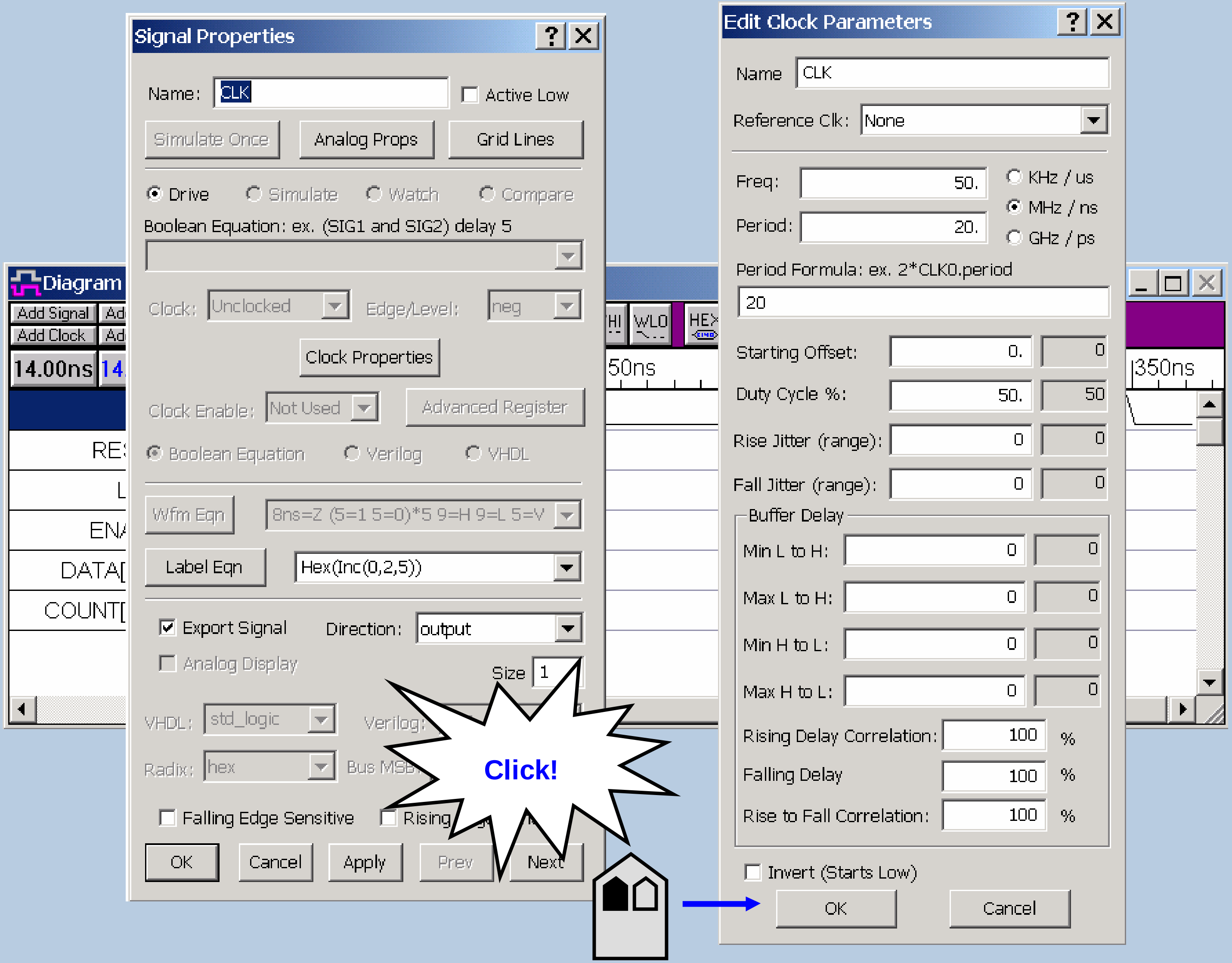
Clock name

Clock frequency

Clock duty cycle

Start high or low

# Creating Clocks



Signal Properties

Name: CLK ☐ Active Low

Simulate Once | Analog Props | Grid Lines

● Drive ○ Simulate ○ Watch ○ Compare

Boolean Equation: ex. (SIG1 and SIG2) delay 5

Clock: Unclocked Edge/Level: neg

Clock Properties

Clock Enable: Not Used | Advanced Register

● Boolean Equation ○ Verilog ○ VHDL

Wfm Eqn: 8ns=Z (5=1 5=0)*5 9=H 9=L 5=V

Label Eqn: Hex(Inc(0,2,5))

☑ Export Signal Direction: output

☐ Analog Display Size 1

VHDL: std_logic Verilog:

Radix: hex Bus MSB

☐ Falling Edge Sensitive ☐ Rising

OK | Cancel | Apply | Prev | Next

Edit Clock Parameters

Name: CLK

Reference Clk: None

Freq: 50. ○ KHz / us

Period: 20. ● MHz / ns ○ GHz / ps

Period Formula: ex. 2*CLK0.period

20

| | | |
|---|---|---|
| Starting Offset: | 0. | 0 |
| Duty Cycle %: | 50. | 50 |
| Rise Jitter (range): | 0 | 0 |
| Fall Jitter (range): | 0 | 0 |

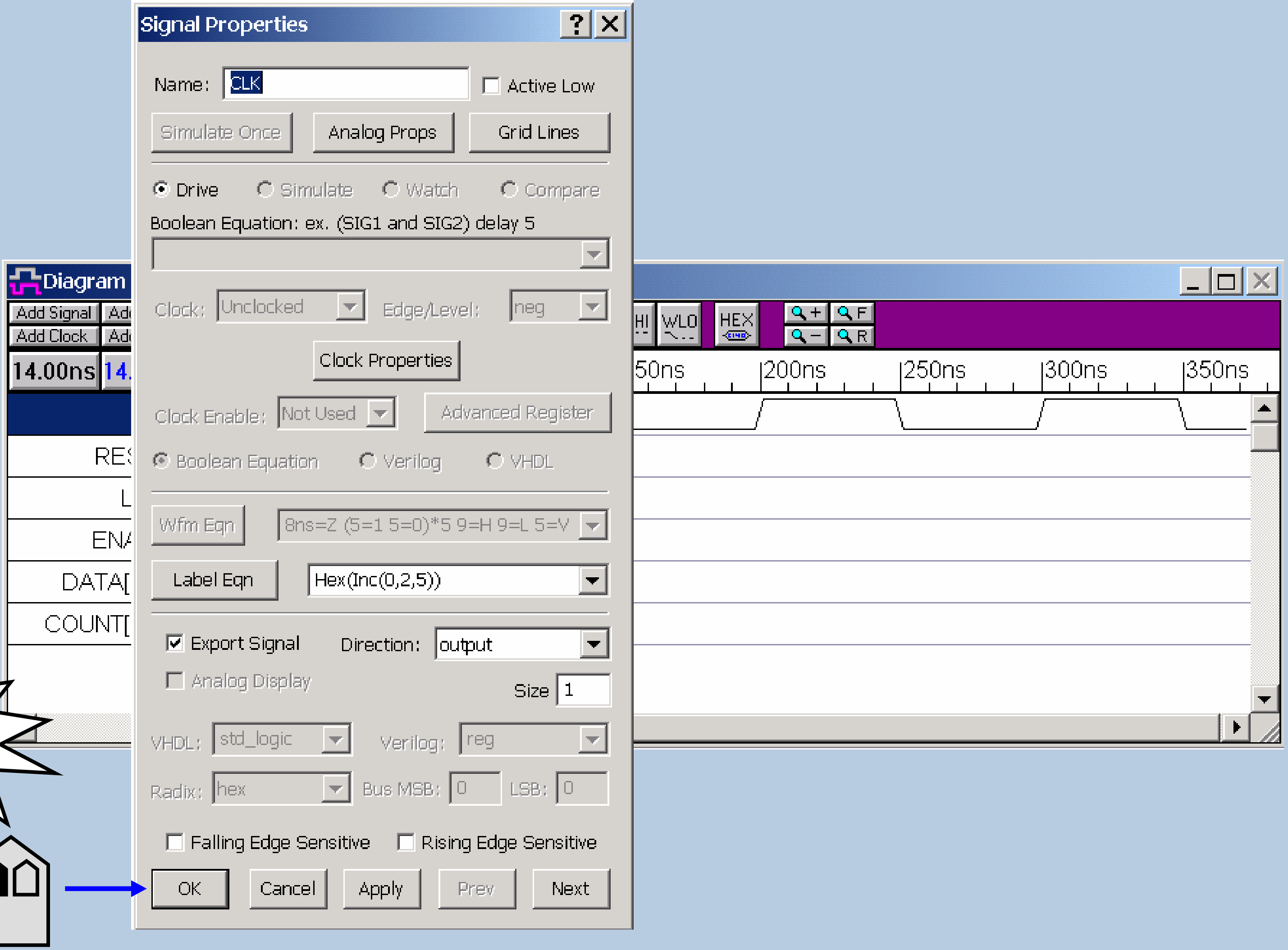
Buffer Delay

| | | |
|---|---|---|
| Min L to H: | 0 | 0 |
| Max L to H: | 0 | 0 |
| Min H to L: | 0 | 0 |
| Max H to L: | 0 | 0 |
| Rising Delay Correlation: | 100 | % |
| Falling Delay | 100 | % |
| Rise to Fall Correlation: | 100 | % |

☐ Invert (Starts Low)

OK | Cancel

# Creating Clocks



Signal Properties

Name: CLK

☐ Active Low

Simulate Once | Analog Props | Grid Lines

● Drive ○ Simulate ○ Watch ○ Compare

Boolean Equation: ex. (SIG1 and SIG2) delay 5

Clock: Unclocked Edge/Level: neg

Clock Properties

Clock Enable: Not Used

Advanced Register

● Boolean Equation ○ Verilog ○ VHDL

Wfm Eqn: 8ns=Z (5=1 5=0)*5 9=H 9=L 5=V

Label Eqn: Hex(Inc(0,2,5))

☑ Export Signal Direction: output

☐ Analog Display Size: 1

VHDL: std_logic Verilog: reg

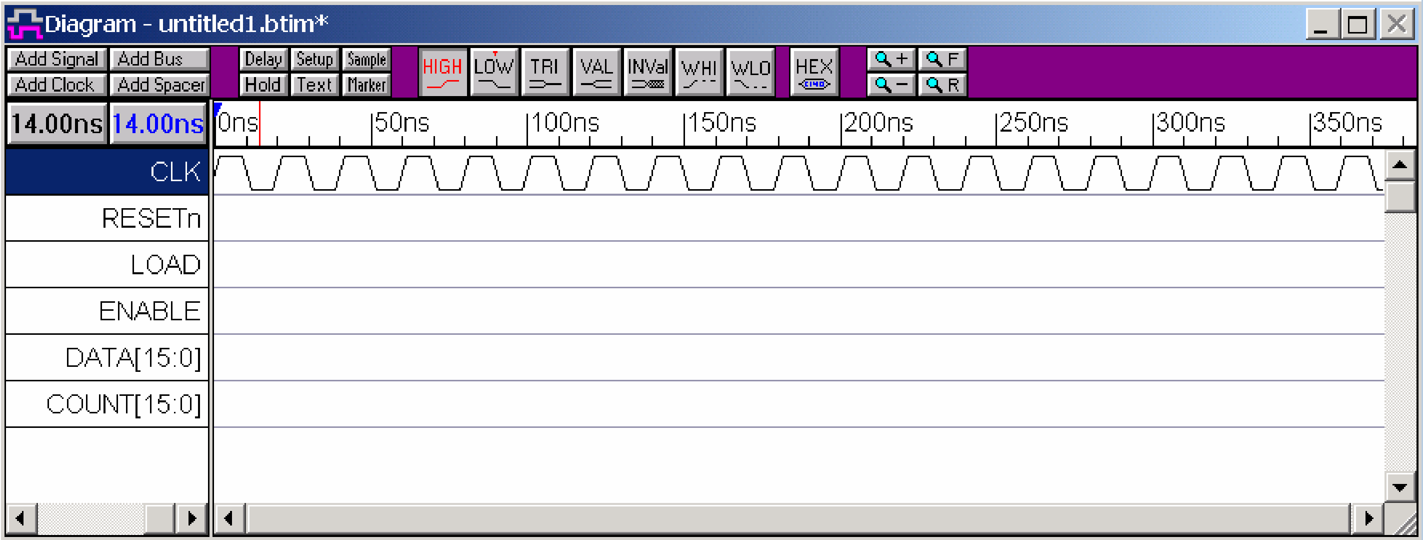
Radix: hex Bus MSB: 0 LSB: 0

☐ Falling Edge Sensitive ☐ Rising Edge Sensitive

OK | Cancel | Apply | Prev | Next

Click!

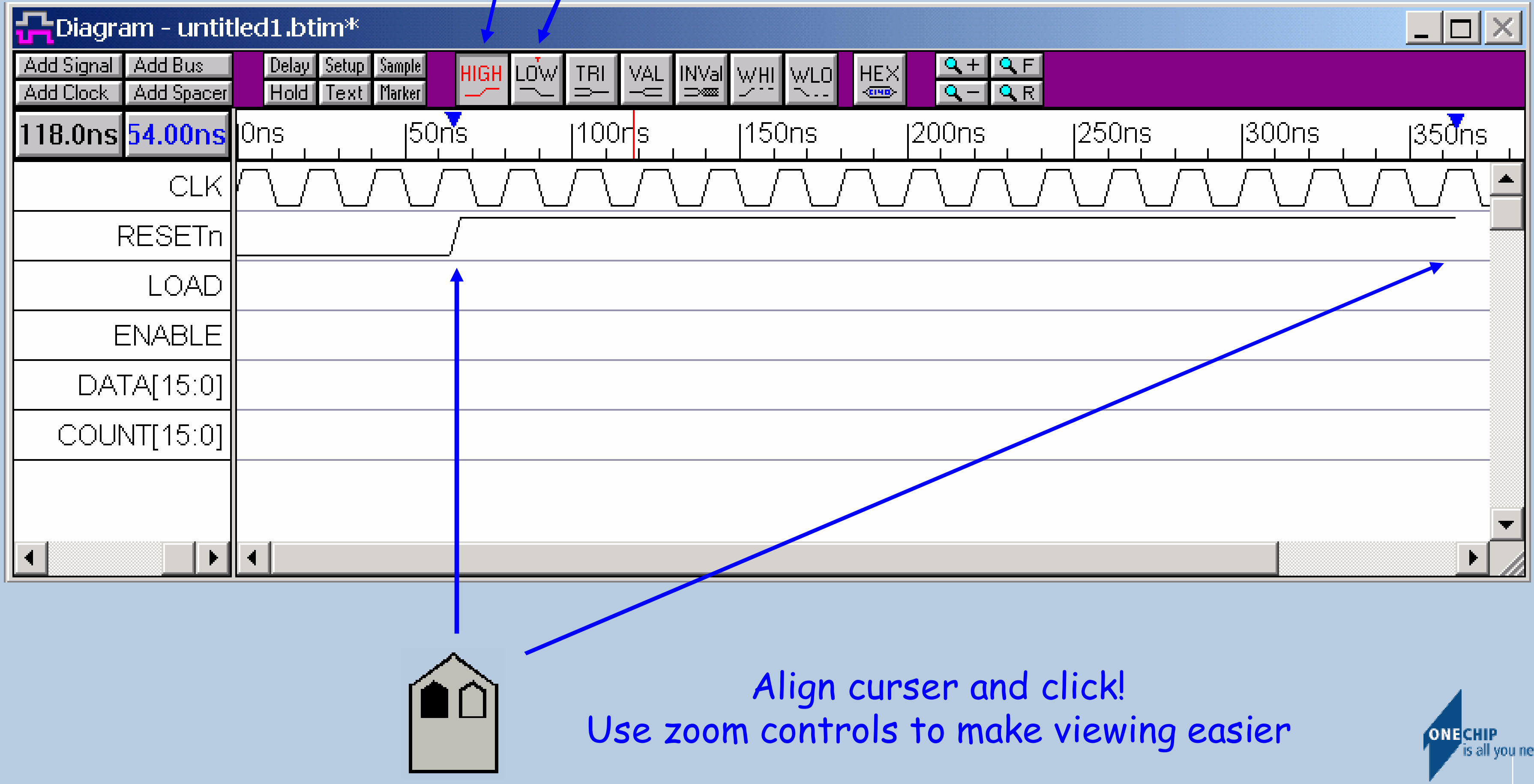
# Creating Clocks



# Drawing Signals

State button toggles automatically

Select “low” state button



Align curser and click!

Use zoom controls to make viewing easier

# Drawing Signals
## *Edge Placement*

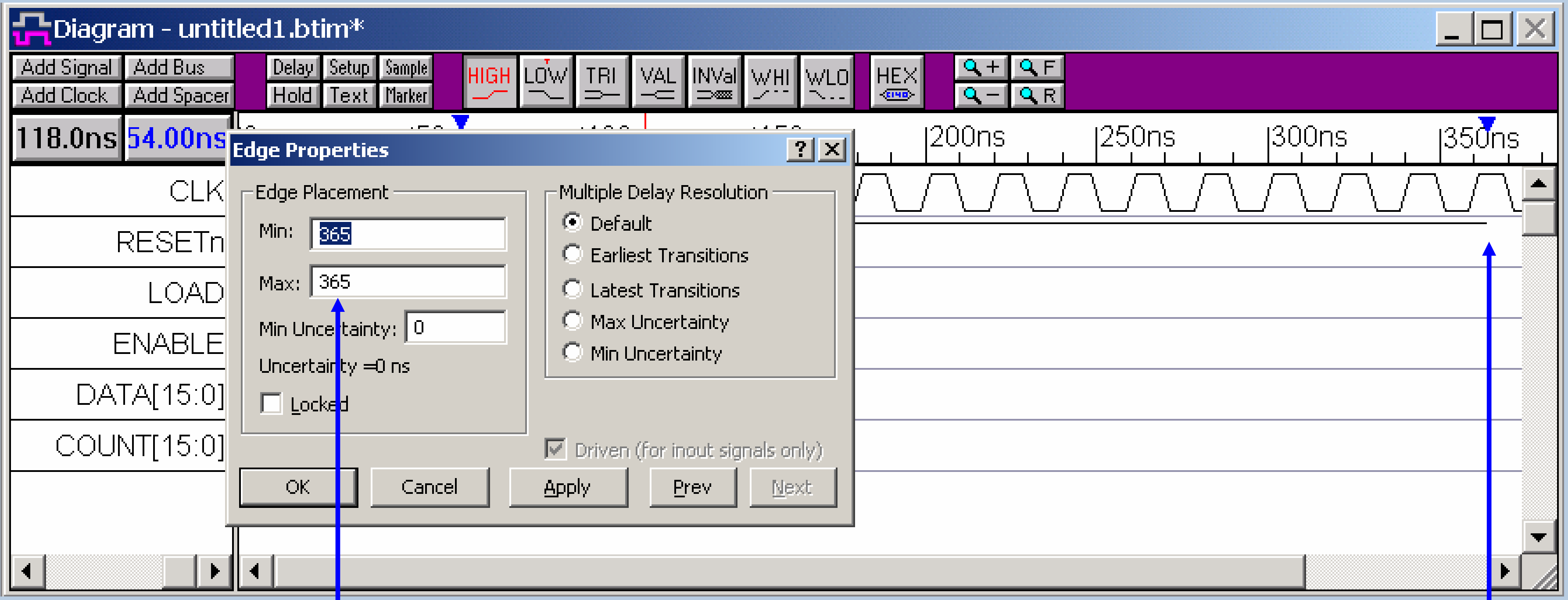


Diagram - untitled1.btim*

Edge Properties

Edge Placement

Min: 365

Max: 365

Min Uncertainty: 0

Uncertainty =0 ns

□ Locked

Multiple Delay Resolution

● Default

○ Earliest Transitions

○ Latest Transitions

○ Max Uncertainty

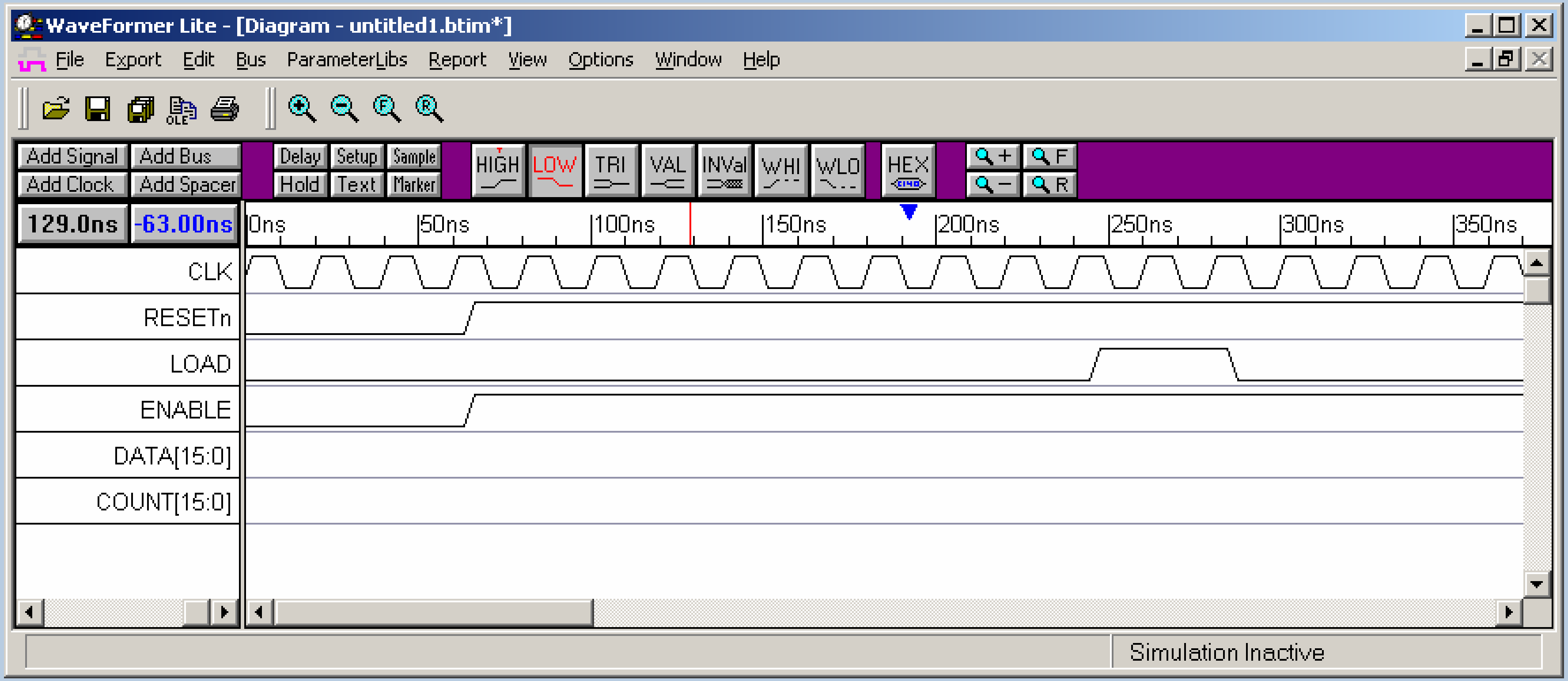
○ Min Uncertainty

☑ Driven (for inout signals only)

Enter time for edge placement

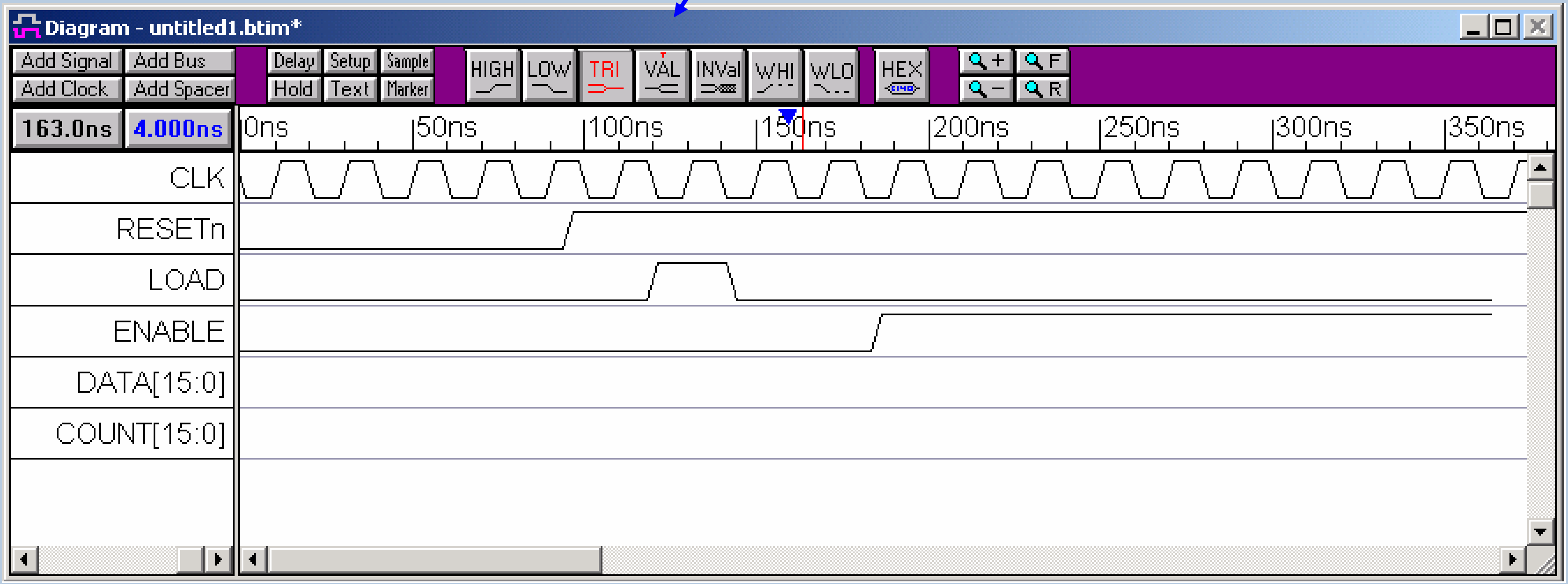
Double click at end of signal

# Editing Signals



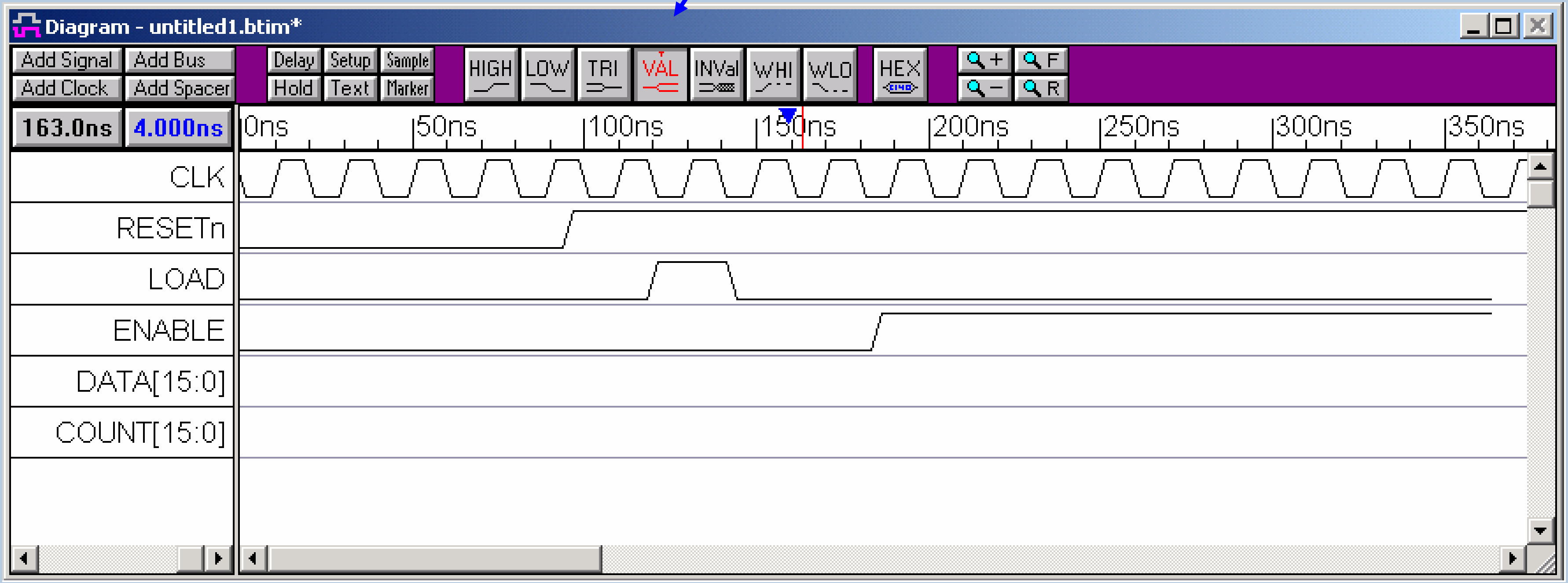
# Drawing Busses

Double click “VAL” state button

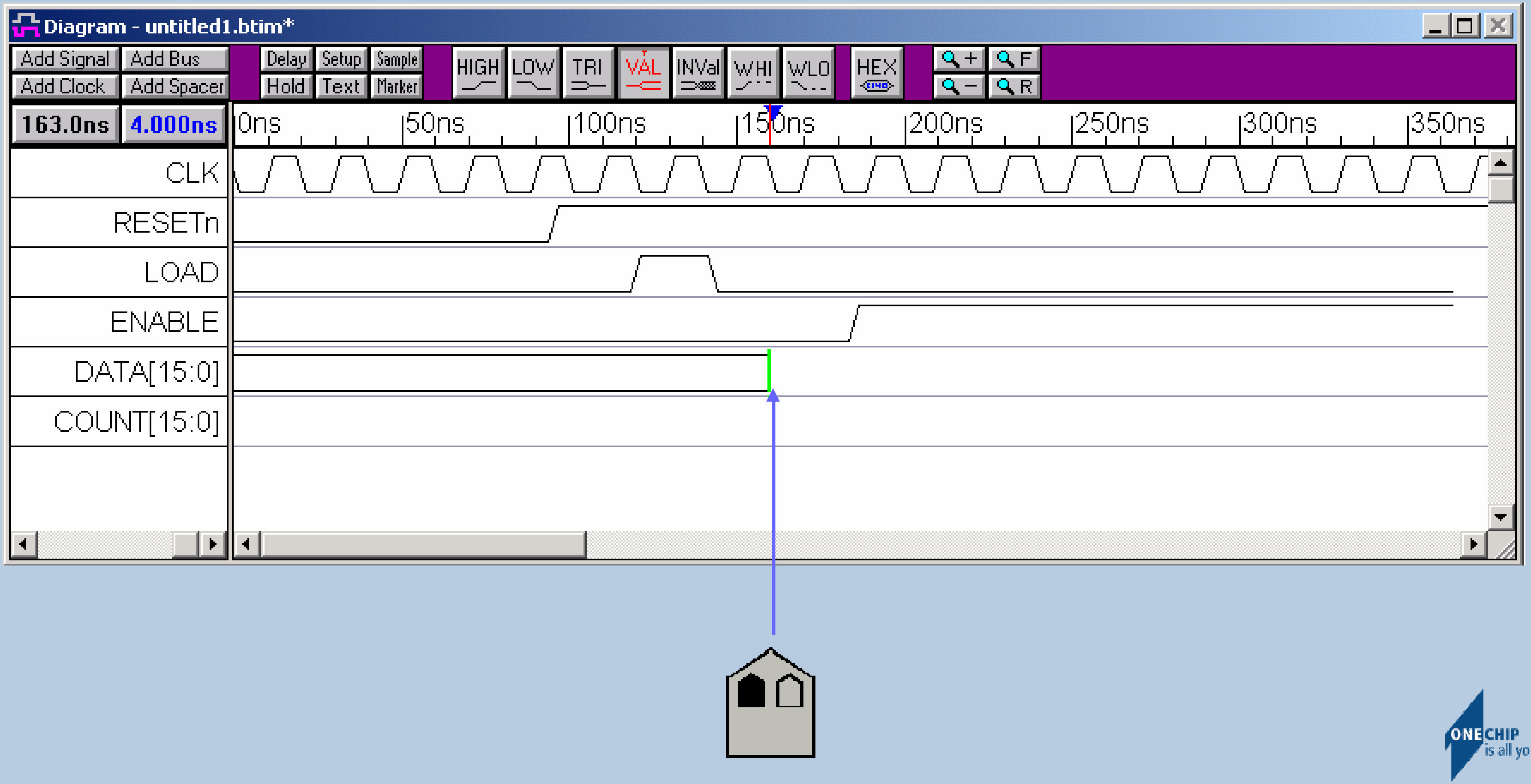


# Drawing Busses

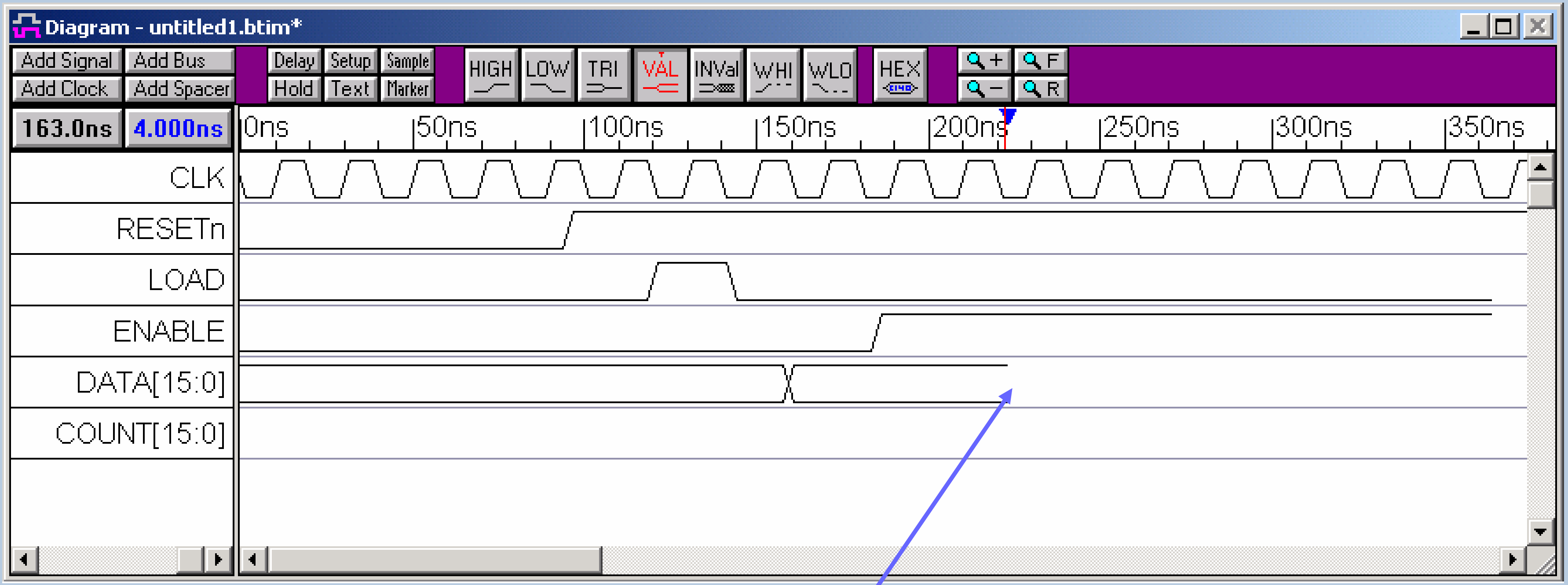
Button will stay in "VAL" state

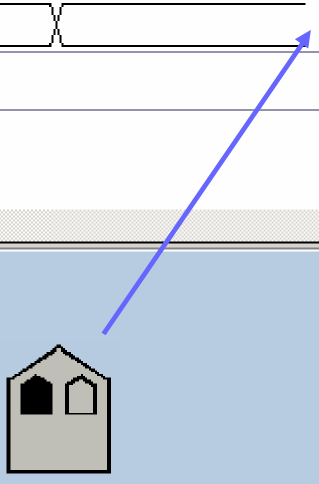


# Drawing Busses

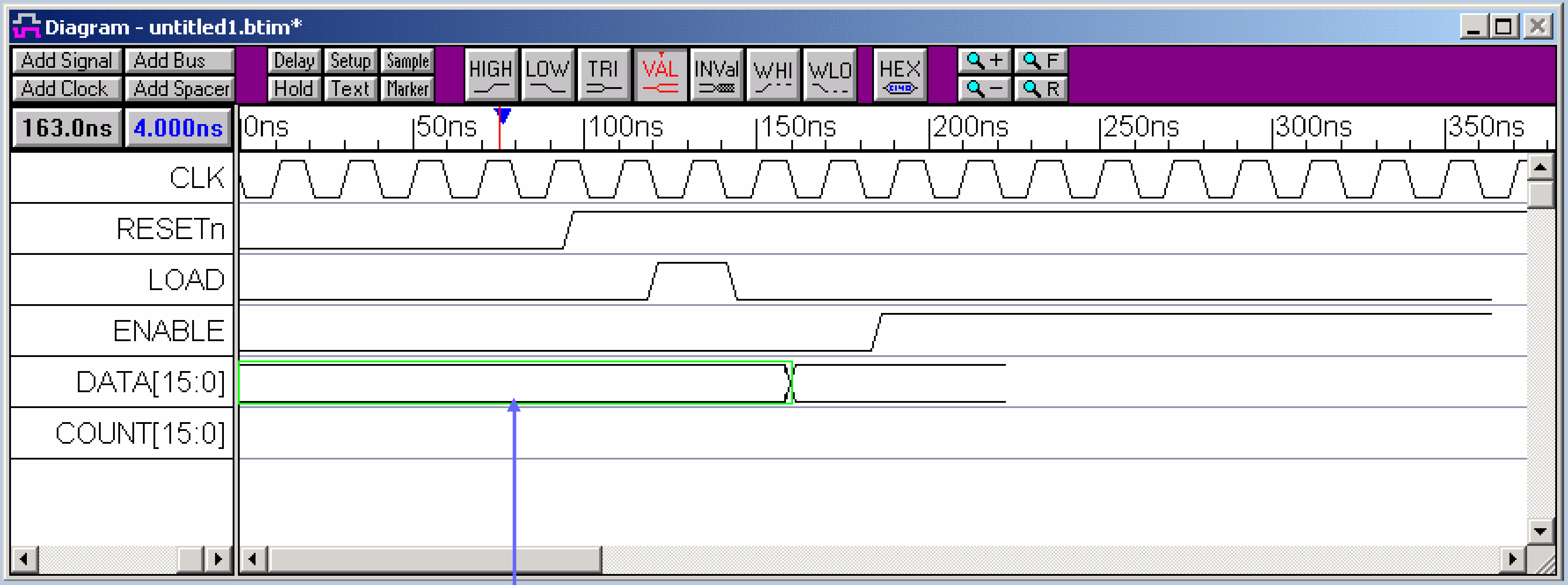


# Drawing Busses





# Drawing Busses



Double Click!

# Drawing Busses

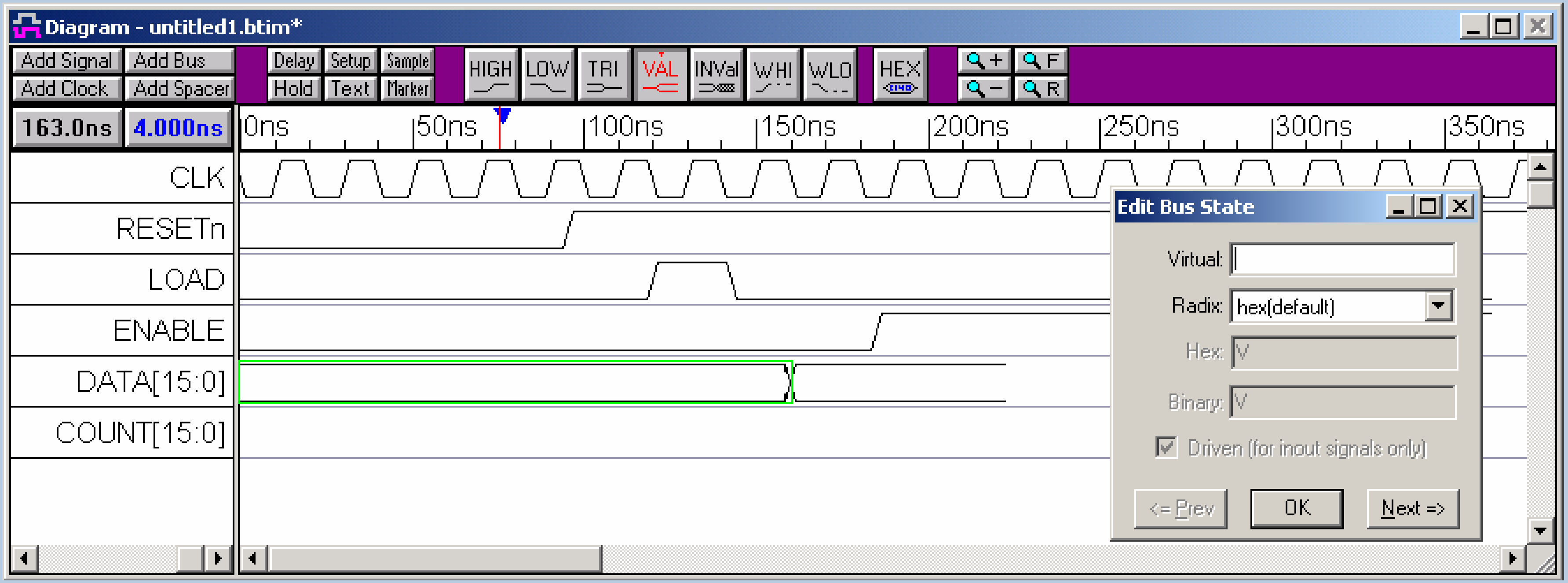


Diagram - untitled1.btim*

Edit Bus State

Virtual:

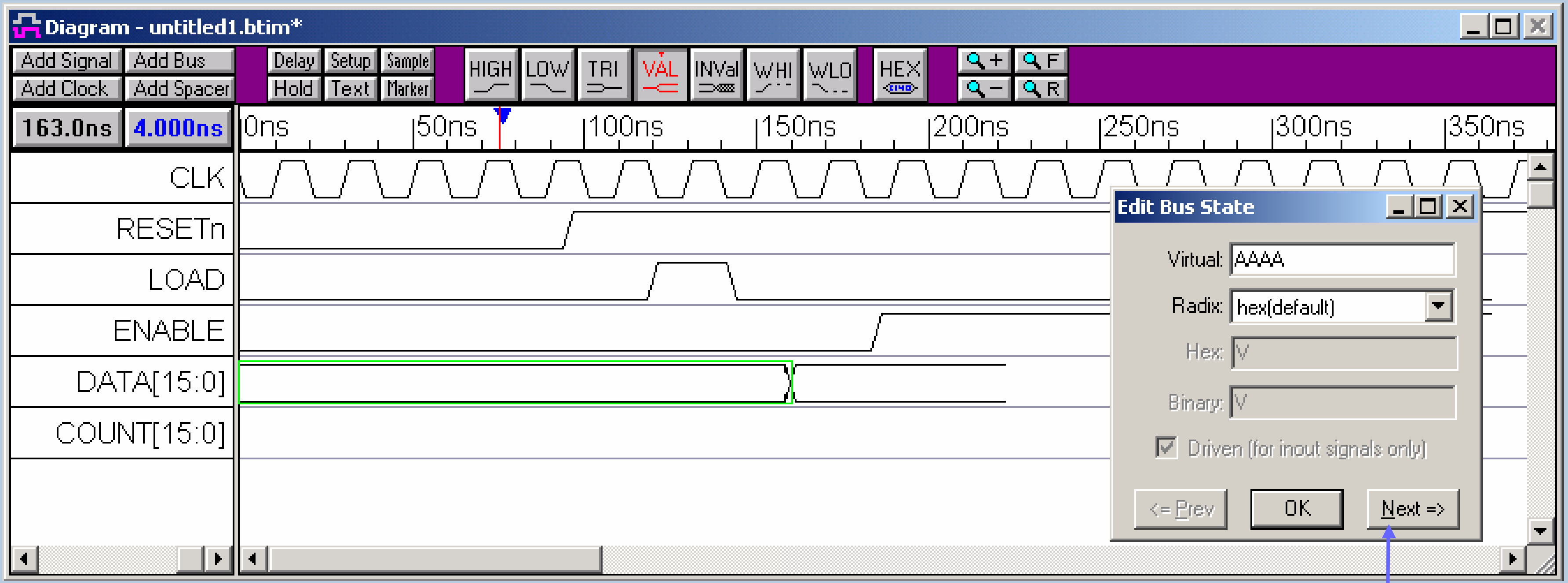
Radix: hex(default)

Hex: V

Binary: V

☑ Driven (for inout signals only)

# Drawing Busses



Edit Bus State

Virtual: AAAA

Radix: hex(default)

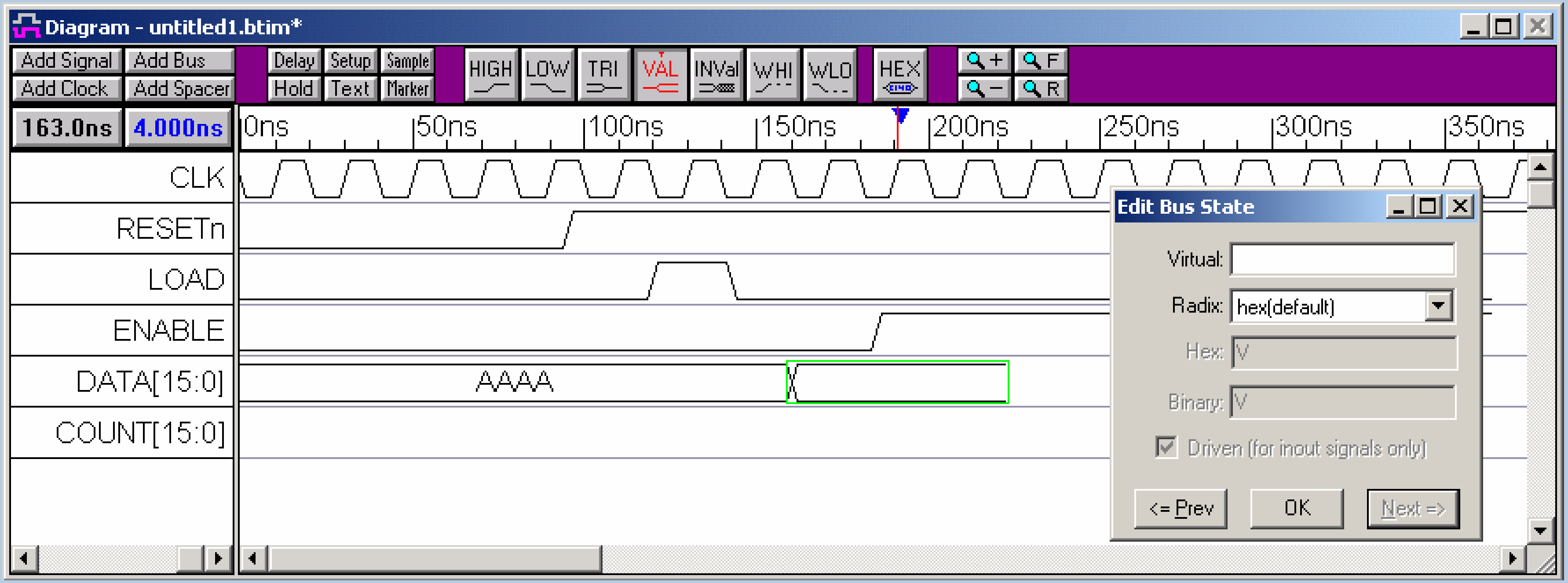
Hex: V

Binary: V

☑ Driven (for inout signals only)

<= Prev | OK | Next =>

# Drawing Busses



Virtual:

Radix: hex(default)

Hex: V

Binary: V

☑ Driven (for inout signals only)

# Drawing Busses

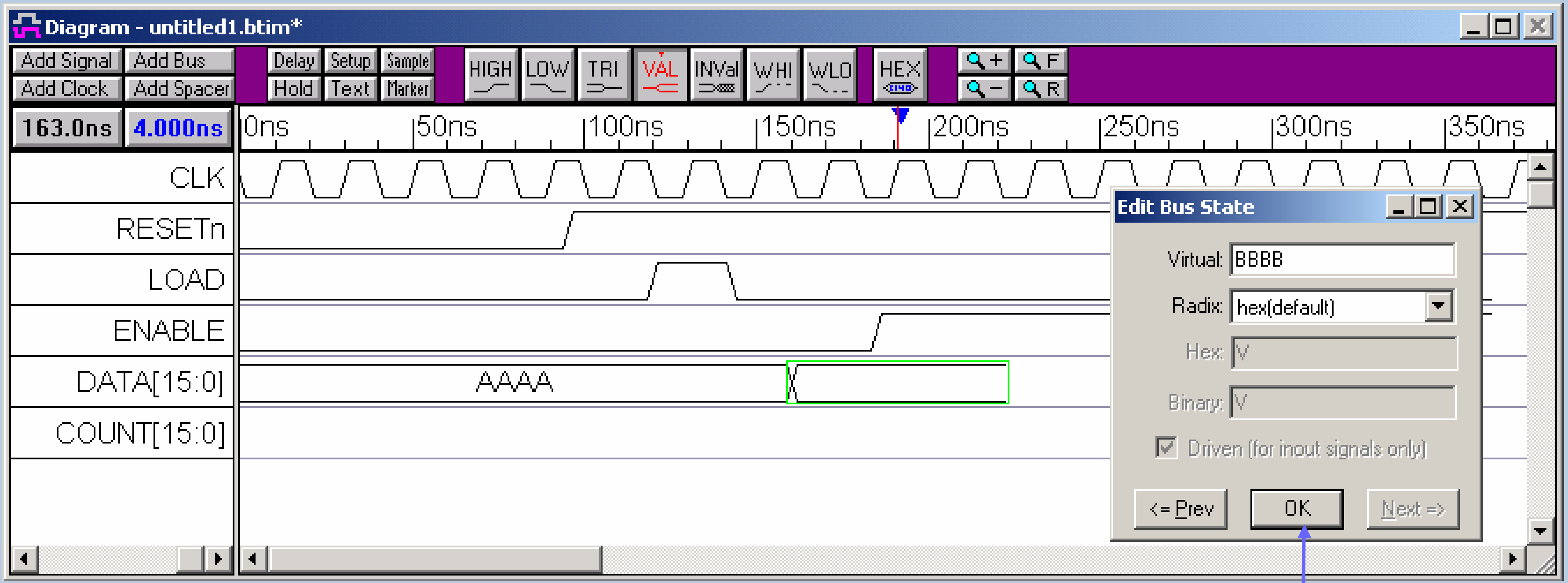


Diagram - untitled1.btim*

Edit Bus State

Virtual: BBBB

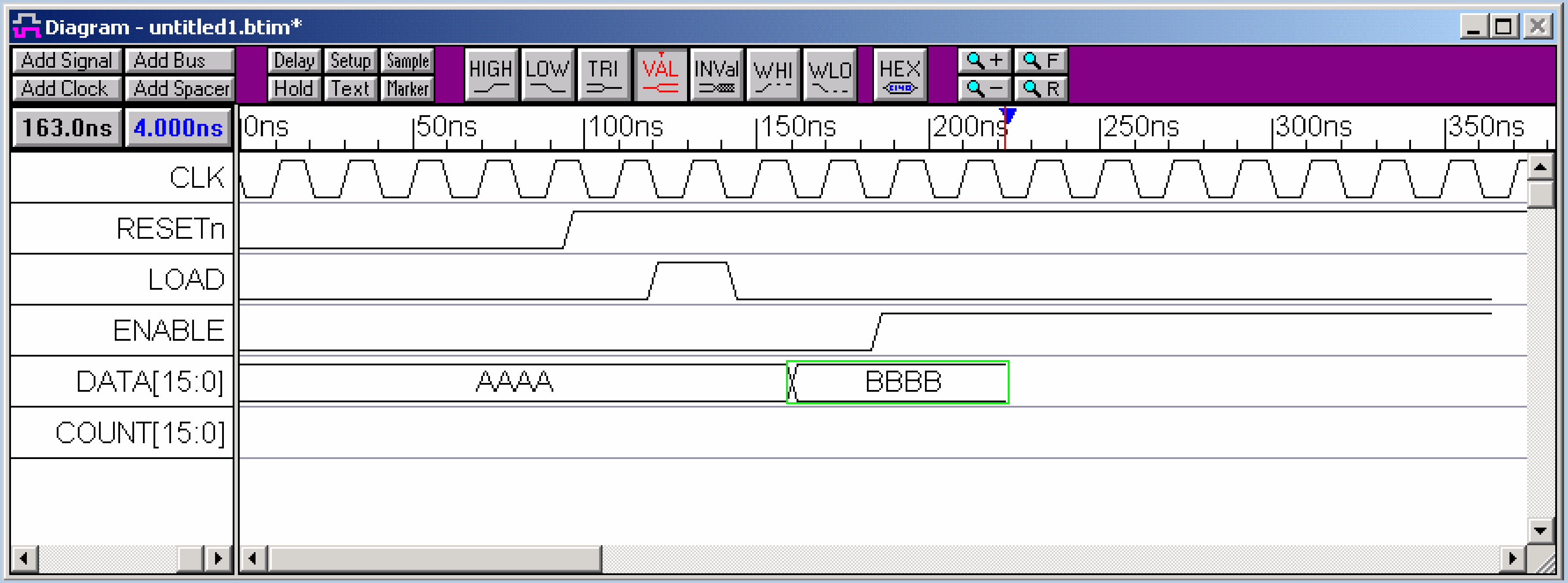
Radix: hex(default)

Hex: V

Binary: V

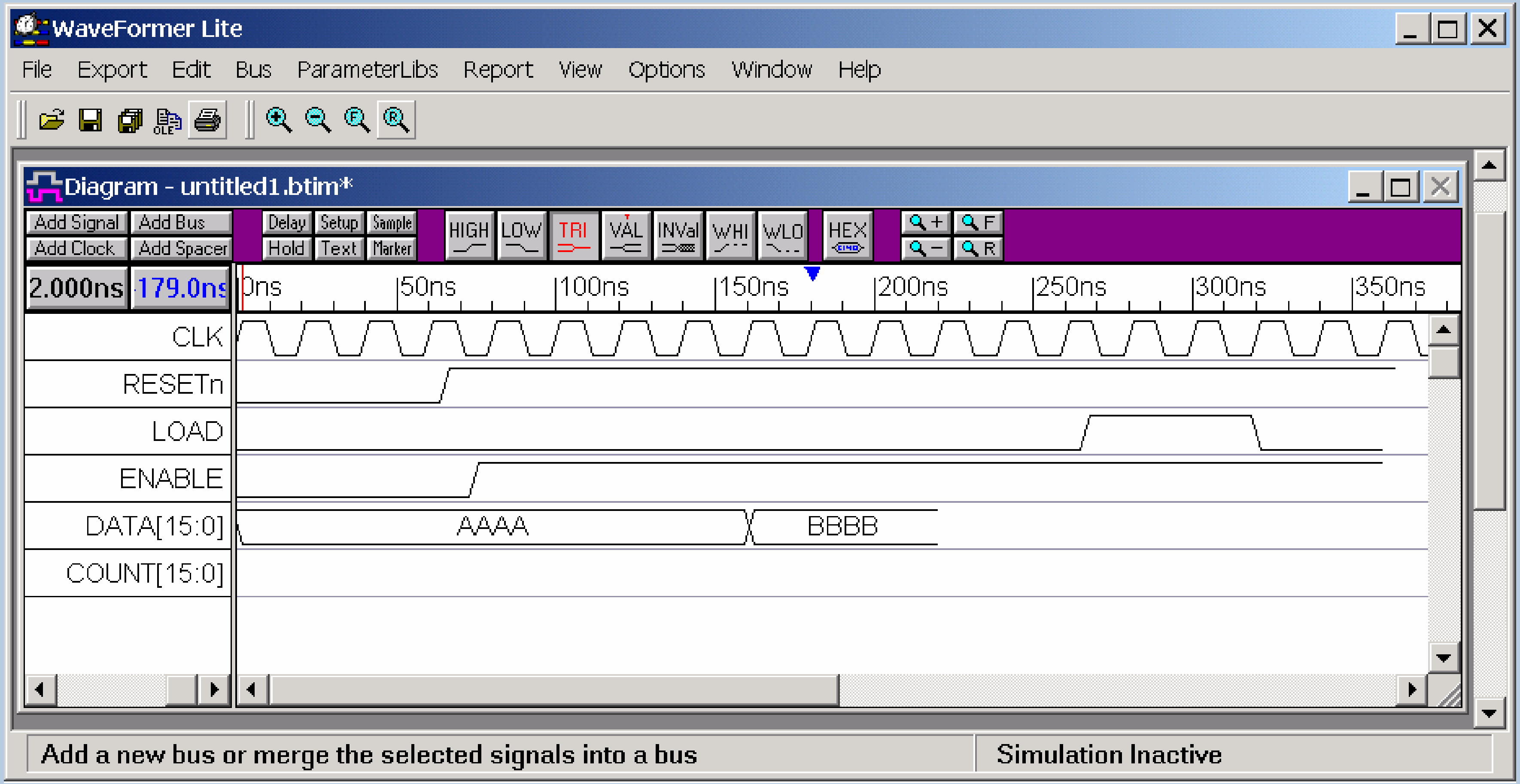
☑ Driven (for inout signals only)

# Drawing Busses



# Editing Signals

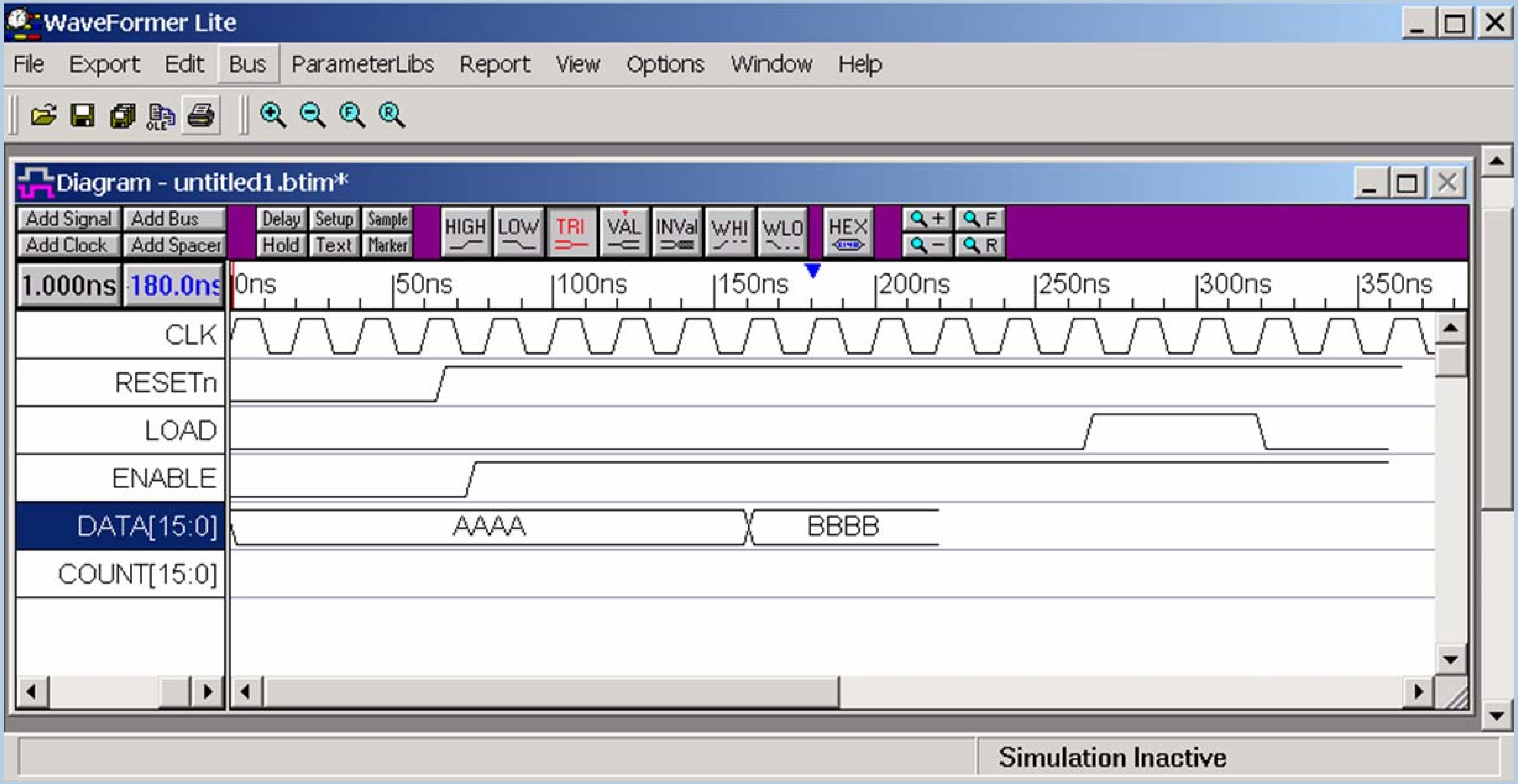
## *Appending and Inserting*



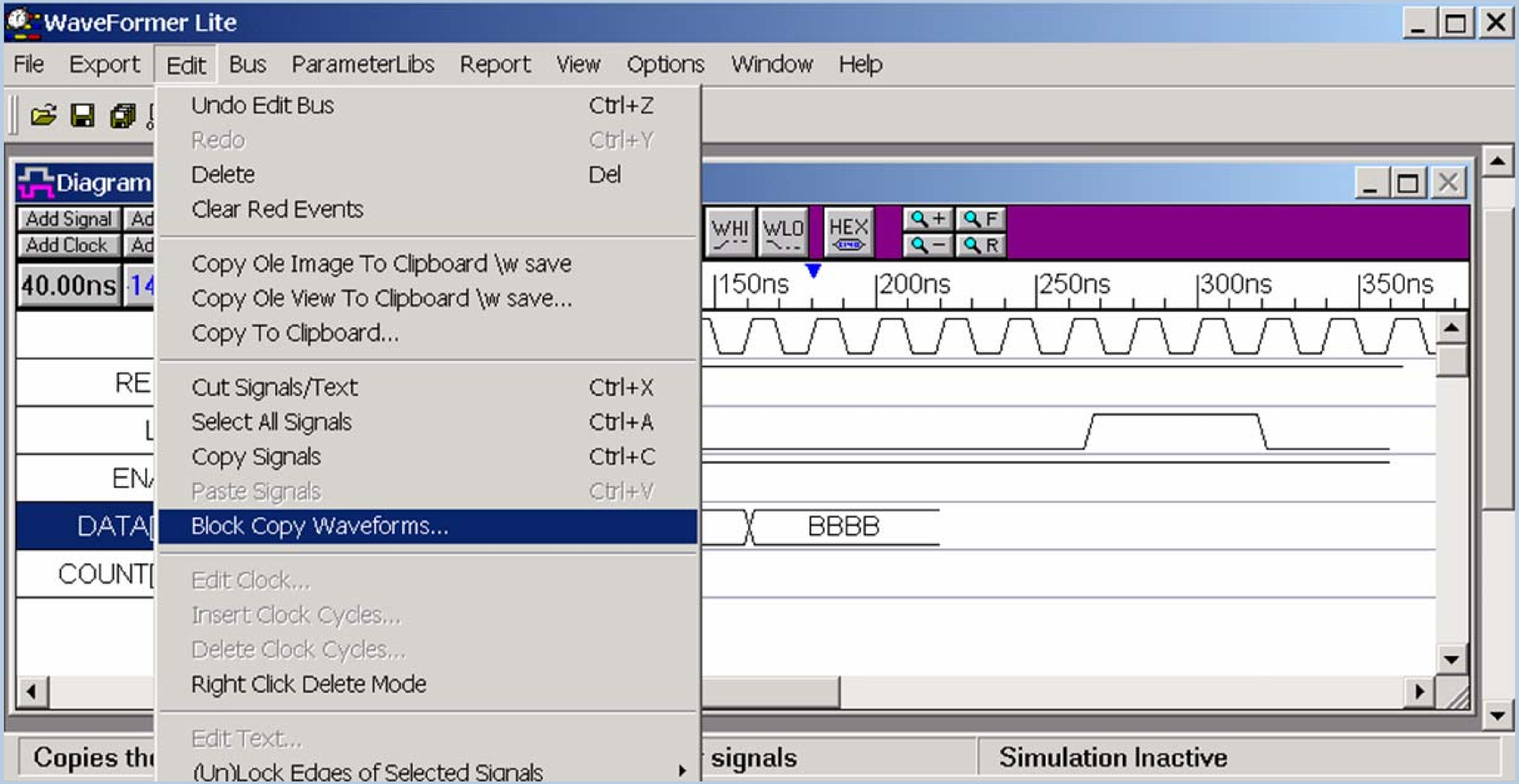
Add a new bus or merge the selected signals into a bus

Simulation Inactive

# Editing Signals
## *Appending and Inserting*

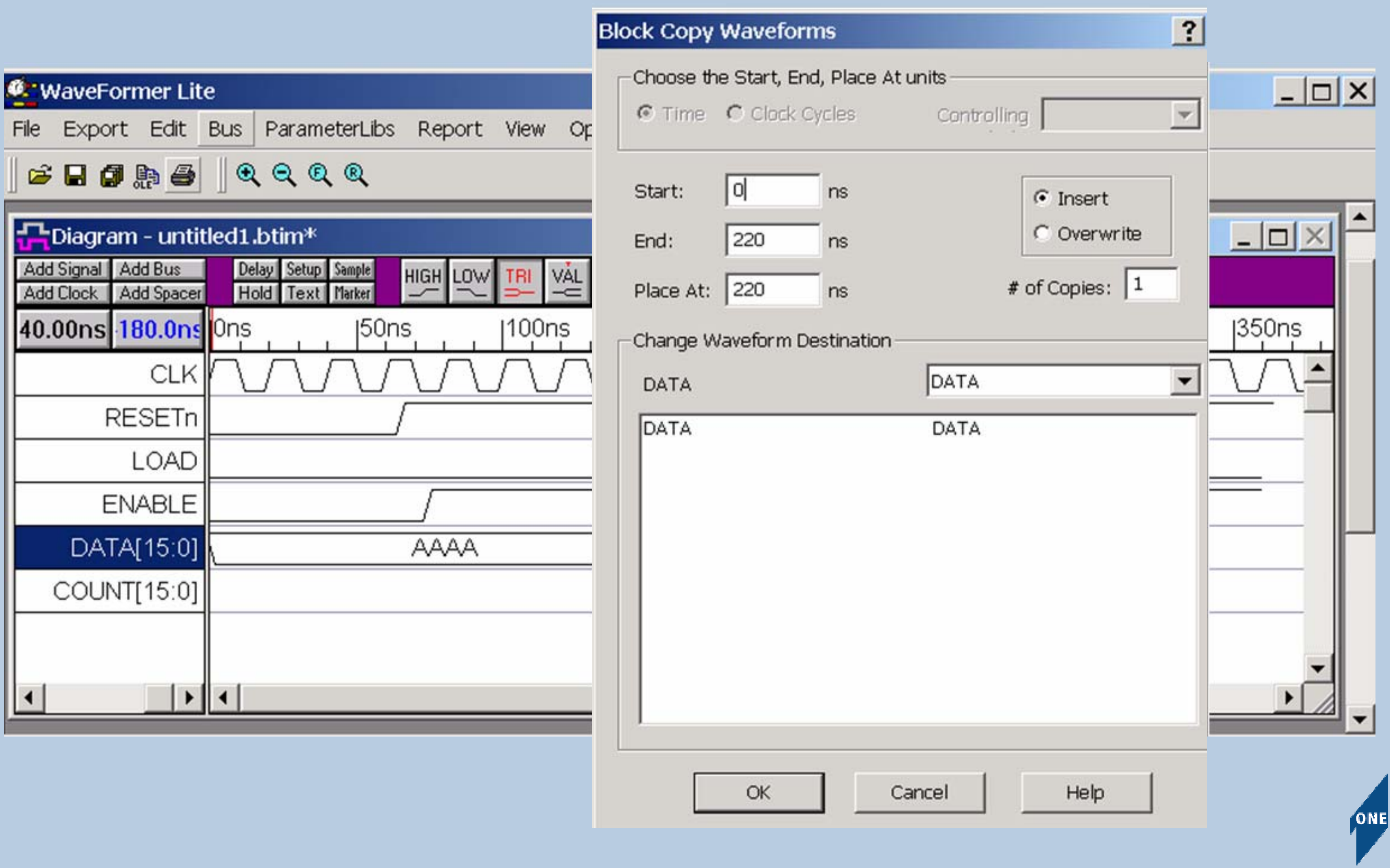


# Editing Signals
## *Appending and Inserting*



| | |
|---|---|
| Undo Edit Bus | Ctrl+Z |
| Redo | Ctrl+Y |
| Delete | Del |
| Clear Red Events | |
| Copy Ole Image To Clipboard \w save | |
| Copy Ole View To Clipboard \w save... | |
| Copy To Clipboard... | |
| Cut Signals/Text | Ctrl+X |
| Select All Signals | Ctrl+A |
| Copy Signals | Ctrl+C |
| Paste Signals | Ctrl+V |
| Block Copy Waveforms... | |
| Edit Clock... | |
| Insert Clock Cycles... | |
| Delete Clock Cycles... | |
| Right Click Delete Mode | |
| Edit Text... | |
| (Un)Lock Edges of Selected Signals | ▸ |

# Editing Signals
## *Appending and Inserting*



Block Copy Waveforms

Choose the Start, End, Place At units

● Time ○ Clock Cycles Controlling

Start: 0 ns

End: 220 ns

Place At: 220 ns

● Insert

○ Overwrite

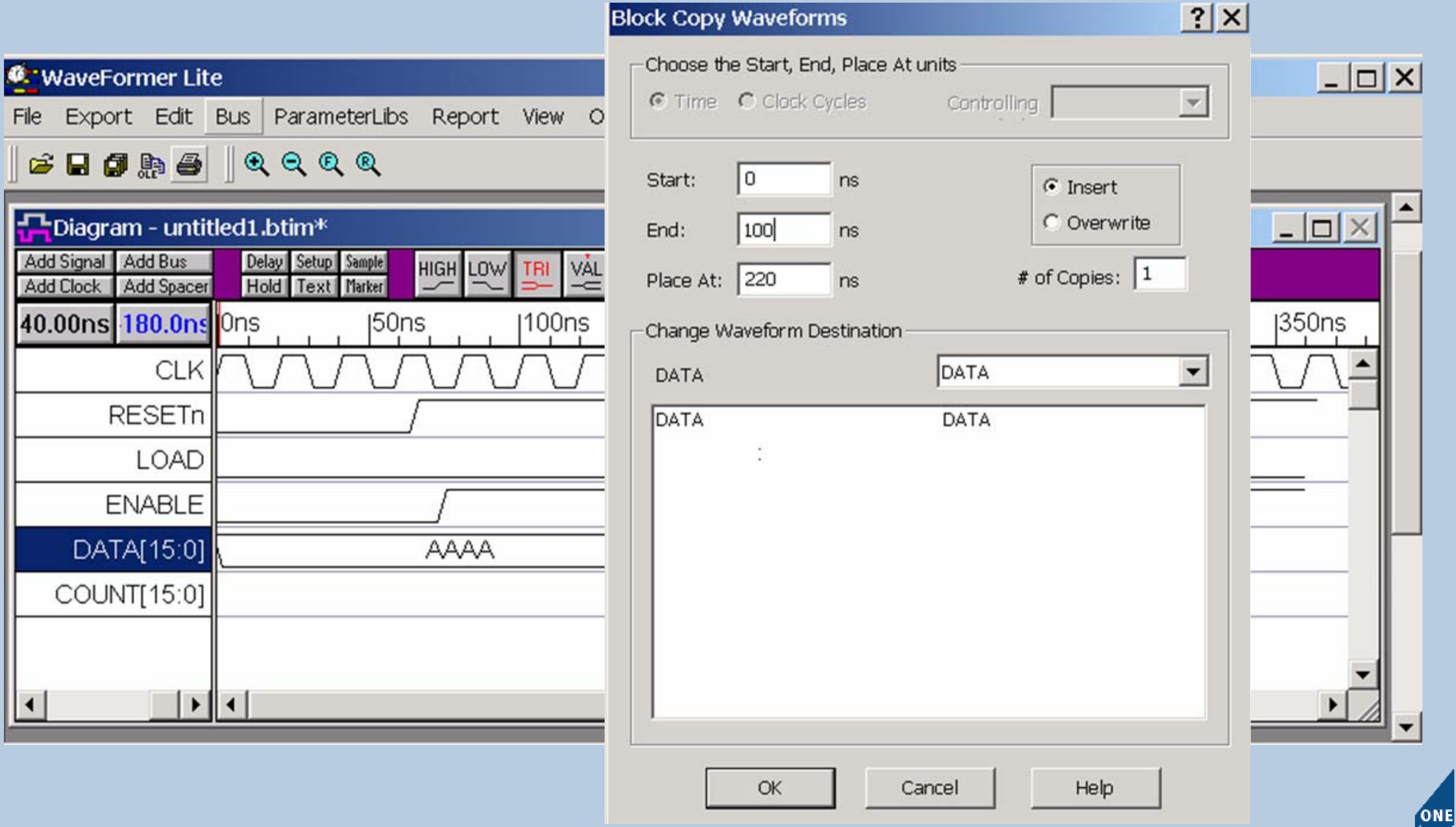
# of Copies: 1

Change Waveform Destination

DATA DATA

| | |
|---|---|
| DATA | DATA |

# Editing Signals
## *Appending and Inserting*



WaveFormer Lite
File Export Edit Bus ParameterLibs Report View O
Diagram - untitled1.btim*
Add Signal Add Bus Delay Setup Sample HIGH LOW TRI VAL
Add Clock Add Spacer Hold Text Marker
40.00ns 180.0ns 0ns 50ns 100ns 350ns
CLK
RESETn
LOAD
ENABLE
DATA[15:0]
AAAA
COUNT[15:0]

Block Copy Waveforms

Choose the Start, End, Place At units

● Time ○ Clock Cycles Controlling

Start: 0 ns

End: 100 ns

Place At: 220 ns

● Insert

○ Overwrite

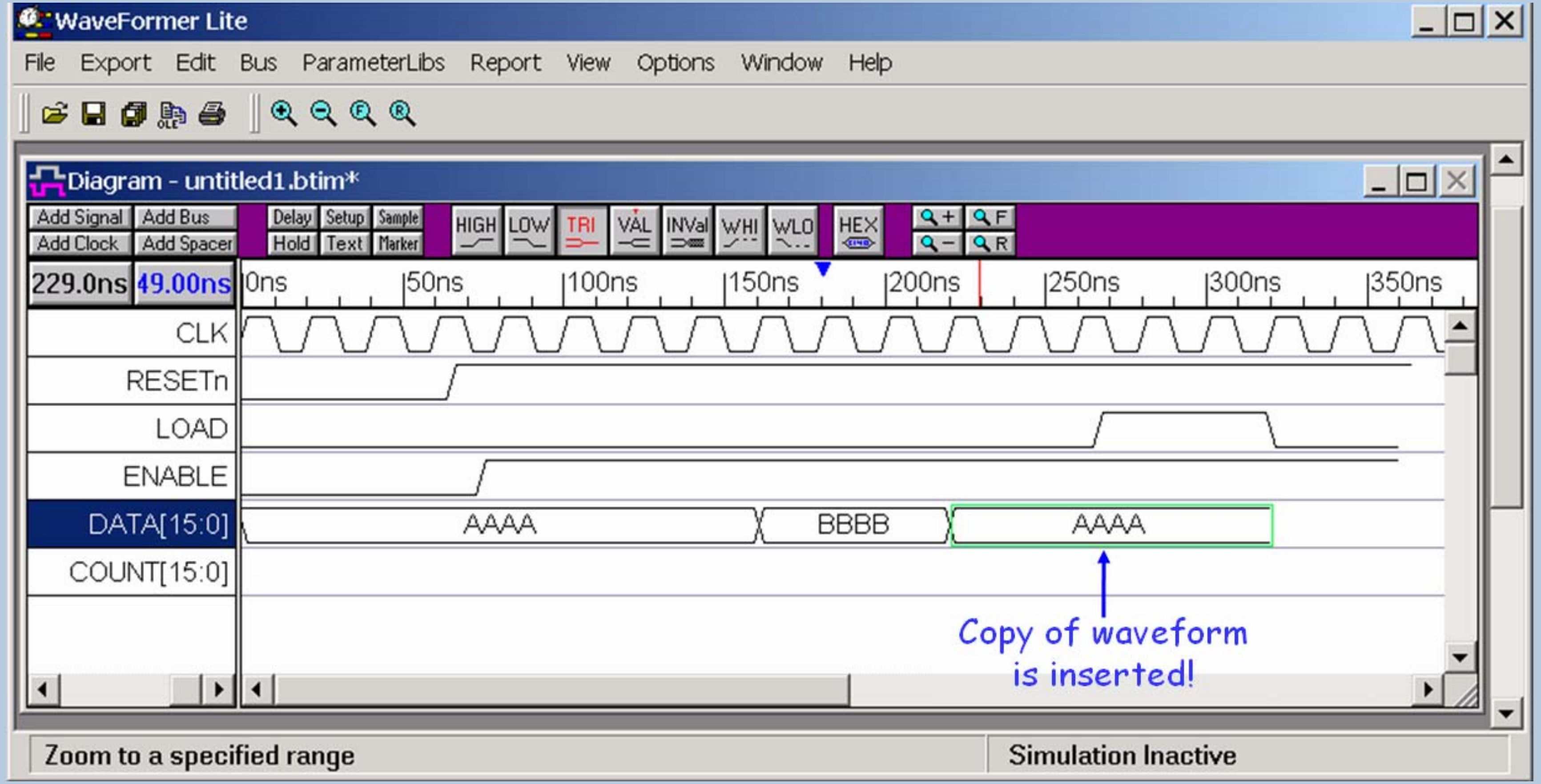
# of Copies: 1

Change Waveform Destination

DATA DATA

| | |
|---|---|
| DATA | DATA |

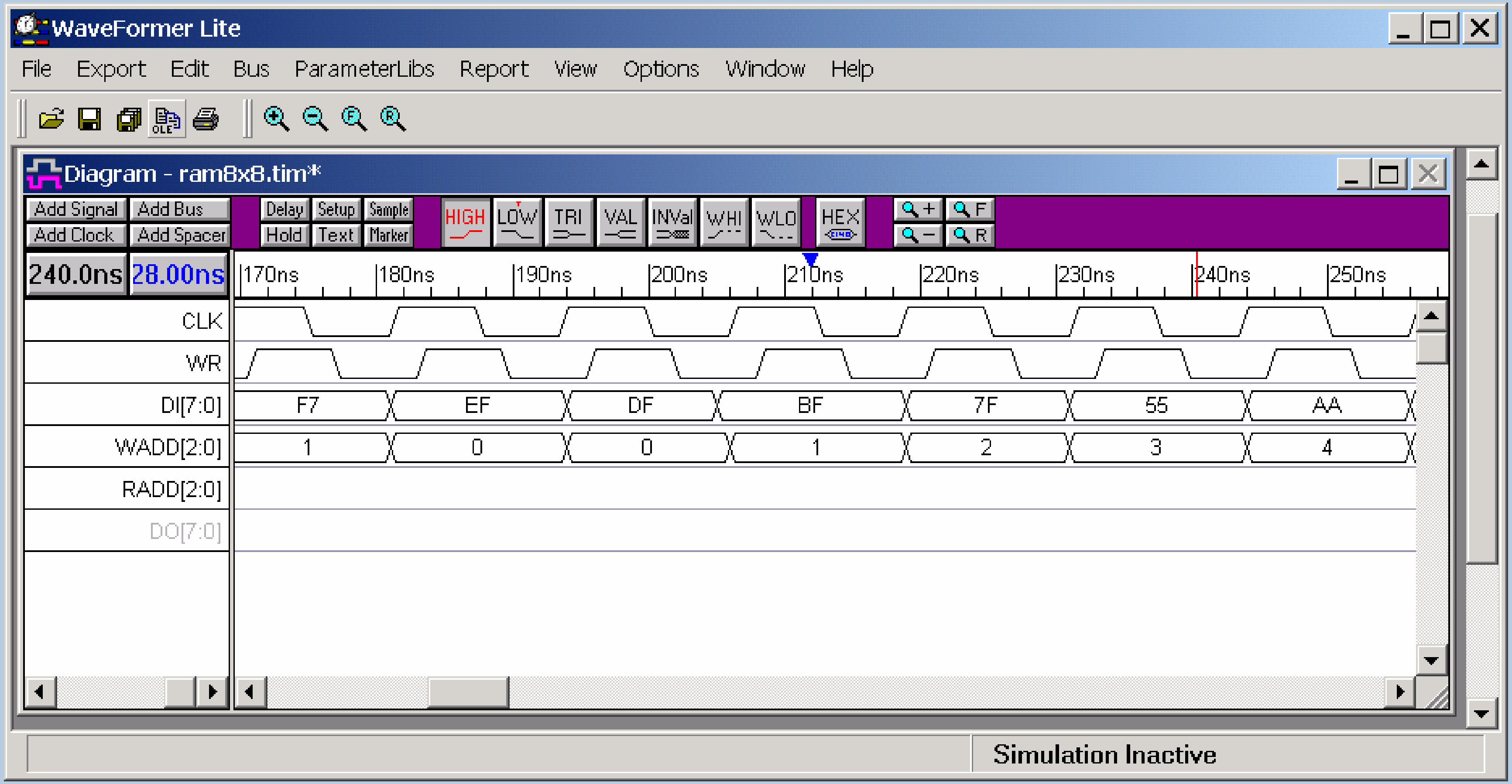
# Editing Signals
## *Appending and Inserting*


WaveFormer Lite
File Export Edit Bus ParameterLibs Report View Options Window Help
Diagram - untitled1.btim*
Add Signal
Add Bus
Add Clock
Add Spacer
Delay Setup Sample
Hold Text Marker
HIGH LOW TRI VAL INVal WHI WLO HEX
229.0ns 49.00ns
0ns 50ns 100ns 150ns 200ns 250ns 300ns 350ns
CLK
RESETn
LOAD
ENABLE
DATA[15:0]
COUNT[15:0]
AAAA
BBBB
AAAA
Zoom to a specified range
Simulation Inactive

Copy of waveform is inserted!

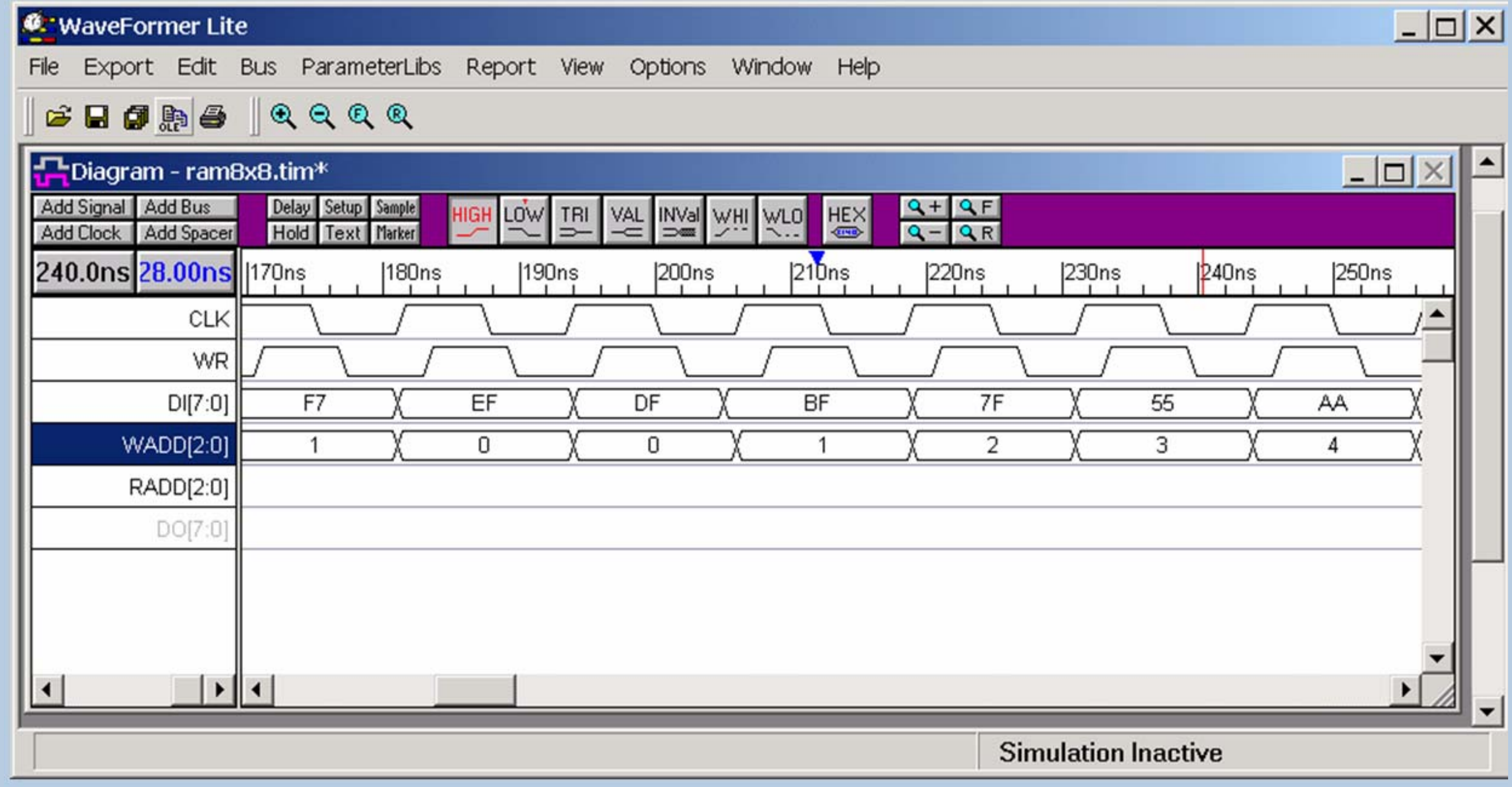
# Copying to a Different Signal

## ■ Signal Can Be Copied



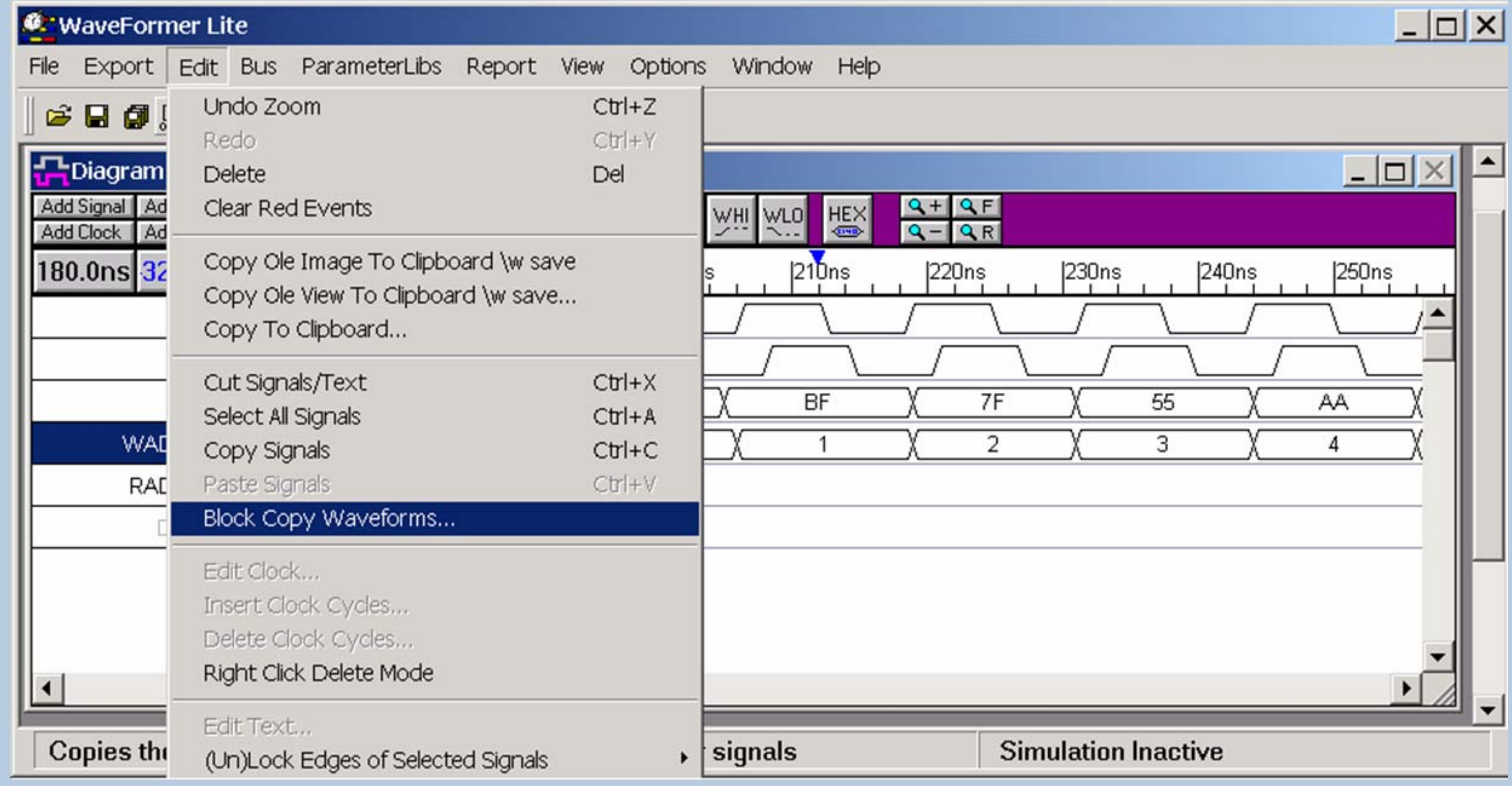
# Copying to a Different Signal

- Signal Can Be Copied



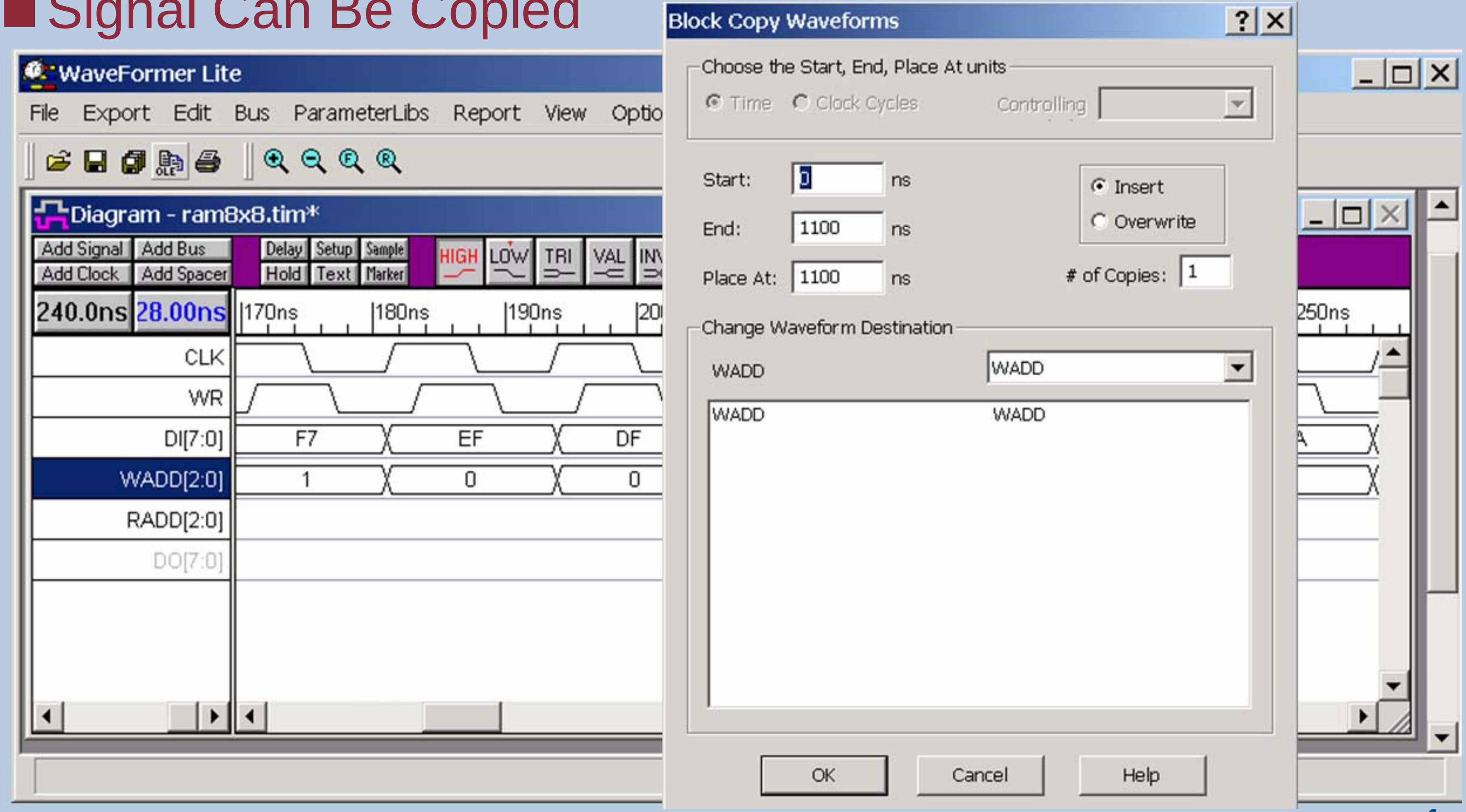
# Copying to a Different Signal

- Signal Can Be Copied



# Copying to a Different Signal

- Signal Can Be Copied



WaveFormer Lite
File Export Edit Bus ParameterLibs Report View Optio
Diagram - ram8x8.tim*
Add Signal Add Bus Delay Setup Sample
Add Clock Add Spacer Hold Text Marker
HIGH LOW TRI VAL INV
240.0ns 28.00ns
170ns 180ns 190ns 20 250ns
CLK
WR
DI[7:0] F7 EF DF
WADD[2:0] 1 0 0
RADD[2:0]
DO[7:0]

Block Copy Waveforms

Choose the Start, End, Place At units
● Time ○ Clock Cycles Controlling

Start: 0 ns

End: 1100 ns

Place At: 1100 ns

● Insert
○ Overwrite

# of Copies: 1

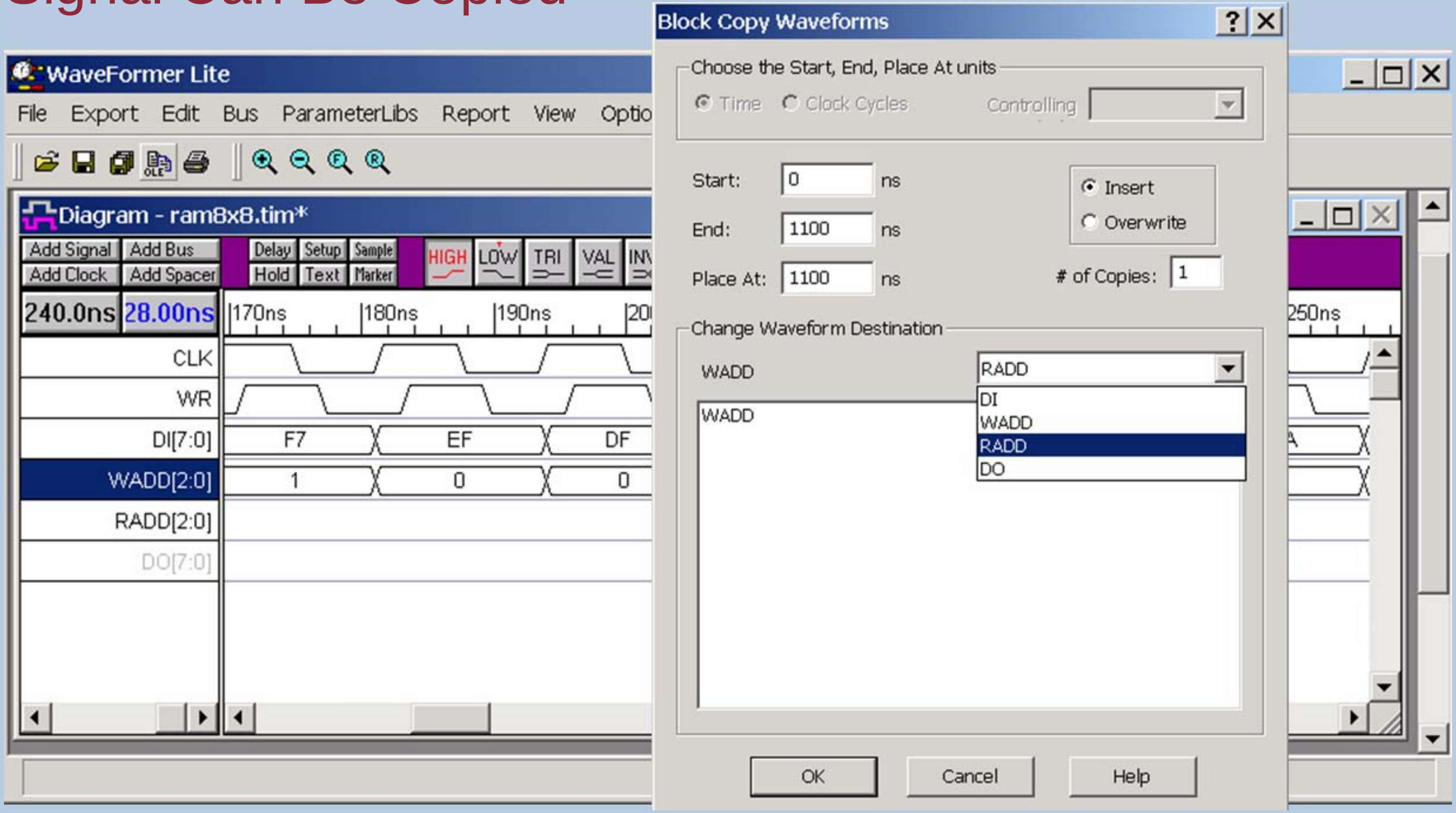
Change Waveform Destination

WADD: WADD

| | |
|---|---|
| WADD | WADD |

# Copying to a Different Signal

- Signal Can Be Copied



Block Copy Waveforms

Choose the Start, End, Place At units: ● Time ○ Clock Cycles

Start: 0 ns

End: 1100 ns

Place At: 1100 ns

● Insert ○ Overwrite

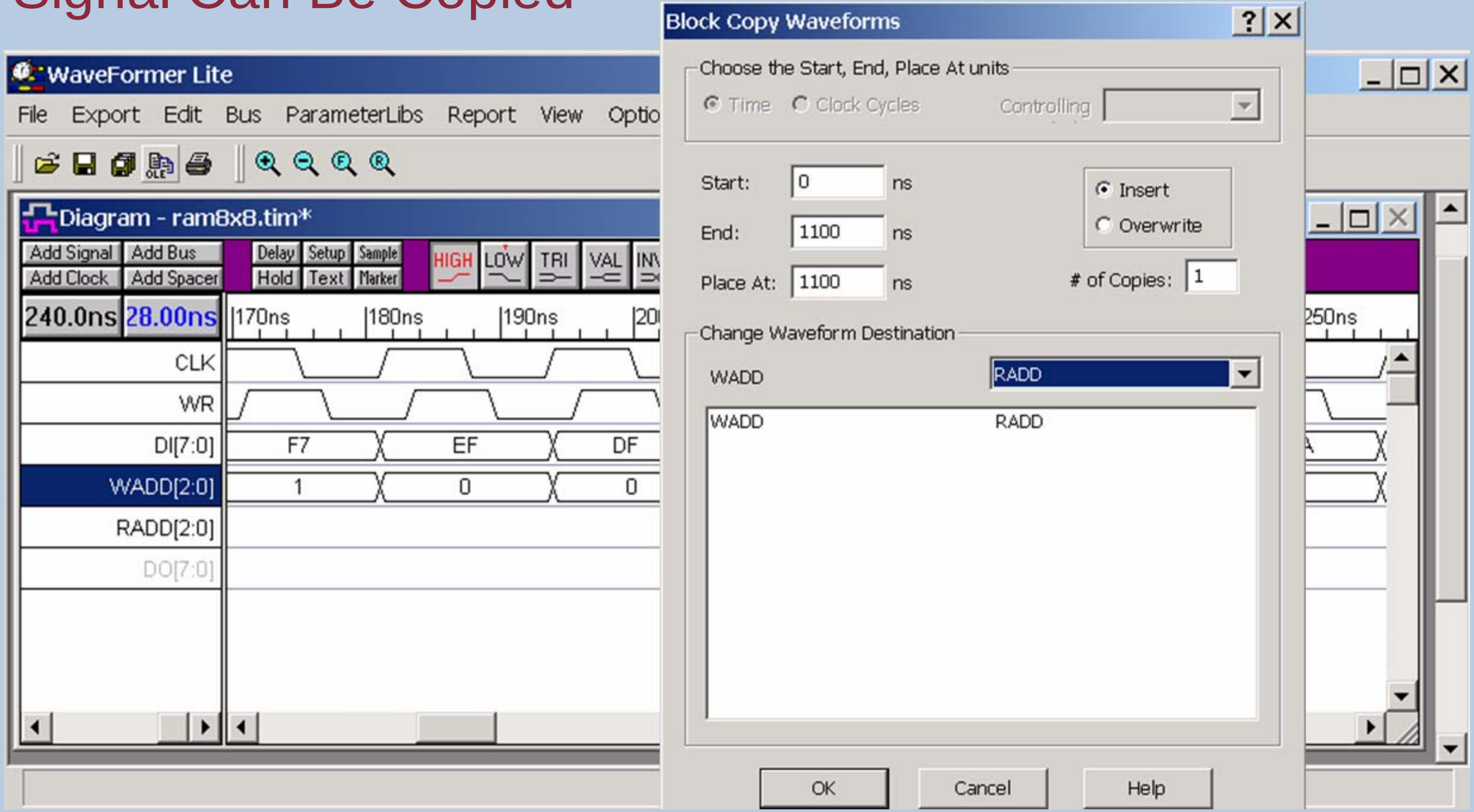
# of Copies: 1

Change Waveform Destination

WADD → RADD

# Copying to a Different Signal

- Signal Can Be Copied



Block Copy Waveforms

Choose the Start, End, Place At units

● Time ○ Clock Cycles Controlling

Start: 0 ns

End: 1100 ns

Place At: 1100 ns

● Insert

○ Overwrite

# of Copies: 1

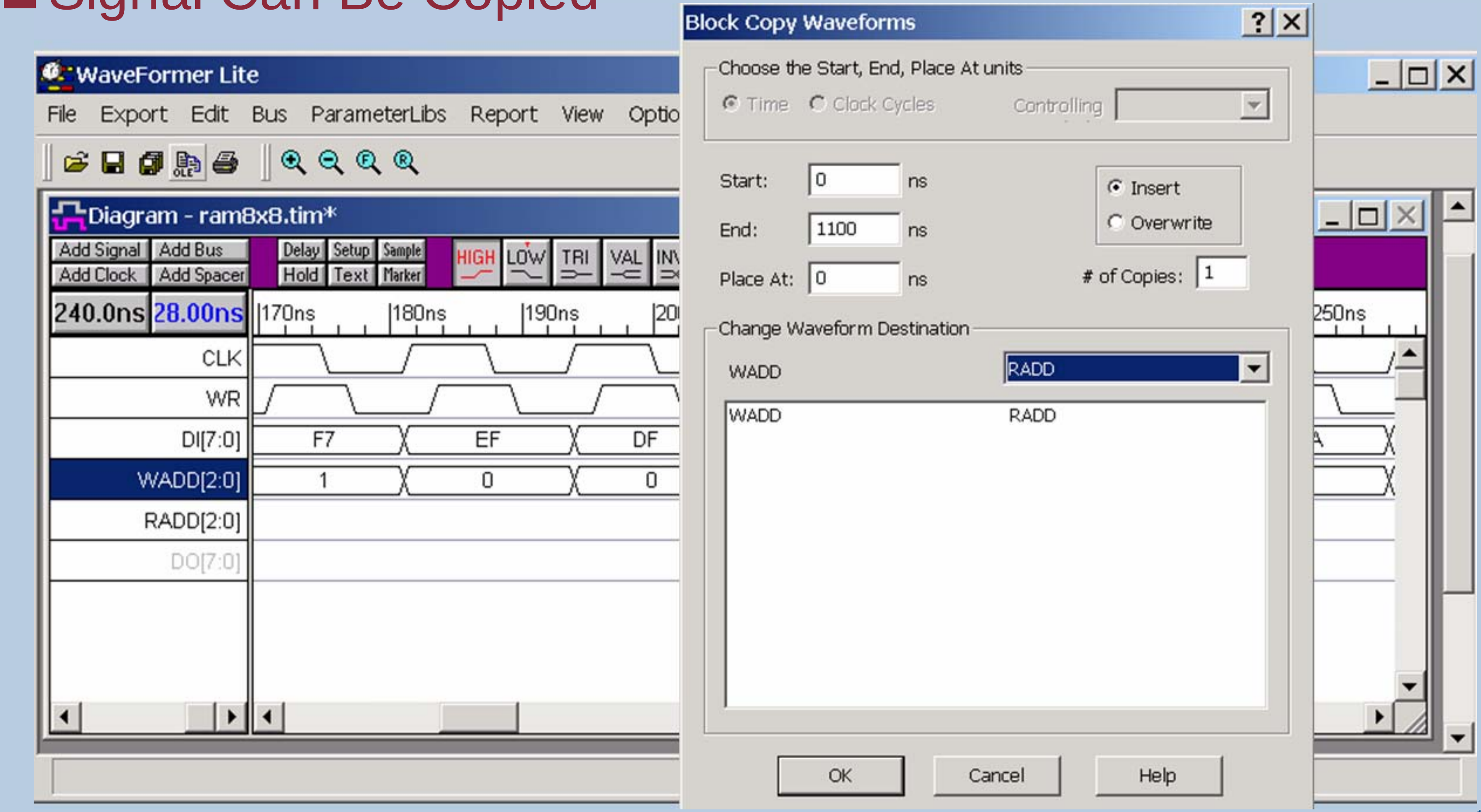
Change Waveform Destination

WADD — RADD

| WADD | RADD |
|---|---|

# Copying to a Different Signal

- Signal Can Be Copied



Block Copy Waveforms

Choose the Start, End, Place At units

● Time ○ Clock Cycles Controlling

Start: 0 ns

End: 1100 ns

Place At: 0 ns

● Insert ○ Overwrite

# of Copies: 1

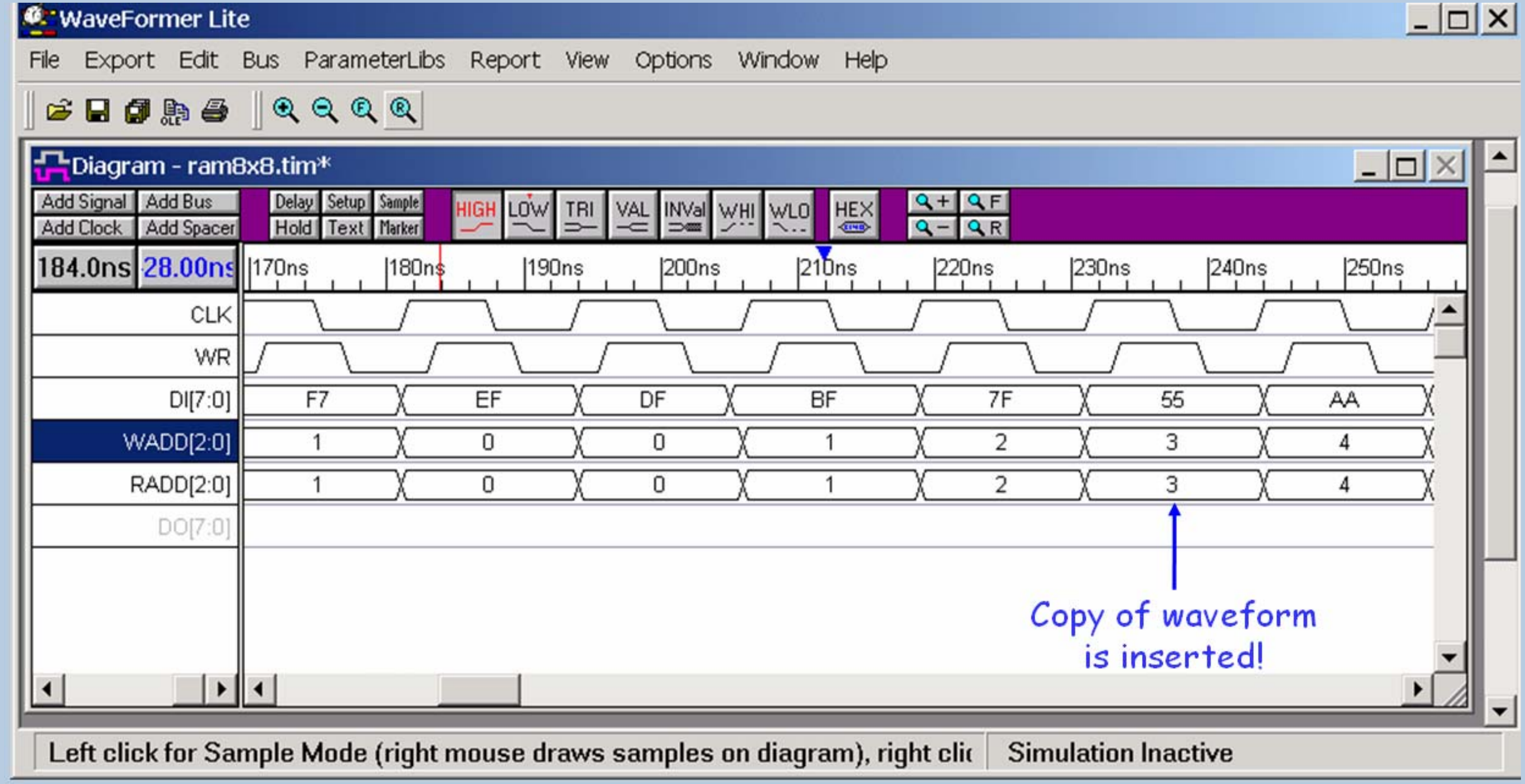
Change Waveform Destination

WADD RADD

| | |
|---|---|
| WADD | RADD |

# Copying to a Different Signal

## ■ Signal Can Be Copied



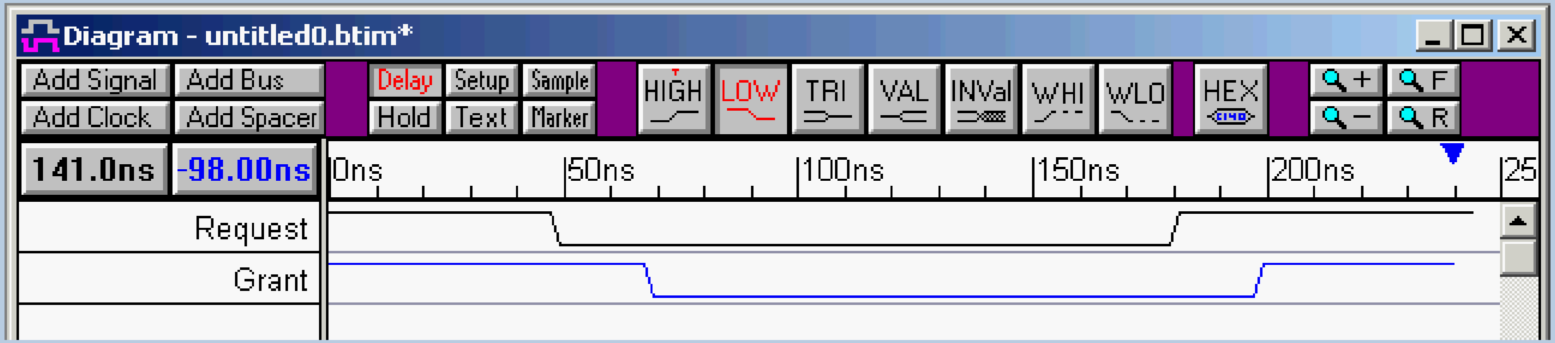
Copy of waveform is inserted!

Left click for Sample Mode (right mouse draws samples on diagram), right clic

Simulation Inactive

# Reactive Test Bench:
## *Stimulus and Expected Response*

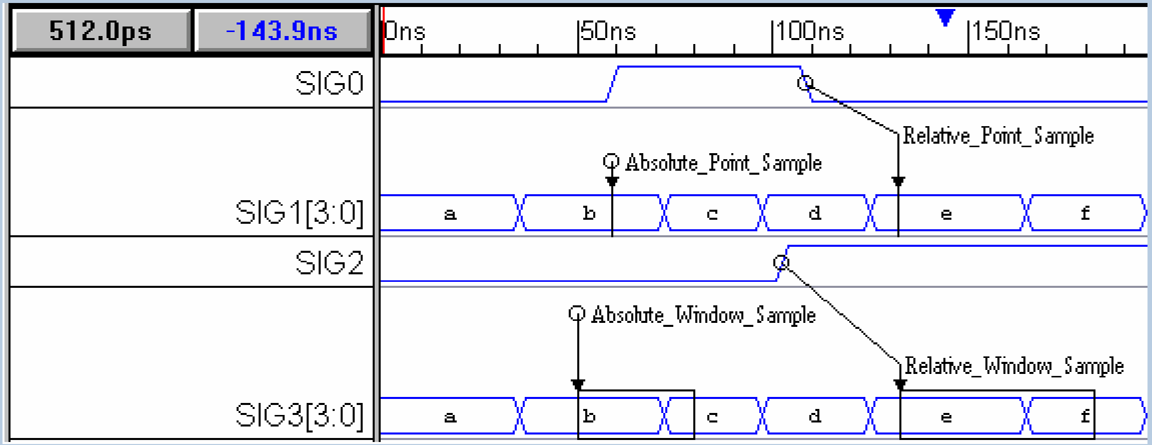
- Draw stimulus waveforms on the input ports of the model under test.
- Draw expected response waveforms on the output ports of the model under test



# Reactive Test Bench:
*Samples*

## Samples Verify MUT Output

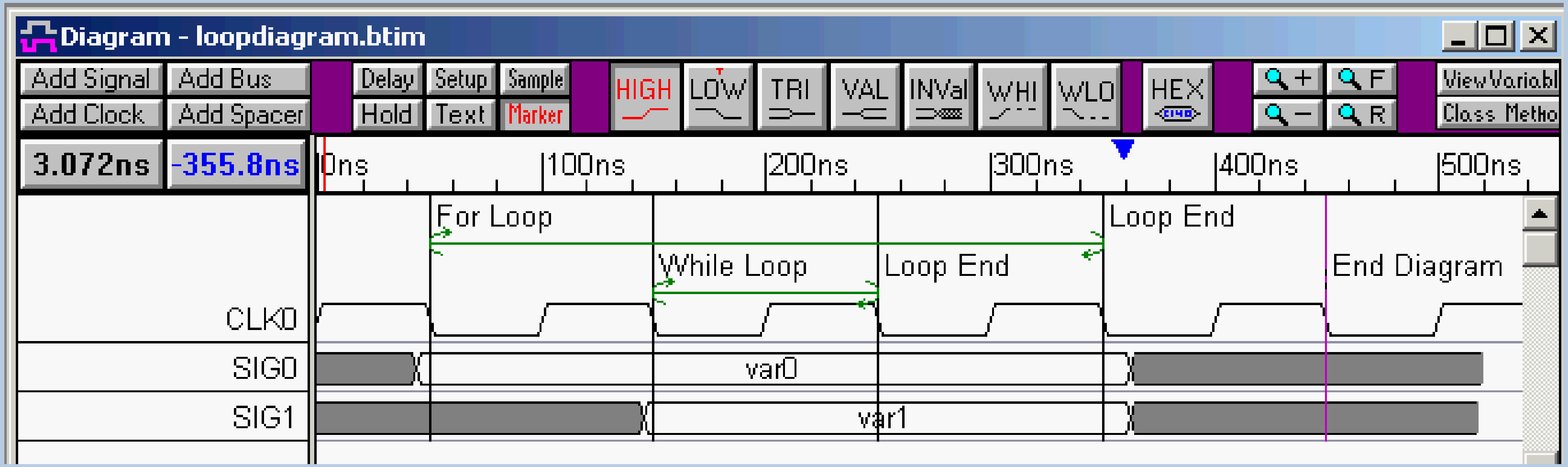
- Sample constructs can monitor and perform actions based on the data sampled
- Sample can work at a single point or over a windowed area
- Sample can perform relative to the beginning of the transaction or relative to another event in the diagram.



# Reactive Test Bench:
*Control & Looping*

## Markers used for Control & Looping Sections of Transactions

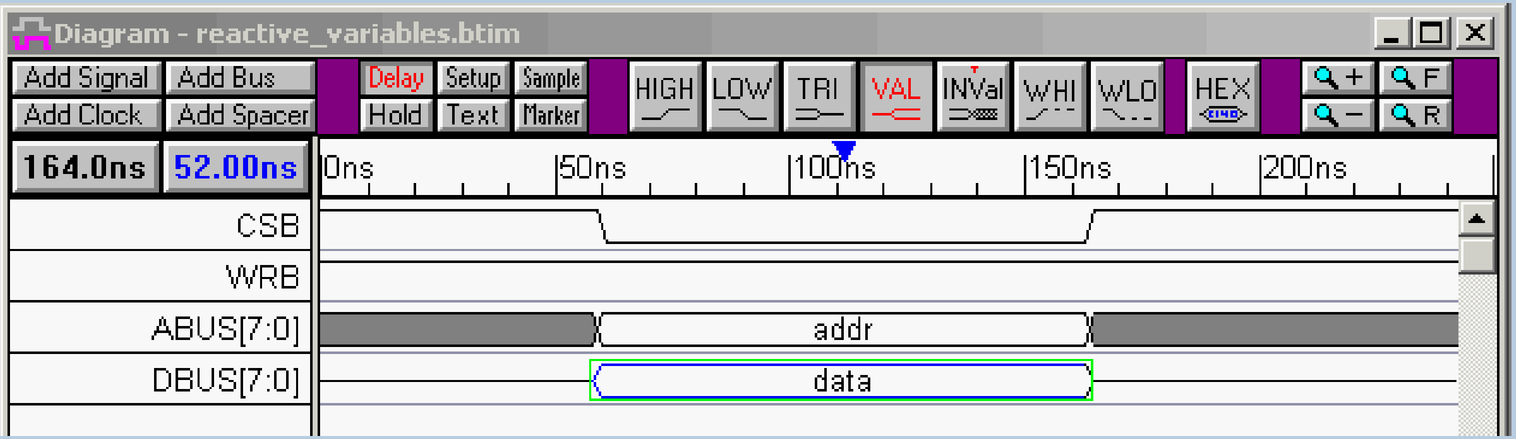
- Specify the end of the transaction
- Create loops using for, while, and repeat loop markers
- Insert HDL code



# Reactive Test Bench:
*Variables*

## Variables Parameterize State Values

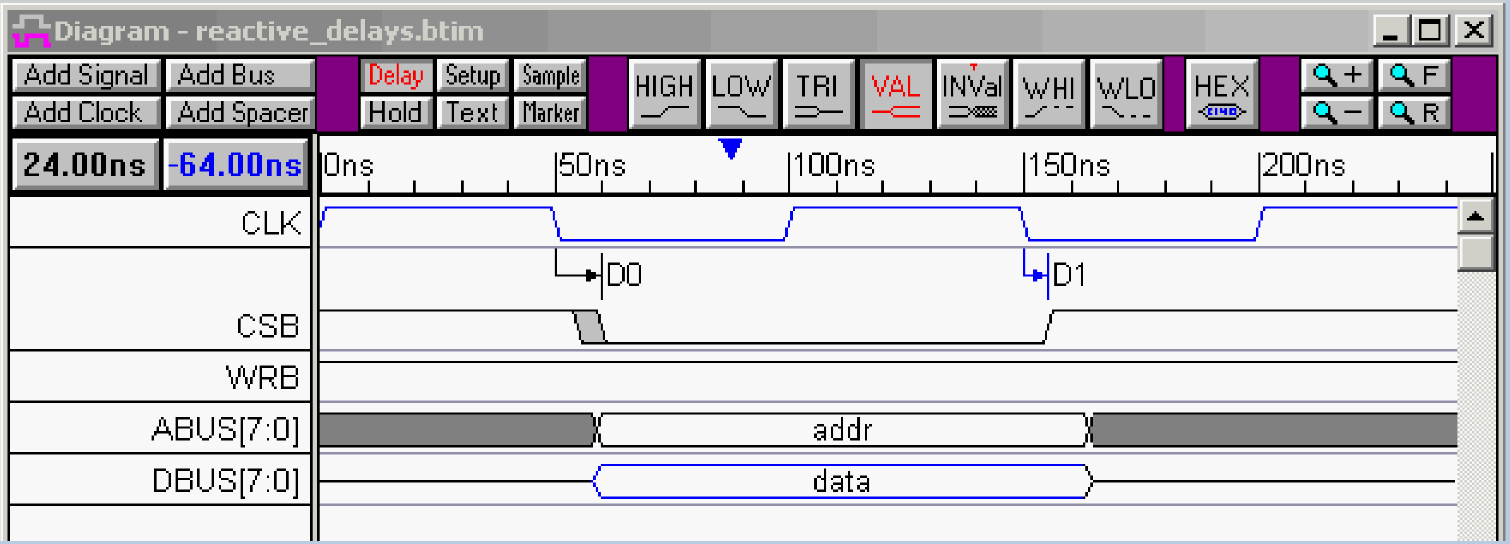
- **Variables can drive values on stimulus waveforms**
- **Variables can store values on expected waveforms**
- **Waveform states can be expressed as conditional expressions using variables**



# Reactive Test Bench:
*Delays*

## Delays Parameterize Time Values

- Delays represent the time between two edges in the diagram
  - Specify min and max values
- Delay values can be time or cycle-based
- Conditionally control when edges occur



# Reactive Test Bench:
## *Help Resources*

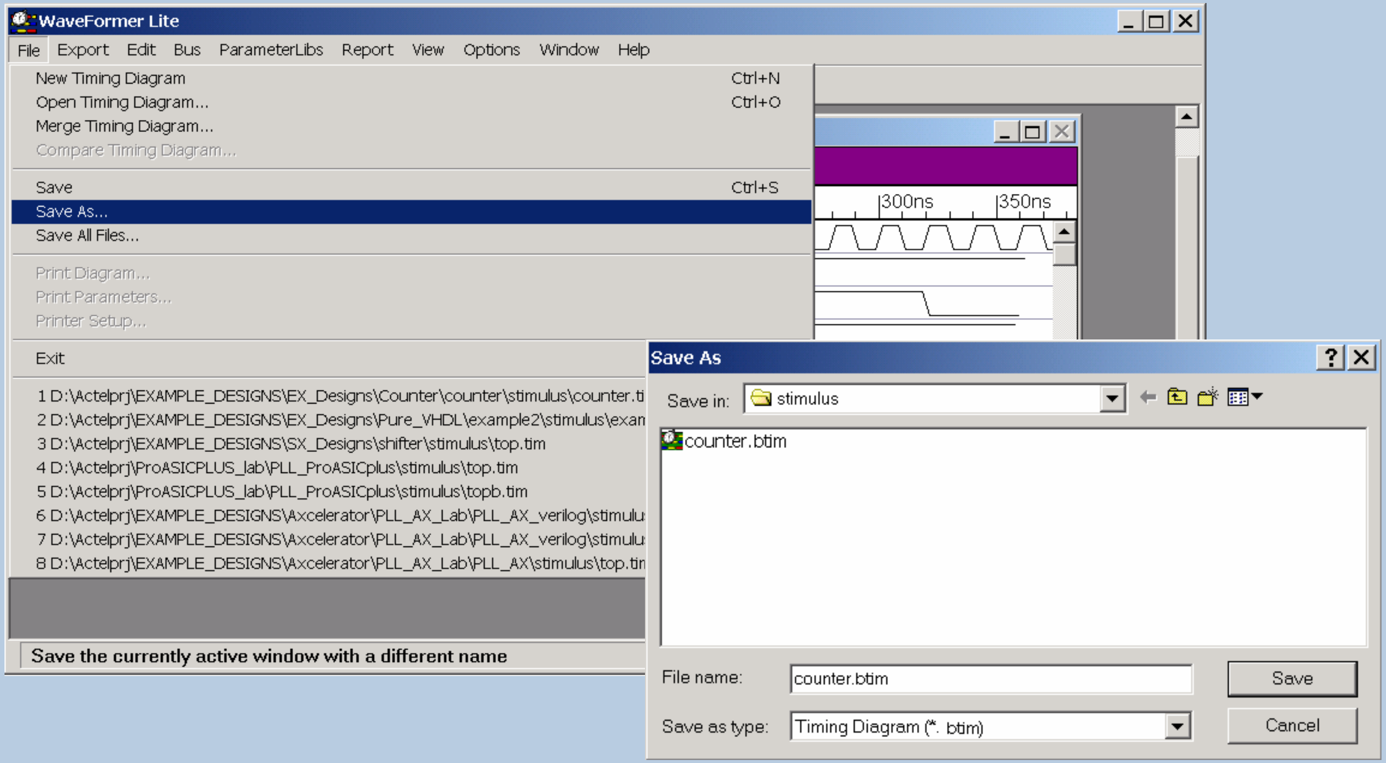
- Online Manual:
  - **Choose Reactive Test Bench Generation Under the Help menu**
- PDF Manual:
  - **Reactive_testbench_Generation_Option.pdf under the Help folder in the SynaptiCAD install directory**
- SynaptiCAD's website: www.syncad.com

# Saving Stimulus

## Save Stimulus

**File > Save**

- **File Name May Contain Name of Top-level Module**
- **Stimulus Appears on Libero File Manager Tab**


WaveFormer Lite
File
Export
Edit
Bus
ParameterLibs
Report
View
Options
Window
Help
New Timing Diagram Ctrl+N
Open Timing Diagram... Ctrl+O
Merge Timing Diagram...
Compare Timing Diagram...
Save Ctrl+S
Save As...
Save All Files...
Print Diagram...
Print Parameters...
Printer Setup...
Exit
1 D:\Actelprj\EXAMPLE_DESIGNS\EX_Designs\Counter\counter\stimulus\counter.ti
2 D:\Actelprj\EXAMPLE_DESIGNS\EX_Designs\Pure_VHDL\example2\stimulus\exan
3 D:\Actelprj\EXAMPLE_DESIGNS\SX_Designs\shifter\stimulus\top.tim
4 D:\Actelprj\ProASICPLUS_lab\PLL_ProASICplus\stimulus\top.tim
5 D:\Actelprj\ProASICPLUS_lab\PLL_ProASICplus\stimulus\topb.tim
6 D:\Actelprj\EXAMPLE_DESIGNS\Axcelerator\PLL_AX_Lab\PLL_AX_verilog\stimulu
7 D:\Actelprj\EXAMPLE_DESIGNS\Axcelerator\PLL_AX_Lab\PLL_AX_verilog\stimulu
8 D:\Actelprj\EXAMPLE_DESIGNS\Axcelerator\PLL_AX_Lab\PLL_AX\stimulus\top.tin
300ns
350ns
Save As
Save
Cancel

Save the currently active window with a different name

Save in: stimulus

counter.btim

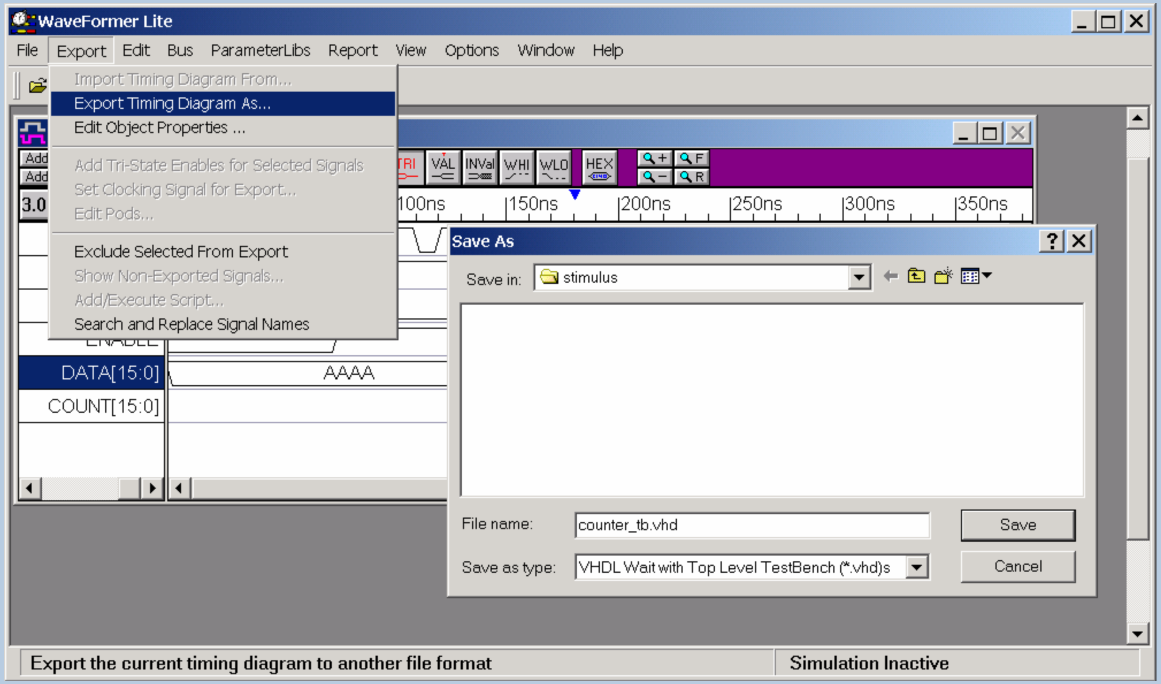
File name: counter.btim

Save as type: Timing Diagram (*. btim)

# Generating the Testbench

## Select Export from WaveFormer Lite Menu

- WaveFormer Lite Has Many Export Options
- Recommendations
  - VHDL Testbench - Select “VHDL with Top Level Testbench”
  - Verilog Testbench - Select “Verilog with Top Level Testbench”


WaveFormer Lite
File
Export
Edit
Bus
ParameterLibs
Report
View
Options
Window
Help
Import Timing Diagram From...
Export Timing Diagram As...
Edit Object Properties ...
Add Tri-State Enables for Selected Signals
Set Clocking Signal for Export...
Edit Pods...
Exclude Selected From Export
Show Non-Exported Signals...
Add/Execute Script...
Search and Replace Signal Names
TRI
VAL
INVal
WHI
WLO
HEX
100ns
150ns
200ns
250ns
300ns
350ns
ENABLE
DATA[15:0]
AAAA
COUNT[15:0]
Save As
Save
Cancel

Save in: stimulus

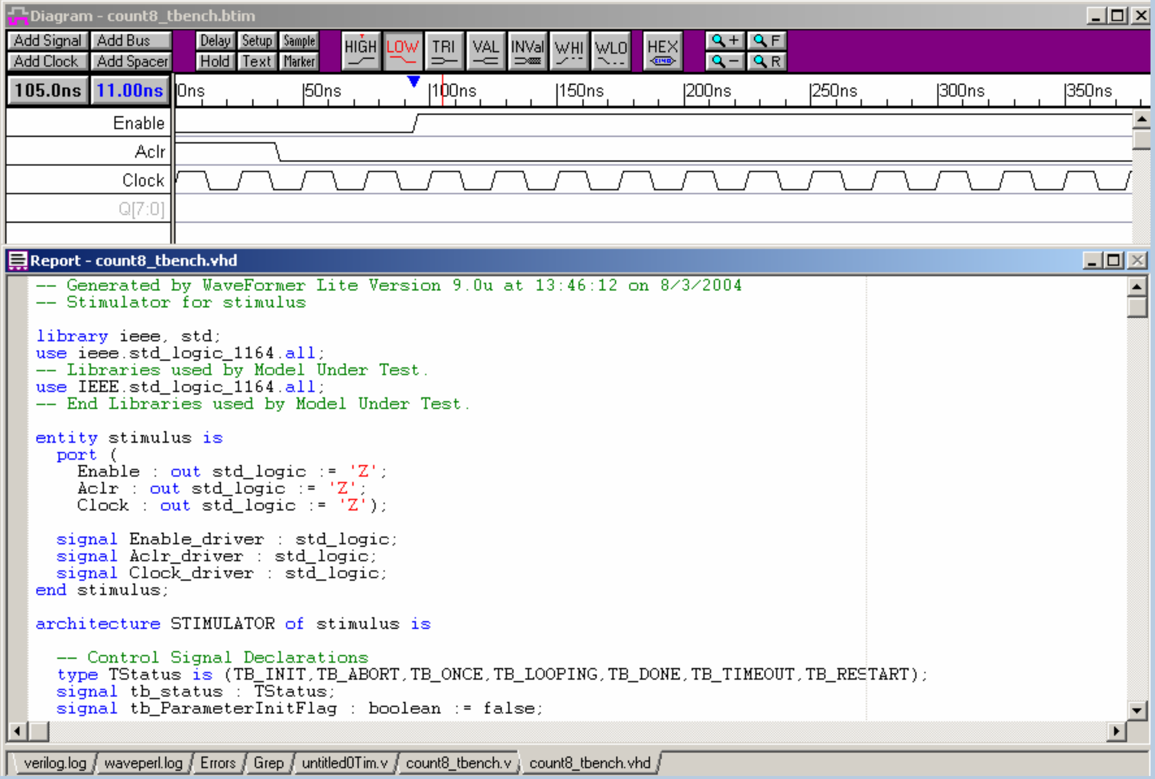
File name: counter_tb.vhd

Save as type: VHDL Wait with Top Level TestBench (*.vhd)s

Export the current timing diagram to another file format

Simulation Inactive

# Waveform and Testbench



```
-- Generated by WaveFormer Lite Version 9.0u at 13:46:12 on 8/3/2004
-- Stimulator for stimulus

library ieee, std;
use ieee.std_logic_1164.all;
-- Libraries used by Model Under Test.
use IEEE.std_logic_1164.all;
-- End Libraries used by Model Under Test.

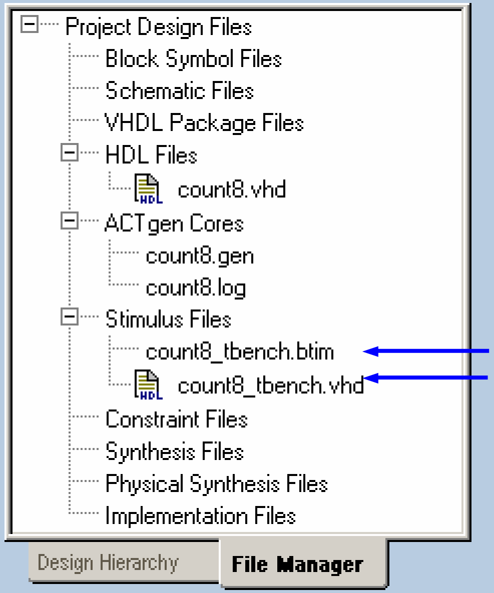
entity stimulus is
  port (
    Enable : out std_logic := 'Z';
    Aclr : out std_logic := 'Z';
    Clock : out std_logic := 'Z');

  signal Enable_driver : std_logic;
  signal Aclr_driver : std_logic;
  signal Clock_driver : std_logic;
end stimulus;

architecture STIMULATOR of stimulus is

  -- Control Signal Declarations
  type TStatus is (TB_INIT,TB_ABORT,TB_ONCE,TB_LOOPING,TB_DONE,TB_TIMEOUT,TB_RESTART);
  signal tb_status : TStatus;
  signal tb_ParameterInitFlag : boolean := false;
```

Stimulus and testbench appear on File Manager tab in Libero



- Project Design Files
  - Block Symbol Files
  - Schematic Files
  - VHDL Package Files
  - HDL Files
    - count8.vhd
  - ACTgen Cores
    - count8.gen
    - count8.log
  - Stimulus Files
    - count8_tbench.btim
    - count8_tbench.vhd
  - Constraint Files
  - Synthesis Files
  - Physical Synthesis Files
  - Implementation Files

stimulus

testbench

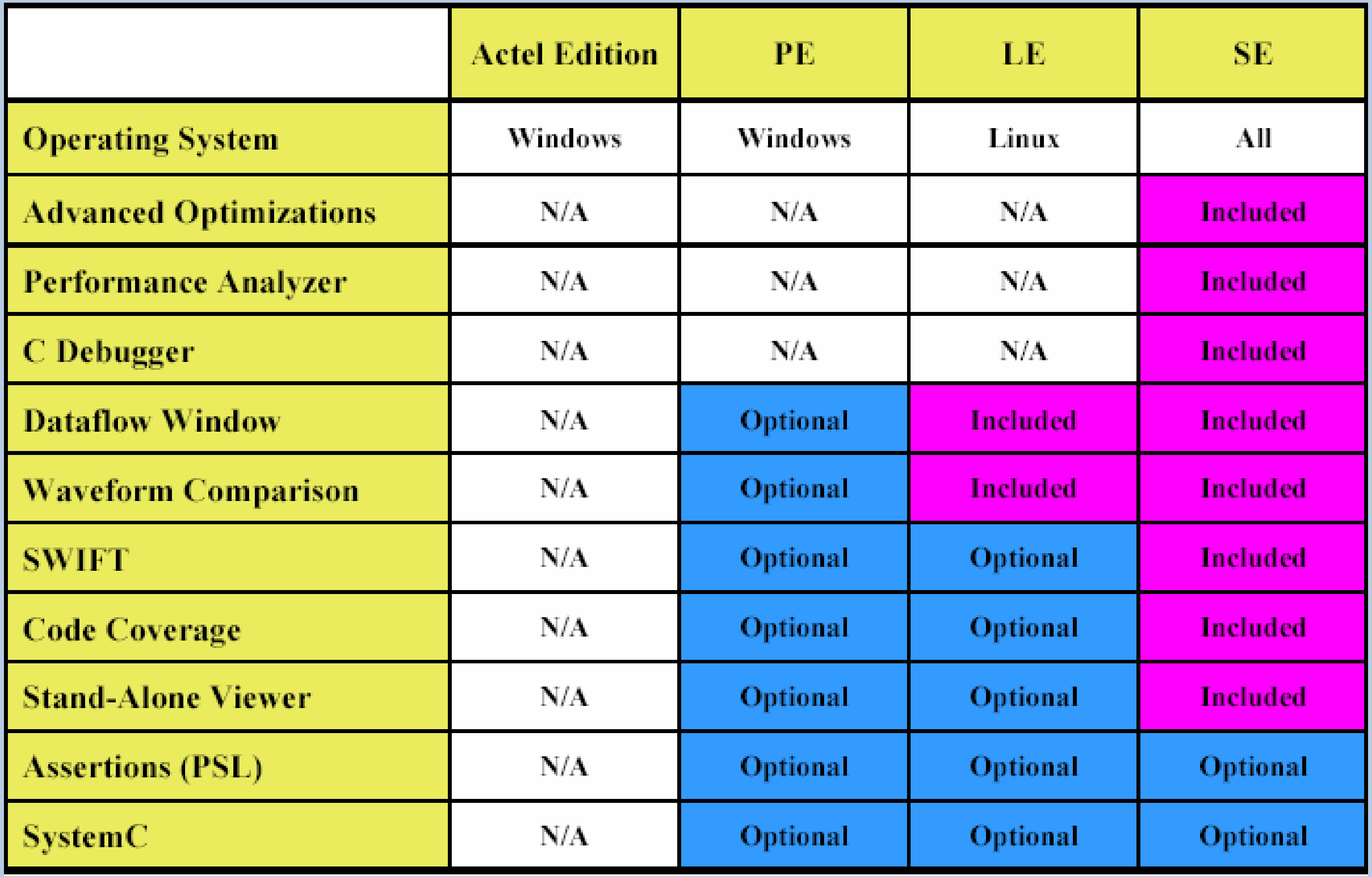
# ModelSim AE

Mentor Graphics®

Model Technology
A MENTOR GRAPHICS COMPANY

ONE CHIP is all you need

# ModelSim AE, PE, LE, & SE

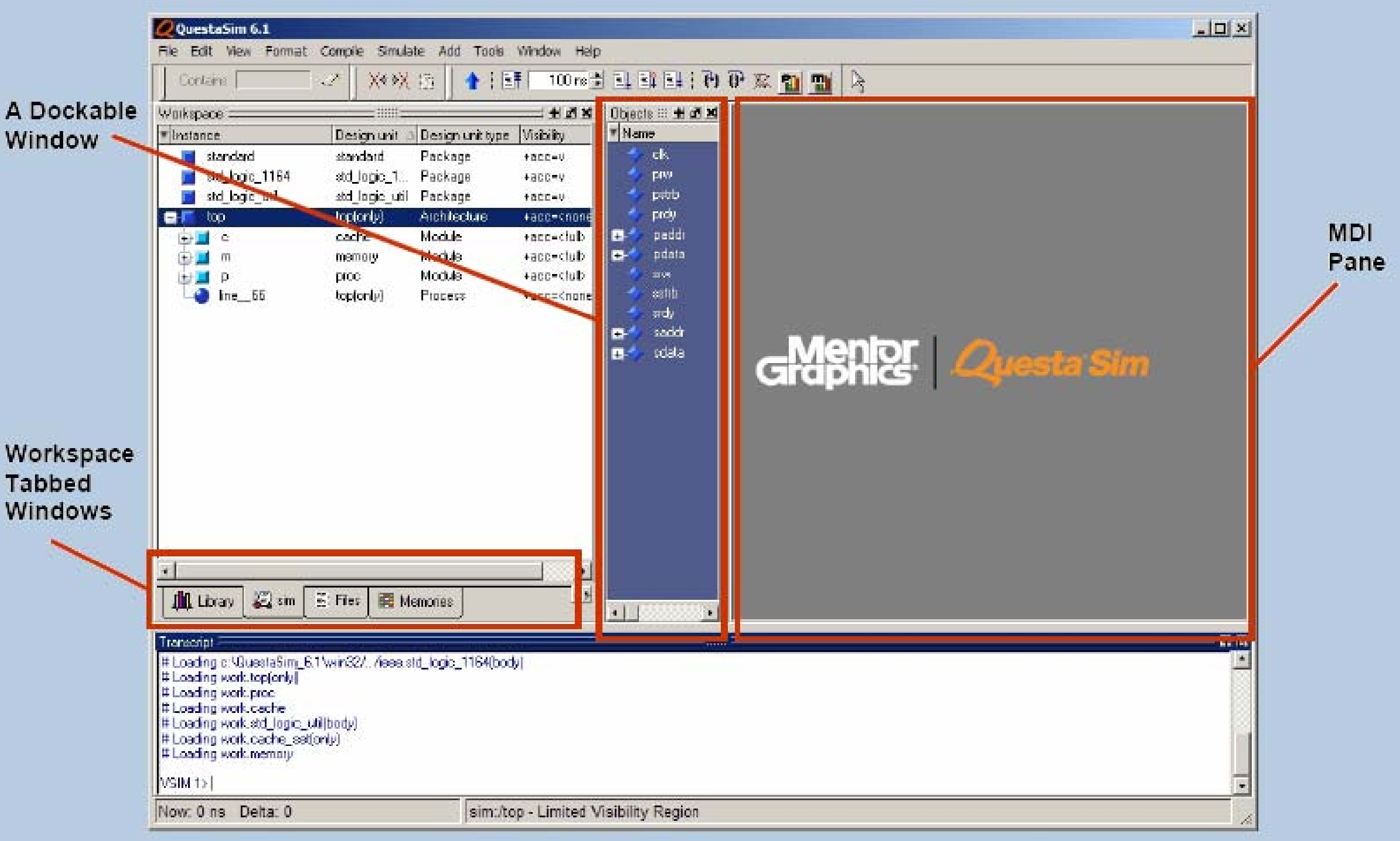


| | Actel Edition | PE | LE | SE |
|---|---|---|---|---|
| Operating System | Windows | Windows | Linux | All |
| Advanced Optimizations | N/A | N/A | N/A | Included |
| Performance Analyzer | N/A | N/A | N/A | Included |
| C Debugger | N/A | N/A | N/A | Included |
| Dataflow Window | N/A | Optional | Included | Included |
| Waveform Comparison | N/A | Optional | Included | Included |
| SWIFT | N/A | Optional | Optional | Included |
| Code Coverage | N/A | Optional | Optional | Included |
| Stand-Alone Viewer | N/A | Optional | Optional | Included |
| Assertions (PSL) | N/A | Optional | Optional | Optional |
| SystemC | N/A | Optional | Optional | Optional |

# ModelSim AE

- Same Functionality as ModelSim PE
  - **Win NT, Win 2000 or Win XP**
    - **Node-Locked**
  - **VHDL or Verilog**
- Reduced Performance
- No Co-simulation (VHDL *and* Verilog) Capability
- Limited to Simulation of  Actel's Gate-level Libraries
- Supported through Actel

# ModelSim Default Window Layout



A Dockable Window

Workspace Tabbed Windows

MDI Pane

| Instance | Design unit | Design unit type | Visibility |
|---|---|---|---|
| standard | standard | Package | +acc=v |
| std_logic_1164 | std_logic_1... | Package | +acc=v |
| std_logic_util | std_logic_util | Package | +acc=v |
| top | top(only) | Architecture | +acc=<none |
| c | cache | Module | +acc=<full |
| m | memory | Module | +acc=<full |
| p | proc | Module | +acc=<full |
| line__66 | top(only) | Process | +acc=<none |

clk
prw
pstrb
prdy
paddr
pdata
srw
sstrb
srdy
saddr
sdata

```
# Loading c:\QuestaSim_6.1\win32/../ieee.std_logic_1164(body)
# Loading work.top(only)
# Loading work.proc
# Loading work.cache
# Loading work.std_logic_util(body)
# Loading work.cache_sst(only)
# Loading work.memory

VSIM 1> |
```

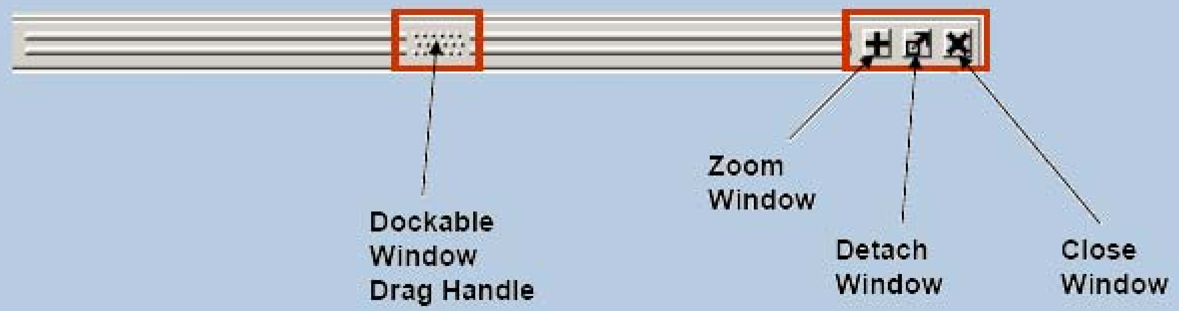
Now: 0 ns    Delta: 0

sim:/top - Limited Visibility Region

# ModelSim Dockable Windows

## Windows Within The Main Window Are Dockable

- **Move The "Drag Handle" To The Desired Location**



## Additional Window Features

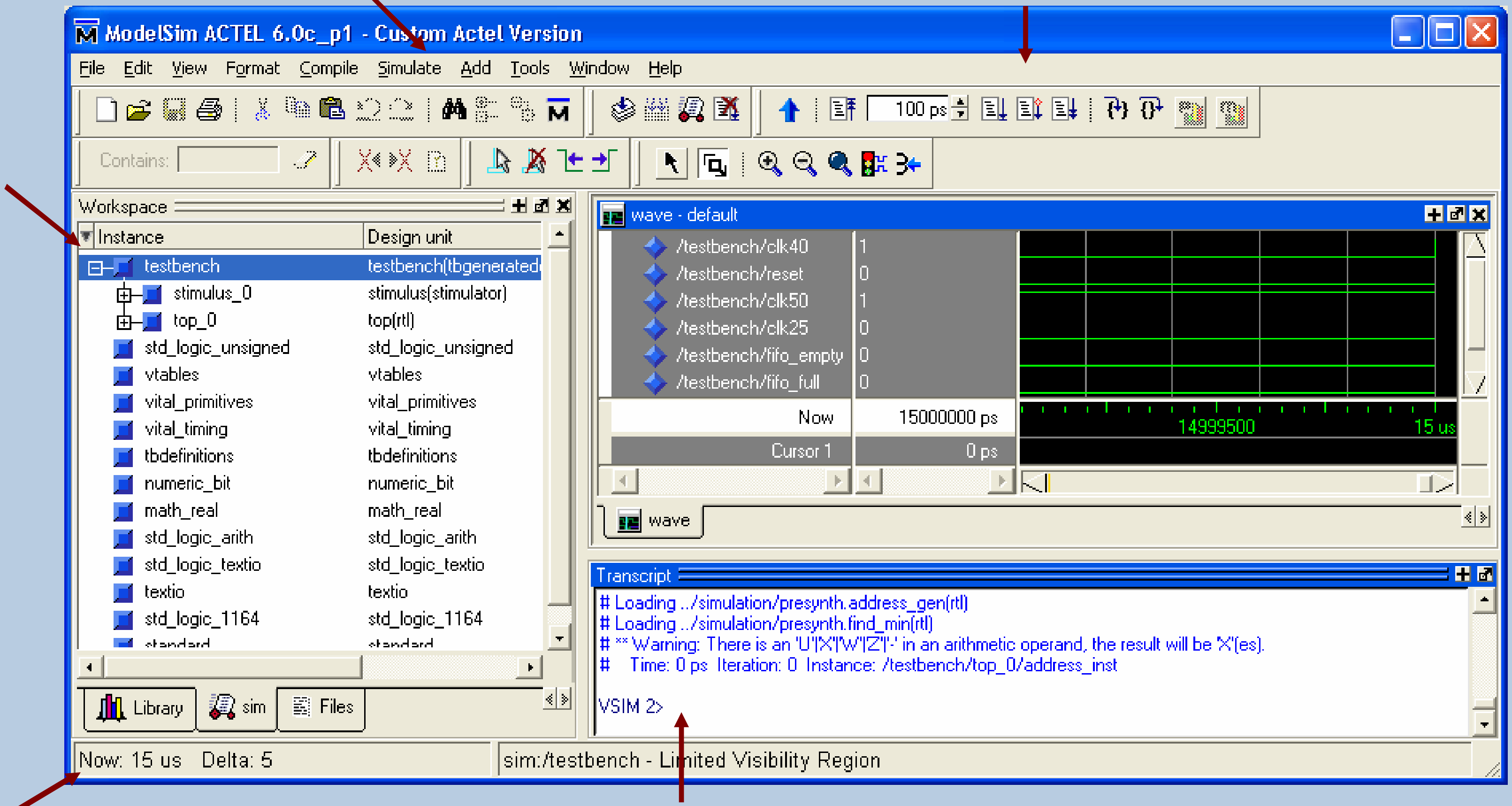
- **Drag & Drop**
  - **HDL Items Can Be Dragged from Dataflow, List, Signals, Source, Structure, Variables, and Wave Windows …**
  - **… And Dropped into either List or Wave Window**
- **Automatic Window Updating**

# ModelSim Main Window

**Menu Bar**

**Tool Bar** ***(Break, Run, Cont, Step,*** **and** ***Step Over)***

**Design Hierarchy**



ModelSim ACTEL 6.0c_p1 - Custom Actel Version
File Edit View Format Compile Simulate Add Tools Window Help
100 ps
Contains:
Workspace
wave - default
Library
sim
Files
wave
Transcript

| Instance | Design unit |
|---|---|
| testbench | testbench(tbgenerated |
| stimulus_0 | stimulus(stimulator) |
| top_0 | top(rtl) |
| std_logic_unsigned | std_logic_unsigned |
| vtables | vtables |
| vital_primitives | vital_primitives |
| vital_timing | vital_timing |
| tbdefinitions | tbdefinitions |
| numeric_bit | numeric_bit |
| math_real | math_real |
| std_logic_arith | std_logic_arith |
| std_logic_textio | std_logic_textio |
| textio | textio |
| std_logic_1164 | std_logic_1164 |
| standard | standard |

| | |
|---|---|
| /testbench/clk40 | 1 |
| /testbench/reset | 0 |
| /testbench/clk50 | 1 |
| /testbench/clk25 | 0 |
| /testbench/fifo_empty | 0 |
| /testbench/fifo_full | 0 |
| Now | 15000000 ps |
| Cursor 1 | 0 ps |

```
# Loading ../simulation/presynth.address_gen(rtl)
# Loading ../simulation/presynth.find_min(rtl)
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ps  Iteration: 0  Instance: /testbench/top_0/address_inst

VSIM 2>
```

Now: 15 us   Delta: 5   sim:/testbench - Limited Visibility Region

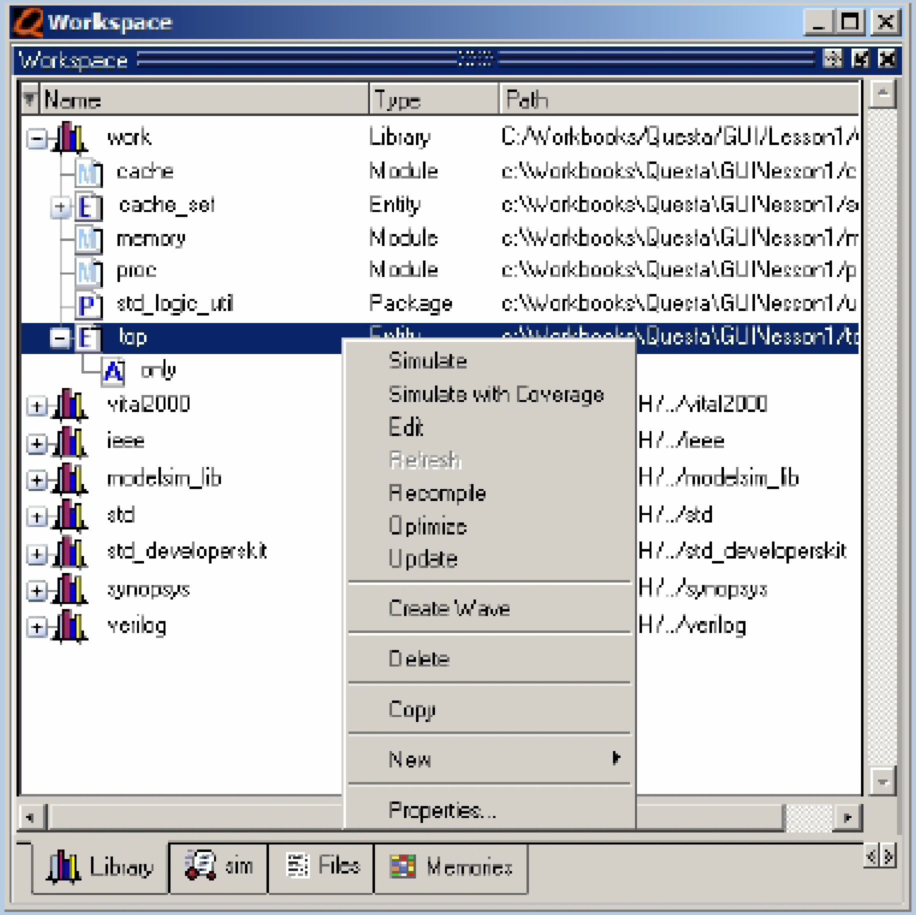
**Status Bar** ***(current time, delta time step, environment)***

## TCL Interpreter

**ModelSim>** prompt before design is loaded.
**VSIM>** prompt is displayed after design is loaded

# Workspace Window

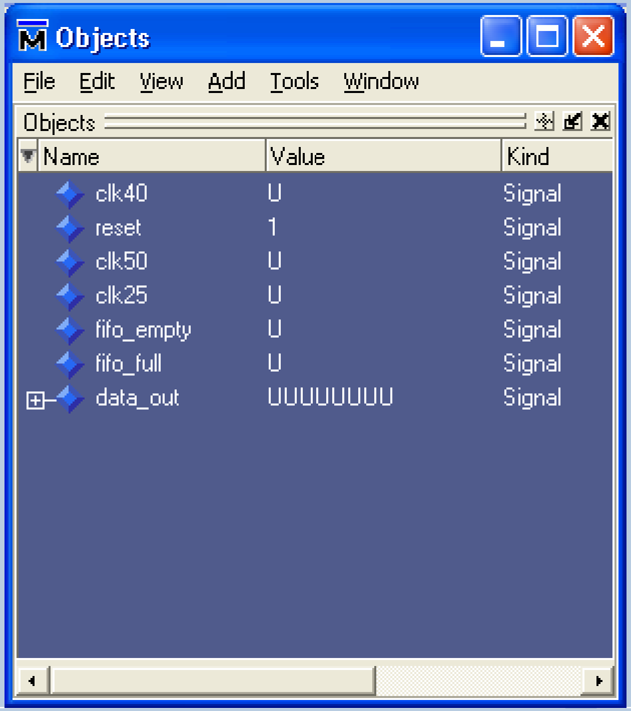
- Workspace provides access to:
  - **Libraries**
  - **Compiled Design Units**
  - **Design Source Files**
  - **Memory Modules**



| Name | Type | Path |
|---|---|---|
| work | Library | C:/Workbooks/Questa/GUI/Lesson1/ |
| cache | Module | c:\Workbooks\Questa\GUI\lesson1/c |
| cache_set | Entity | c:\Workbooks\Questa\GUI\lesson1/s |
| memory | Module | c:\Workbooks\Questa\GUI\lesson1/m |
| proc | Module | c:\Workbooks\Questa\GUI\lesson1/p |
| std_logic_util | Package | c:\Workbooks\Questa\GUI\lesson1/u |
| top | Entity | c:\Workbooks\Questa\GUI\lesson1/t |
| only | | |
| vital2000 | | H/../vital2000 |
| ieee | | H/../ieee |
| modelsim_lib | | H/../modelsim_lib |
| std | | H/../std |
| std_developerskit | | H/../std_developerskit |
| synopsys | | H/../synopsys |
| verilog | | H/../verilog |

# Objects Window

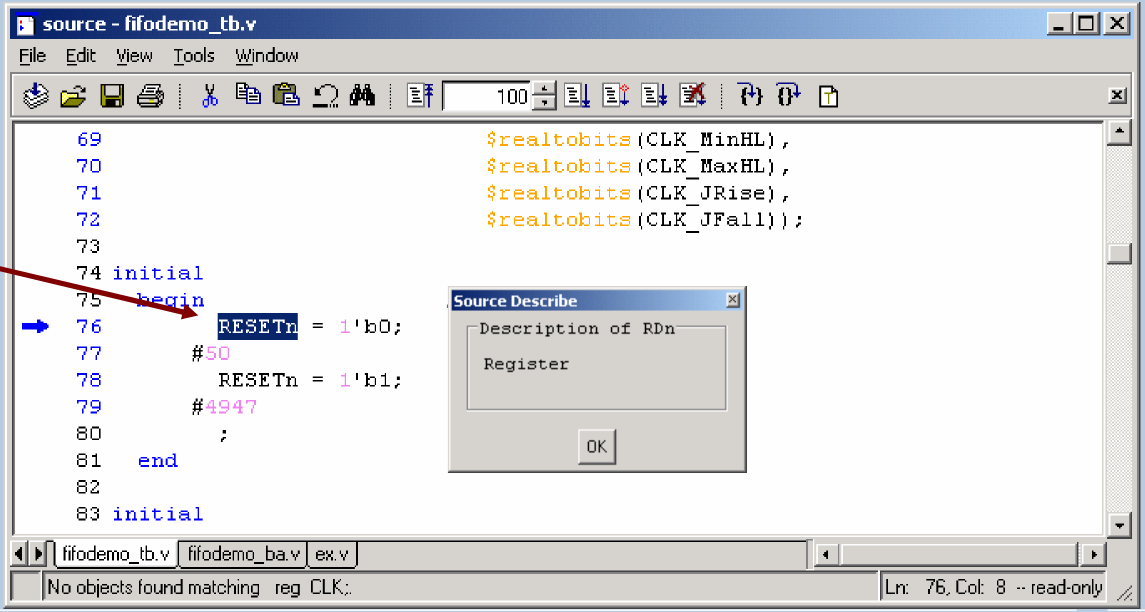
- Shows Names and Values of HDL Items in Current Region Selected in the Workspace
  - **Objects include signals, nets, registers, constants and variables not declared in a process, generics and parameters**
- Items Can Be Sorted in Ascending, Descending or Declaration Order
- Hierarchy (+) Expandable
  - **VHDL Items - Signals**
  - **Verilog Items - Nets, Register Variables**
  - **Named Events**
- "Drag & Drop"
  - **Wave & List windows**
    - **Force Apply Stimulus**
    - **Filter Signal Types (`input,output` etc)**
    - **Find HDL Items**



| Name | Value | Kind |
|---|---|---|
| clk40 | U | Signal |
| reset | 1 | Signal |
| clk50 | U | Signal |
| clk25 | U | Signal |
| fifo_empty | U | Signal |
| fifo_full | U | Signal |
| ⊞ data_out | UUUUUUUU | Signal |

# Source Window

- Can Be Un-docked From The MDI Pane Of The Main Window
  - **Color-coded Comments, Keywords, Strings, Numbers, Executable Lines, Identifiers, System Tasks, Text**
- Full Edit Capability
  - **Save, Compile and Restart**
- Drag and Drop
- Describe
- Examine



```
                                   $realtobits(CLK_MinHL),
                                   $realtobits(CLK_MaxHL),
                                   $realtobits(CLK_JRise),
                                   $realtobits(CLK_JFall));

initial
  begin
    RESETn = 1'b0;
   #50
    RESETn = 1'b1;
   #4947
    ;
  end

initial
```

Source Describe

Description of RDn

Register

OK

No objects found matching  reg CLK;.

Ln:  76, Col:  8 -- read-only

# Wave Window

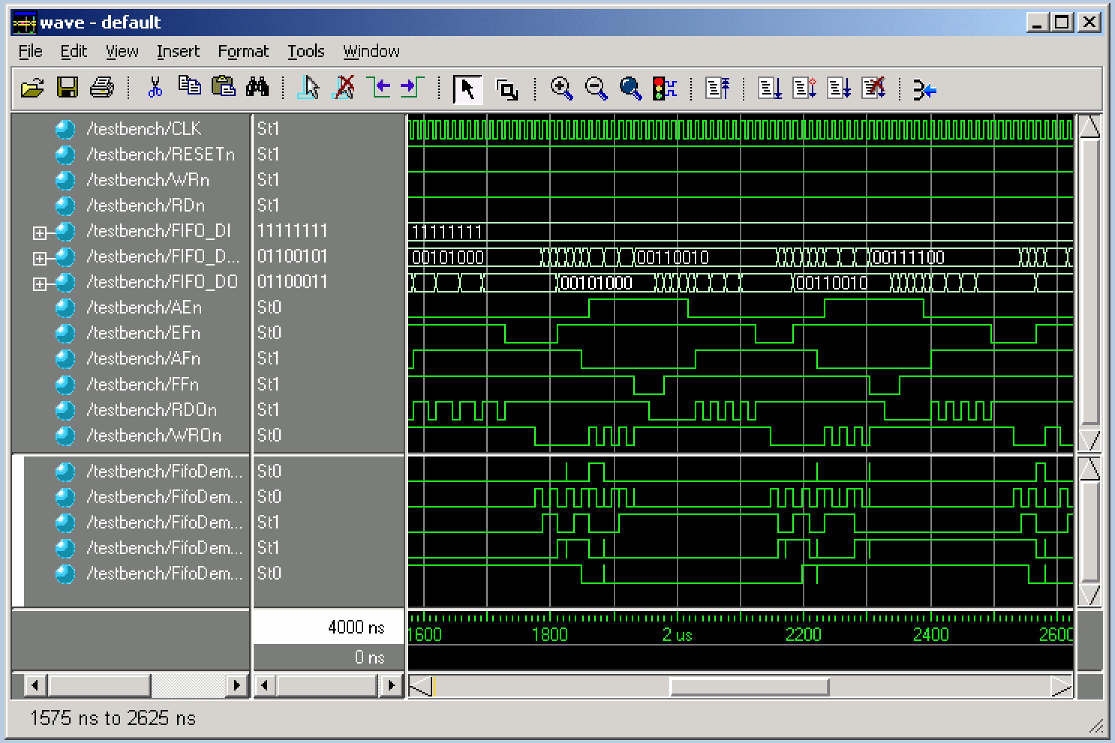
Multiple Cursors

Virtuals

Drag & Drop

Multiple Panes

Zooming



| | |
|---|---|
| /testbench/CLK | St1 |
| /testbench/RESETn | St1 |
| /testbench/WRn | St1 |
| /testbench/RDn | St1 |
| /testbench/FIFO_DI | 11111111 |
| /testbench/FIFO_D... | 01100101 |
| /testbench/FIFO_DO | 01100011 |
| /testbench/AEn | St0 |
| /testbench/EFn | St0 |
| /testbench/AFn | St1 |
| /testbench/FFn | St1 |
| /testbench/RDOn | St1 |
| /testbench/WROn | St0 |
| /testbench/FifoDem... | St0 |
| /testbench/FifoDem... | St0 |
| /testbench/FifoDem... | St1 |
| /testbench/FifoDem... | St1 |
| /testbench/FifoDem... | St0 |
| | 4000 ns |
| | 0 ns |

1575 ns to 2625 ns

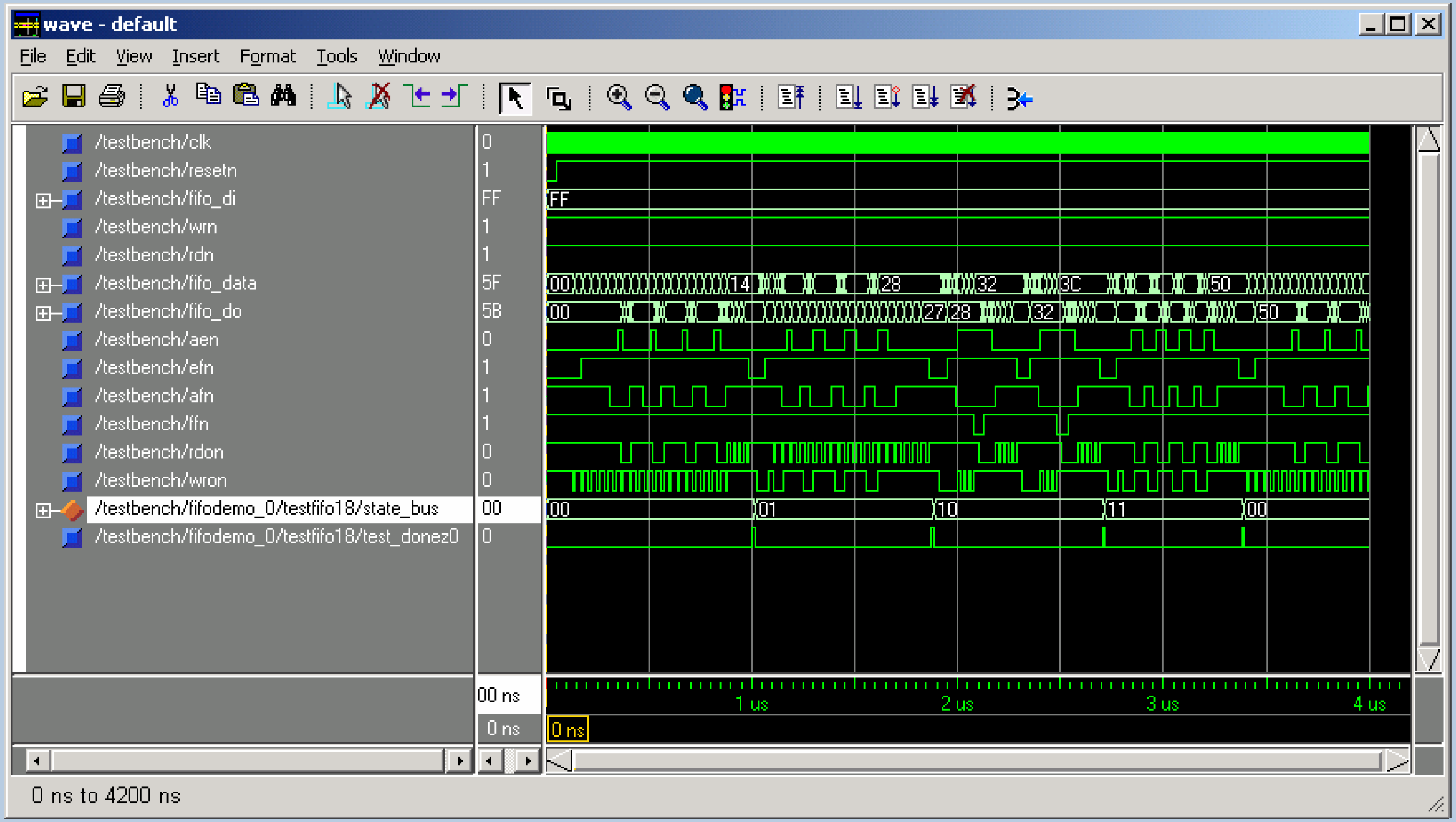
Simulation Control

Item formatting

Cursor Measurements

# Creating Busses in Wave Window

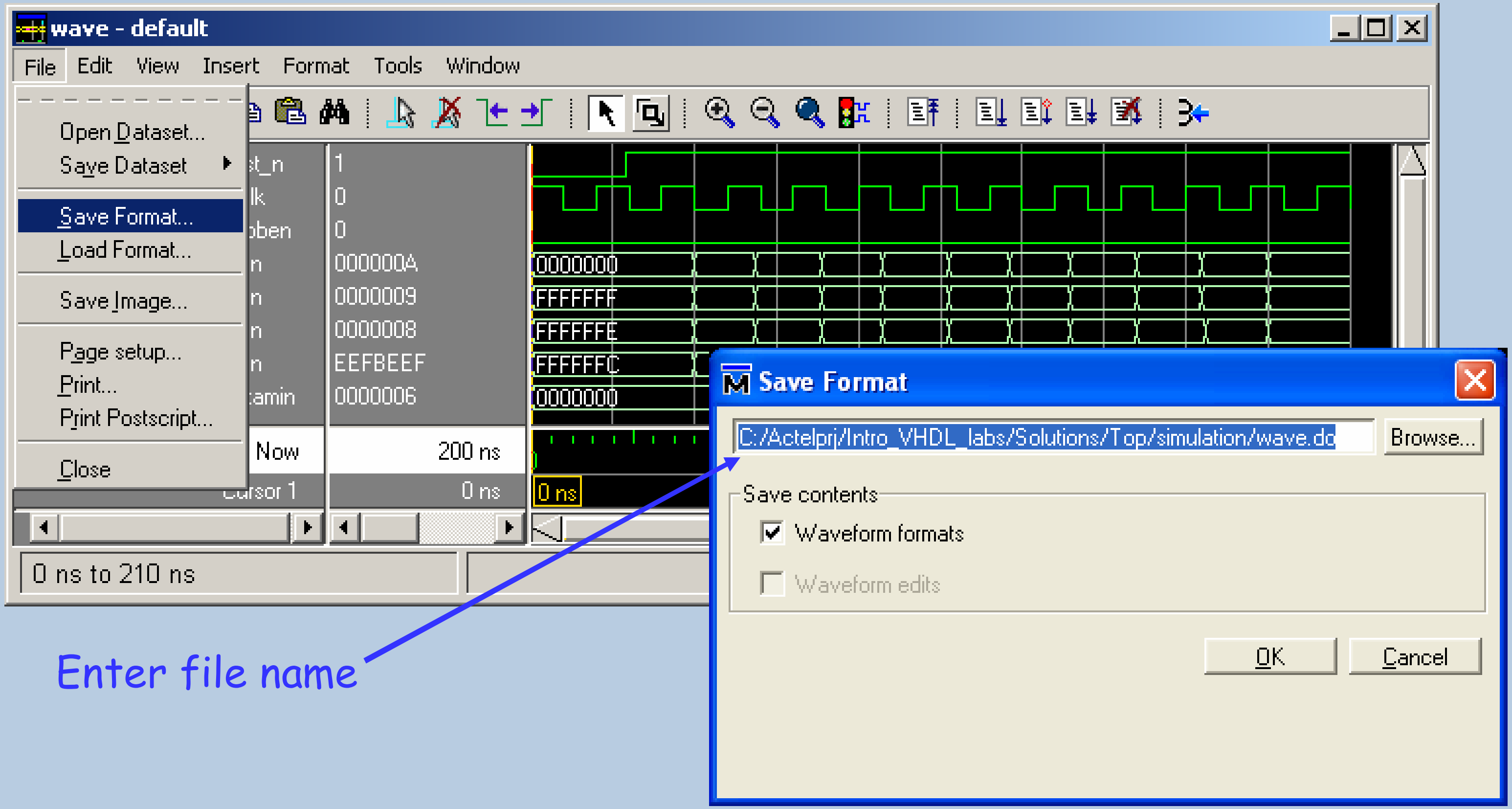
- Scalar Signals Can Be Combined into Vectors



```
/testbench/clk                              0
/testbench/resetn                           1
/testbench/fifo_di                          FF
/testbench/wrn                              1
/testbench/rdn                              1
/testbench/fifo_data                        5F
/testbench/fifo_do                          5B
/testbench/aen                              0
/testbench/efn                              1
/testbench/afn                              1
/testbench/ffn                              1
/testbench/rdon                             0
/testbench/wron                             0
/testbench/fifodemo_0/testfifo18/state_bus  00
/testbench/fifodemo_0/testfifo18/test_donez0 0
                                            00 ns
                                            0 ns
0 ns to 4200 ns
```

# Saving Wave Data

- Signals Added to Wave Window Can Be Saved for Future Simulation Runs
  - ***File > Save from Wave Window***



C:/Actelprj/Intro_VHDL_labs/Solutions/Top/simulation/wave.do

Save contents

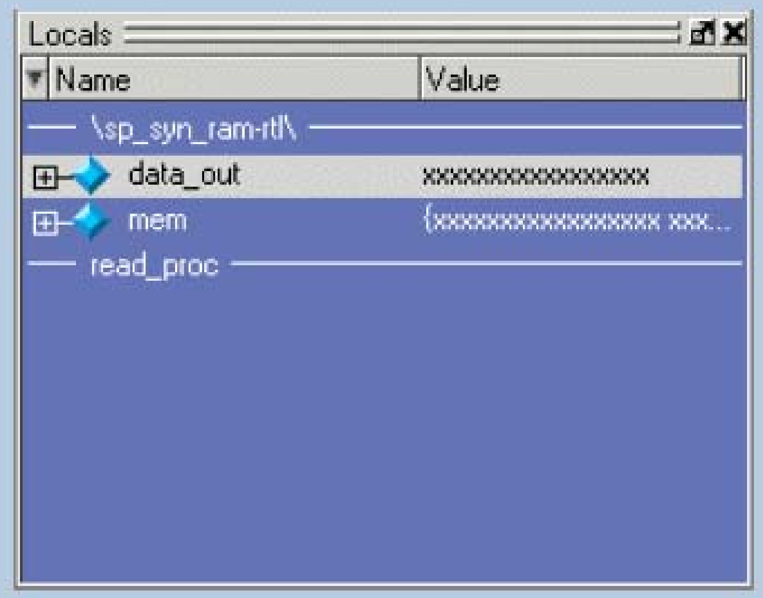
☑ Waveform formats

☐ Waveform edits

Enter file name

# Locals Pane

- Displays Data Objects That Are Immediately Visible From The Statement That Will Be Executed Next
- Contents Of The Window Change From One Statement To The Next



Locals

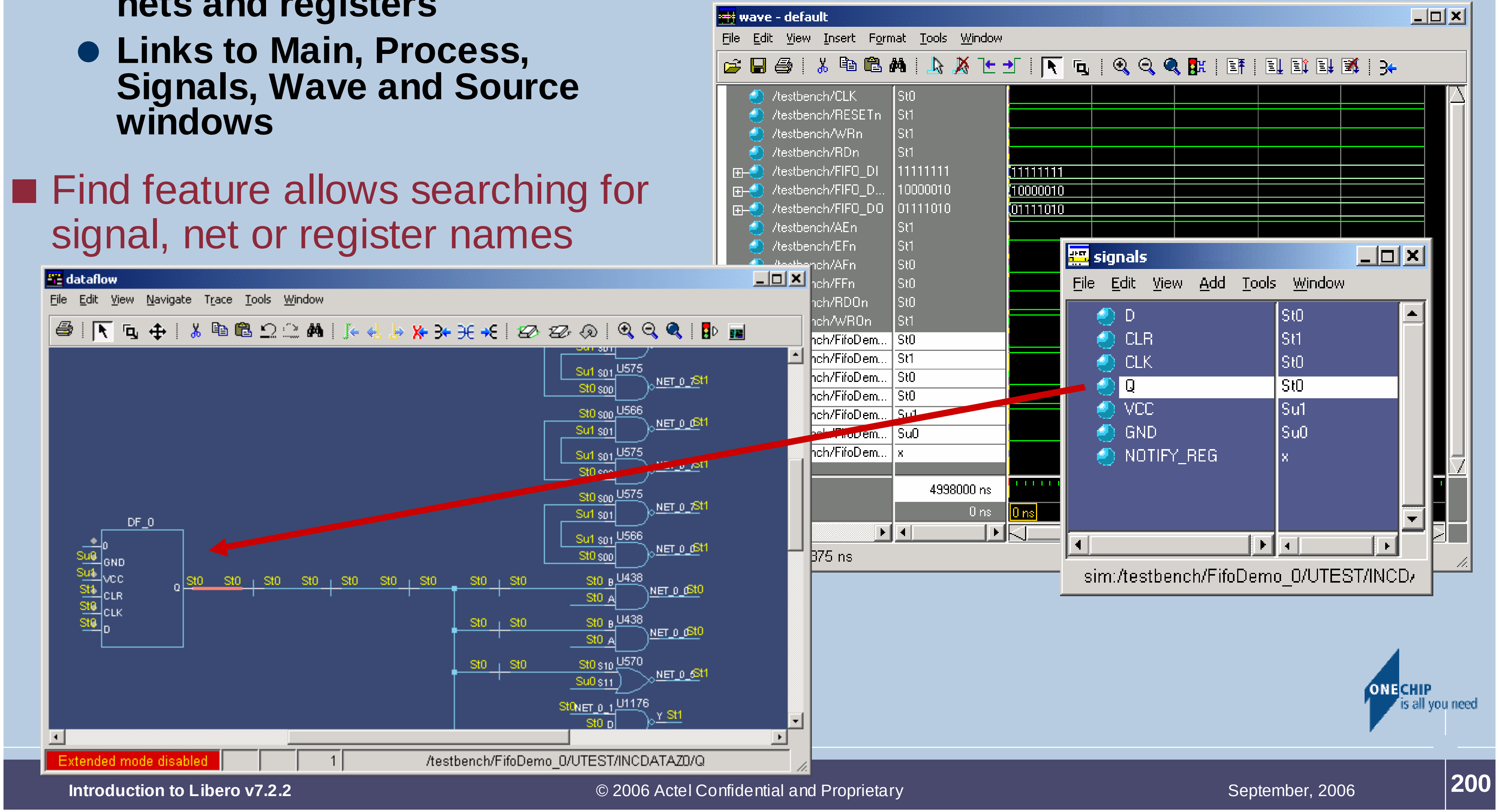
| Name | Value |
|---|---|
| \sp_syn_ram-rtl\ | |
| data_out | xxxxxxxxxxxxxxxxxx |
| mem | {xxxxxxxxxxxxxxxxxx xxx... |
| read_proc | |

# DataFlow Window

Explore physical connectivity of design

- Displays processes, signals, nets and registers
- Links to Main, Process, Signals, Wave and Source windows

- Find feature allows searching for signal, net or register names



wave - default

File Edit View Insert Format Tools Window

| | | |
|---|---|---|
| /testbench/CLK | St0 | |
| /testbench/RESETn | St1 | |
| /testbench/WRn | St1 | |
| /testbench/RDn | St1 | |
| /testbench/FIFO_DI | 11111111 | 11111111 |
| /testbench/FIFO_D... | 10000010 | 10000010 |
| /testbench/FIFO_DO | 01111010 | 01111010 |
| /testbench/AEn | St1 | |
| /testbench/EFn | St1 | |
| /testbench/AFn | St0 | |
| ...nch/FFn | St0 | |
| ...nch/RDOn | St0 | |
| ...nch/WROn | St1 | |
| ...nch/FifoDem... | St0 | |
| ...nch/FifoDem... | St1 | |
| ...nch/FifoDem... | St0 | |
| ...nch/FifoDem... | St0 | |
| ...nch/FifoDem... | Su1 | |
| ...nch/FifoDem... | Su0 | |
| ...nch/FifoDem... | x | |

4998000 ns

0 ns

...375 ns

signals

File Edit View Add Tools Window

| | |
|---|---|
| D | St0 |
| CLR | St1 |
| CLK | St0 |
| Q | St0 |
| VCC | Su1 |
| GND | Su0 |
| NOTIFY_REG | x |

sim:/testbench/FifoDemo_0/UTEST/INCD/

dataflow

File Edit View Navigate Trace Tools Window

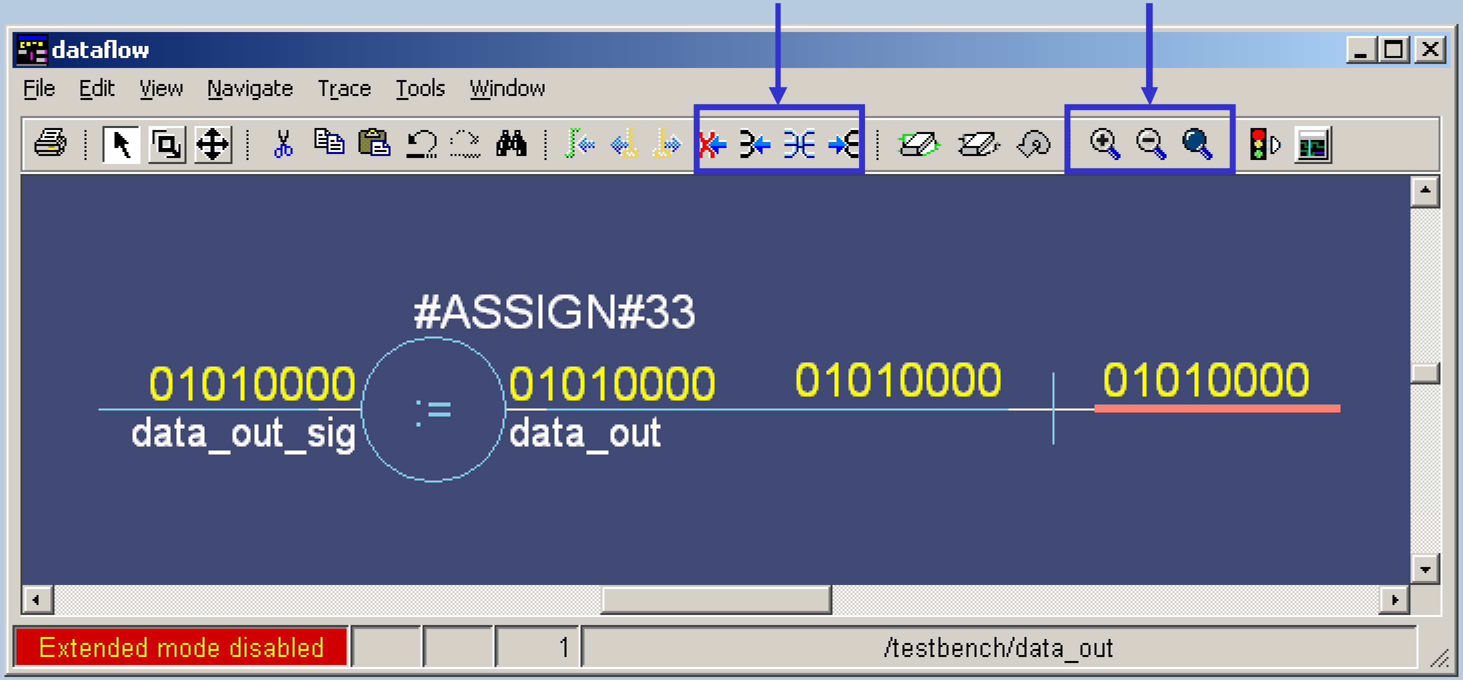
Extended mode disabled | 1 | /testbench/FifoDemo_0/UTEST/INCDATAZ0/Q

# Dataflow Window
## *ModelSim AE Simulator*

- The ModelSim AE simulator has a limited Dataflow functionality
  - Only one process and it’s attached signals or one signal and it’s attached processes are displayed

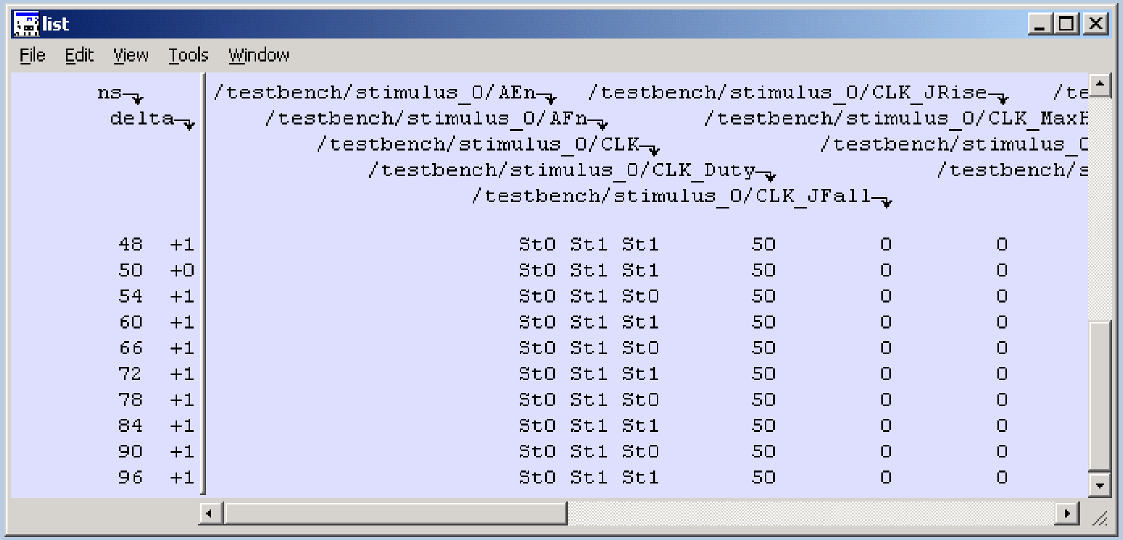
Display net drivers or readers

Zoom control



# List Window

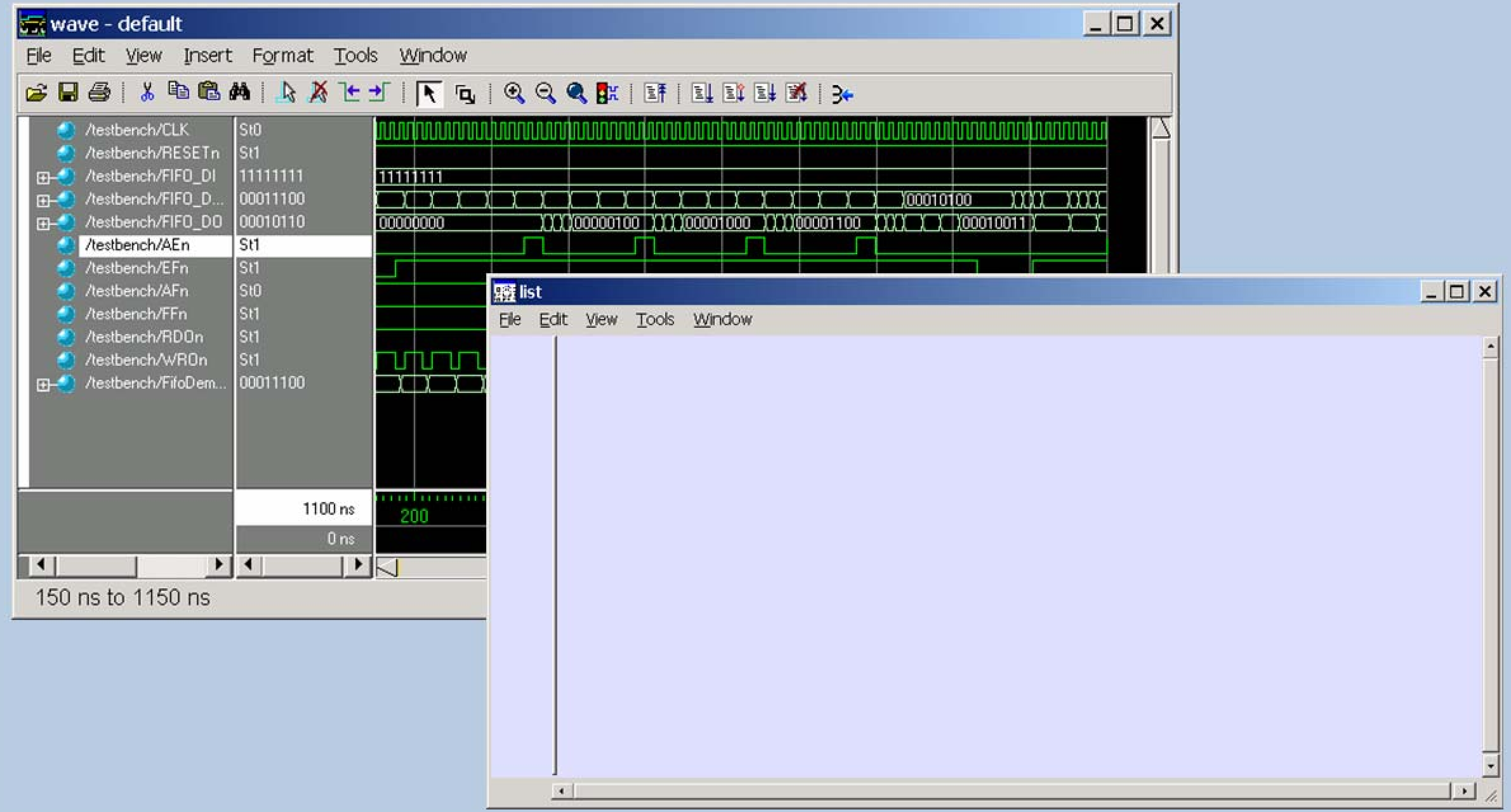
- Simulation Results in Tabular Format
  - **VHDL - Signals and Process Variables**
  - **Verilog - Nets and Registers**
- “Drag & Drop”
- Find Function
- Trigger / Strobe Properties
- Write List
  - **Tabular**
  - **Event**
  - **TSSI**
- Markers - Add, Delete or Goto



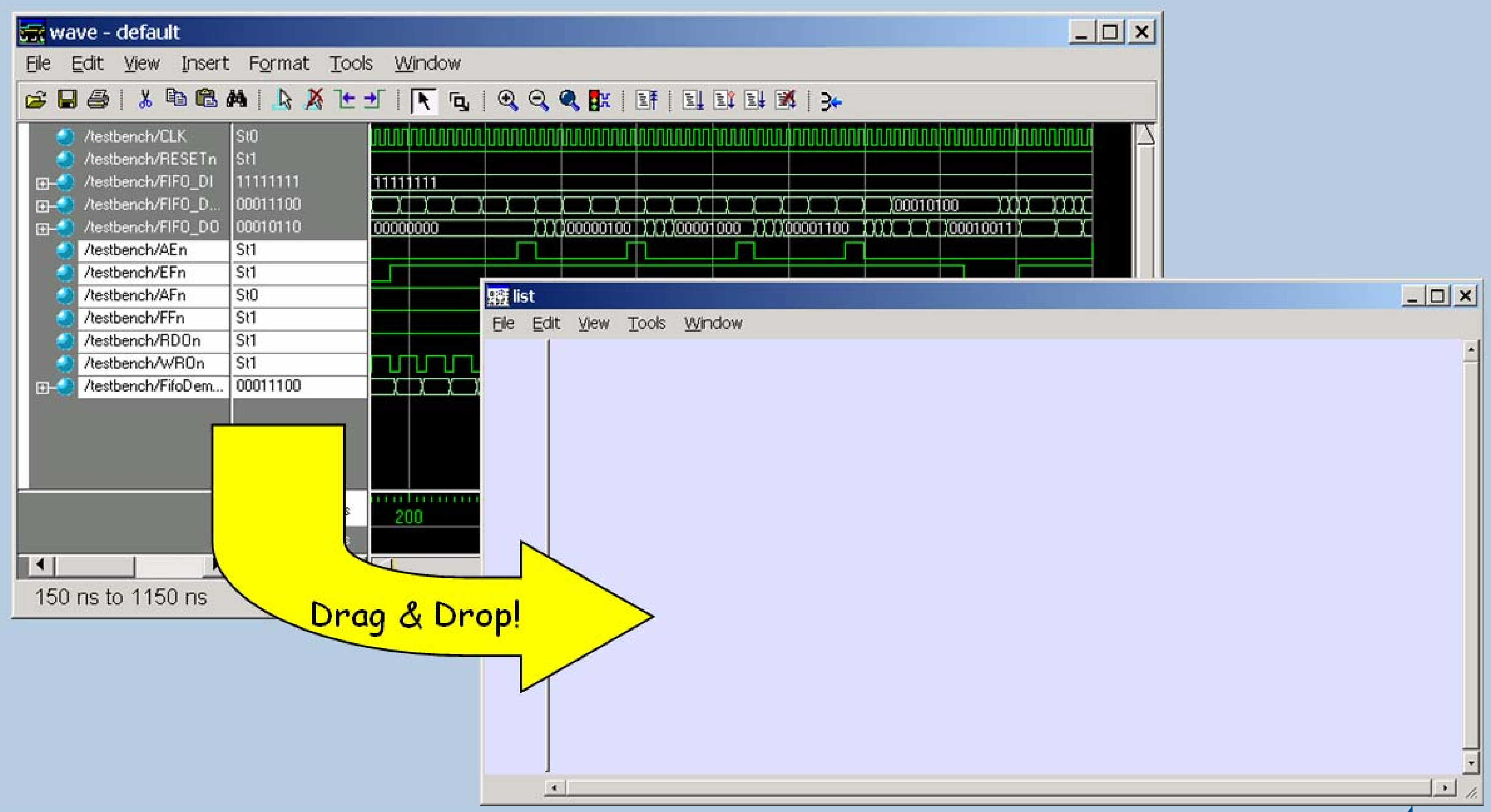
```
      ns    /testbench/stimulus_0/AEn    /testbench/stimulus_0/CLK_JRise    /te
   delta        /testbench/stimulus_0/AFn        /testbench/stimulus_0/CLK_MaxF
                    /testbench/stimulus_0/CLK            /testbench/stimulus_C
                        /testbench/stimulus_0/CLK_Duty           /testbench/s
                                /testbench/stimulus_0/CLK_JFall

      48  +1                        St0 St1 St1      50        0         0
      50  +0                        St0 St1 St1      50        0         0
      54  +1                        St0 St1 St0      50        0         0
      60  +1                        St0 St1 St1      50        0         0
      66  +1                        St0 St1 St0      50        0         0
      72  +1                        St0 St1 St1      50        0         0
      78  +1                        St0 St1 St0      50        0         0
      84  +1                        St0 St1 St1      50        0         0
      90  +1                        St0 St1 St0      50        0         0
      96  +1                        St0 St1 St1      50        0         0
```

# Saving Tabular Output



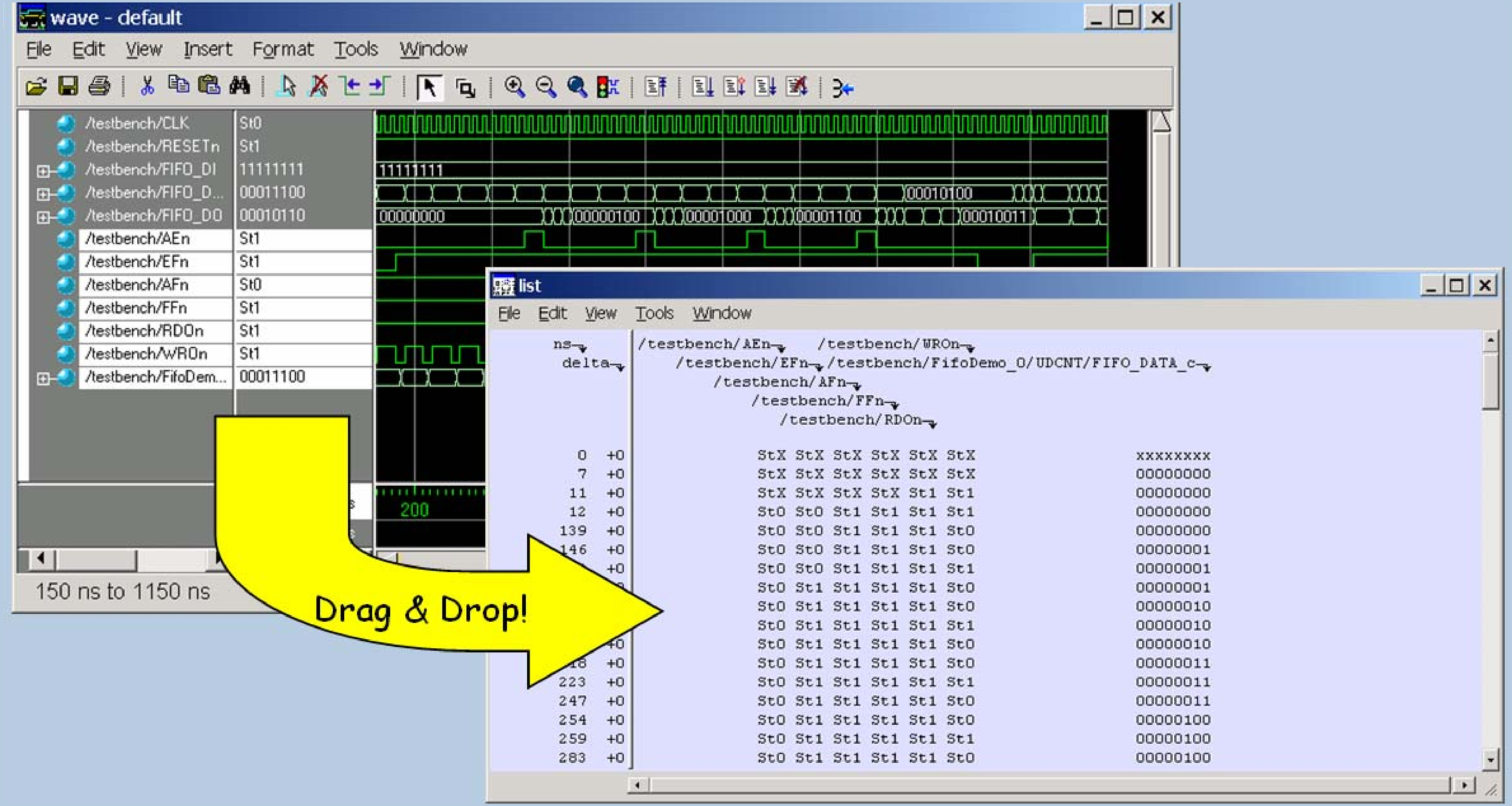
# Saving Tabular Output



| | |
|---|---|
| /testbench/CLK | St0 |
| /testbench/RESETn | St1 |
| /testbench/FIFO_DI | 11111111 |
| /testbench/FIFO_D... | 00011100 |
| /testbench/FIFO_DO | 00010110 |
| /testbench/AEn | St1 |
| /testbench/EFn | St1 |
| /testbench/AFn | St0 |
| /testbench/FFn | St1 |
| /testbench/RDOn | St1 |
| /testbench/WROn | St1 |
| /testbench/FifoDem... | 00011100 |

150 ns to 1150 ns

# Saving Tabular Output



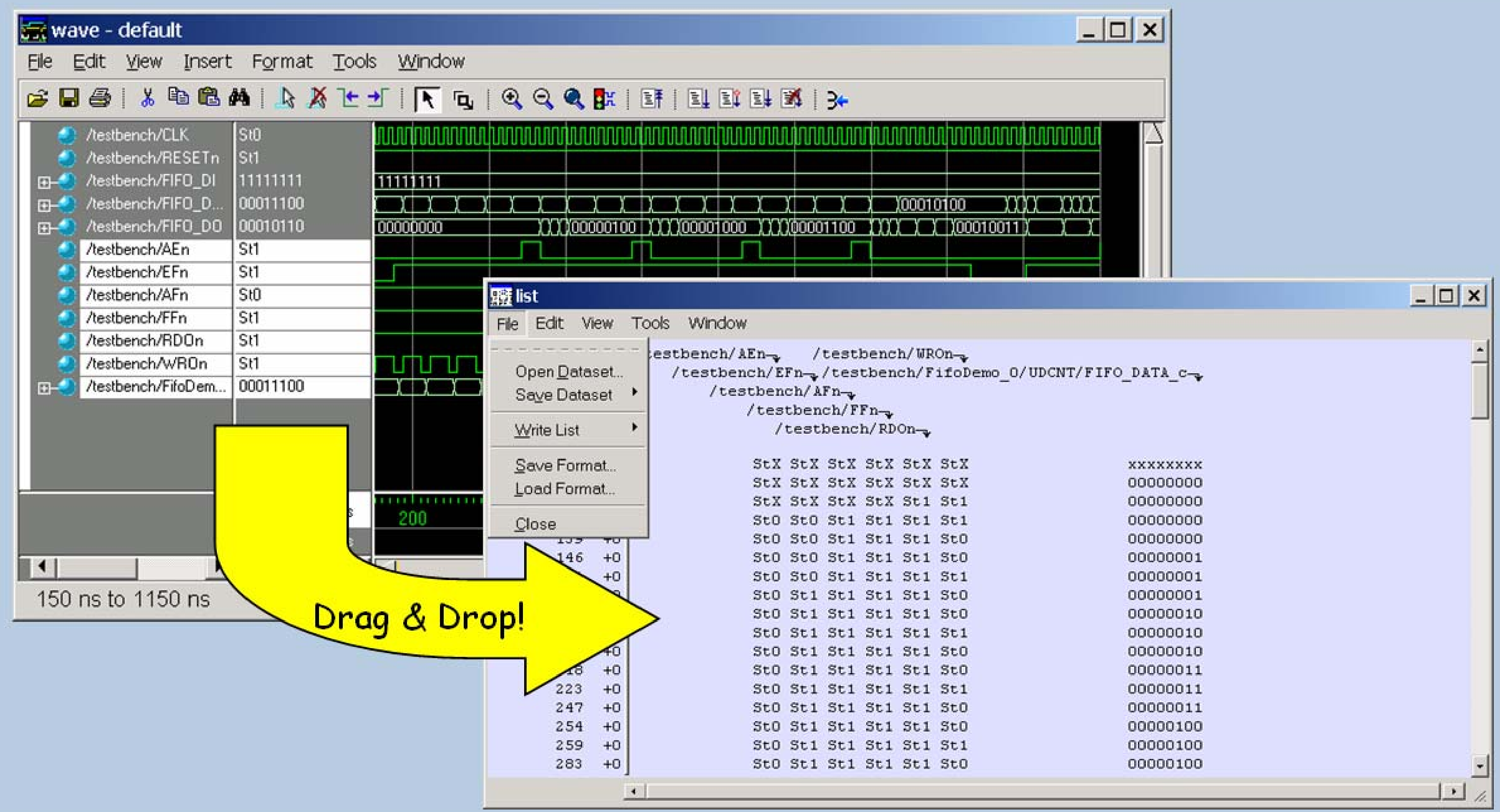
wave - default
File Edit View Insert Format Tools Window
list
File Edit View Tools Window
Drag & Drop!
150 ns to 1150 ns
200

| | |
|---|---|
| /testbench/CLK | St0 |
| /testbench/RESETn | St1 |
| /testbench/FIFO_DI | 11111111 |
| /testbench/FIFO_D... | 00011100 |
| /testbench/FIFO_DO | 00010110 |
| /testbench/AEn | St1 |
| /testbench/EFn | St1 |
| /testbench/AFn | St0 |
| /testbench/FFn | St1 |
| /testbench/RDOn | St1 |
| /testbench/WROn | St1 |
| /testbench/FifoDem... | 00011100 |

```
       ns     /testbench/AEn      /testbench/WROn
    delta          /testbench/EFn /testbench/FifoDemo_0/UDCNT/FIFO_DATA_c
                        /testbench/AFn
                             /testbench/FFn
                                 /testbench/RDOn

        0  +0           StX StX StX StX StX StX           xxxxxxxx
        7  +0           StX StX StX StX StX StX           00000000
       11  +0           StX StX StX StX St1 St1           00000000
       12  +0           St0 St0 St1 St1 St1 St1           00000000
      139  +0           St0 St0 St1 St1 St1 St0           00000000
      146  +0           St0 St0 St1 St1 St1 St0           00000001
           +0           St0 St0 St1 St1 St1 St1           00000001
                        St0 St1 St1 St1 St1 St0           00000001
                        St0 St1 St1 St1 St1 St0           00000010
                        St0 St1 St1 St1 St1 St1           00000010
           +0           St0 St1 St1 St1 St1 St0           00000010
       18  +0           St0 St1 St1 St1 St1 St0           00000011
      223  +0           St0 St1 St1 St1 St1 St1           00000011
      247  +0           St0 St1 St1 St1 St1 St0           00000011
      254  +0           St0 St1 St1 St1 St1 St0           00000100
      259  +0           St0 St1 St1 St1 St1 St1           00000100
      283  +0           St0 St1 St1 St1 St1 St0           00000100
```

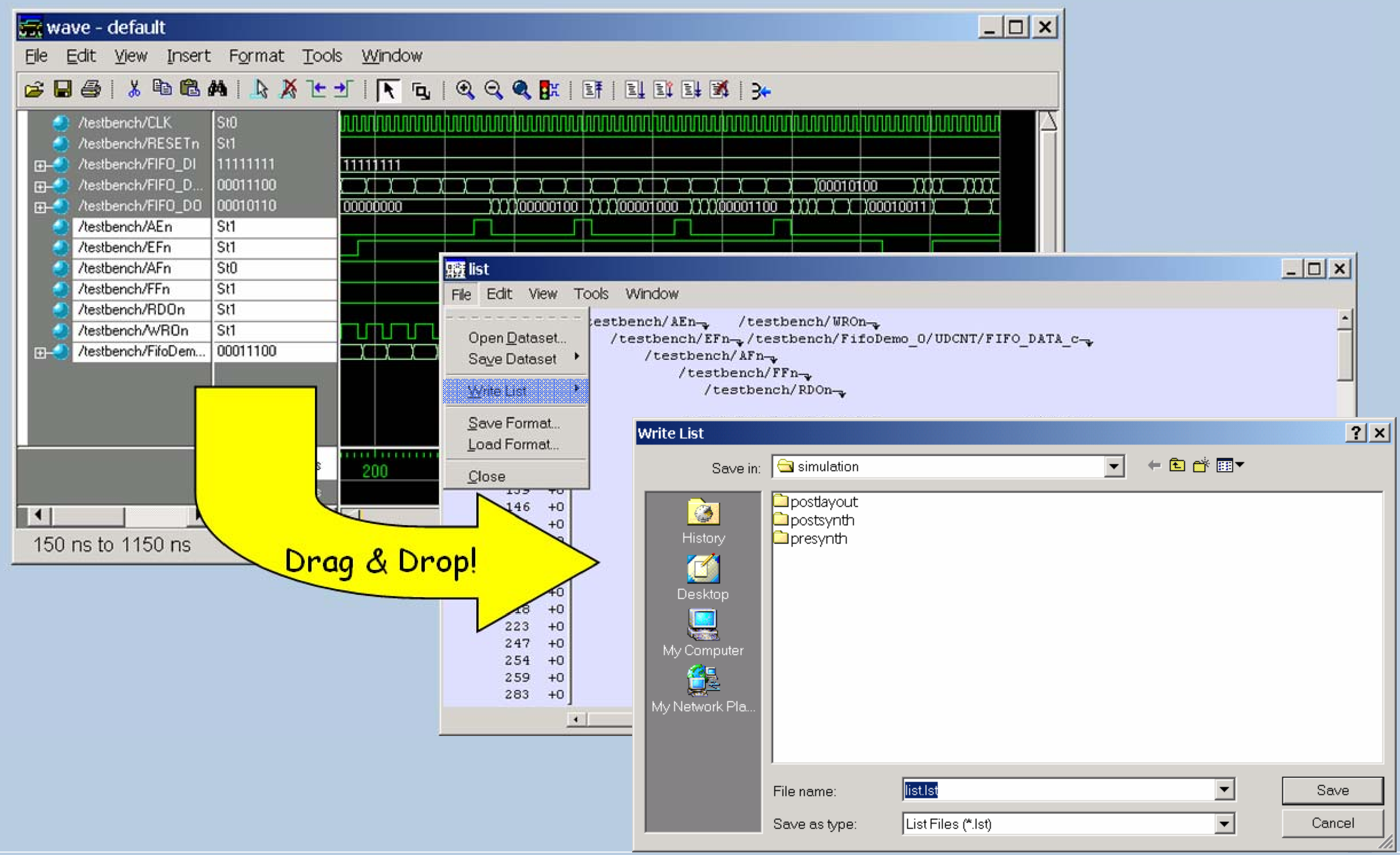
# Saving Tabular Output



```
/testbench/CLK        St0
/testbench/RESETn     St1
/testbench/FIFO_DI    11111111
/testbench/FIFO_D...  00011100
/testbench/FIFO_DO    00010110
/testbench/AEn        St1
/testbench/EFn        St1
/testbench/AFn        St0
/testbench/FFn        St1
/testbench/RDOn       St1
/testbench/WROn       St1
/testbench/FifoDem... 00011100
```

```
estbench/AEn    /testbench/WROn
   /testbench/EFn /testbench/FifoDemo_0/UDCNT/FIFO_DATA_c
        /testbench/AFn
            /testbench/FFn
               /testbench/RDOn

                 StX StX StX StX StX StX          xxxxxxxx
                 StX StX StX StX StX StX          00000000
                 StX StX StX StX St1 St1          00000000
                 St0 St0 St1 St1 St1 St1          00000000
                 St0 St0 St1 St1 St1 St0          00000000
 146   +0        St0 St0 St1 St1 St1 St0          00000001
       +0        St0 St0 St1 St1 St1 St1          00000001
                 St0 St1 St1 St1 St1 St0          00000001
                 St0 St1 St1 St1 St1 St0          00000010
                 St0 St1 St1 St1 St1 St1          00000010
       +0        St0 St1 St1 St1 St1 St0          00000010
       +0        St0 St1 St1 St1 St1 St0          00000011
 223   +0        St0 St1 St1 St1 St1 St1          00000011
 247   +0        St0 St1 St1 St1 St1 St0          00000011
 254   +0        St0 St1 St1 St1 St1 St0          00000100
 259   +0        St0 St1 St1 St1 St1 St1          00000100
 283   +0        St0 St1 St1 St1 St1 St0          00000100
```



Drag & Drop!

| | |
|---|---|
| /testbench/CLK | St0 |
| /testbench/RESETn | St1 |
| /testbench/FIFO_DI | 11111111 |
| /testbench/FIFO_D... | 00011100 |
| /testbench/FIFO_DO | 00010110 |
| /testbench/AEn | St1 |
| /testbench/EFn | St1 |
| /testbench/AFn | St0 |
| /testbench/FFn | St1 |
| /testbench/RDOn | St1 |
| /testbench/WROn | St1 |
| /testbench/FifoDem... | 00011100 |

```
estbench/AEn       /testbench/WROn
   /testbench/EFn  /testbench/FifoDemo_0/UDCNT/FIFO_DATA_c
         /testbench/AFn
               /testbench/FFn
                    /testbench/RDOn
   146   +0
   223   +0
   247   +0
   254   +0
   259   +0
   283   +0
```

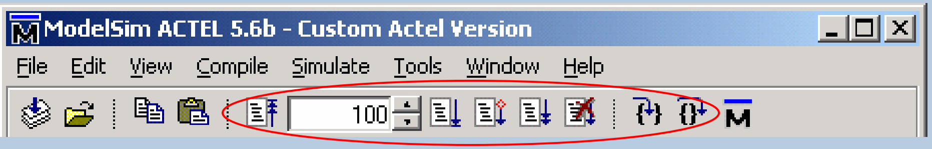
File name: list.lst

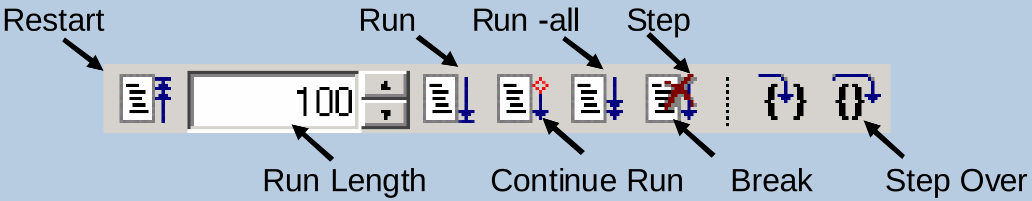
Save as type: List Files (*.lst)

# Advancing Simulation Time

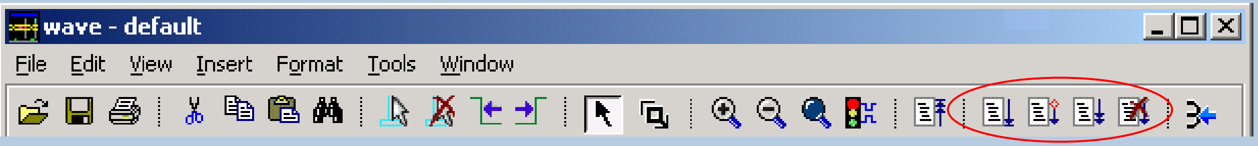
## Three Methods

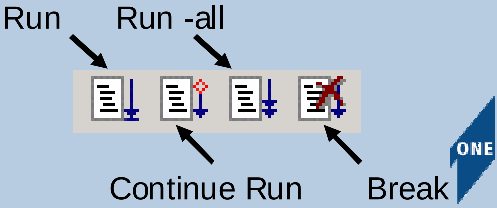
- **At VSIM prompt:**
- **VSIM 12> run 100 ms**
- **In Main Window Tool Bar:**


ModelSim ACTEL 5.6b - Custom Actel Version
File Edit View Compile Simulate Tools Window Help
100



- **In Wave Window Tool Bar:**



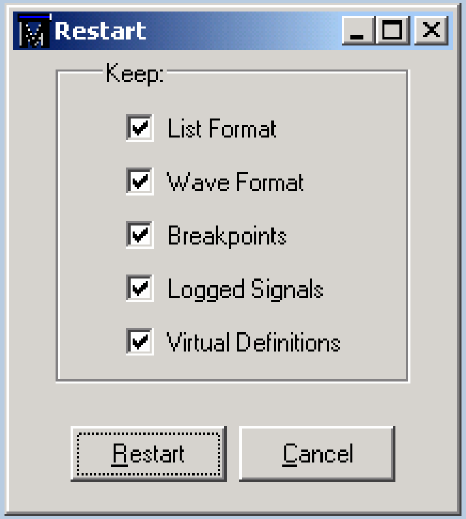


# Re-starting Simulation

## Restart to Zero

- Force Restart at VSIM Prompt
- VSIM 12> restart –f

- In Main Window Run > Restart or Restart Button
- Displays Restart Dialog



Restart

Keep:

☑ List Format

☑ Wave Format

☑ Breakpoints

☑ Logged Signals

☑ Virtual Definitions

## Keep Current

- Listed Signals
- Waved Signals
- Breakpoints
- Logged Signals
- Virtual Signals

# ModelSim Macro Files

## ModelSim Commands Can Be Saved in Macro File

- **The ‘do’ Command Executes Commands**
- **Macro File Can Have any Name and Extension**

## Syntax:

**do<filename> [<parameter_value>]**

## Example:

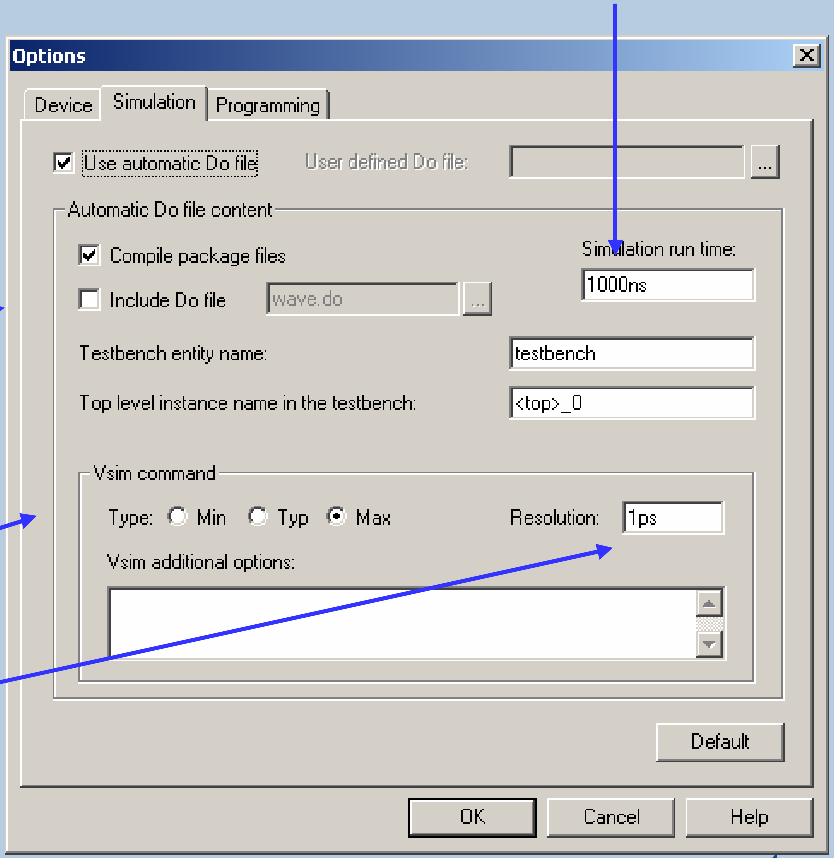
**do run.do**

- **This Command Executes File run.do**

```
vlib presynth
vmap presynth ./presynth
vcom -93 -work presynth D:/Actelprj/count32/hdl/count32.vhd
vcom -93 -work presynth D:/Actelprj/count32/stimulus/count32.vhd
vsim presynth.testbench
add wave /testbench/*
run 1000ns
```

# Libero Simulation Options

- Simulation Options Can Be Set from Simulation Tab under Options
  - **Results Saved in run.do File**



Options

☑ Use automatic Do file

User defined Do file:

Automatic Do file content

☑ Compile package files

□ Include Do file: wave.do

Simulation run time: 1000ns

Testbench entity name: testbench

Top level instance name in the testbench: <top>_0

Vsim command

Type: ○ Min ○ Typ ● Max

Resolution: 1ps

Vsim additional options:

Specify simulation run time

Use Automatic Do File allows Libero to automatically set up the simulation for the user

Include Do file allows Libero to include user-defined script. User can enter name of script file

Select min, typ, max simulation conditions for post-layout simulation

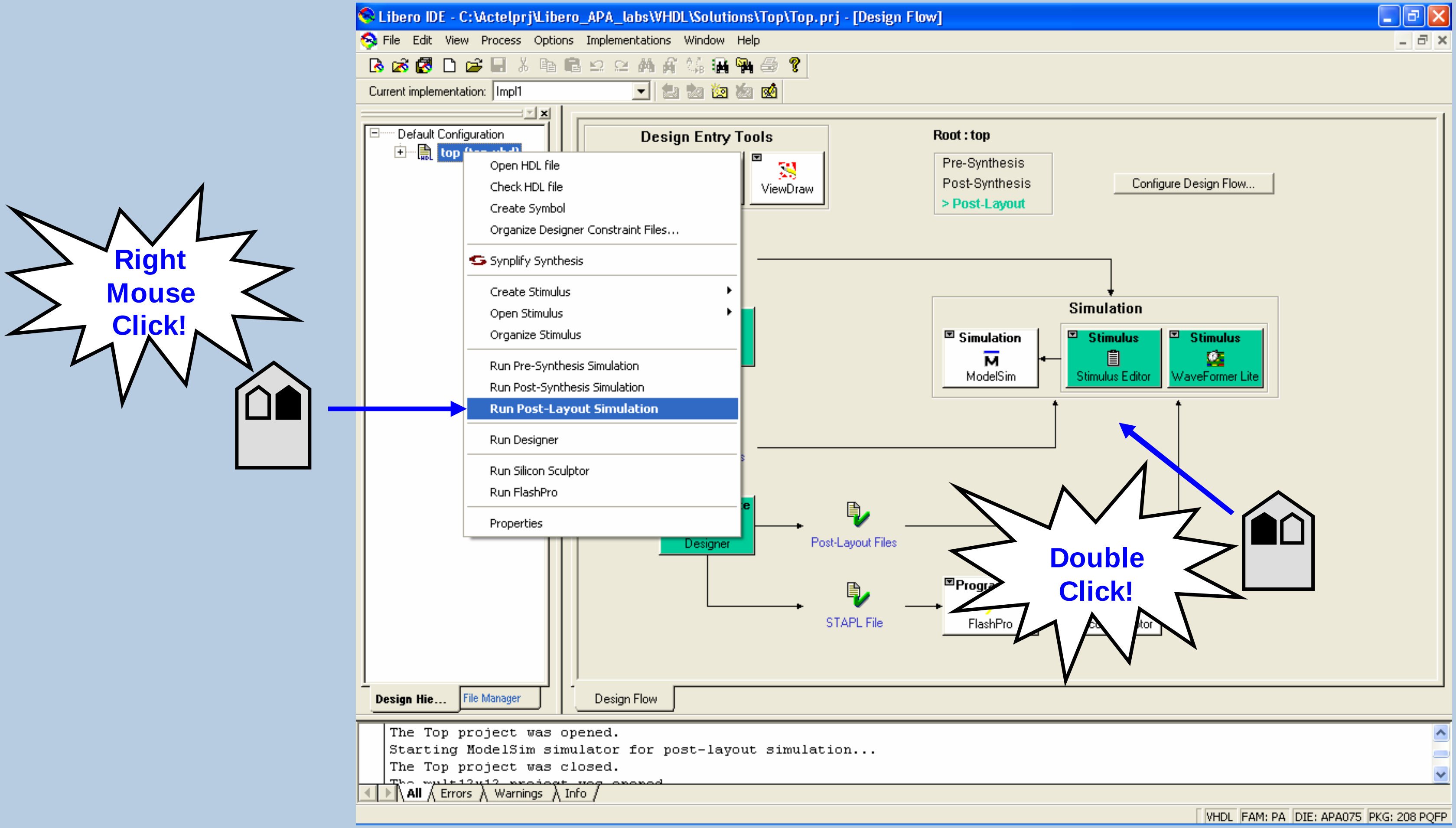
Default resolution based on family choice

**1ps for 500K, APA, 54SXA, AX**

**1ns for all other families**

# Invoking ModelSim
## *Pre- or Post-Synthesis*

- Click “Simulation” Design Flow Window or …

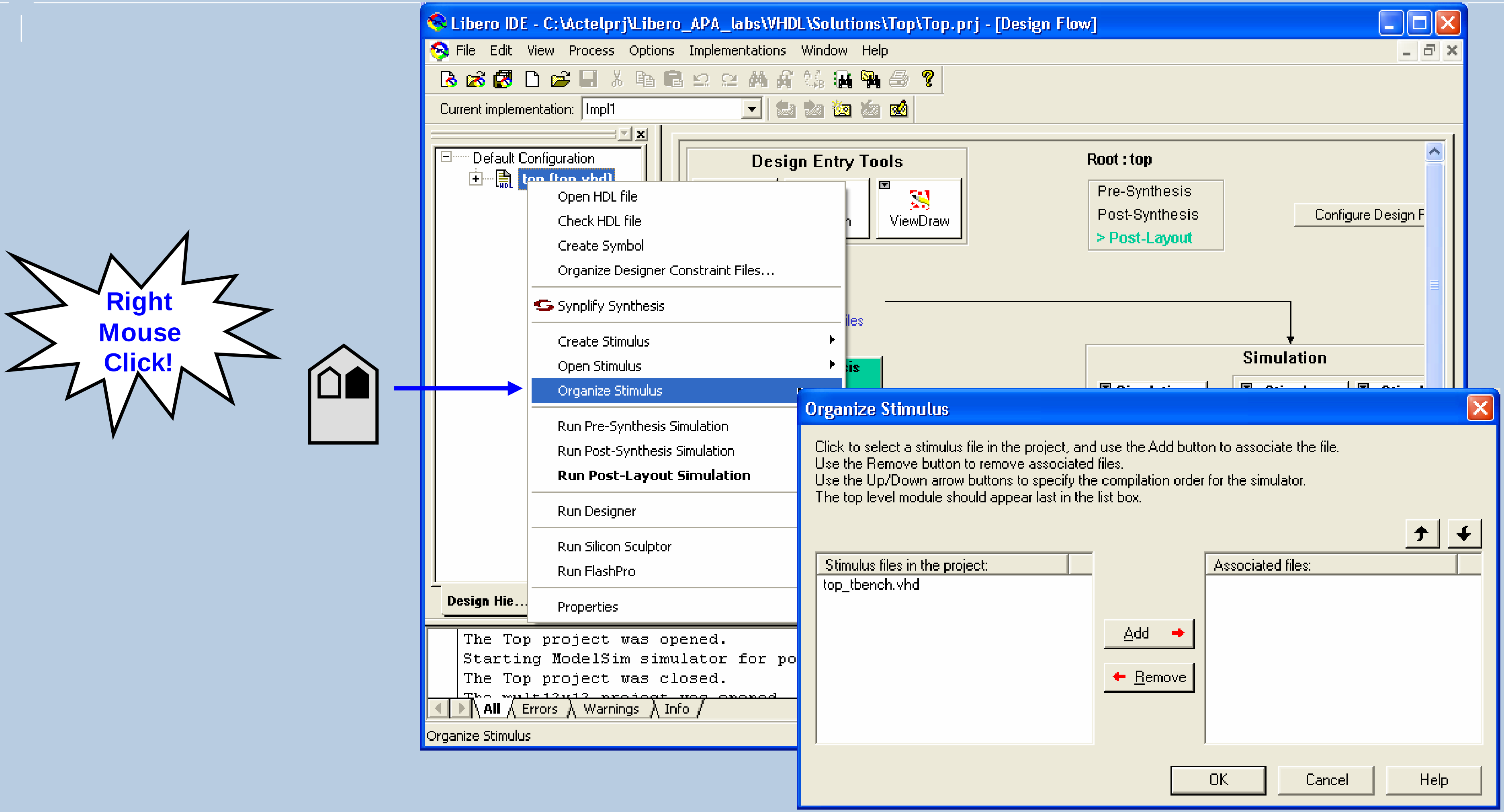


```
The Top project was opened.
Starting ModelSim simulator for post-layout simulation...
The Top project was closed.
```

Right Mouse Click!

Double Click!

# Associating Stimulus



```
The Top project was opened.
Starting ModelSim simulator for po
The Top project was closed.
```

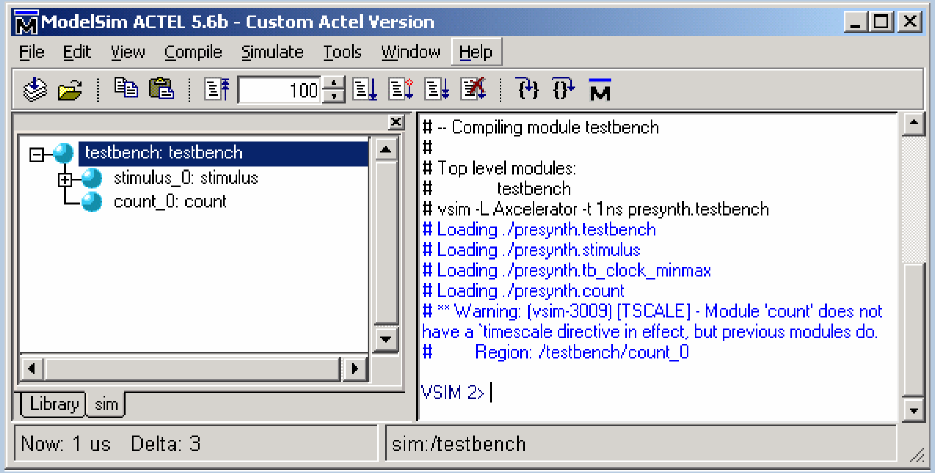
Organize Stimulus

Click to select a stimulus file in the project, and use the Add button to associate the file.
Use the Remove button to remove associated files.
Use the Up/Down arrow buttons to specify the compilation order for the simulator.
The top level module should appear last in the list box.

Stimulus files in the project: top_tbench.vhd

# Pre-Synthesis Simulation

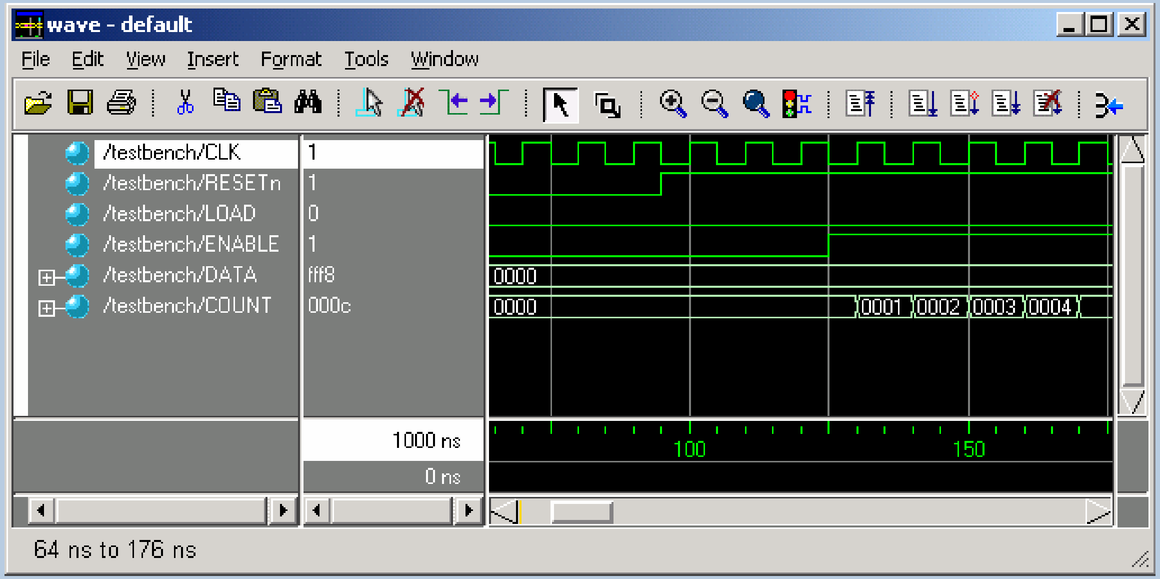
- ModelSim Automatically Compiles Design and Runs Simulation for 1 µS
  - **(External) Signals from Testbench Automatically Added to Wave Window**
  - **Additional (Internal) Signals Can Be Added by User**


ModelSim ACTEL 5.6b - Custom Actel Version
File Edit View Compile Simulate Tools Window Help
100
testbench: testbench
stimulus_0: stimulus
count_0: count
Library sim

```
# -- Compiling module testbench
#
# Top level modules:
#         testbench
# vsim -L Axcelerator -t 1ns presynth.testbench
# Loading ./presynth.testbench
# Loading ./presynth.stimulus
# Loading ./presynth.tb_clock_minmax
# Loading ./presynth.count
# ** Warning: (vsim-3009) [TSCALE] - Module 'count' does not
have a `timescale directive in effect, but previous modules do.
#       Region: /testbench/count_0

VSIM 2> |
```

Now: 1 us   Delta: 3   sim:/testbench



```
/testbench/CLK      1
/testbench/RESETn   1
/testbench/LOAD     0
/testbench/ENABLE   1
/testbench/DATA     fff8
/testbench/COUNT    000c

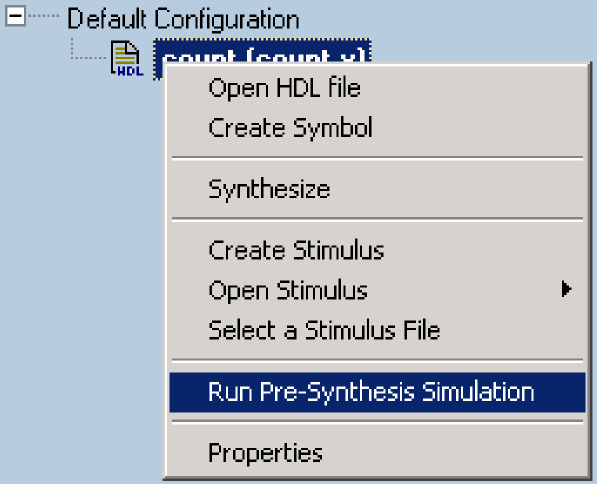
1000 ns
0 ns

64 ns to 176 ns
```

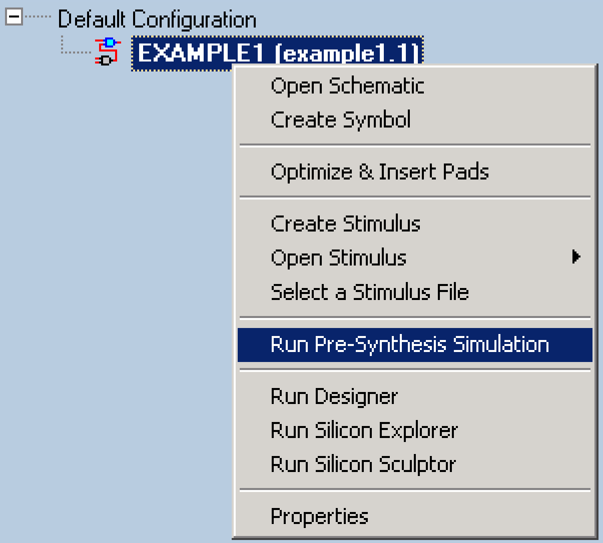
# Simulating Designs
*Summary*

- Capture Design
  - Generate RTL Netlist (VHDL or Verilog)

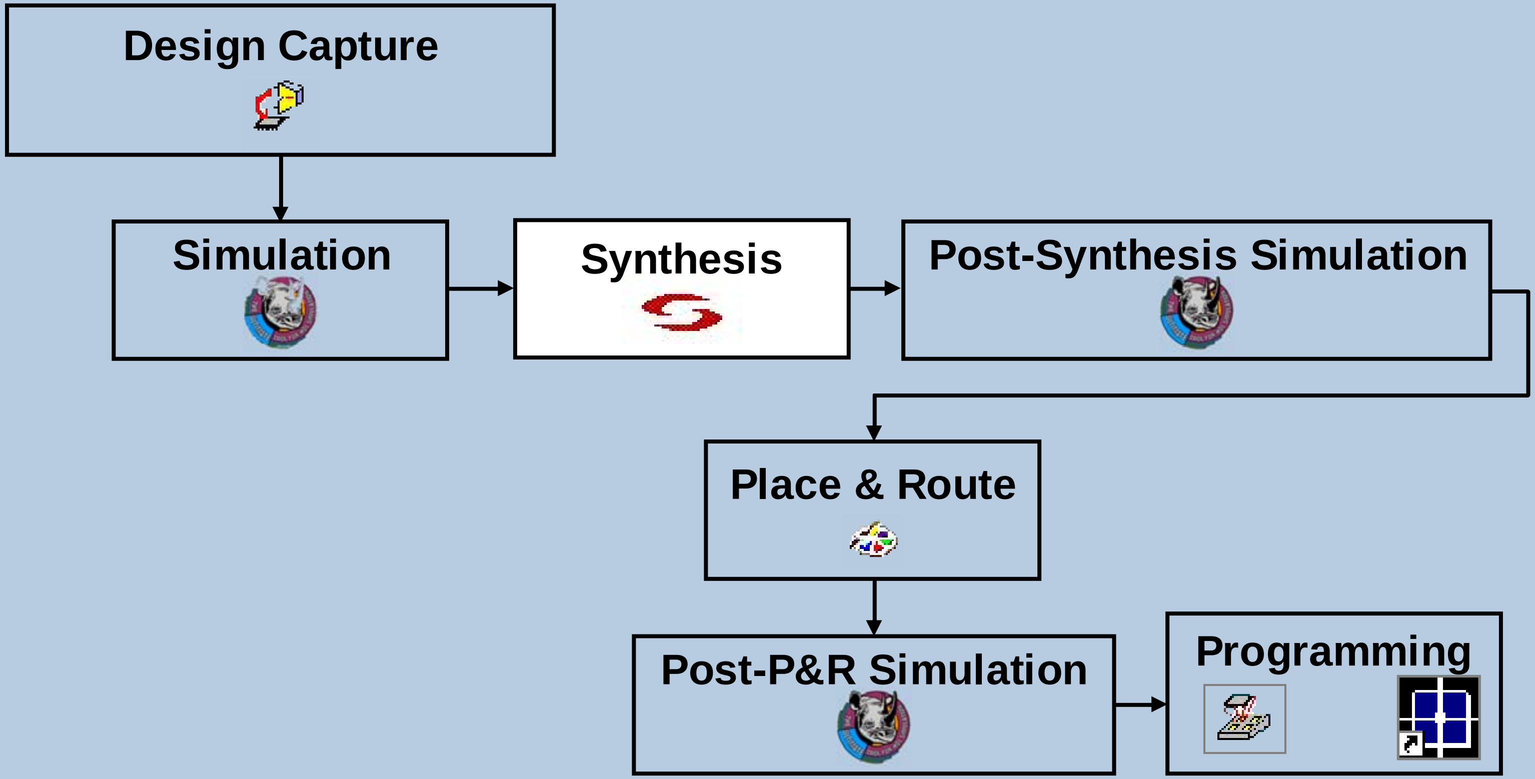
    OR
  - Create Schematic
    - May Include RTL blocks
    - Structural VHDL or Verilog Netlist Automatically Created before Simulation



- Create Testbench
  - Use WaveFormer Lite, or Text Editor
- Associate Stimulus
- Run Pre-Synthesis Simulation



# Synthesis



Design Capture

Simulation

Synthesis

Post-Synthesis Simulation

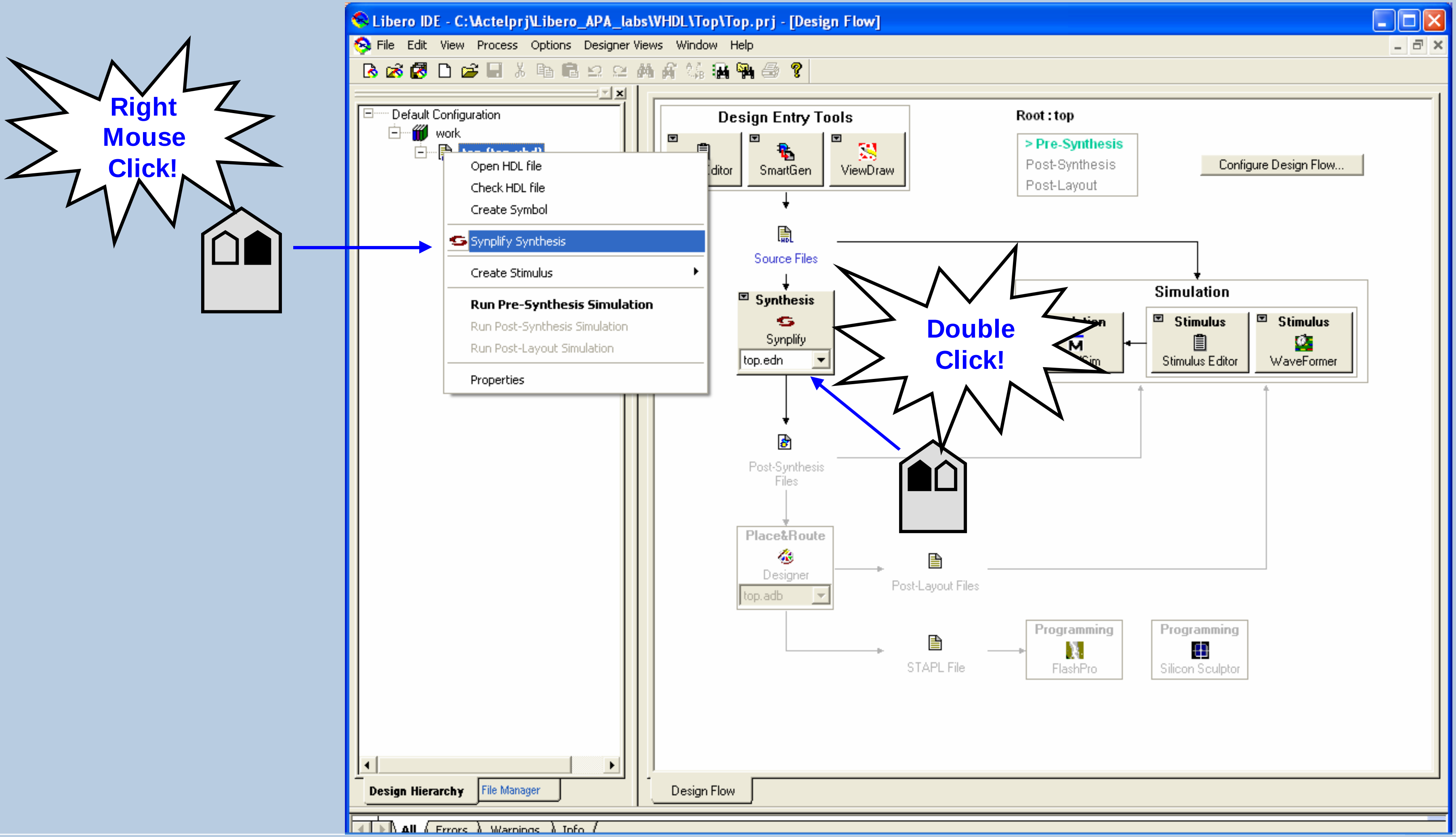
Place & Route

Post-P&R Simulation

Programming

# Invoking Synplicity

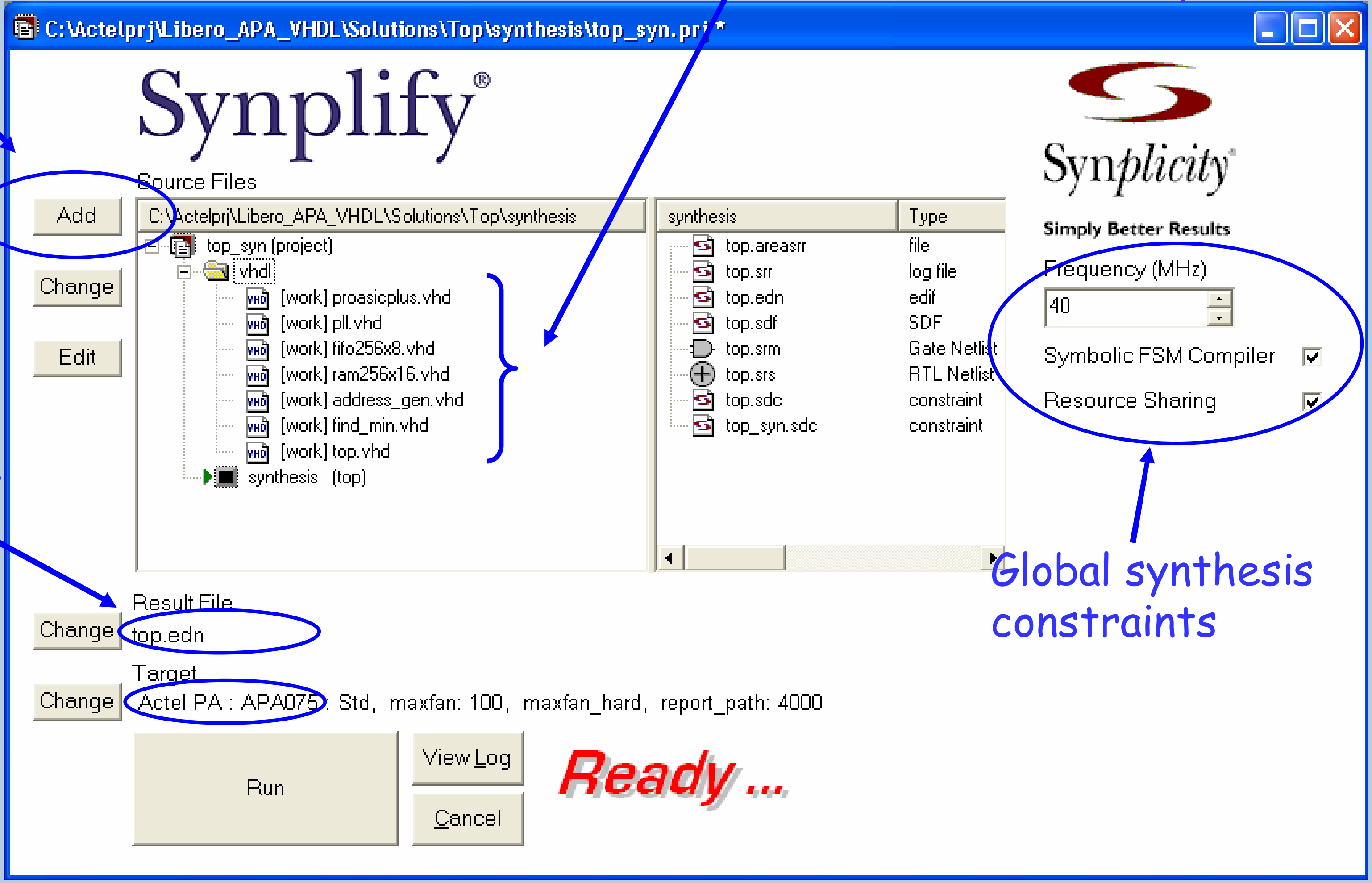
- Click “Synthesis” in Design Flow Window or ..



# Synplify Interface

Add constraint files or VHDL packages

Libero automatically lists files lowest levels first, top last



C:\Actelprj\Libero_APA_VHDL\Solutions\Top\synthesis\top_syn.prj *

Source Files

C:\Actelprj\Libero_APA_VHDL\Solutions\Top\synthesis

```
top_syn (project)
  vhdl
    [work] proasicplus.vhd
    [work] pll.vhd
    [work] fifo256x8.vhd
    [work] ram256x16.vhd
    [work] address_gen.vhd
    [work] find_min.vhd
    [work] top.vhd
  synthesis  (top)
```

| synthesis | Type |
|---|---|
| top.areasrr | file |
| top.srr | log file |
| top.edn | edif |
| top.sdf | SDF |
| top.srm | Gate Netlist |
| top.srs | RTL Netlist |
| top.sdc | constraint |
| top_syn.sdc | constraint |

Frequency (MHz): 40

Symbolic FSM Compiler ☑

Resource Sharing ☑

Result File: top.edn

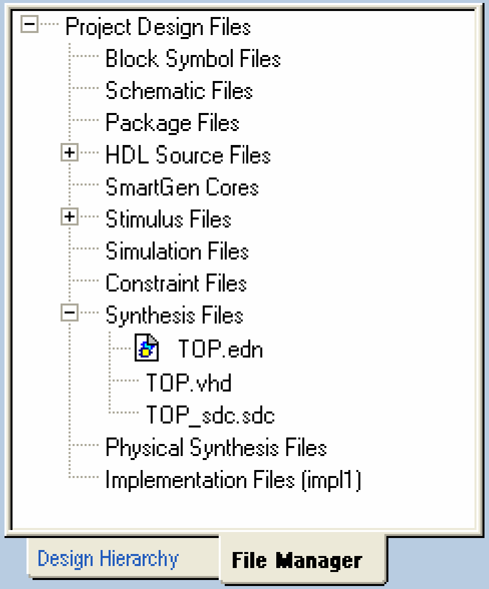
Target: Actel PA : APA075: Std, maxfan: 100, maxfan_hard, report_path: 4000

Change target and result file

Global synthesis constraints

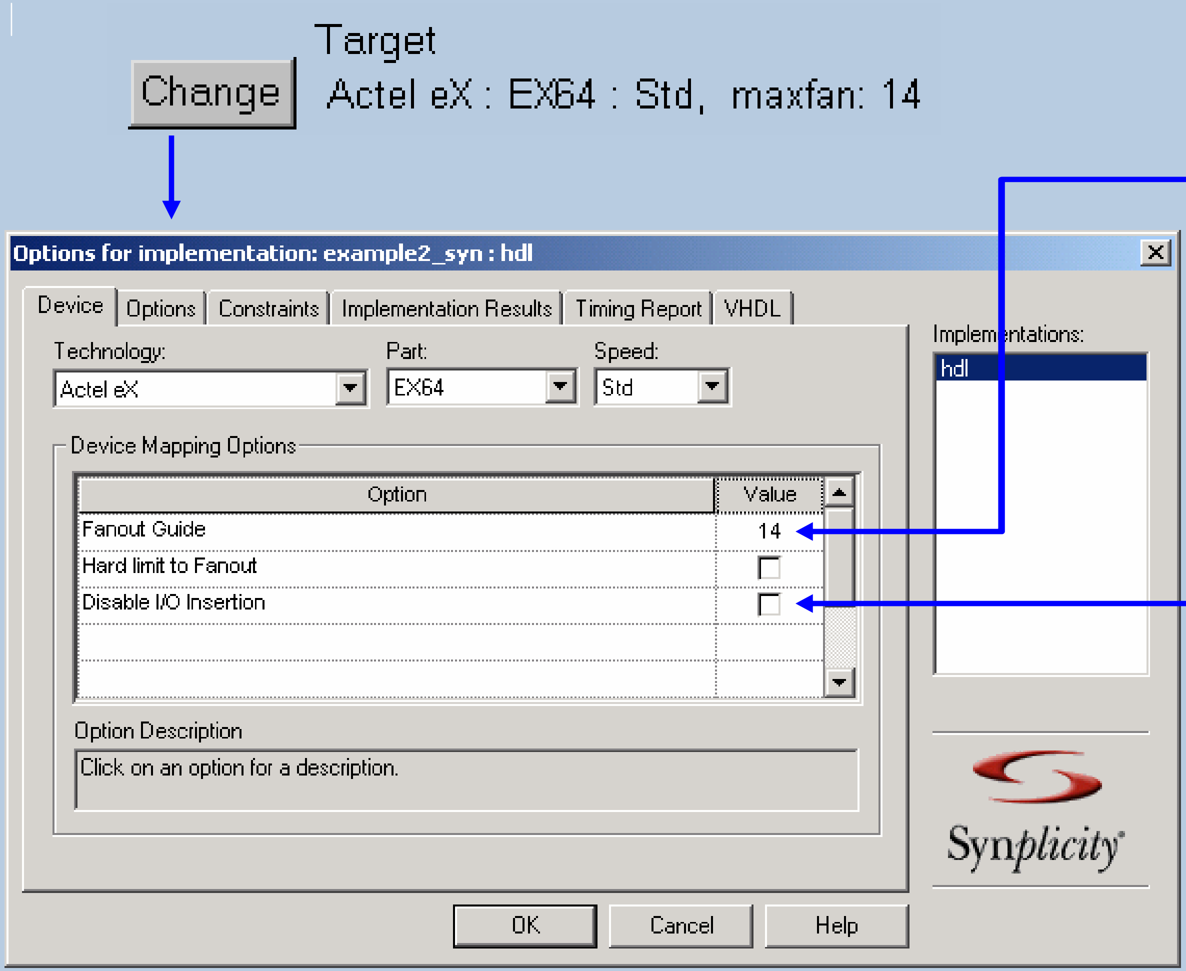
# Result File

- Synplicity Produces an EDIF Netlist
  - **<design>.edn**
- Libero Automatically Produces Structural VHDL or Verilog Netlist
  - **<design>.vhd or <design>.v**
  - **Results Appear on File Manager Tab under Synthesis Files**



- Project Design Files
  - Block Symbol Files
  - Schematic Files
  - Package Files
  - HDL Source Files
  - SmartGen Cores
  - Stimulus Files
  - Simulation Files
  - Constraint Files
  - Synthesis Files
    - TOP.edn
    - TOP.vhd
    - TOP_sdc.sdc
  - Physical Synthesis Files
  - Implementation Files (impl1)

# Setting the Target Options



Target

Change | Actel eX : EX64 : Std, maxfan: 14

Options for implementation: example2_syn : hdl

Technology: Actel eX

Part: EX64

Speed: Std

Implementations: hdl

Device Mapping Options

| Option | Value |
|---|---|
| Fanout Guide | 14 |
| Hard limit to Fanout | □ |
| Disable I/O Insertion | □ |

Option Description

Click on an option for a description.

High fanout = slow, small designs
Low fanout = fast, large designs
Use defaults for first pass

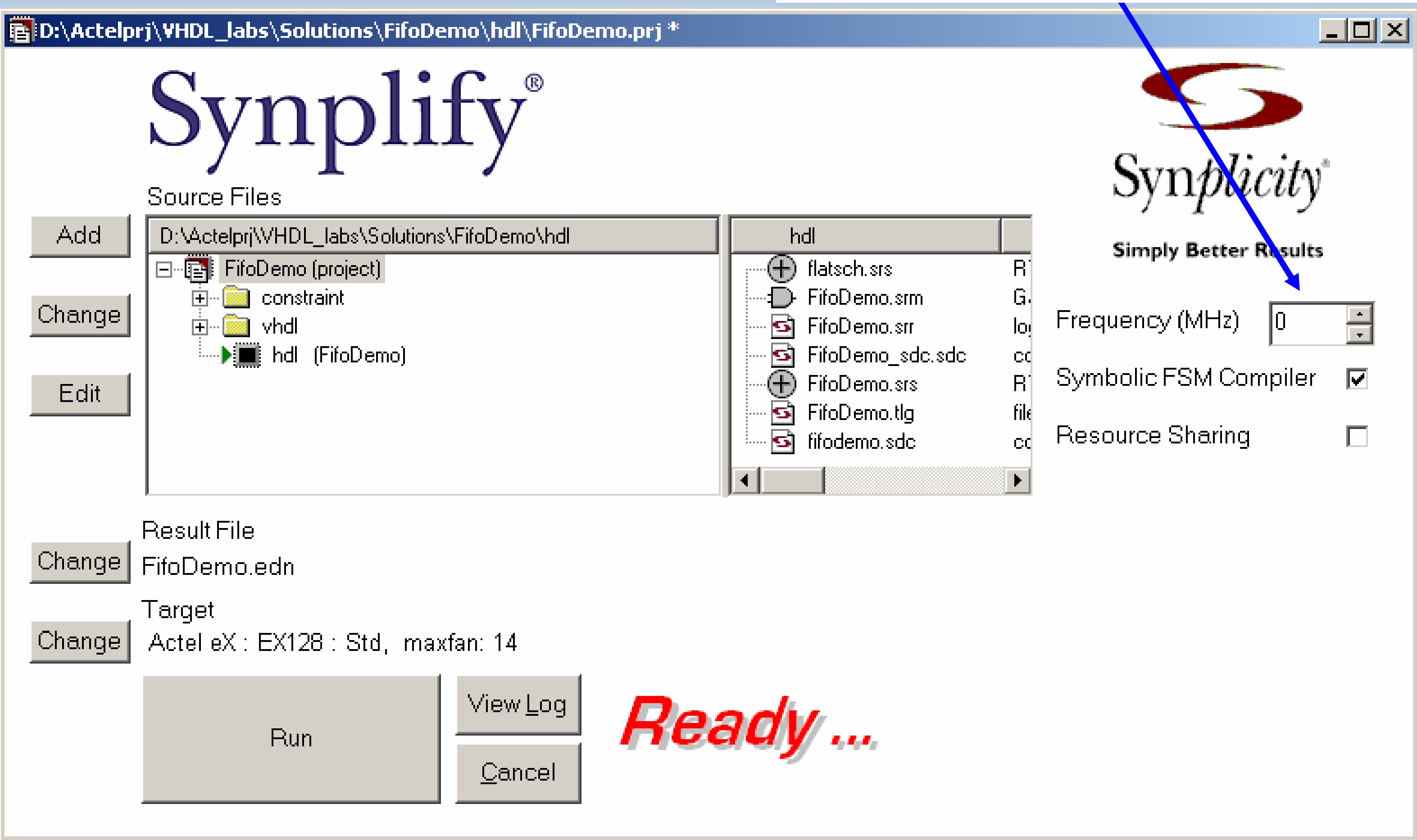
By default, Synplify will insert Actel I/O macros on all the HDL I/O ports.
When synthesizing lower-level blocks, this must be disabled.

# Global Constraints

- Frequency
- Symbolic FSM Compiler
- Configure HDL Compiler
- Resource Sharing

# Global Frequency

Global clock frequency is applied to all clock domains in the design
Low value means optimize for area



D:\Actelprj\VHDL_labs\Solutions\FifoDemo\hdl\FifoDemo.prj *

Source Files

D:\Actelprj\VHDL_labs\Solutions\FifoDemo\hdl

- FifoDemo (project)
  - constraint
  - vhdl
  - hdl (FifoDemo)

hdl

- flatsch.srs
- FifoDemo.srm
- FifoDemo.srr
- FifoDemo_sdc.sdc
- FifoDemo.srs
- FifoDemo.tlg
- fifodemo.sdc

Frequency (MHz) 0

Symbolic FSM Compiler ☑

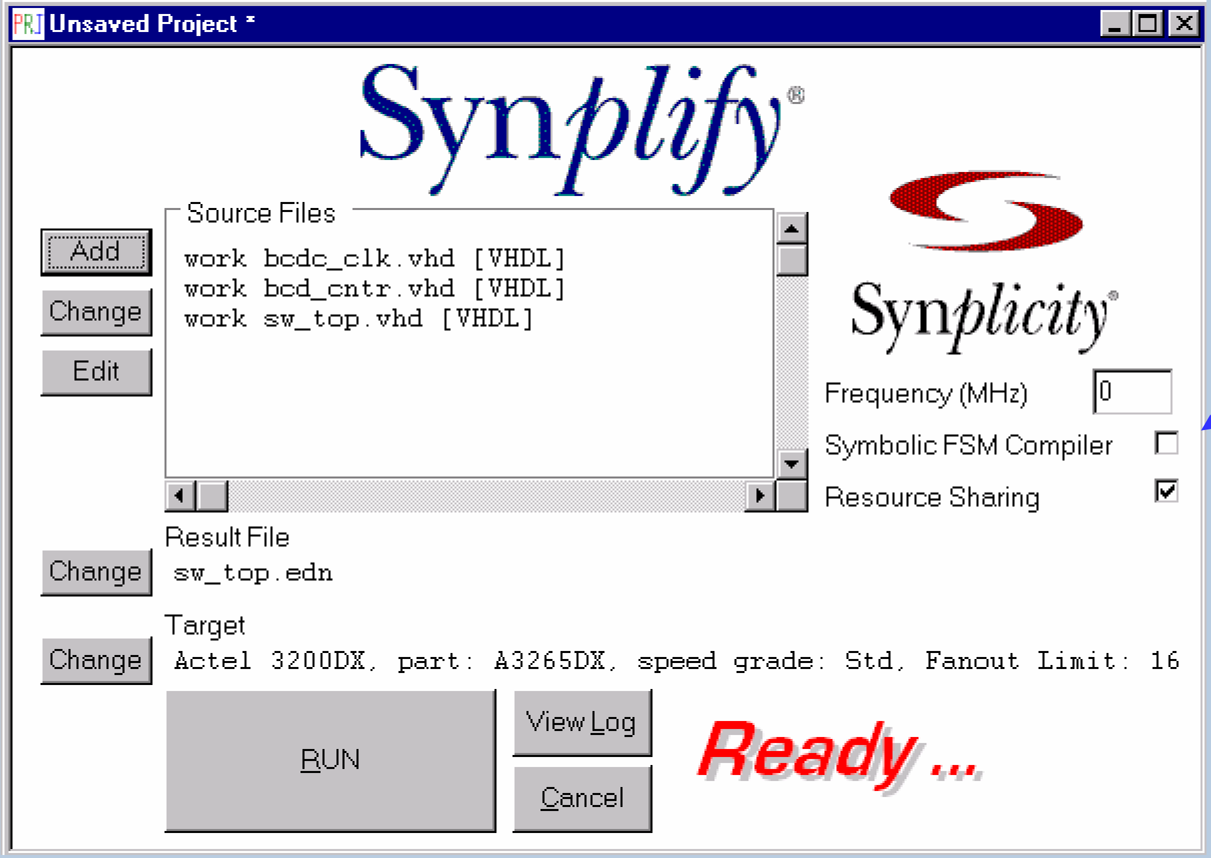
Resource Sharing ☐

Result File
FifoDemo.edn

Target
Actel eX : EX128 : Std, maxfan: 14

Ready ...

# Symbolic FSM Compiler



Unsaved Project *

Source Files

```
work bcdc_clk.vhd [VHDL]
work bcd_cntr.vhd [VHDL]
work sw_top.vhd [VHDL]
```

Frequency (MHz) 0

Symbolic FSM Compiler □

Resource Sharing ☑

Result File

sw_top.edn

Target

Actel 3200DX, part: A3265DX, speed grade: Std, Fanout Limit: 16

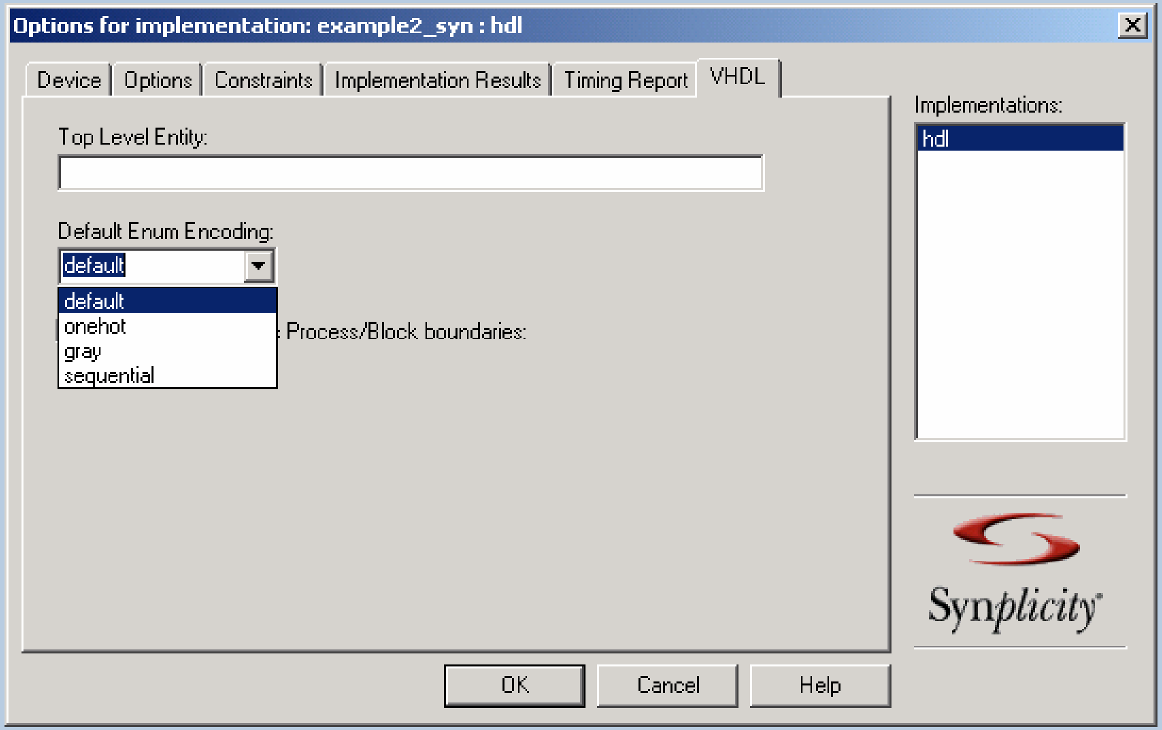
When checked, it selects proper encoding for all state machines.

Encoding method can be set on individual state machines with syn_encoding directive in the HDL code

# State Machine Encoding (VHDL)

## Options > Configure VHDL Compiler

Sets the default encoding style for enumerated types



Options for implementation: example2_syn : hdl

Top Level Entity:

Default Enum Encoding: default

- default
- onehot
- gray
- sequential

: Process/Block boundaries:

Implementations: hdl

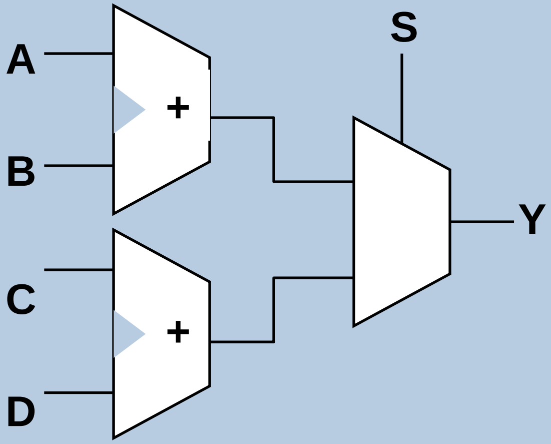
Override encoding style on an individual basis using syn_encoding directive in constraint editor or the HDL source code

| # of states | default encoding |
|---|---|
| 1 - 4 | sequential |
| 5 - 24 | one-hot |
| > 24 | gray |

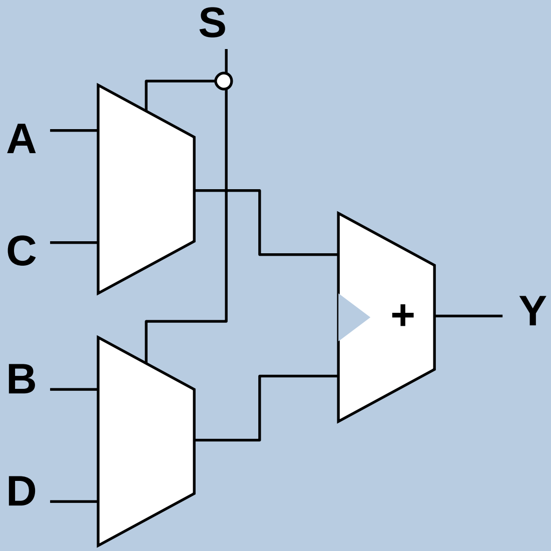
# Resource Sharing

- When enabled, Synplify performs automatic sharing of operator resources, including adders, subtractors, incrementers, and decrementers.

```
if (s = ‘0’) then
Y <= A + B;
else
Y <= C + D;
end if;
```

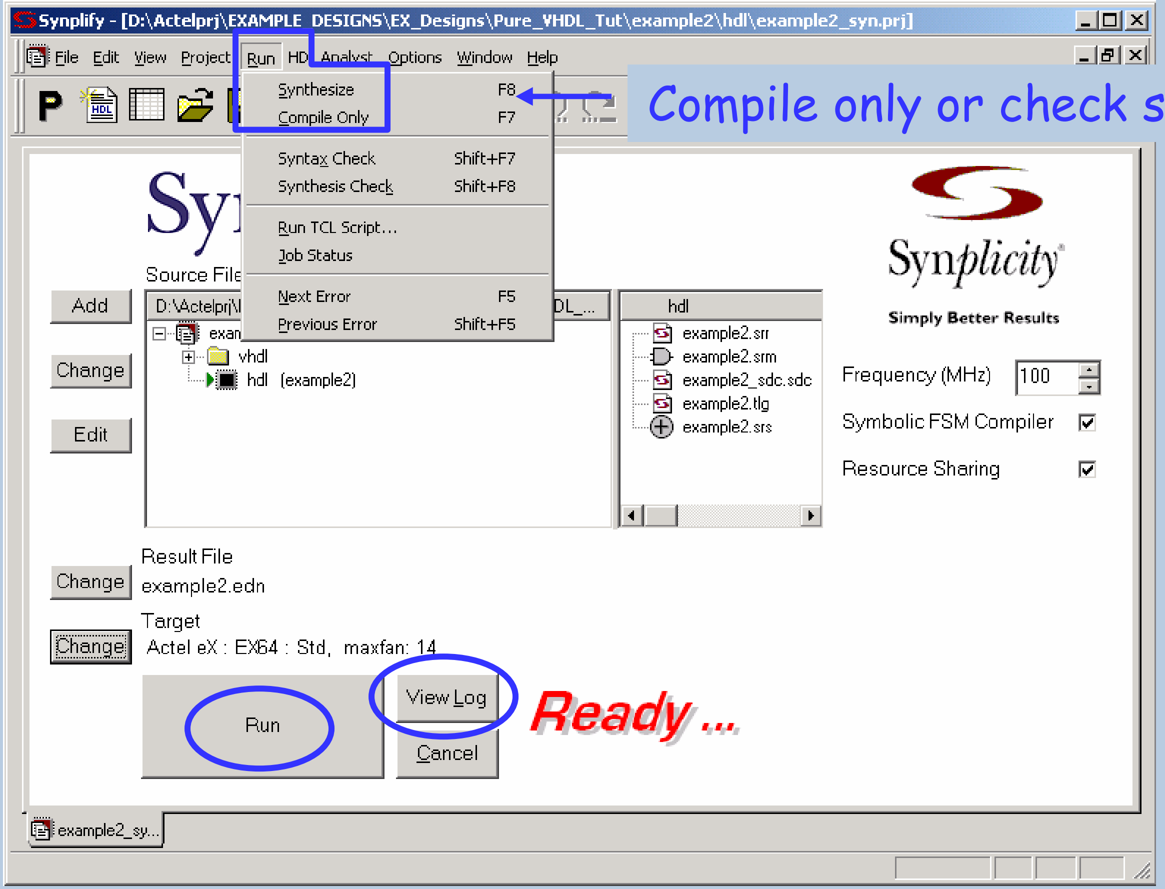


Without resource sharing



With resource sharing

# Performing Synthesis



Synplify - [D:\Actelprj\EXAMPLE_DESIGNS\EX_Designs\Pure_VHDL_Tut\example2\hdl\example2_syn.prj]

Frequency (MHz) 100

Symbolic FSM Compiler ☑

Resource Sharing ☑

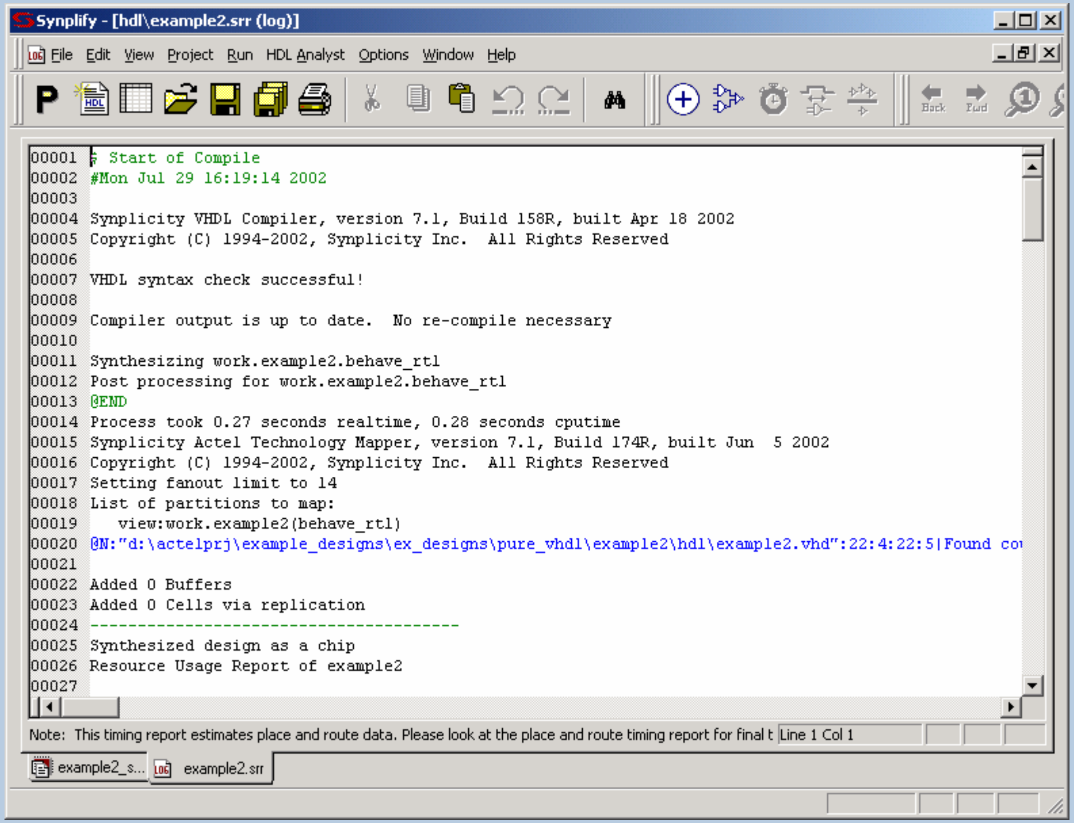
Result File
example2.edn

Target
Actel eX : EX64 : Std, maxfan: 14

Compile only or check syntax

Ready ...

# View Log



Synplify - [hdl\example2.srr (log)]
File Edit View Project Run HDL Analyst Options Window Help
Back Fwd
example2_s...
example2.srr

```
# Start of Compile
#Mon Jul 29 16:19:14 2002

Synplicity VHDL Compiler, version 7.1, Build 158R, built Apr 18 2002
Copyright (C) 1994-2002, Synplicity Inc.  All Rights Reserved

VHDL syntax check successful!

Compiler output is up to date.  No re-compile necessary

Synthesizing work.example2.behave_rtl
Post processing for work.example2.behave_rtl
@END
Process took 0.27 seconds realtime, 0.28 seconds cputime
Synplicity Actel Technology Mapper, version 7.1, Build 174R, built Jun  5 2002
Copyright (C) 1994-2002, Synplicity Inc.  All Rights Reserved
Setting fanout limit to 14
List of partitions to map:
   view:work.example2(behave_rtl)
@N:"d:\actelprj\example_designs\ex_designs\pure_vhdl\example2\hdl\example2.vhd":22:4:22:5|Found co

Added 0 Buffers
Added 0 Cells via replication
---------------------------------------
Synthesized design as a chip
Resource Usage Report of example2

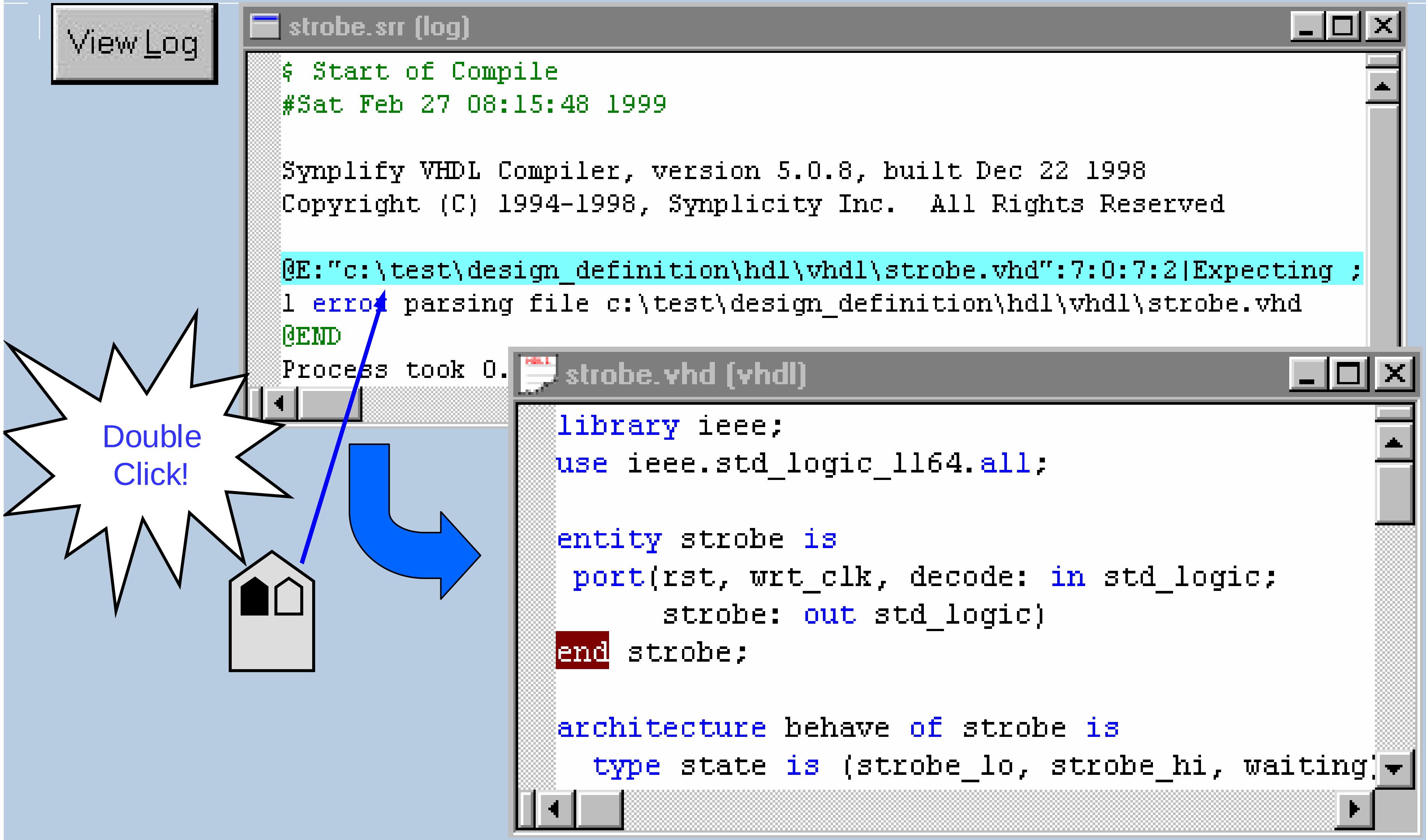
```

Note:  This timing report estimates place and route data. Please look at the place and route timing report for final t Line 1 Col 1

- Synplify Log contains Plenty of Valuable Information:!
  - **Warnings and Errors**
    - **Double-click and Jump to Code!**
  - **Fanout Limit**
  - **Extraction Information (Found Counter, FSM, Adder, etc.)**
  - **Net Loading**
  - **Logic Buffering and Replication Information**
  - **Resource Usage**
  - **Critical Path Timing Analysis**

ONE CHIP is all you need

# Reading the Log File
## *Errors*



Double Click!

```
$ Start of Compile
#Sat Feb 27 08:15:48 1999

Synplify VHDL Compiler, version 5.0.8, built Dec 22 1998
Copyright (C) 1994-1998, Synplicity Inc.  All Rights Reserved

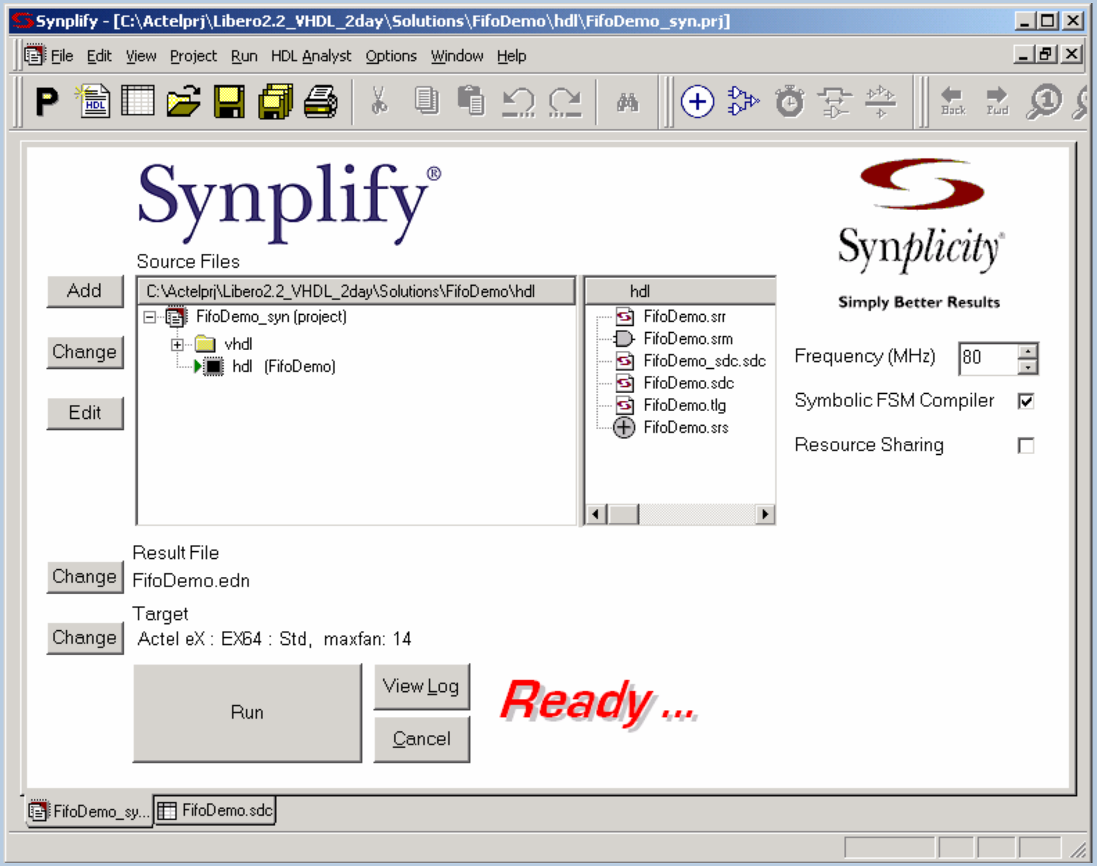
@E:"c:\test\design_definition\hdl\vhdl\strobe.vhd":7:0:7:2|Expecting ;
1 error parsing file c:\test\design_definition\hdl\vhdl\strobe.vhd
@END
Process took 0.
```

```
library ieee;
use ieee.std_logic_1164.all;

entity strobe is
 port(rst, wrt_clk, decode: in std_logic;
      strobe: out std_logic)
end strobe;

architecture behave of strobe is
  type state is (strobe_lo, strobe_hi, waiting
```

# Constraint Editor



Synplify - [C:\Actelprj\Libero2.2_VHDL_2day\Solutions\FifoDemo\hdl\FifoDemo_syn.prj]

Source Files

C:\Actelprj\Libero2.2_VHDL_2day\Solutions\FifoDemo\hdl

- FifoDemo_syn (project)
  - vhdl
  - hdl (FifoDemo)

hdl

- FifoDemo.srr
- FifoDemo.srm
- FifoDemo_sdc.sdc
- FifoDemo.sdc
- FifoDemo.tlg
- FifoDemo.srs

Frequency (MHz) 80

Symbolic FSM Compiler ☑

Resource Sharing □

Result File
FifoDemo.edn

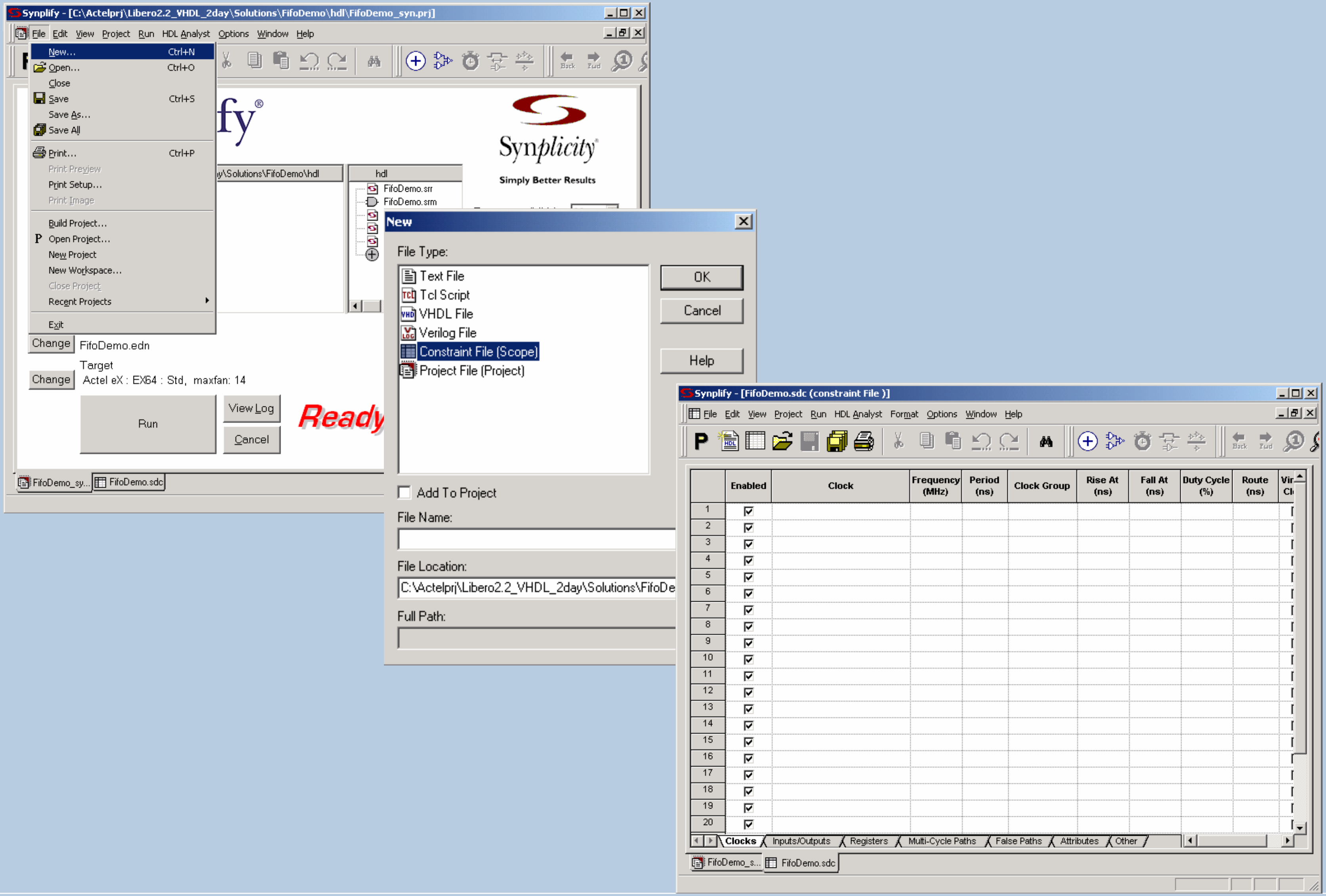
Target
Actel eX : EX64 : Std, maxfan: 14

Ready ...

- Synplify facilitates constraint entry with a spreadsheet-like constraint editor.
- File->New
- Select Constraint File (Spreadsheet)

  **Select Files of type Constraint Files**
- Press OK
- Extremely easy to use

# Constraint Editor



y\Solutions\FifoDemo\hdl

FifoDemo.edn

Target

Actel eX : EX64 : Std, maxfan: 14

File Type: Constraint File (Scope)

□ Add To Project

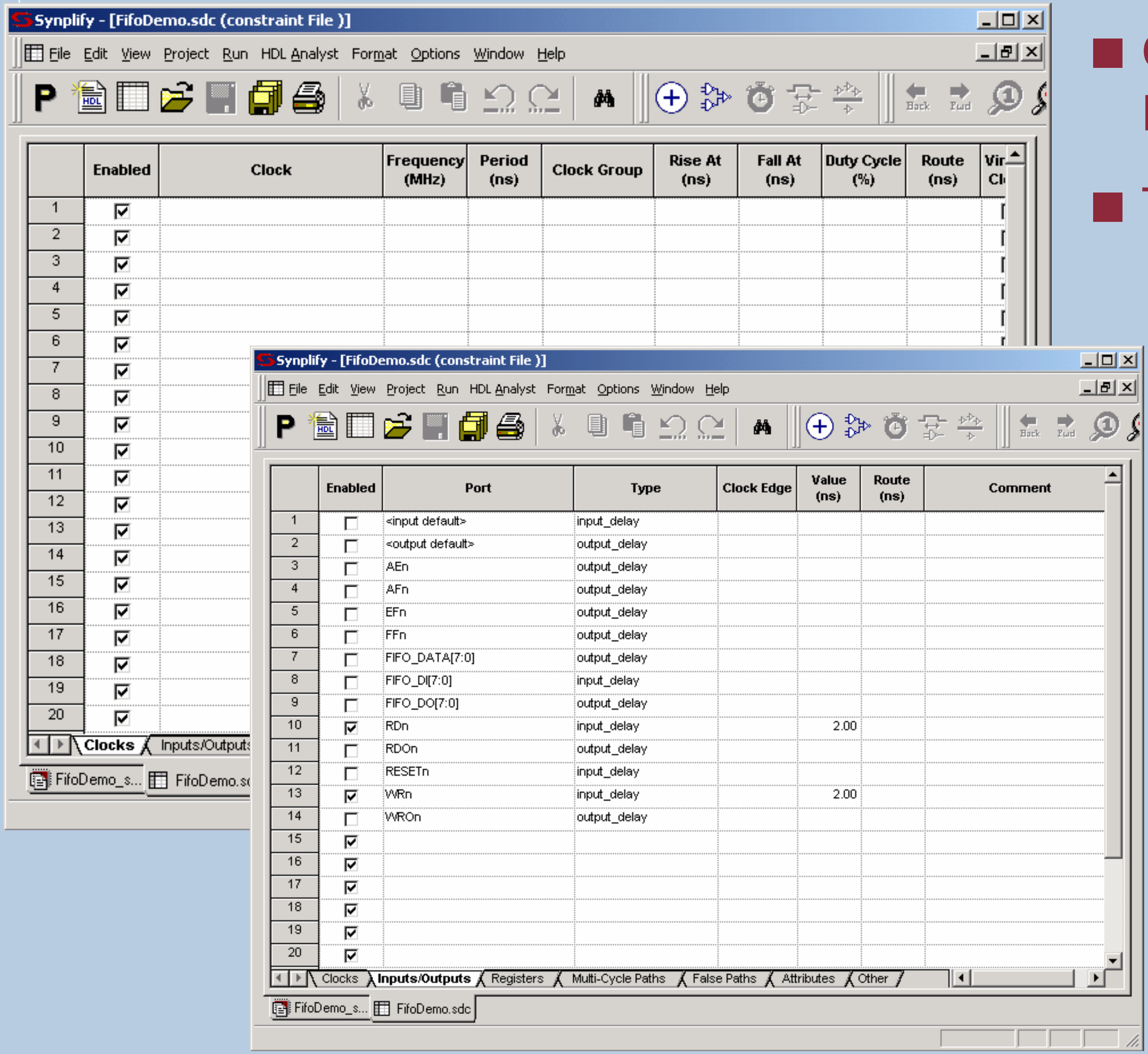
File Name:

File Location: C:\Actelprj\Libero2.2_VHDL_2day\Solutions\FifoDe

Full Path:

| | Enabled | Clock | Frequency (MHz) | Period (ns) | Clock Group | Rise At (ns) | Fall At (ns) | Duty Cycle (%) | Route (ns) | Vir Cl |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ☑ | | | | | | | | | |
| 2 | ☑ | | | | | | | | | |
| 3 | ☑ | | | | | | | | | |
| 4 | ☑ | | | | | | | | | |
| 5 | ☑ | | | | | | | | | |
| 6 | ☑ | | | | | | | | | |
| 7 | ☑ | | | | | | | | | |
| 8 | ☑ | | | | | | | | | |
| 9 | ☑ | | | | | | | | | |
| 10 | ☑ | | | | | | | | | |
| 11 | ☑ | | | | | | | | | |
| 12 | ☑ | | | | | | | | | |
| 13 | ☑ | | | | | | | | | |
| 14 | ☑ | | | | | | | | | |
| 15 | ☑ | | | | | | | | | |
| 16 | ☑ | | | | | | | | | |
| 17 | ☑ | | | | | | | | | |
| 18 | ☑ | | | | | | | | | |
| 19 | ☑ | | | | | | | | | |
| 20 | ☑ | | | | | | | | | |

# Constraint Editor (Cont.)

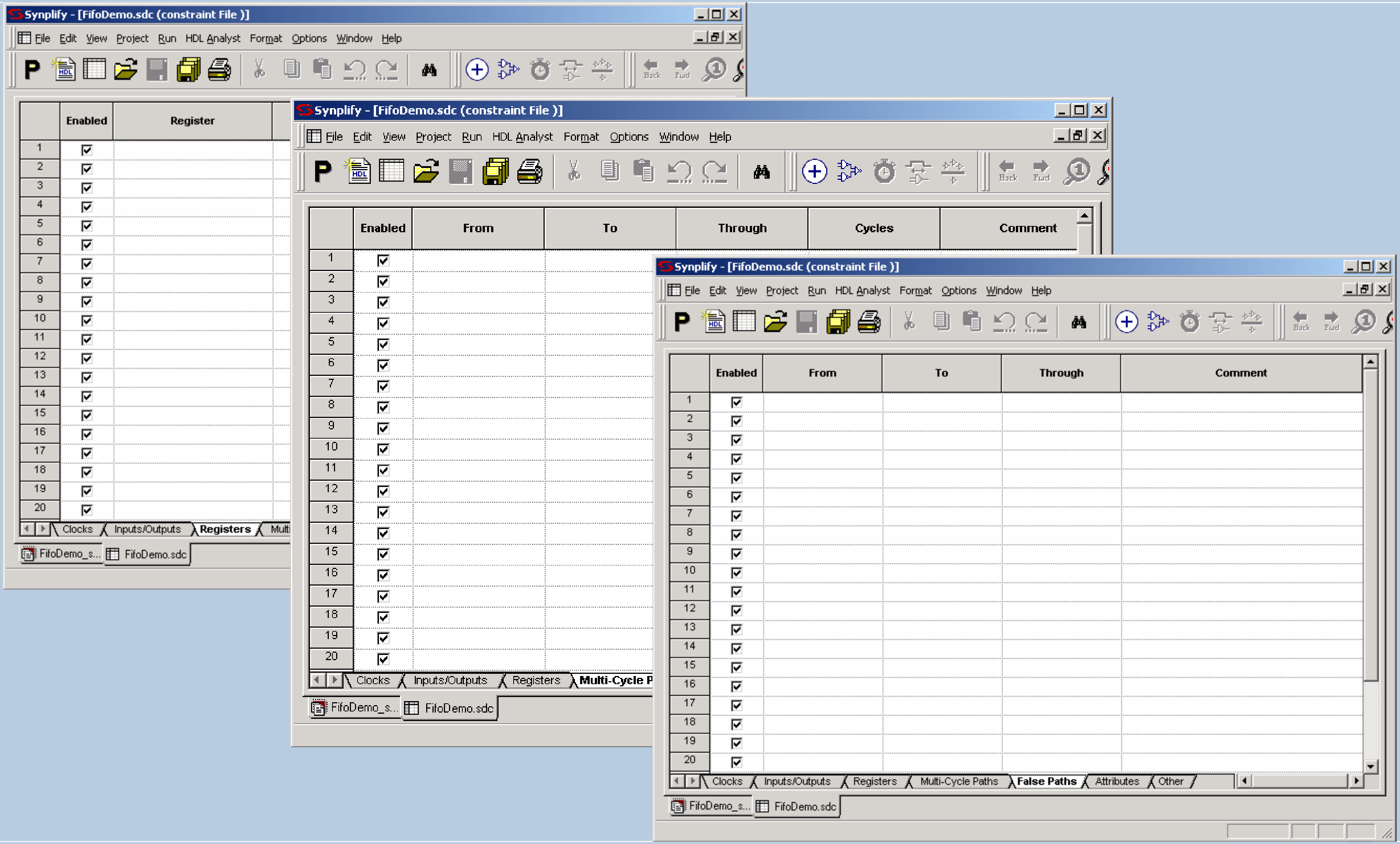

Synplify - [FifoDemo.sdc (constraint File )]
File Edit View Project Run HDL Analyst Format Options Window Help
Clocks
Inputs/Outputs
Registers
Multi-Cycle Paths
False Paths
Attributes
Other
FifoDemo_s...
FifoDemo.sdc

|  | Enabled | Clock | Frequency (MHz) | Period (ns) | Clock Group | Rise At (ns) | Fall At (ns) | Duty Cycle (%) | Route (ns) | Vir Cl |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ☑ |  |  |  |  |  |  |  |  |  |
| 2 | ☑ |  |  |  |  |  |  |  |  |  |
| 3 | ☑ |  |  |  |  |  |  |  |  |  |
| 4 | ☑ |  |  |  |  |  |  |  |  |  |
| 5 | ☑ |  |  |  |  |  |  |  |  |  |
| 6 | ☑ |  |  |  |  |  |  |  |  |  |
| 7 | ☑ |  |  |  |  |  |  |  |  |  |
| 8 | ☑ |  |  |  |  |  |  |  |  |  |
| 9 | ☑ |  |  |  |  |  |  |  |  |  |
| 10 | ☑ |  |  |  |  |  |  |  |  |  |
| 11 | ☑ |  |  |  |  |  |  |  |  |  |
| 12 | ☑ |  |  |  |  |  |  |  |  |  |
| 13 | ☑ |  |  |  |  |  |  |  |  |  |
| 14 | ☑ |  |  |  |  |  |  |  |  |  |
| 15 | ☑ |  |  |  |  |  |  |  |  |  |
| 16 | ☑ |  |  |  |  |  |  |  |  |  |
| 17 | ☑ |  |  |  |  |  |  |  |  |  |
| 18 | ☑ |  |  |  |  |  |  |  |  |  |
| 19 | ☑ |  |  |  |  |  |  |  |  |  |
| 20 | ☑ |  |  |  |  |  |  |  |  |  |

|  | Enabled | Port | Type | Clock Edge | Value (ns) | Route (ns) | Comment |
|---|---|---|---|---|---|---|---|
| 1 | □ | <input default> | input_delay |  |  |  |  |
| 2 | □ | <output default> | output_delay |  |  |  |  |
| 3 | □ | AEn | output_delay |  |  |  |  |
| 4 | □ | AFn | output_delay |  |  |  |  |
| 5 | □ | EFn | output_delay |  |  |  |  |
| 6 | □ | FFn | output_delay |  |  |  |  |
| 7 | □ | FIFO_DATA[7:0] | output_delay |  |  |  |  |
| 8 | □ | FIFO_DI[7:0] | input_delay |  |  |  |  |
| 9 | □ | FIFO_DO[7:0] | output_delay |  |  |  |  |
| 10 | ☑ | RDn | input_delay |  | 2.00 |  |  |
| 11 | □ | RDOn | output_delay |  |  |  |  |
| 12 | □ | RESETn | input_delay |  |  |  |  |
| 13 | ☑ | WRn | input_delay |  | 2.00 |  |  |
| 14 | □ | WROn | output_delay |  |  |  |  |
| 15 | ☑ |  |  |  |  |  |  |
| 16 | ☑ |  |  |  |  |  |  |
| 17 | ☑ |  |  |  |  |  |  |
| 18 | ☑ |  |  |  |  |  |  |
| 19 | ☑ |  |  |  |  |  |  |
| 20 | ☑ |  |  |  |  |  |  |

- Constraint Editor supports a Drag and Drop interface.
- There are sheets for entering:
  - **Clock Frequency or Period**
  - **Clock to Clock timing**
  - **Input/Output Constraints**
  - **Registers Constraints**
  - **Multi-Cycle Paths**
  - **False Paths**
  - **Attributes**

# Constraint Editor (Cont.)



Synplify - [FifoDemo.sdc (constraint File )]

File Edit View Project Run HDL Analyst Format Options Window Help
Clocks
Inputs/Outputs
Registers
Mult
FifoDemo_s...
FifoDemo.sdc

| | Enabled | Register |
|---|---|---|
| 1 | ☑ | |
| 2 | ☑ | |
| 3 | ☑ | |
| 4 | ☑ | |
| 5 | ☑ | |
| 6 | ☑ | |
| 7 | ☑ | |
| 8 | ☑ | |
| 9 | ☑ | |
| 10 | ☑ | |
| 11 | ☑ | |
| 12 | ☑ | |
| 13 | ☑ | |
| 14 | ☑ | |
| 15 | ☑ | |
| 16 | ☑ | |
| 17 | ☑ | |
| 18 | ☑ | |
| 19 | ☑ | |
| 20 | ☑ | |

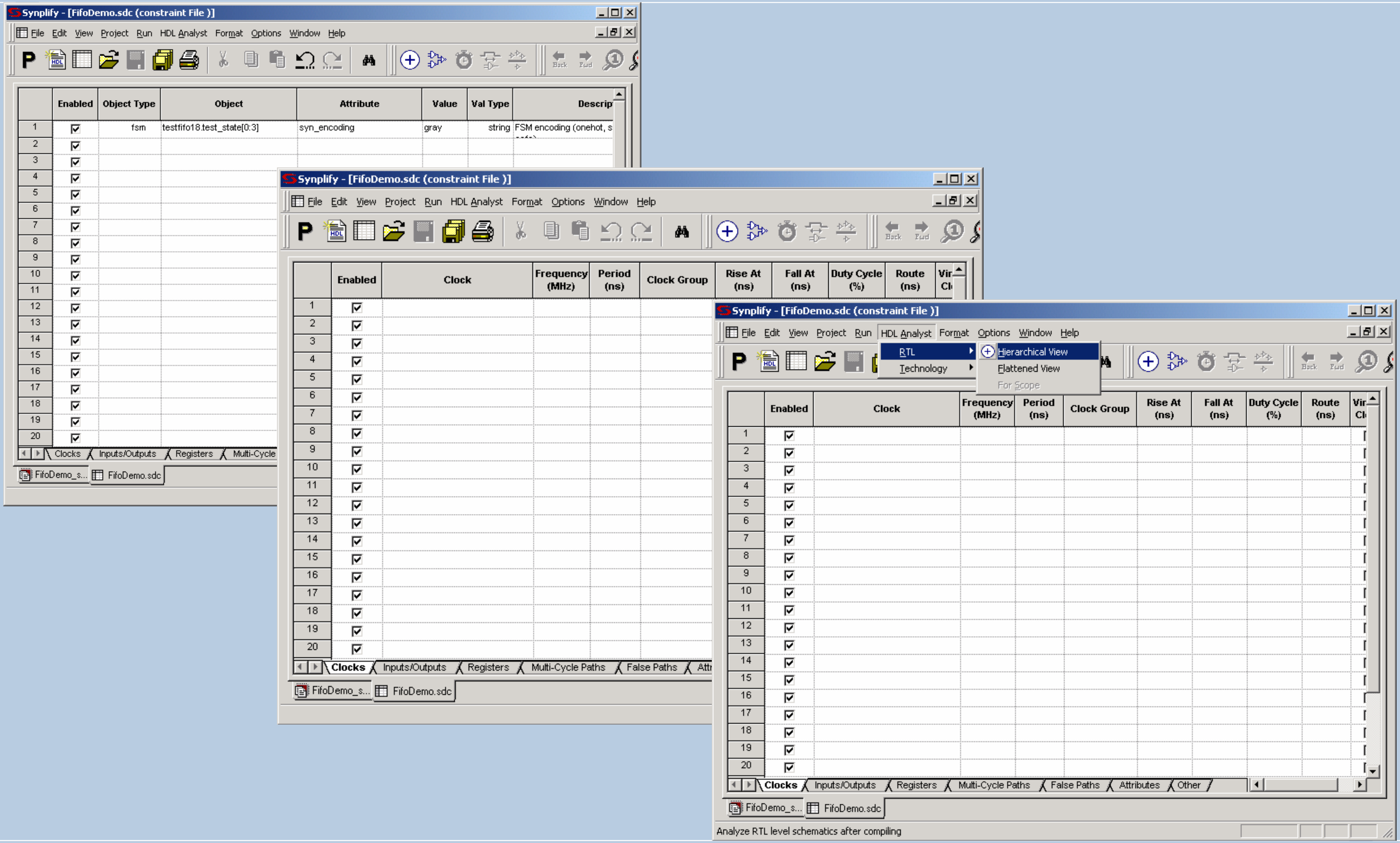
Synplify - [FifoDemo.sdc (constraint File )]

| | Enabled | From | To | Through | Cycles | Comment |
|---|---|---|---|---|---|---|
| 1 | ☑ | | | | | |
| 2 | ☑ | | | | | |
| 3 | ☑ | | | | | |
| 4 | ☑ | | | | | |
| 5 | ☑ | | | | | |
| 6 | ☑ | | | | | |
| 7 | ☑ | | | | | |
| 8 | ☑ | | | | | |
| 9 | ☑ | | | | | |
| 10 | ☑ | | | | | |
| 11 | ☑ | | | | | |
| 12 | ☑ | | | | | |
| 13 | ☑ | | | | | |
| 14 | ☑ | | | | | |
| 15 | ☑ | | | | | |
| 16 | ☑ | | | | | |
| 17 | ☑ | | | | | |
| 18 | ☑ | | | | | |
| 19 | ☑ | | | | | |
| 20 | ☑ | | | | | |

Synplify - [FifoDemo.sdc (constraint File )]

| | Enabled | From | To | Through | Comment |
|---|---|---|---|---|---|
| 1 | ☑ | | | | |
| 2 | ☑ | | | | |
| 3 | ☑ | | | | |
| 4 | ☑ | | | | |
| 5 | ☑ | | | | |
| 6 | ☑ | | | | |
| 7 | ☑ | | | | |
| 8 | ☑ | | | | |
| 9 | ☑ | | | | |
| 10 | ☑ | | | | |
| 11 | ☑ | | | | |
| 12 | ☑ | | | | |
| 13 | ☑ | | | | |
| 14 | ☑ | | | | |
| 15 | ☑ | | | | |
| 16 | ☑ | | | | |
| 17 | ☑ | | | | |
| 18 | ☑ | | | | |
| 19 | ☑ | | | | |
| 20 | ☑ | | | | |

# Constraint Editor (Cont.)


Synplify - [FifoDemo.sdc (constraint File )]
File Edit View Project Run HDL Analyst Format Options Window Help
Back Fwd
Clocks Inputs/Outputs Registers Multi-Cycle Paths False Paths Attributes Other
FifoDemo_s... FifoDemo.sdc
RTL
Technology
Hierarchical View
Flattened View
For Scope

Synplify - [FifoDemo.sdc (constraint File )]

| | Enabled | Object Type | Object | Attribute | Value | Val Type | Descrip |
|---|---|---|---|---|---|---|---|
| 1 | ☑ | fsm | testfifo18.test_state[0:3] | syn_encoding | gray | string | FSM encoding (onehot, s |
| 2 | ☑ | | | | | | |
| 3 | ☑ | | | | | | |
| 4 | ☑ | | | | | | |
| 5 | ☑ | | | | | | |
| 6 | ☑ | | | | | | |
| 7 | ☑ | | | | | | |
| 8 | ☑ | | | | | | |
| 9 | ☑ | | | | | | |
| 10 | ☑ | | | | | | |
| 11 | ☑ | | | | | | |
| 12 | ☑ | | | | | | |
| 13 | ☑ | | | | | | |
| 14 | ☑ | | | | | | |
| 15 | ☑ | | | | | | |
| 16 | ☑ | | | | | | |
| 17 | ☑ | | | | | | |
| 18 | ☑ | | | | | | |
| 19 | ☑ | | | | | | |
| 20 | ☑ | | | | | | |

Synplify - [FifoDemo.sdc (constraint File )]

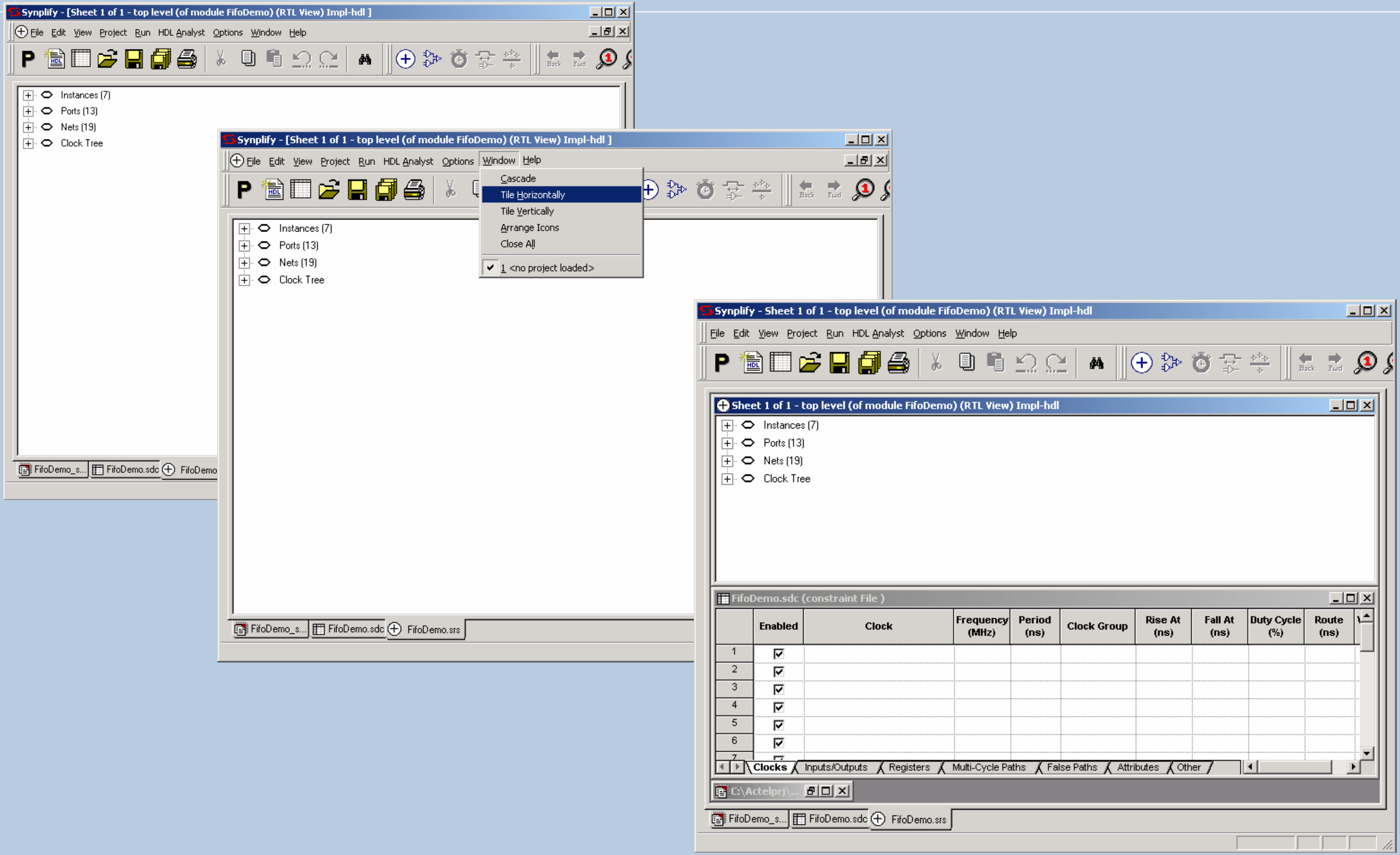
| | Enabled | Clock | Frequency (MHz) | Period (ns) | Clock Group | Rise At (ns) | Fall At (ns) | Duty Cycle (%) | Route (ns) | Vir Cl |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ☑ | | | | | | | | | |
| 2 | ☑ | | | | | | | | | |
| 3 | ☑ | | | | | | | | | |
| 4 | ☑ | | | | | | | | | |
| 5 | ☑ | | | | | | | | | |
| 6 | ☑ | | | | | | | | | |
| 7 | ☑ | | | | | | | | | |
| 8 | ☑ | | | | | | | | | |
| 9 | ☑ | | | | | | | | | |
| 10 | ☑ | | | | | | | | | |
| 11 | ☑ | | | | | | | | | |
| 12 | ☑ | | | | | | | | | |
| 13 | ☑ | | | | | | | | | |
| 14 | ☑ | | | | | | | | | |
| 15 | ☑ | | | | | | | | | |
| 16 | ☑ | | | | | | | | | |
| 17 | ☑ | | | | | | | | | |
| 18 | ☑ | | | | | | | | | |
| 19 | ☑ | | | | | | | | | |
| 20 | ☑ | | | | | | | | | |

Synplify - [FifoDemo.sdc (constraint File )]

| | Enabled | Clock | Frequency (MHz) | Period (ns) | Clock Group | Rise At (ns) | Fall At (ns) | Duty Cycle (%) | Route (ns) | Vir Cl |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ☑ | | | | | | | | | |
| 2 | ☑ | | | | | | | | | |
| 3 | ☑ | | | | | | | | | |
| 4 | ☑ | | | | | | | | | |
| 5 | ☑ | | | | | | | | | |
| 6 | ☑ | | | | | | | | | |
| 7 | ☑ | | | | | | | | | |
| 8 | ☑ | | | | | | | | | |
| 9 | ☑ | | | | | | | | | |
| 10 | ☑ | | | | | | | | | |
| 11 | ☑ | | | | | | | | | |
| 12 | ☑ | | | | | | | | | |
| 13 | ☑ | | | | | | | | | |
| 14 | ☑ | | | | | | | | | |
| 15 | ☑ | | | | | | | | | |
| 16 | ☑ | | | | | | | | | |
| 17 | ☑ | | | | | | | | | |
| 18 | ☑ | | | | | | | | | |
| 19 | ☑ | | | | | | | | | |
| 20 | ☑ | | | | | | | | | |

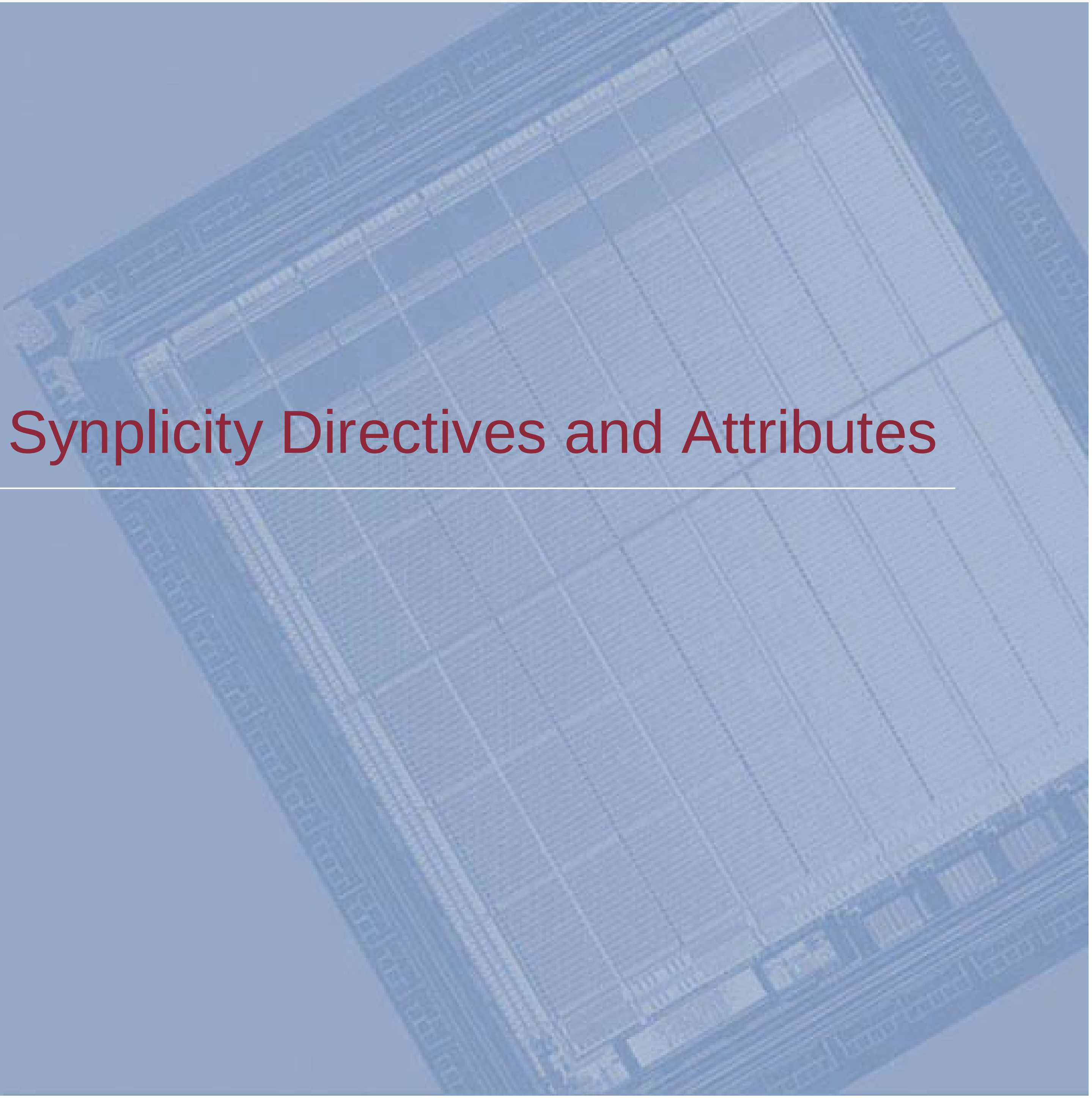
Analyze RTL level schematics after compiling

# Constraint Editor (Cont.)



Synplify - [Sheet 1 of 1 - top level (of module FifoDemo) (RTL View) Impl-hdl ]
File Edit View Project Run HDL Analyst Options Window Help
Instances (7)
Ports (13)
Nets (19)
Clock Tree
FifoDemo_s...
FifoDemo.sdc
FifoDemo
Cascade
Tile Horizontally
Tile Vertically
Arrange Icons
Close All
1 <no project loaded>
FifoDemo.srs
Synplify - Sheet 1 of 1 - top level (of module FifoDemo) (RTL View) Impl-hdl
Sheet 1 of 1 - top level (of module FifoDemo) (RTL View) Impl-hdl
FifoDemo.sdc (constraint File )
Clocks
Inputs/Outputs
Registers
Multi-Cycle Paths
False Paths
Attributes
Other
C:\Actelprj\...

| | Enabled | Clock | Frequency (MHz) | Period (ns) | Clock Group | Rise At (ns) | Fall At (ns) | Duty Cycle (%) | Route (ns) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | ☑ | | | | | | | | |
| 2 | ☑ | | | | | | | | |
| 3 | ☑ | | | | | | | | |
| 4 | ☑ | | | | | | | | |
| 5 | ☑ | | | | | | | | |
| 6 | ☑ | | | | | | | | |



# Synplicity Directives and Attributes

# Synplicity Directives and Attributes

- Let You Direct Analysis, Optimization, and Mapping of Design during Synthesis
- Attributes Control *Mapping* Optimizations
  - **Attributes Can Be Entered in either .sdc Constraint File or HDL Source Code**
    - **Synplify Supports Limited Number of Attributes that Can Be Entered in Attribute Pane of the SCOPE Editor**
    - ***Most* Attributes Are Entered in your VHDL or Verilog Code**
- Directives Control *Compiler* Optimizations
  - **Directives *Must* Be Entered in HDL Source Code**

# `alspreserve`
*Actel-Specific Attribute*

- Keeps Net from Being Collapsed in Designer (Back-end) Tools
  - **Must also Add `syn_keep` to Ensure Synplicity Retains Net**
  - **Synplicity Adds `alspreserve` Attribute to EDIF Netlist**

# alspreserve
## *Syntax*

- Verilog Syntax

```
object /* synthesis alspreserve = 1 */ ;
```

  - Example:

```
module foo ( in, out);
  input [6:0] in;   output   out;   wire     out;
  wire      or_out1    /* synthesis syn_keep=1 alspreserve=1 */;
  wire      and_out1;    wire      and_out2;
  wire      and_out3  /* synthesis syn_keep=1 alspreserve=1 */;
```

- VHDL Syntax

```
attribute alspreserve of object : signal is true ;
```

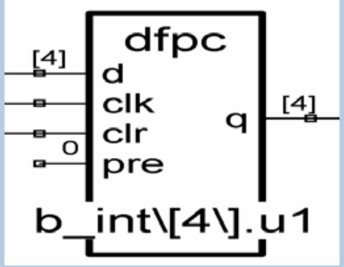
  - Example:

```
architecture comb of foo is
    signal and_out1, and_out2, and_out3, or_out1 : std_logic;

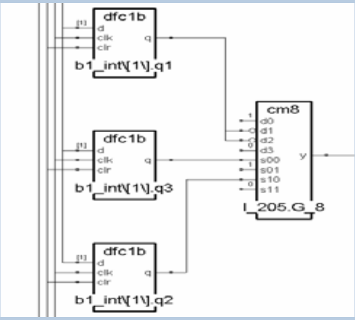
    attribute syn_keep of and_out3 : signal is true;
    attribute syn_keep of or_out1  : signal is true;
    attribute alspreserve: boolean;
    attribute alspreserve of and_out3 :signal is true;
    attribute alspreserve of or_out1 : signal is true;
```

# syn_radhardlevel
## *Actel Antifuse FPGA Specific Attribute*

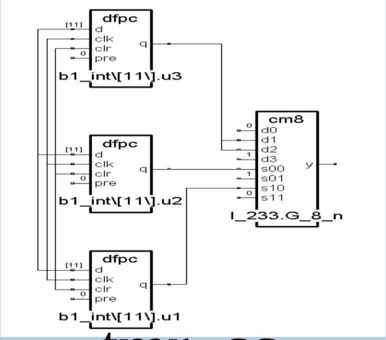
- Sets Register Model for Module, Architecture or Registers
- Often Used for Radiation-Hardened Designs
- **`syn_radhardlevel <string value>`**
  - **`cc` - Use Combinational Cells to Implement Storage Elements**
  - **`tmr` - Use Triple-Module Redundancy to Implement Registers**
  - **`tmr_cc` - Use Triple-Module Redundancy where Storage Element Is Composed of Combinational Cells**
  - **none - Use Standard Registers**



cc



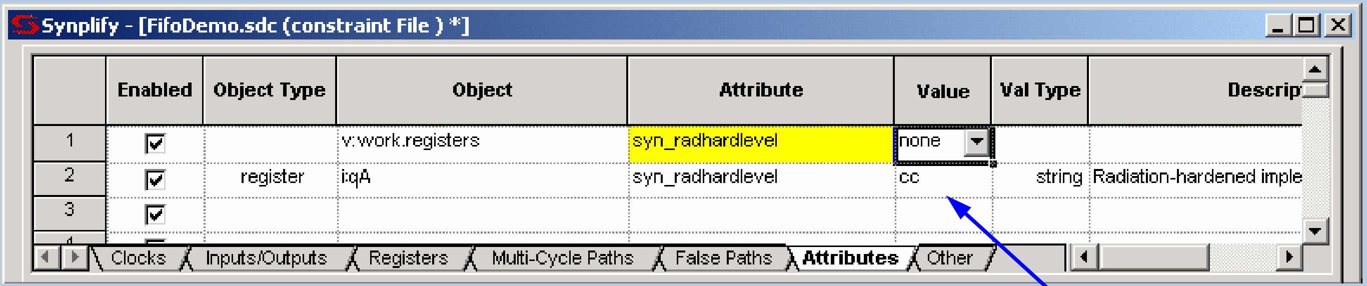
tmr



tmr_cc

# syn_radhardlevel
*Example (cont.)*

SCOPE attribute tab:

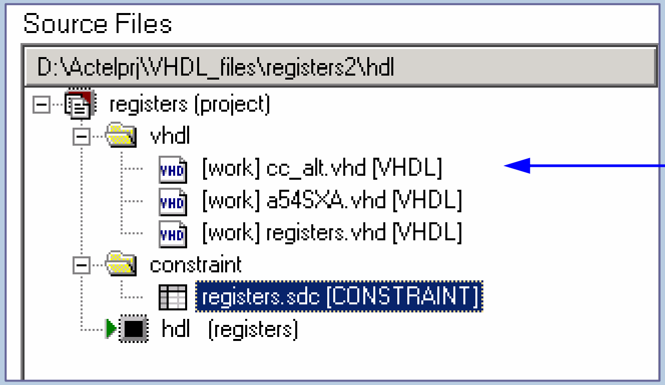


Synplify - [FifoDemo.sdc (constraint File ) *]

| | Enabled | Object Type | Object | Attribute | Value | Val Type | Descrip |
|---|---|---|---|---|---|---|---|
| 1 | ☑ | | v:work.registers | syn_radhardlevel | none | | |
| 2 | ☑ | register | i:qA | syn_radhardlevel | cc | string | Radiation-hardened imple |
| 3 | ☑ | | | | | | |

use C-module flip-flop for qA

Source files:

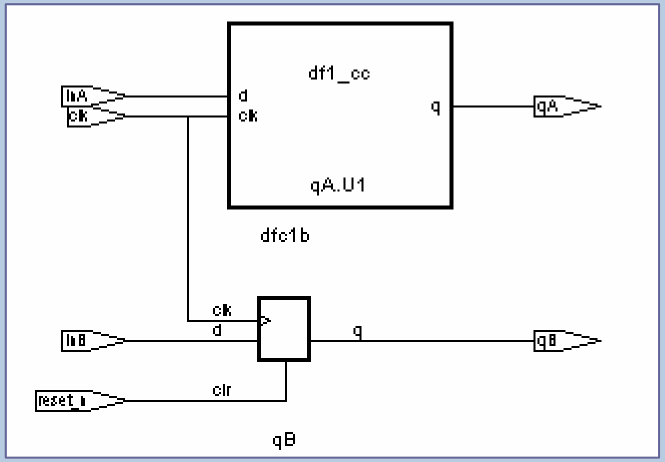


Source Files

D:\Actelprj\VHDL_files\registers2\hdl

registers (project)<br>
vhdl<br>
[work] cc_alt.vhd [VHDL]<br>
[work] a54SXA.vhd [VHDL]<br>
[work] registers.vhd [VHDL]<br>
constraint<br>
registers.sdc [CONSTRAINT]<br>
hdl (registers)

Add to infer C-module flip-flops



# syn_encoding
*Attribute*

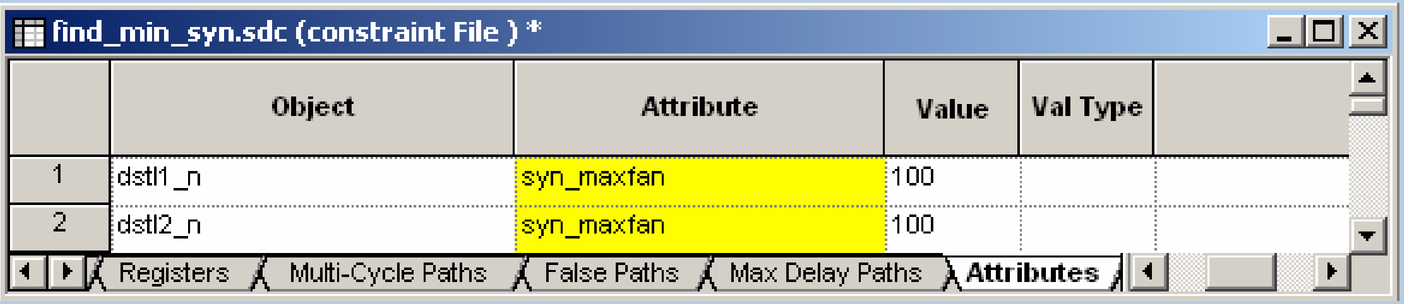
- Sets Encoding Style for State Machines
  - Overrides Default Style
- Default Style - Compiler Selects Encoding Style Based on Number of States as Follows:
  - 1 - 4 States: Sequential
  - 5 - 24 States: One-hot
  - > 24 States: Gray
- syn_encoding Can Have the Following Values:
  - onehot
  - gray
  - sequential
  - safe

# `syn_maxfan`
## *Attribute*

- Controls Maximum Fanout of Instance, Net, or Port
- Limit Specified by this Attribute May Be Treated as Hard or Soft Depending on Where It Was Specified
  - **Soft Limit May Not Be Honored if it Degrades Performance**
- You Can Apply **`syn_maxfan`** Attribute to Module, Register, Instance, Port, or Net
  - **For ProASIC and APA Designs Only – You Can also Apply to Module or Entity**

# syn_maxfan
*Usage*

- SCOPE Constraint Editor Usage



find_min_syn.sdc (constraint File ) *

| | Object | Attribute | Value | Val Type |
|---|---|---|---|---|
| 1 | dstl1_n | syn_maxfan | 100 | |
| 2 | dstl2_n | syn_maxfan | 100 | |

- SDC File Syntax

```
define_attribute { object } syn_maxfan { integer }
```

- **Example – Limit Fanout for Signal `clk` to 200:**

```
. . .
define_attribute {clk} syn_maxfan {200}
. . .
```

# syn_maxfan
*Syntax*

## Verilog Syntax

```
object /* synthesis syn_maxfan = "value" */ ;
```

- **Example:**

```
module test (registered_data_out, clock, reset, data_in);
output [31:0] registered_data_out;  input clock, reset;
input [31:0] data_in;
input reset /* synthesis syn_maxfan=1000 */;
// Other code
```

## VHDL Syntax

```
attribute syn_maxfan of object : object_type is "value" ;
```

- **Example:**

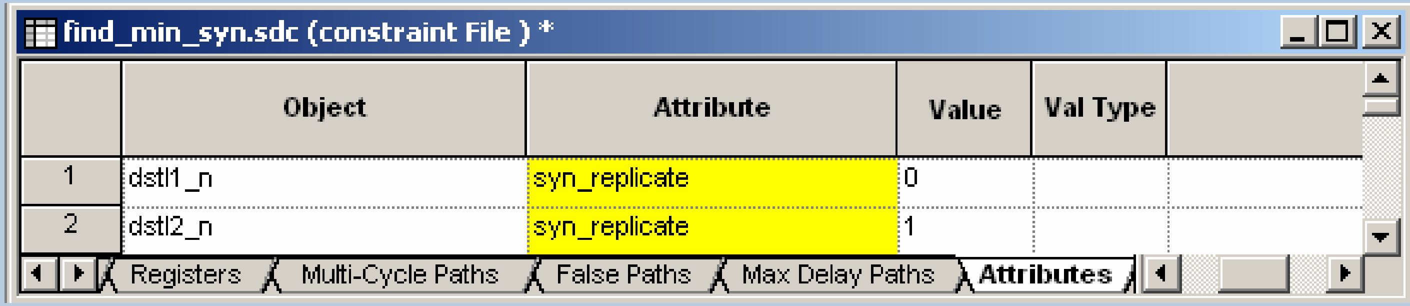
```
entity test is
        port(clock, reset : in bit;
             data_in : in bit_vector(31 downto 0);
             registered_data_out: out bit_vector(31 downto 0))
attribute syn_maxfan : integer;
attribute syn_maxfan of reset : signal is 1000;
-- Other code
```

# `syn_replicate` *Attribute*

- Prevents Replication of Register
  - **`assign syn_replicate = 0` Turns Off Register Replication**
  - **Cannot Force Tool to Replicate**
  - **Works along with `max_fanout` Value**
  - **Only Supported on Individual Register**
- When Will Synplify Replicate or Buffer?
  - **Generally Flip-flops Are Replicated to Achieve Fan-out Control**
  - **For Combinatorial Cells, Buffers Are Added**

# syn_replicate
*Usage*

## SCOPE Constraint Editor Usage



find_min_syn.sdc (constraint File ) *

|  | Object | Attribute | Value | Val Type |
|---|---|---|---|---|
| 1 | dstl1_n | syn_replicate | 0 |  |
| 2 | dstl2_n | syn_replicate | 1 |  |

## SDC File Syntax

1 enables replication
0 disables replication

```
define_global_attribute syn_replicate = { 1 | 0 }
```

**Example - Disables All Replication in Design:**

```
. . .
define_global_attribute syn_replicate {0}
. . .
```

# syn_replicate
## *Usage (cont.)*

0 disables replication

- Verilog Syntax

```
object /* synthesis syn_replicate = 1 | 0 */;
```

- **Example:**

```
module norep (Reset, Clk, Drive, OK, ADPad, IPad, ADOut);

 .   .   .
reg [31:0] IPad;
reg DriveA /* synthesis syn_replicate = 0 */;
assign ADPad = DriveA ? ADOut : 32'bz;
always @(posedge Clk or negedge Reset)
        if (!Reset) begin
           DriveA <= 0;
           IPad   <= 0;  end
        else        begin
           DriveA <= Drive & OK;
           IPad   <= ADPad;  end
endmodule
```

# syn_replicate

*Usage (cont.)*

## ■ VHDL Syntax

false disables replication

```
attribute syn_replicate of object : object_type is
   true | false ;
```

- **Example:**

```
entity norep is port (
                 Reset : in std_logic;
                 Clk : in std_logic;
                 Drive : in std_logic;
                 OK : in std_logic;
                 ADPad : inout std_logic_vector (31 downto 0);
                 IPad : out std_logic_vector (31 downto 0);
                 ADOut : in std_logic_vector (31 downto 0));
end norep;
architecture archnorep of norep is
signal DriveA : std_logic;
attribute syn_replicate : boolean;
attribute syn_replicate of DriveA : signal is false;

begin

-- Other code
```

# `syn_sharing`
*Directive*

- Enables/Disables Resource Sharing of Operators inside Module during Synthesis
  - **By Default, Directive Is *Enabled* (Value 1 for Verilog, true for VHDL).**
  - **If Resource Sharing Check Box in Project View is Disabled, You Can Still Enable Resource Sharing Using `syn_sharing` Directive**

# syn_sharing

*Usage*

## Verilog Syntax

```
object /* synthesis syn_sharing = 1 | 0 */ ;
```

- **Example:**

```
module my_design(out,in,clk_in) /* synthesis syn_sharing=0 */;


// Other code
```

## VHDL Syntax

```
attribute syn_sharing of object : object_type is " true | false";
```

object can be architecture name

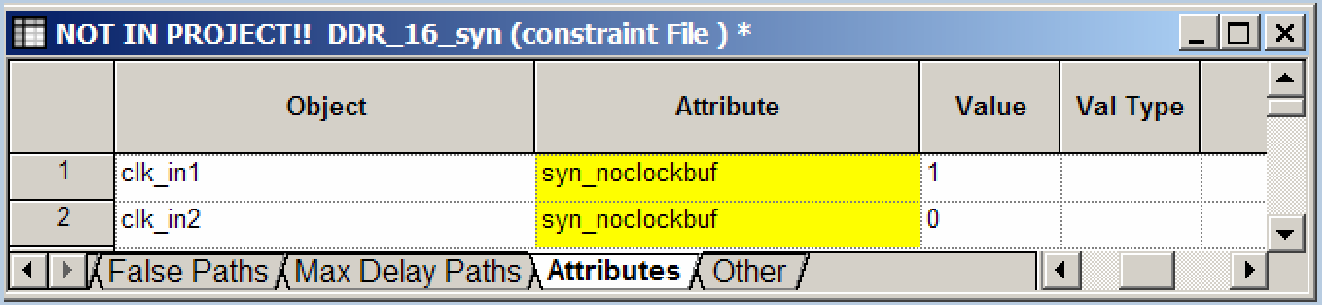
- **Example:**

```
entity alu is
        port ( a, b : in std_logic_vector (7 downto 0);
               . . . );
end alu;
architecture behave of alu is
--  Turn on resource sharing for the architecture.
attribute syn_sharing of behave : architecture is "true";
begin
-- Other code
```

# syn_noclockbuf
## *Synthesis Attribute*

- Selects/Deselects Automatic Clock Buffering
  - **Value of '1' (or Boolean TRUE) Turns OFF Automatic Clock Buffering**
  - **You Can Apply syn_noclockbuf Attribute to Module, Register, Instance, Port, or Net**

- Synplicity SCOPE Constraint Editor Usage



NOT IN PROJECT!! DDR_16_syn (constraint File ) *

| | Object | Attribute | Value | Val Type |
|---|---|---|---|---|
| 1 | clk_in1 | syn_noclockbuf | 1 | |
| 2 | clk_in2 | syn_noclockbuf | 0 | |

# syn_noclockbuf
*Attribute Usage (cont.)*

## Verilog Syntax

```
object /* synthesis syn_noclockbuf = "value" */ ;
```

- **Example:**

```
module test (registered_data_out, clock, reset, data_in);
output [31:0] registered_data_out;  input clock;
input [31:0] data_in;
input reset /* synthesis syn_noclockbuf=1 */;
// Other code
```

## VHDL Syntax

```
attribute syn_noclockbuf of object : object_type is "value" ;
```

- **Example:**

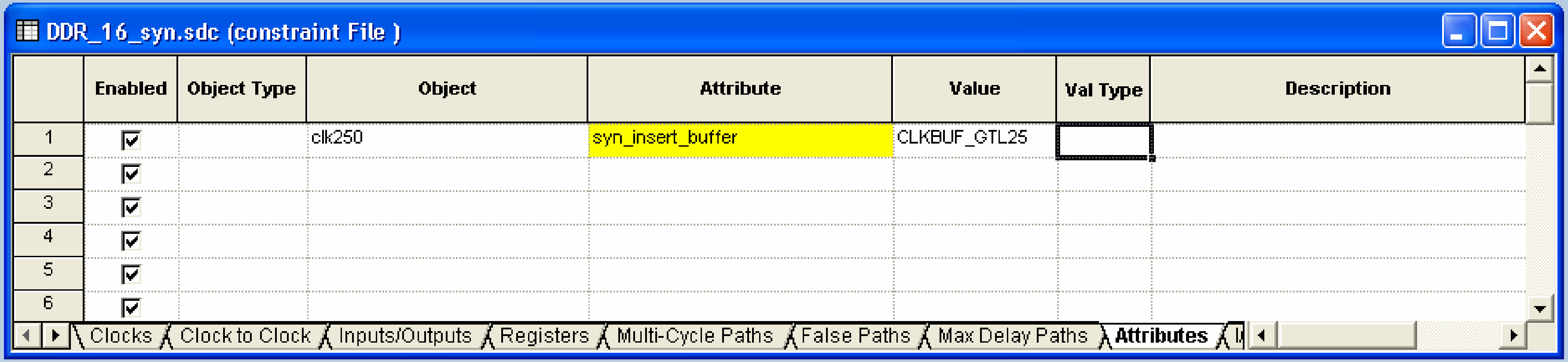
```
entity test is
        port(clock, reset : in bit;
             data_in : in bit_vector(31 downto 0);
             registered_data_out: out bit_vector(31 downto 0))
attribute syn_noclockbuf : boolean;
attribute syn_noclockbuf of reset : signal is true;
-- Other code
```

# `syn_insert_buffer`
## *Synthesis Attribute*

## Directs Synplify To Infer Specific Pads

- **No Instantiation Required**
- **Simple To Use: SCOPE, VHDL Or Verilog**
- **Can Operate On Top Level INPUT Ports Only**
- **Can Infer All INPUT And Global PADS**
- **Not Documented in Help, SCOPE Menu Drop Down**

## Synplicity SCOPE Constraint Editor Usage



DDR_16_syn.sdc (constraint File )

| | Enabled | Object Type | Object | Attribute | Value | Val Type | Description |
|---|---|---|---|---|---|---|---|
| 1 | ☑ | | clk250 | syn_insert_buffer | CLKBUF_GTL25 | | |
| 2 | ☑ | | | | | | |
| 3 | ☑ | | | | | | |
| 4 | ☑ | | | | | | |
| 5 | ☑ | | | | | | |
| 6 | ☑ | | | | | | |

# syn_insert_buffer
*Attribute Usage*

## Verilog Syntax

**object /* synthesis syn_insert_buffer = <name> */;**

- **Example:**

```
module design1 (clk250, . . .);
input clk250 /*synthesis syn_insert_buffer = “CLKBUF_GTL25”*/;
output . . .;
```

## VHDL Syntax

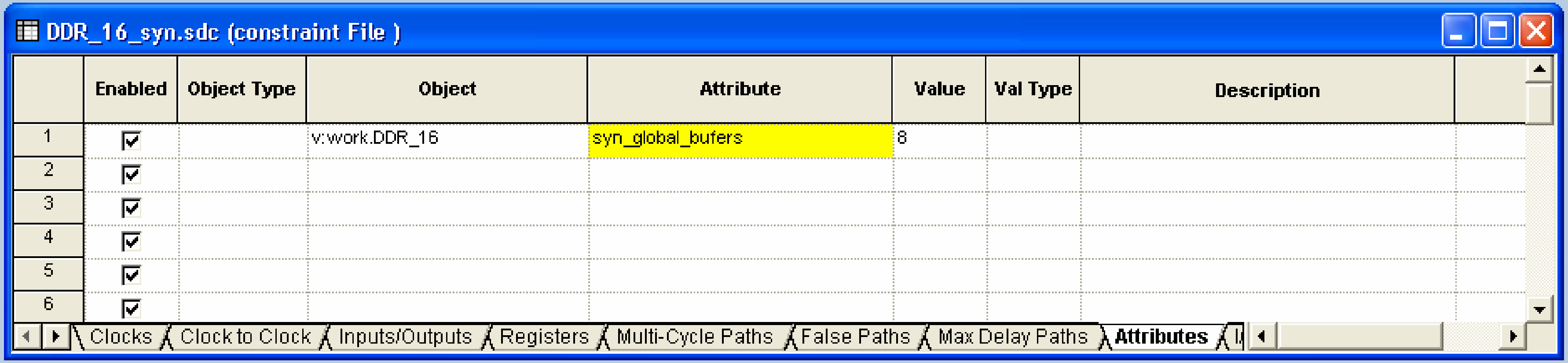
**attribute syn_insert_buffer of object : signal is <name>;**

- **Example:**

```
entity design1 is
port ( clk250:   in std_logic;
        . . .);
attribute syn_insert_buffer  : string;
attribute syn_insert_buffer  of clk250 : signal is "CLKBUF_GTL25";
end design1;
```

# syn_global_buffers
## *Synthesis Attribute (ProASIC3\E)*

- Specifies The Number Of Global Buffers To Be Used
  - **Use This Attribute To Restrict The Number Of Global Buffer Resources Used by Synplicity**
  - **Attribute Is Applied Globally On The Top-level Module Or Entity**
  - **Value Can Be Any Integer Between 6 And 18**
- Synplicity SCOPE Constraint Editor Usage



|  | Enabled | Object Type | Object | Attribute | Value | Val Type | Description |
|---|---|---|---|---|---|---|---|
| 1 | ☑ |  | v:work.DDR_16 | syn_global_bufers | 8 |  |  |
| 2 | ☑ |  |  |  |  |  |  |
| 3 | ☑ |  |  |  |  |  |  |
| 4 | ☑ |  |  |  |  |  |  |
| 5 | ☑ |  |  |  |  |  |  |
| 6 | ☑ |  |  |  |  |  |  |

# syn_global_buffers

*Attribute Usage*

## Verilog Syntax

**object /* synthesis syn_global_buffers = <maximum> */;**

- **Example:**

```
module top (clk1, clk2, clk3, clk4, clk5, clk6,
clk7,clk8,clk9,  clk10, clk11, clk12, clk13, clk14, clk15,
d1, d2, d3, d4, d5, q1, q2, reset)

/* synthesis syn_global_buffers = 10 */;
```

## VHDL Syntax

**attribute syn_global_buffers of object : object_type is <maximum>;**

- **Example:**

```
entity top is

   port(      . . .       );

end top;

 architecture behave of top is

attribute syn_global_buffers : integer;

attribute syn_global_buffers of behave : architecture is 10;
```

# Actel Attribute and Directive Summary

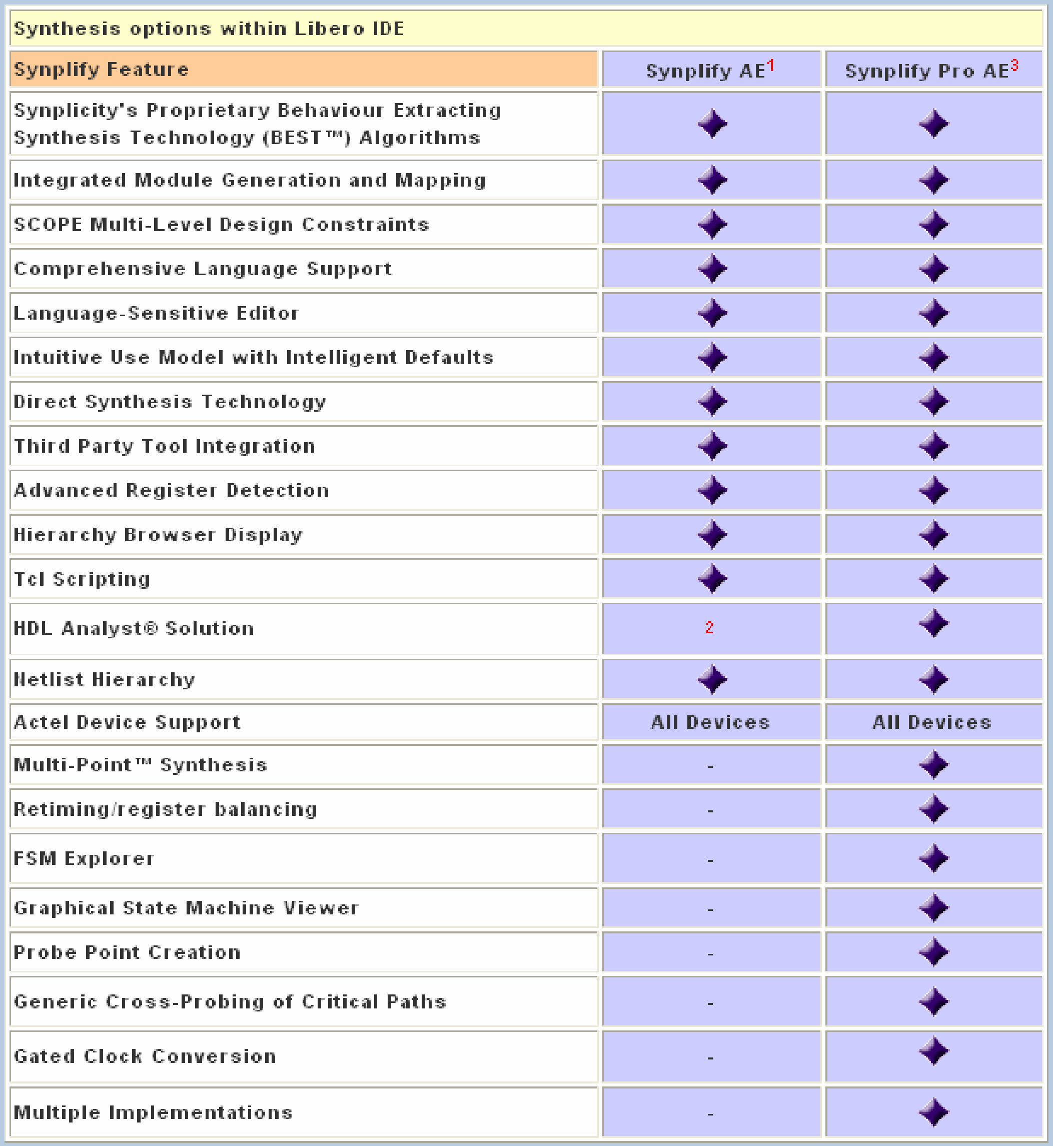
| NAME | TYPE | VALUE | DESCRIPTION |
|---|---|---|---|
| **alspreserve** | A | Boolean | Prevents a net from being removed during Place and Route |
| **syn_encoding** | A | sequential, onehot, gray, safe | Specifies encoding style for state machines |
| **syn_keep** | D | 1/0<br>true / false | Prevents an internal signal from being removed during synthesis and optimization |
| **syn_maxfan** | A | integer | Controls the maximum fanout or an instance, net or port |
| **syn_noclockbuf** | A | 1/0<br>true / false | Disables automatic insertion of clock buffers |
| **syn_radhardlevel** | A | string | Specifies register design technique to apply to a module, architecture or instance |
| **syn_replicate** | A | 1/0 | Disables register replication |
| **syn_sharing** | D | 1/0<br>true / false | Enables / disables the resource sharing operators insida a module during synthesis |
| **syn_insert_buffer** | A | 1/0<br>true / false | Directs Synplify to use specific I/O pads |
| **syn_global_buffers** | A | integer | Specifies the number of global buffers to be used in a ProASIC3\E design |

ONECHIP is all you need

# Synplify and Synplify PRO for Actel

- Synplify for Actel Is Equivalent to Synplicity's Synplify Product.
  - **Included in Libero Gold**
  - **Limited to Actel Products Only**
- Synplify Pro AE has Additional Features
  - **Included in Libero Platinum**
  - **Limited to Actel products only**

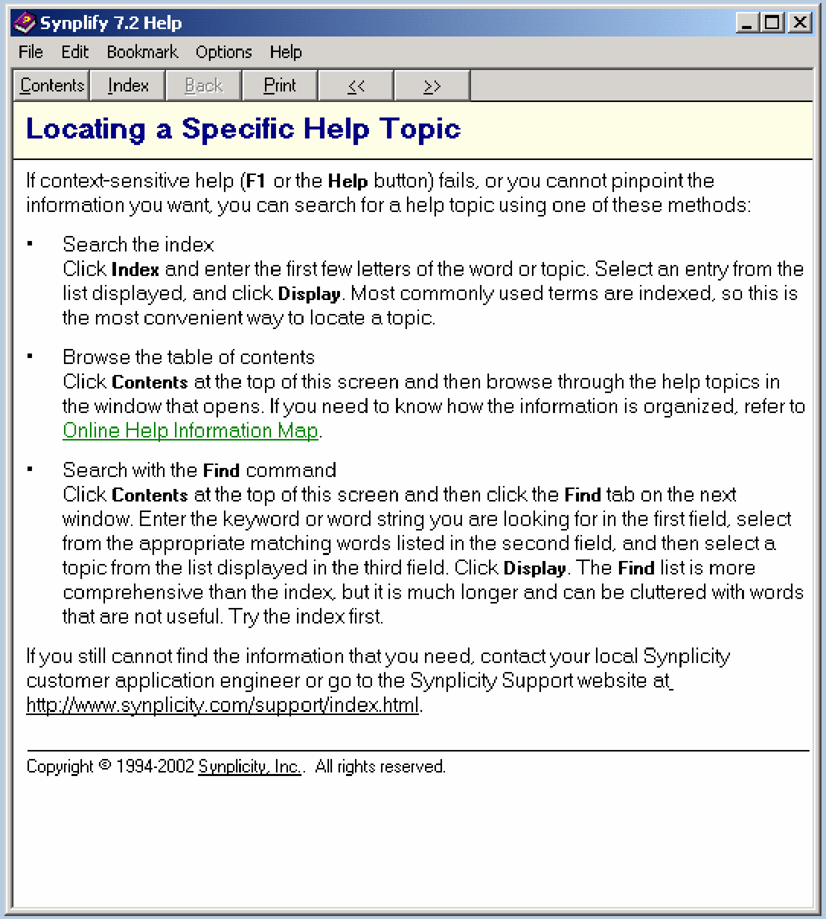
# Synplify® AE and Synplify Pro®
## *Features Comparison*



Synthesis options within Libero IDE

| Synplify Feature | Synplify AE[1] | Synplify Pro AE[3] |
|---|---|---|
| Synplicity's Proprietary Behaviour Extracting Synthesis Technology (BEST™) Algorithms | ◆ | ◆ |
| Integrated Module Generation and Mapping | ◆ | ◆ |
| SCOPE Multi-Level Design Constraints | ◆ | ◆ |
| Comprehensive Language Support | ◆ | ◆ |
| Language-Sensitive Editor | ◆ | ◆ |
| Intuitive Use Model with Intelligent Defaults | ◆ | ◆ |
| Direct Synthesis Technology | ◆ | ◆ |
| Third Party Tool Integration | ◆ | ◆ |
| Advanced Register Detection | ◆ | ◆ |
| Hierarchy Browser Display | ◆ | ◆ |
| Tcl Scripting | ◆ | ◆ |
| HDL Analyst® Solution | [2] | ◆ |
| Netlist Hierarchy | ◆ | ◆ |
| Actel Device Support | All Devices | All Devices |
| Multi-Point™ Synthesis | - | ◆ |
| Retiming/register balancing | - | ◆ |
| FSM Explorer | - | ◆ |
| Graphical State Machine Viewer | - | ◆ |
| Probe Point Creation | - | ◆ |
| Generic Cross-Probing of Critical Paths | - | ◆ |
| Gated Clock Conversion | - | ◆ |
| Multiple Implementations | - | ◆ |

# Synplicity Help


Synplify 7.2 Help
File Edit Bookmark Options Help
Contents Index Back Print << >>

## Locating a Specific Help Topic

If context-sensitive help (**F1** or the **Help** button) fails, or you cannot pinpoint the information you want, you can search for a help topic using one of these methods:

- Search the index
  Click **Index** and enter the first few letters of the word or topic. Select an entry from the list displayed, and click **Display**. Most commonly used terms are indexed, so this is the most convenient way to locate a topic.
- Browse the table of contents
  Click **Contents** at the top of this screen and then browse through the help topics in the window that opens. If you need to know how the information is organized, refer to Online Help Information Map.
- Search with the **Find** command
  Click **Contents** at the top of this screen and then click the **Find** tab on the next window. Enter the keyword or word string you are looking for in the first field, select from the appropriate matching words listed in the second field, and then select a topic from the list displayed in the third field. Click **Display**. The **Find** list is more comprehensive than the index, but it is much longer and can be cluttered with words that are not useful. Try the index first.

If you still cannot find the information that you need, contact your local Synplicity customer application engineer or go to the Synplicity Support website at http://www.synplicity.com/support/index.html.

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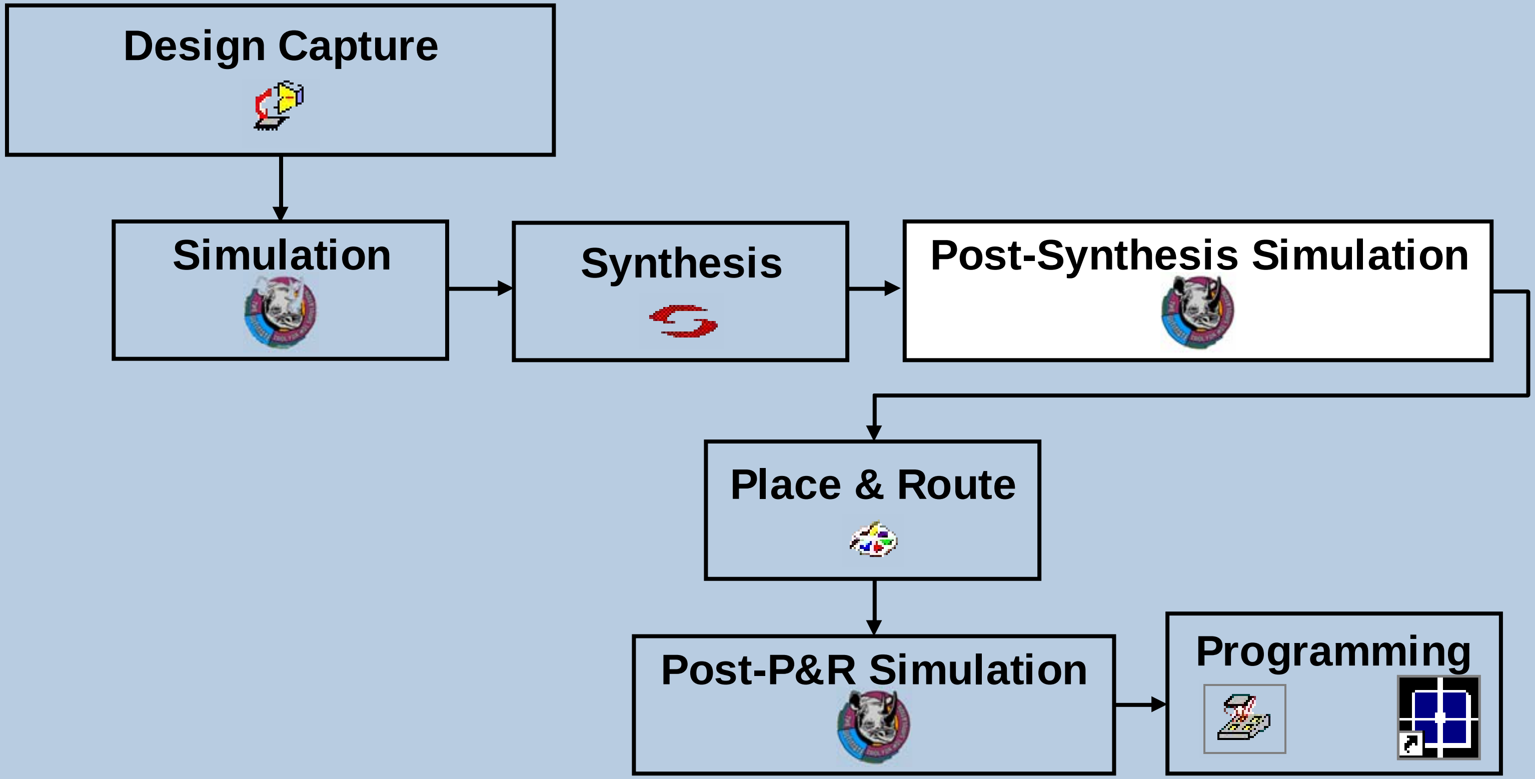
- Synplicity Has Complete On-line Manual
  - Invoked from Help Pulldown or by Pressing F1

# Post-Synthesis Simulation



Design Capture

Simulation

Synthesis

Post-Synthesis Simulation

Place & Route

Post-P&R Simulation

Programming

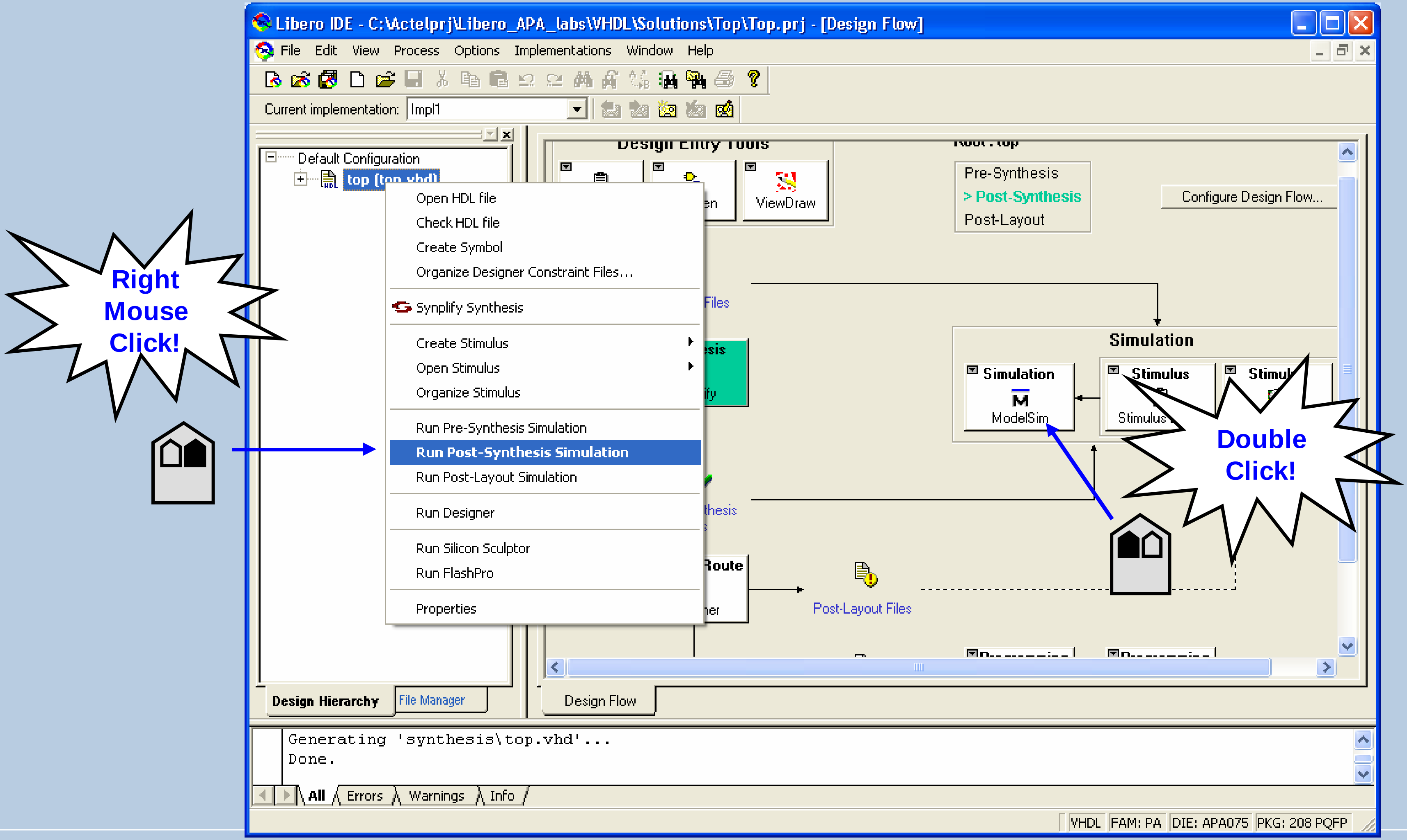
# Post-Synthesis Simulation

## Steps:

- Synthesize Design with Synplicity
  - Generate EDIF Netlist from Synplicity
  - Libero Automatically Creates Structural VHDL or Verilog Netlist
- Run Post-synthesis Simulation on Structural Netlist

# Post-Synthesis Simulation

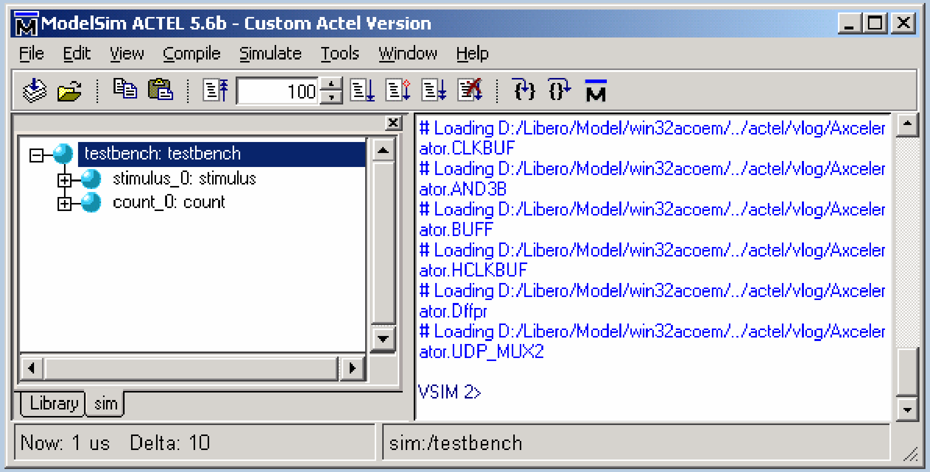
- Click on “Simulation” in Design Flow window or…



```
Generating 'synthesis\top.vhd'...
Done.
```

# Post-Synthesis Simulation

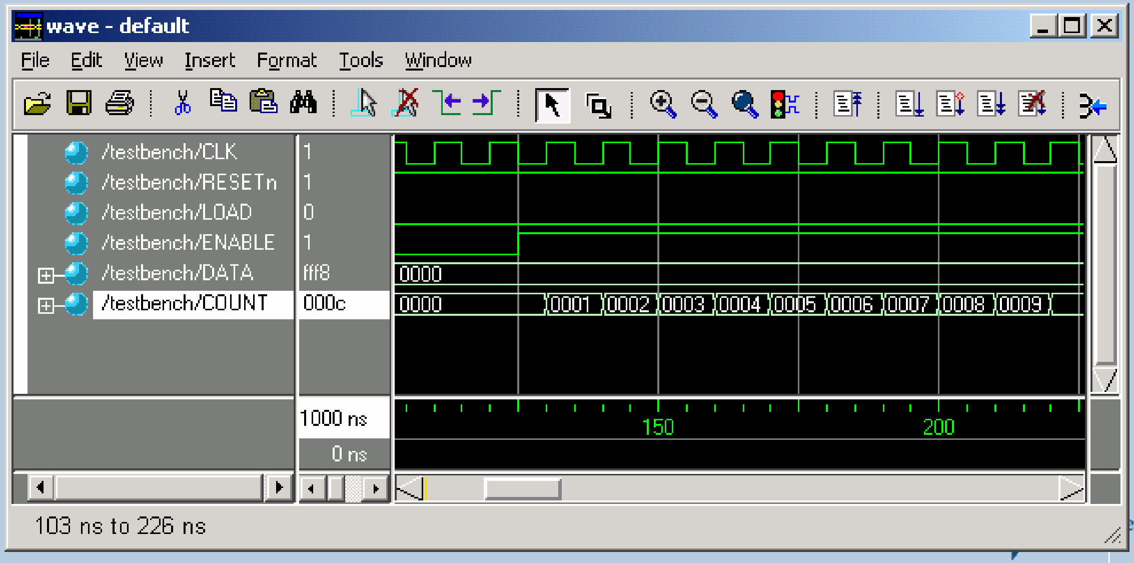
- ModelSim automatically compiles structural netlist exported from Designer
  - Runs simulation for 1 uS
  - Structural library mapping handled by Libero
  - Pre-compiled libraries do not require compiling prior to simulation


ModelSim ACTEL 5.6b - Custom Actel Version
File Edit View Compile Simulate Tools Window Help
100
testbench: testbench
stimulus_0: stimulus
count_0: count
Library
sim

```
# Loading D:/Libero/Model/win32acoem/../actel/vlog/Axcelerator.CLKBUF
# Loading D:/Libero/Model/win32acoem/../actel/vlog/Axcelerator.AND3B
# Loading D:/Libero/Model/win32acoem/../actel/vlog/Axcelerator.BUFF
# Loading D:/Libero/Model/win32acoem/../actel/vlog/Axcelerator.HCLKBUF
# Loading D:/Libero/Model/win32acoem/../actel/vlog/Axcelerator.Dffpr
# Loading D:/Libero/Model/win32acoem/../actel/vlog/Axcelerator.UDP_MUX2

VSIM 2>
```

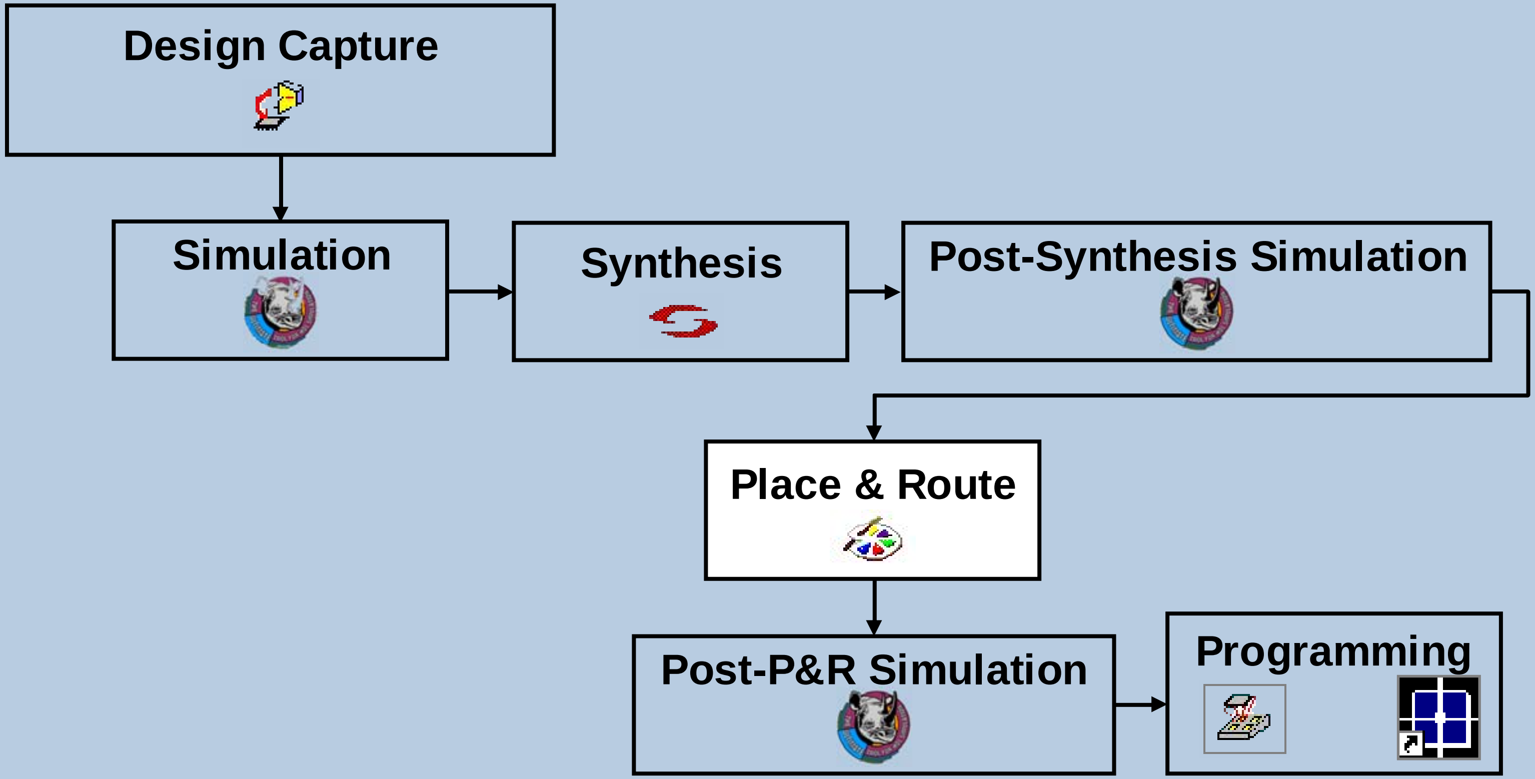
Now: 1 us Delta: 10 sim:/testbench



| | |
|---|---|
| /testbench/CLK | 1 |
| /testbench/RESETn | 1 |
| /testbench/LOAD | 0 |
| /testbench/ENABLE | 1 |
| /testbench/DATA | fff8 |
| /testbench/COUNT | 000c |

103 ns to 226 ns

# Place and Route



Design Capture

Simulation

Synthesis

Post-Synthesis Simulation

Place & Route

Post-P&R Simulation

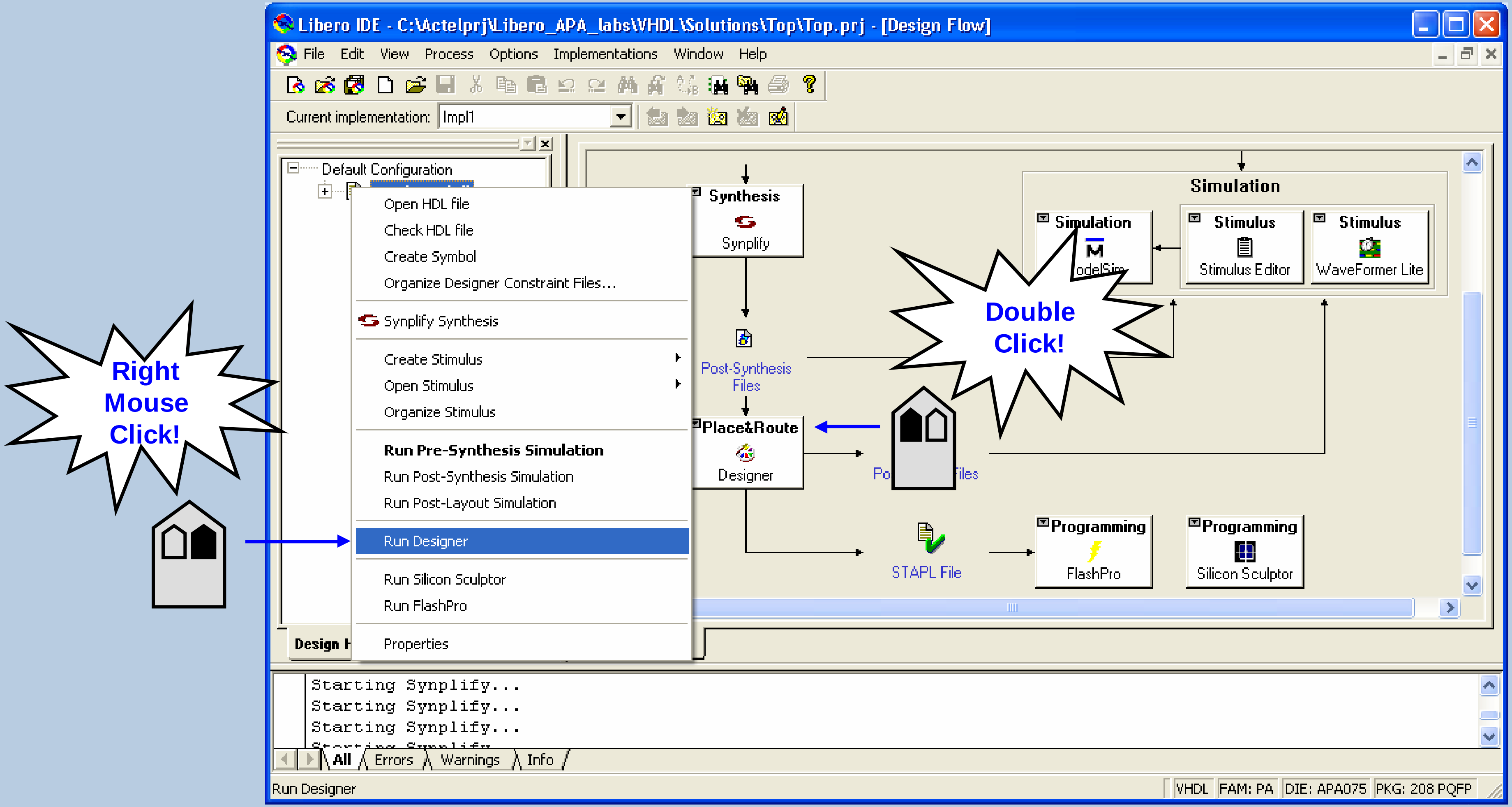
Programming

# Designer

Actel

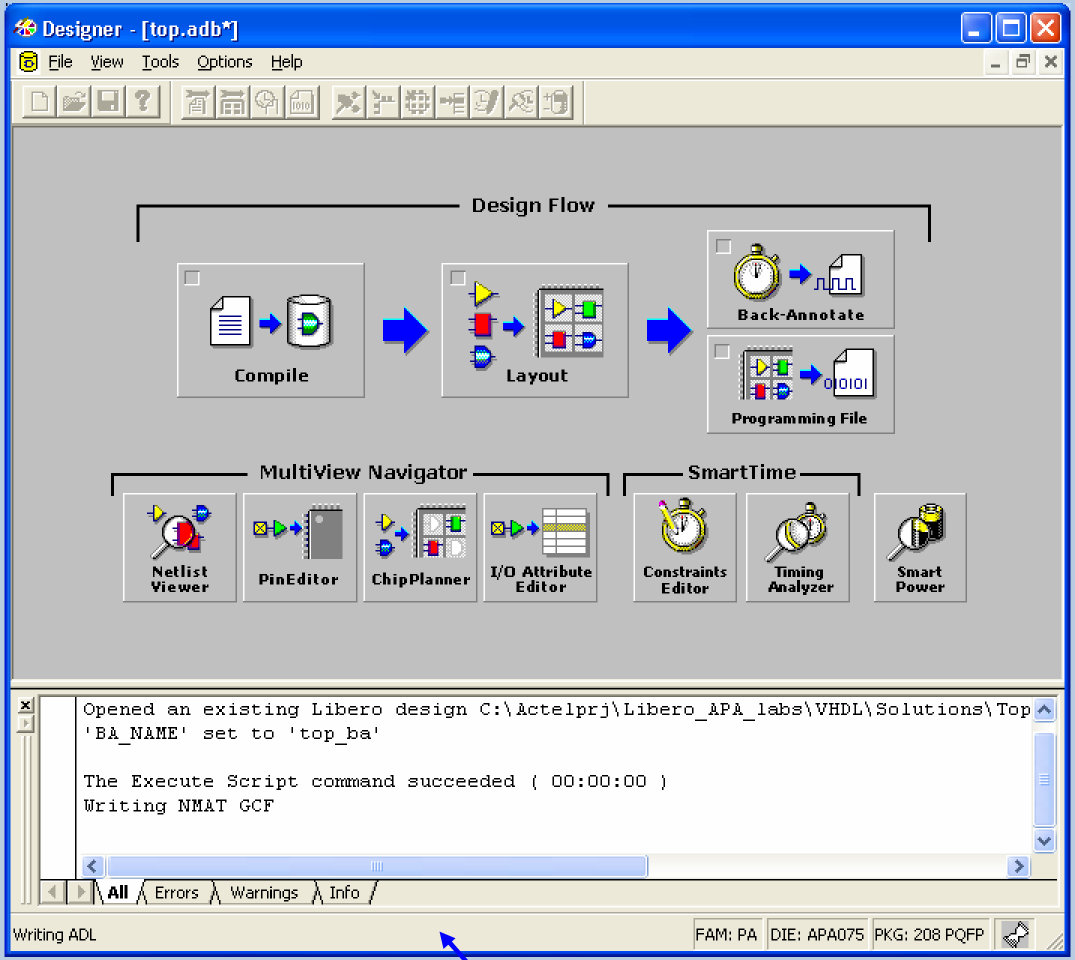
# Open Design for Place & Route

- Click on “Place & Route” in Design Flow Window or…



```
Starting Synplify...
Starting Synplify...
Starting Synplify...
```

# Designer Interface



```
Opened an existing Libero design C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top
'BA_NAME' set to 'top_ba'

The Execute Script command succeeded ( 00:00:00 )
Writing NMAT GCF
```

- Designer Provides Graphical Flow Manager to Lead Designer through Design Flow
- Completed Tasks Highlighted
- Design Flow Steps Listed at Top
- User Tools Grouped Below

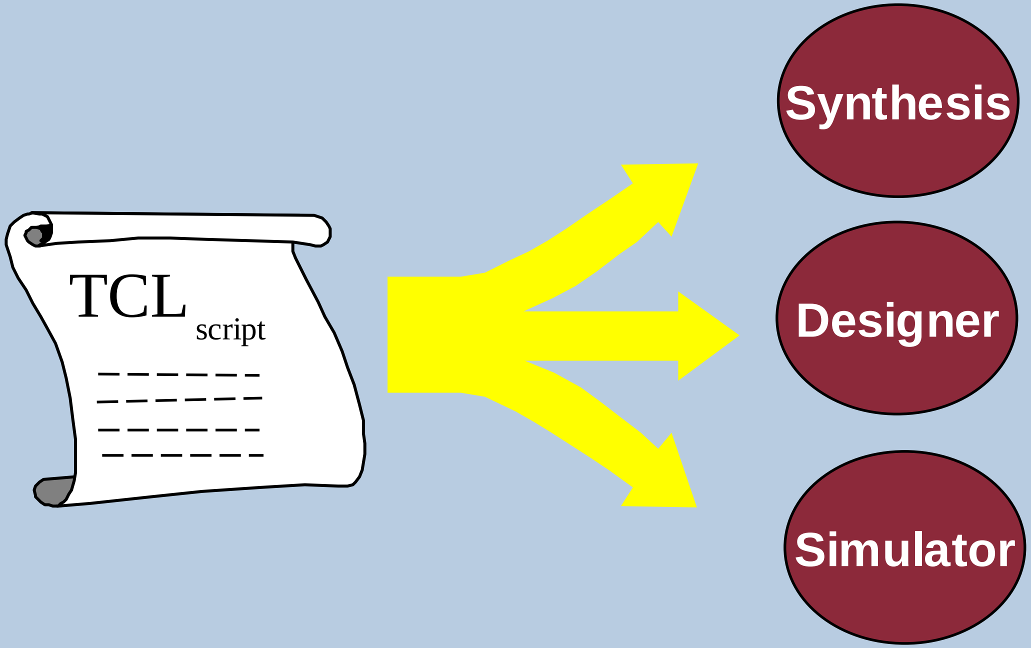
Designer Error Manager Tabs (same as Libero)

# Designer TCL Script Support

Industry-standard Language

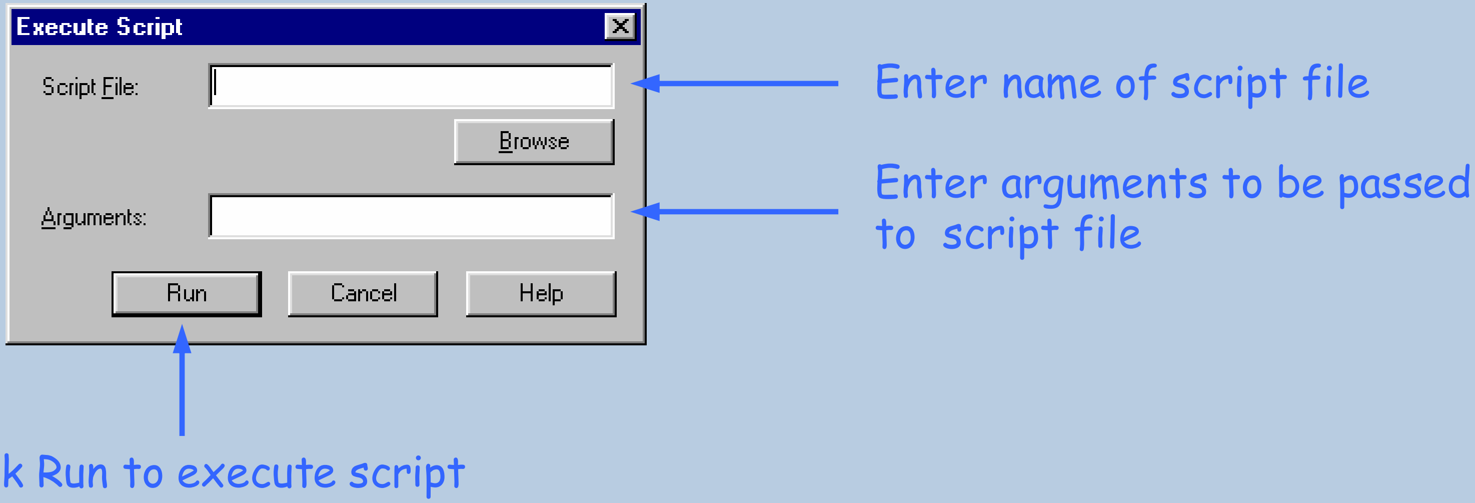
- Tool Command Language

- Launch Multiple Tools from Single Script
- Launch Multiple Design Runs



# Running Scripts within Designer

- In File Menu, Click Execute Script File
  - **Displays Execute Script Dialog Box**



Enter name of script file

Enter arguments to be passed to script file

Click Run to execute script

## Tcl Scripts can be Executed from the Command Line:

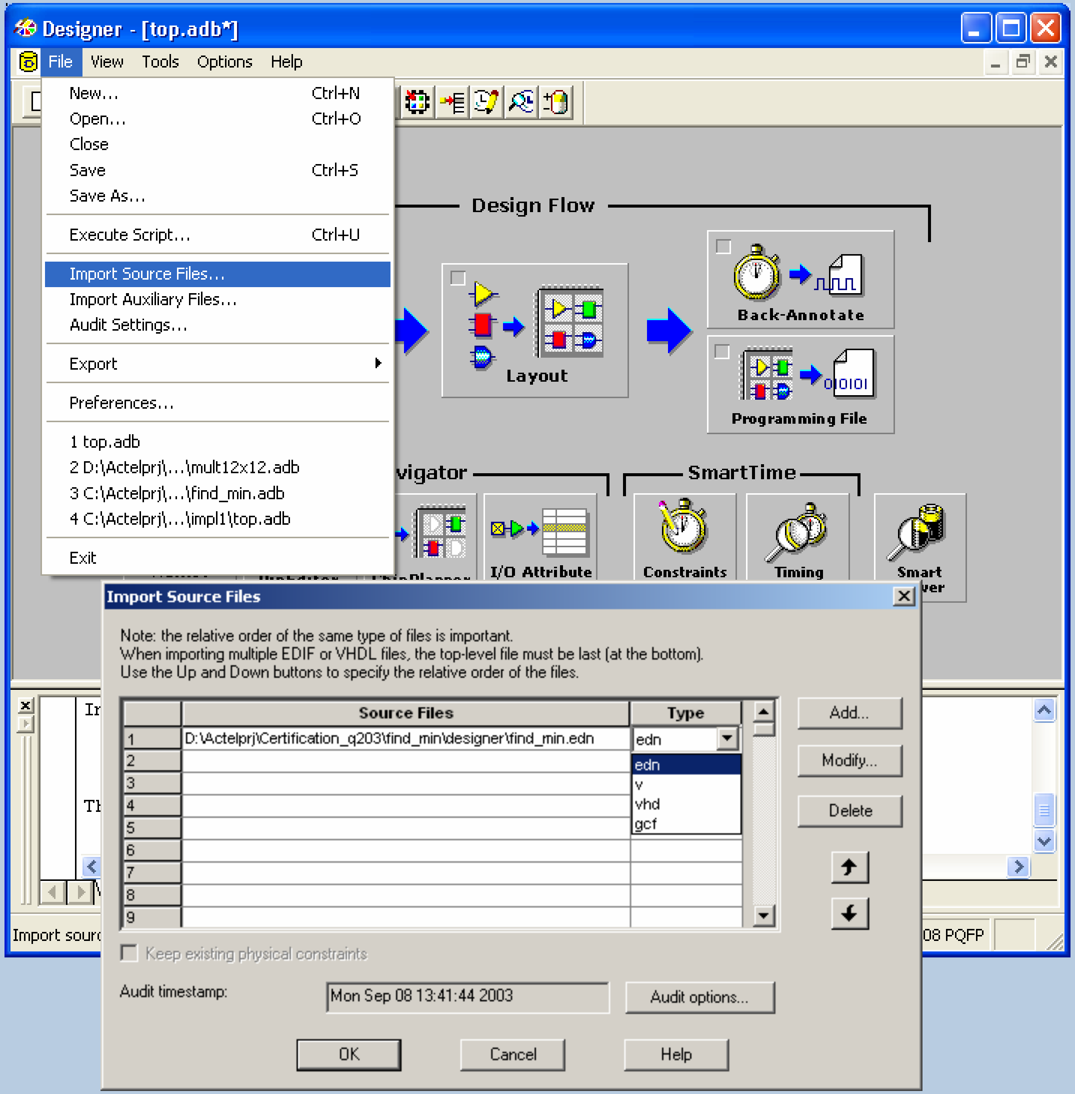
**Example:**

```
d:\Libero\Designer\bin\designer script:my_script
```

# Recording Scripts

- Designer Can Export Tcl Script File that Contains Commands Executed in Current Session
- Exported Tcl Script can be used to …
  - **… re-Execute Same Commands Interactively or in Batch**
  - **… Become More Familiar with Tcl Syntax**

# Importing Source Files



Note: the relative order of the same type of files is important.
When importing multiple EDIF or VHDL files, the top-level file must be last (at the bottom).
Use the Up and Down buttons to specify the relative order of the files.

| | Source Files | Type |
|---|---|---|
| 1 | D:\Actelprj\Certification_q203\find_min\designer\find_min.edn | edn |
| 2 | | edn |
| 3 | | v |
| 4 | | vhd |
| 5 | | gcf |
| 6 | | |
| 7 | | |
| 8 | | |
| 9 | | |

□ Keep existing physical constraints

Audit timestamp: Mon Sep 08 13:41:44 2003

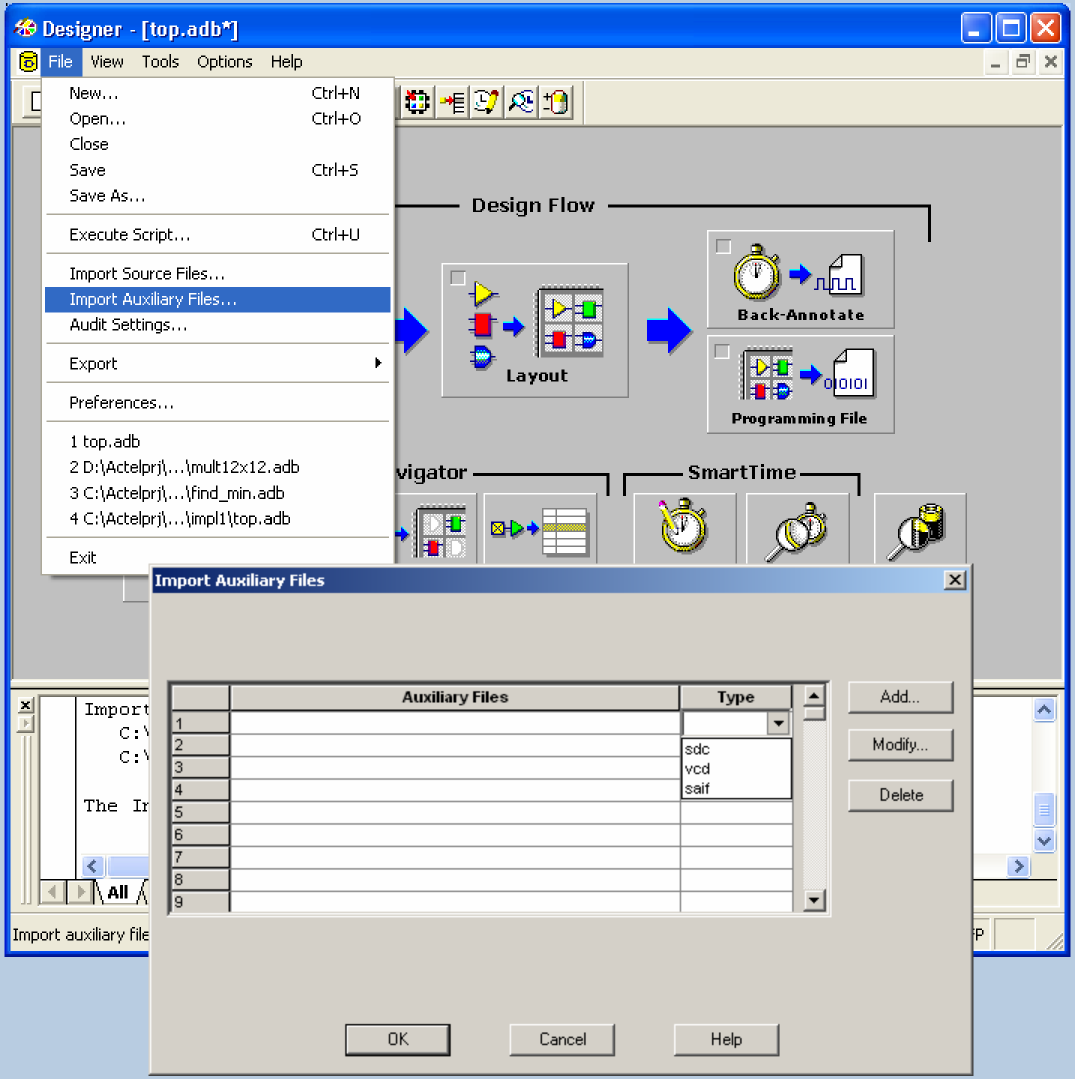
Multiple files can be imported at the same time

Libero sends Netlist and Constraint files to Designer Automatically

Import File types:

| File Type | Extension |
|---|---|
| EDIF | *.ed* |
| VHDL | *.vhd |
| Verilog | *.v |
| Actel ADL Netlist | *.adl |
| Criticality | *.crt |
| Timing Constraint File | *.sdc |
| ProASIC Constraint File | *.gcf |
| Physical Design Constraint File | *.pdc |

# Importing Auxiliary Files



Optional step to import pin files, timing constraints, etc.

Import Auxiliary files after compile completes

Import File types:

| File Type | Extension |
|---|---|
| Criticality | *.crt |
| PIN | *.pin |
| SDC | *.sdc |
| Physical Design Constraint | *.pdc |
| Value Change Dump | *.vcd |
| Switching Activity Intermediate File/Format | *.saif |
| Design Constraint File | *.dcf |

# Entering Constraints in Designer

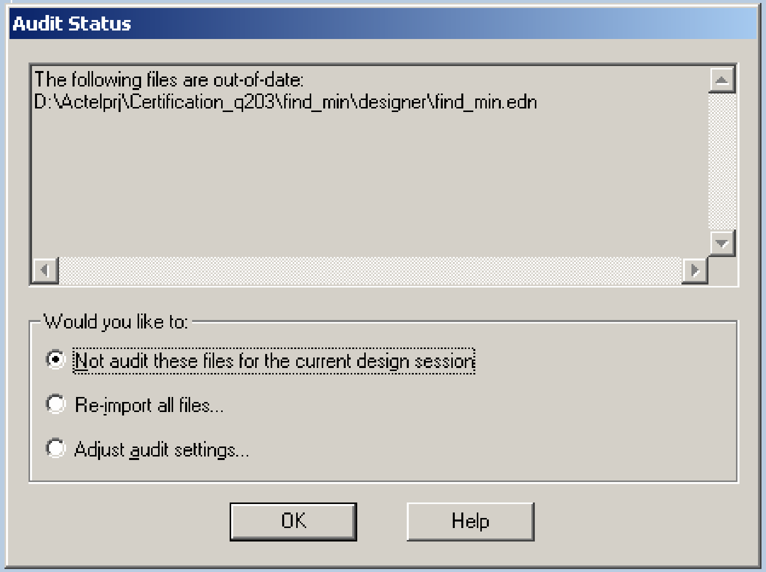
- Option 1 - Import Files in Designer
  - **Source or Auxiliary Files**
- Option 2 - Import Files in TCL Script
- Option 3 - Set All Constraints Directly in Designer
  - **Physical - PinEdit**
  - **Timing – SmartTime or Timer**

# Constraint File Types

- Physical
  - Pin Locations
    - SX-A, SX-S - .pin File
    - APA - .gcf File
    - Axcelerator, ProASIC3/E - .pdc File
  - All I/O Attributes
    - Axcelerator, ProASIC3/E - .pdc File
- Timing
  - All Constraints
    - All FPGA families – .sdc File

ONE CHIP is all you need

# Designer File Auditing

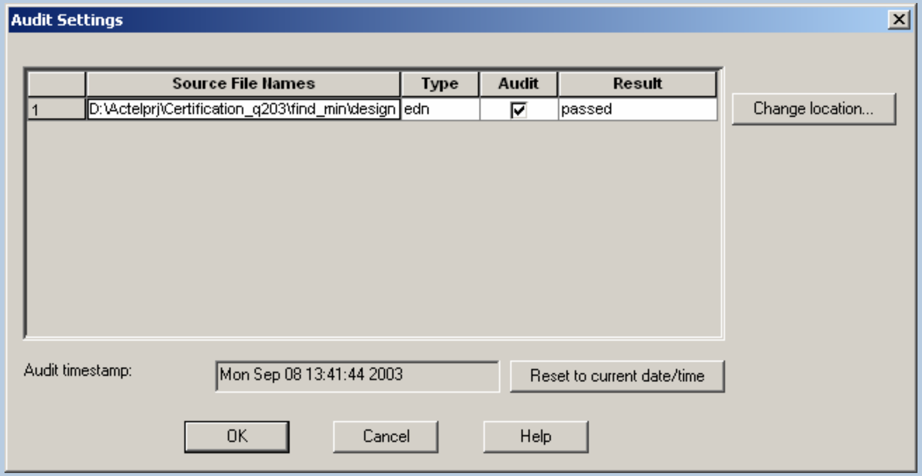


Audit Status

The following files are out-of-date:
D:\Actelprj\Certification_q203\find_min\designer\find_min.edn

Would you like to:

- ● Not audit these files for the current design session
- ○ Re-import all files...
- ○ Adjust audit settings...



Audit Settings

| | Source File Names | Type | Audit | Result |
|---|---|---|---|---|
| 1 | D:\Actelprj\Certification_q203\find_min\design | edn | ☑ | passed |

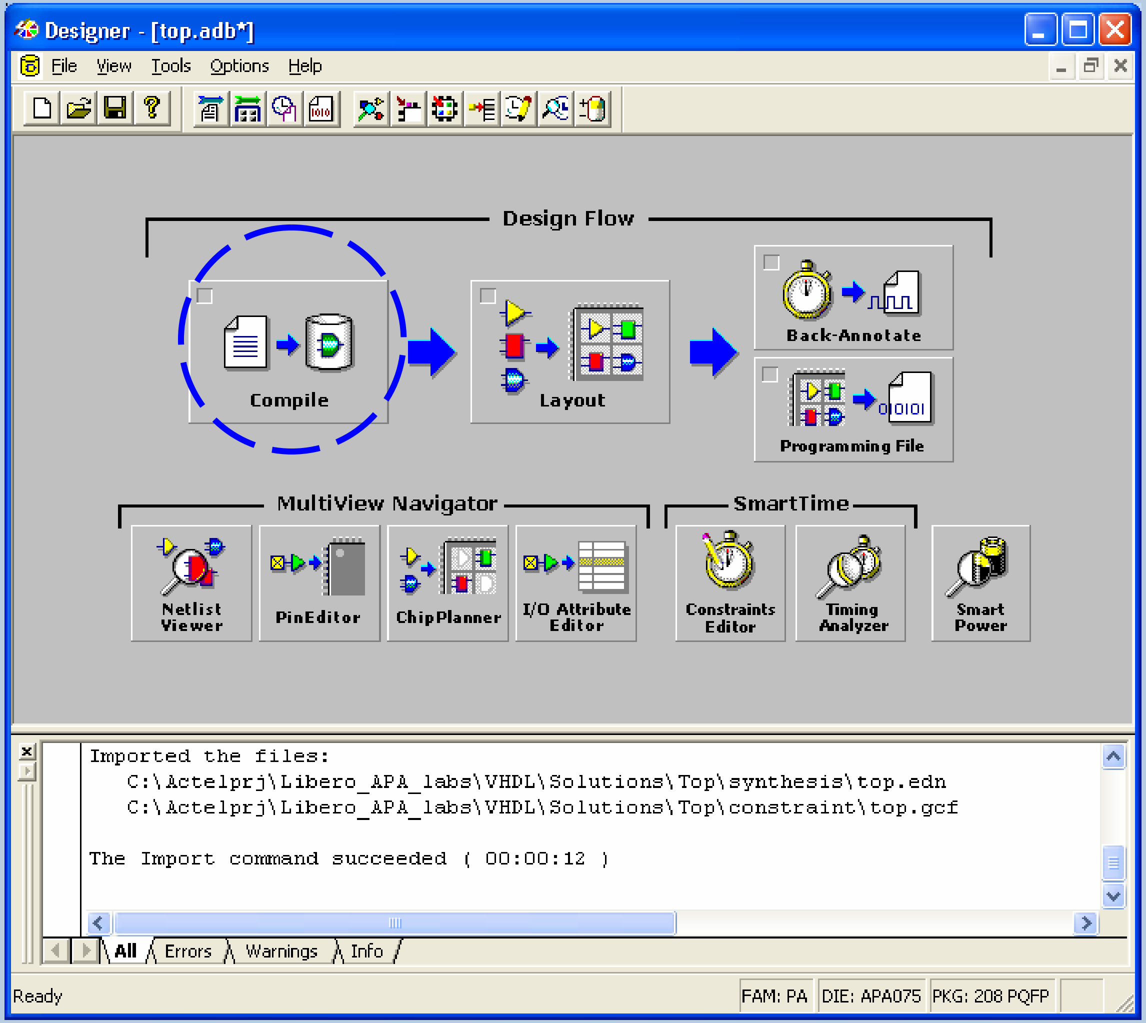
Audit timestamp: Mon Sep 08 13:41:44 2003

- Designer Audits Source Files to Ensure Imported Files Are Current
  - **All Imported Source Files Are Date- and Time-stamped**
  - **Designer Notifies You if File Is Changed**
- Audit Settings Can Be Changed (File > Audit Settings)
  - **Enable / Disable Auditing**
  - **Move File to New Location**
  - **Associate File with Current Date and Time**

# Importing Files into Designer
*Summary*

- Import the Following Source Files
  - EDIF, VHDL, Verilog Netlists
  - PDC, SDC, and GCF Files
  - Source Files Are Audited per User Settings
- Import the Following Auxiliary Files
  - DCF, SDC, PDC, VCD, and SAIF Files

# Designer
## *Compile*



```
Imported the files:
   C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\synthesis\top.edn
   C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\constraint\top.gcf

The Import command succeeded ( 00:00:12 )
```

Reads Netlist

Compiles Design into Actel Database (ADB) File

Runs Combiner

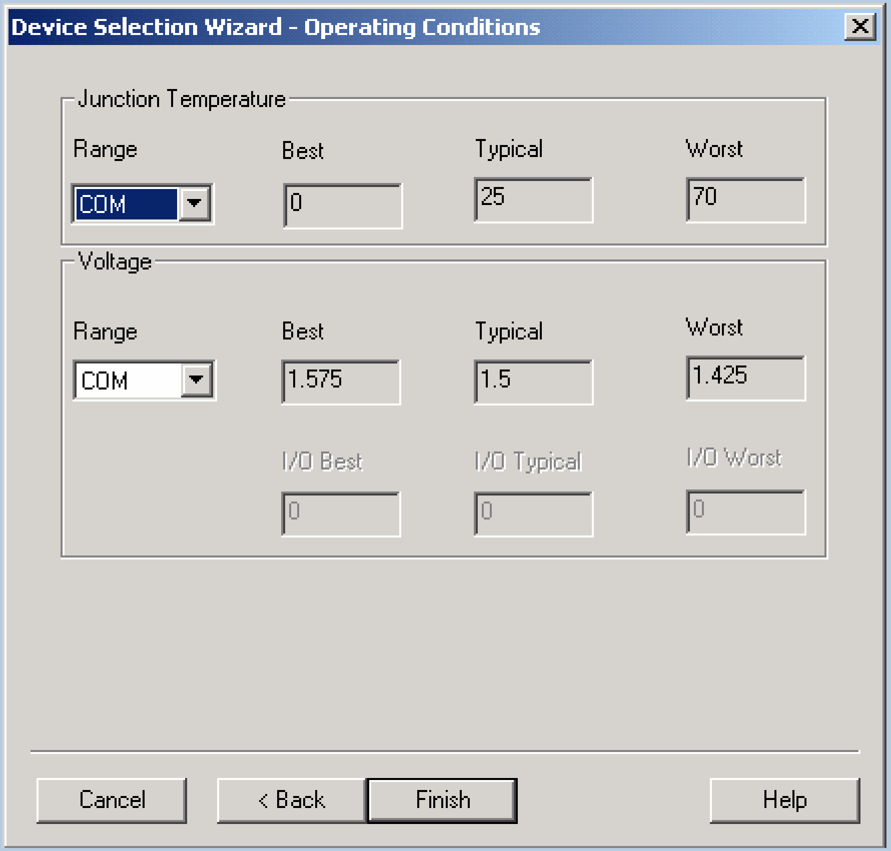
Performs Design Rule Checking

Checks for Netlist Errors (Bad Connections and Fanout Problems)

Removes Unused Logic (gobble)

Verifies that Design fits into Selected Device

# Compile Wizard



Device Selection Wizard - Operating Conditions

Junction Temperature

| Range | Best | Typical | Worst |
|---|---|---|---|
| COM | 0 | 25 | 70 |

Voltage

| Range | Best | Typical | Worst |
|---|---|---|---|
| COM | 1.575 | 1.5 | 1.425 |

| I/O Best | I/O Typical | I/O Worst |
|---|---|---|
| 0 | 0 | 0 |

Select:

- Die
- Package
- Speed Grade
- Die Voltage

Select Restrict Pin Usage

- Reserve JTAG Pins
- Reserve ActionProbe Pins

Select Ambient Temperature

- Commercial (0 - 70ºC)
- Industrial (-40 - 85ºC)
- Military (-55 - 125ºC)
- Custom

Select Voltage Range

TM15

# ProASIC$^{\underline{\text{PLUS}}}$ Netlist Optimization

## Slide 280

**TM15** Add slides on ProASIC3 combining

mccarthytim, 9/8/2006

# Netlist Optimization Constraints

## *ProASIC$^{PLUS}$ Designs*

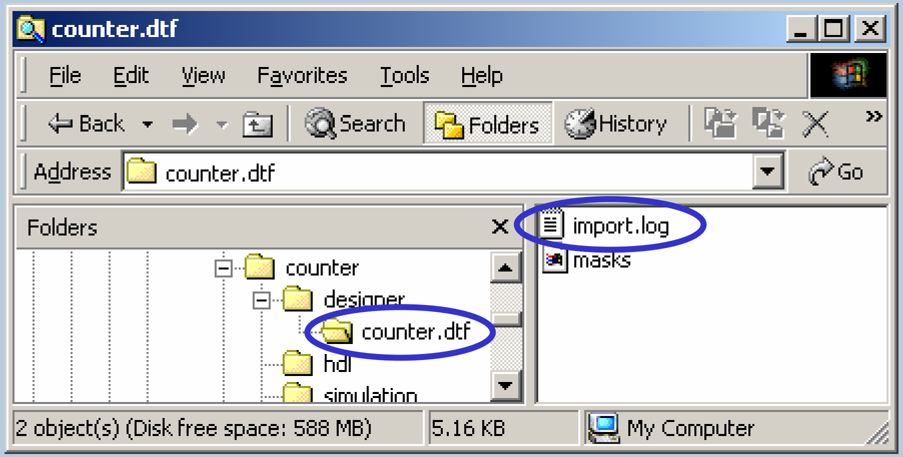
- Attempts to Remove All Cells from Netlist that Have No Effect on Circuit's Functional Behavior
  - **Reduces Overall Size of Design**
  - **Produces Faster Place and Route Times**
  - **Takes Advantage of Inverted Inputs of Logic Tiles**
- By Default *All* Optimizations Are Performed on Netlist
- Original Netlist Preserved
  - **Removed Cells Back-annotated with 0ns Delay in SmartTime**

# Netlist Optimization Constraints
## *Options*

- ***buffer*** **- Removes All Buffers Provided Maximum Fanout Not Exceeded**
- ***inverter*** **- Removes All Inverters Provided Maximum Fanout Not Exceeded**
- ***clocktree*** **- Removes All Inverters and Buffers in Nets Connected to Clock Inputs on All Flip-Flop Cell Types**
- ***resettree*** **- Removes All Inverters and Buffers in Nets Connected to Reset Inputs on All Flip-Flop Cell Types**
- ***const*** **- Replaces All Logical Elements with One or More Constant Inputs (Connected to Logical "1" or "0") by Simplified Logic Function**
  - **If Replacement Logic Function Is Inverter or Buffer, that Element Is Removed**
- ***dangling*** **- Recursively Removes All Cells Driving Unconnected Nets**

# Import Log
## *Flash Designs*

- Import Log Written after Compile Step in Designer
  - Created under <name>.dtf directory
- What it Reveals
  - Promoted Globals
  - Distribution of Fanout
  - Device Utilization (RAMs, PLLs, IOs, Global Routes, Logic)
  - Internal and External Nets (Min, Average and Max fanout)
  - High Fanout Net Candidates to be Mapped to Spines
  - Internal Clocks



# Designer Import Log
## *Flash Designs*

```
. . .
Compile Output:
NOTE [removed_pwr_gnd_cells]:
  Removed 2 power/ground cells from the design.
 Optimizing Netlist.

Promoting nets to globals.

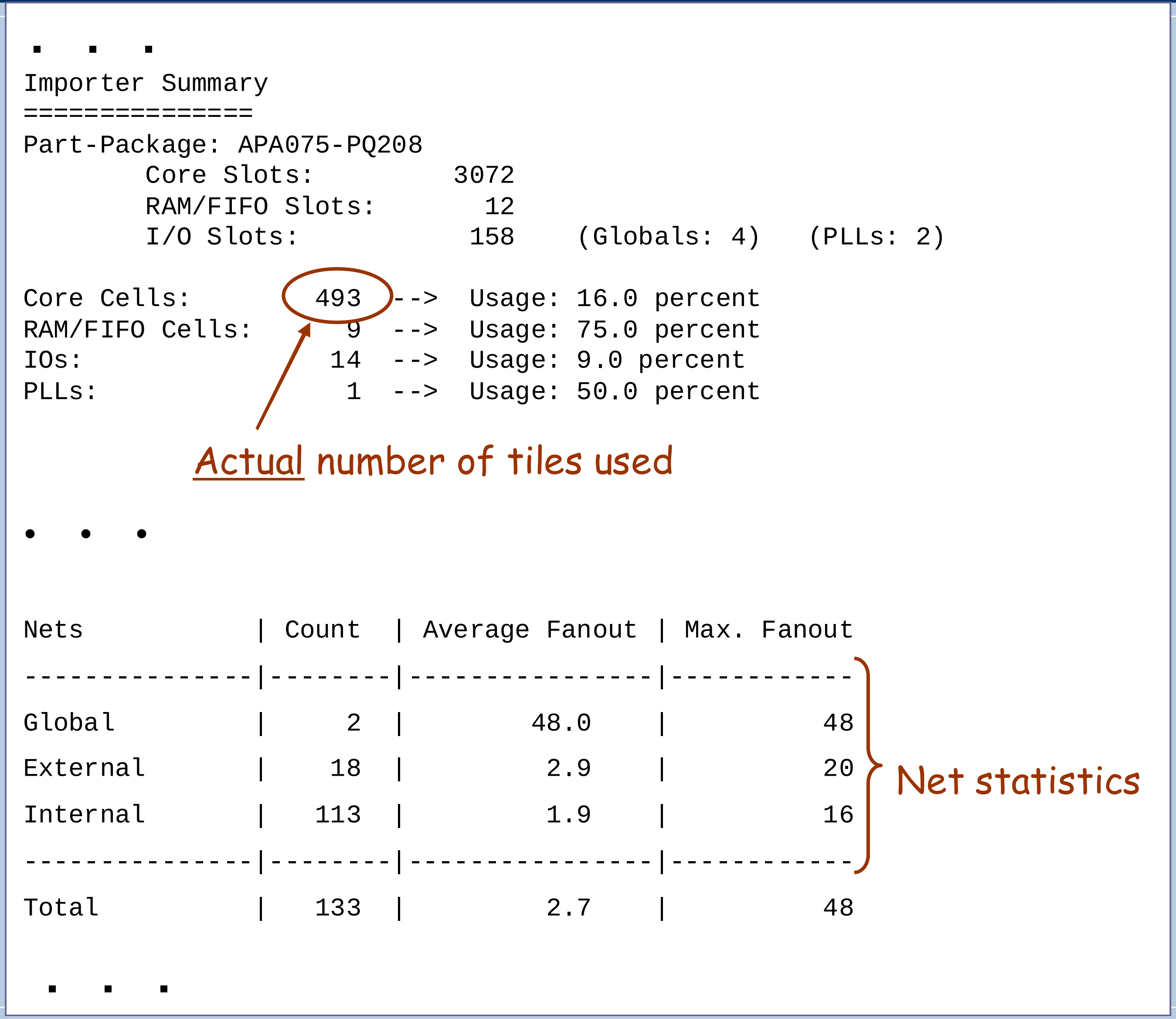
Following nets are possible candidates for Globals/Spines :
Fanout     Type                  Driver               Name
 48        CLK_NET               CLK_pad/MUXTILE      CLK_c
 48        SET/RESET_NET         RESET_pad/MUXTILE    RESET_c

Following nets are assigned to global resources:
Fanout     Name
  48       CLK_c
  48       RESET_c
. . .
```

Removed cells

Nets assigned to global resources

# Designer Import Log (cont.)



```
. . .
Importer Summary
================
Part-Package: APA075-PQ208
        Core Slots:         3072
        RAM/FIFO Slots:       12
        I/O Slots:           158    (Globals: 4)   (PLLs: 2)

Core Cells:          493 --> Usage: 16.0 percent
RAM/FIFO Cells:        9 --> Usage: 75.0 percent
IOs:                  14 --> Usage: 9.0 percent
PLLs:                  1 --> Usage: 50.0 percent
```

Actual number of tiles used

```
• • •

Nets           | Count  | Average Fanout | Max. Fanout
---------------|--------|----------------|------------
Global         |     2  |       48.0     |         48
External       |    18  |        2.9     |         20
Internal       |   113  |        1.9     |         16
---------------|--------|----------------|------------
Total          |   133  |        2.7     |         48

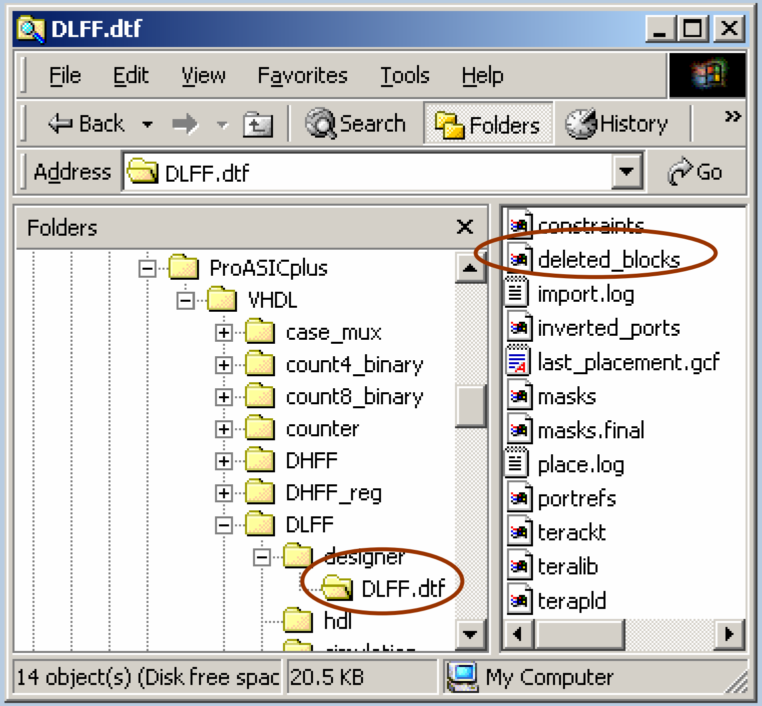
 . . .
```

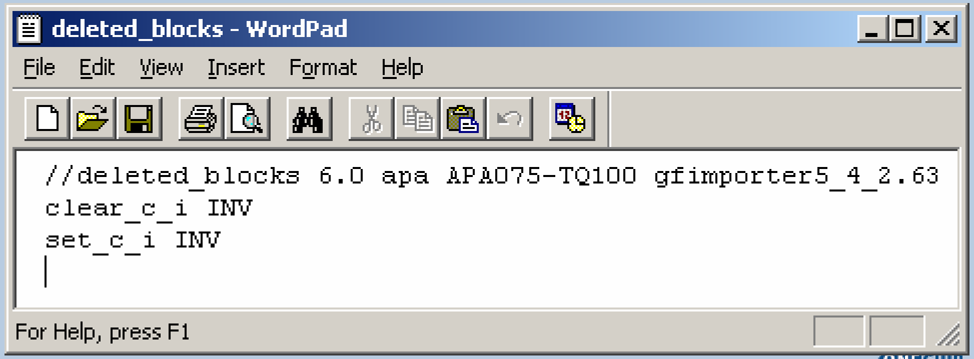
Net statistics

# Identifying Removed Cells
*Flash Designs*

## While Compile or Layout Is Running, Temporary File Named `deleted_blocks` Is Created under `<name>.dtf` Directory

- Lists All Deleted Cells
- This File Automatically Removed after Layout Is Finished
  - *Save File before Layout Completes or Run Place Option without Route*





```
//deleted_blocks 6.0 apa APA075-TQ100 gfimporter5_4_2.63
clear_c_i INV
set_c_i INV
```

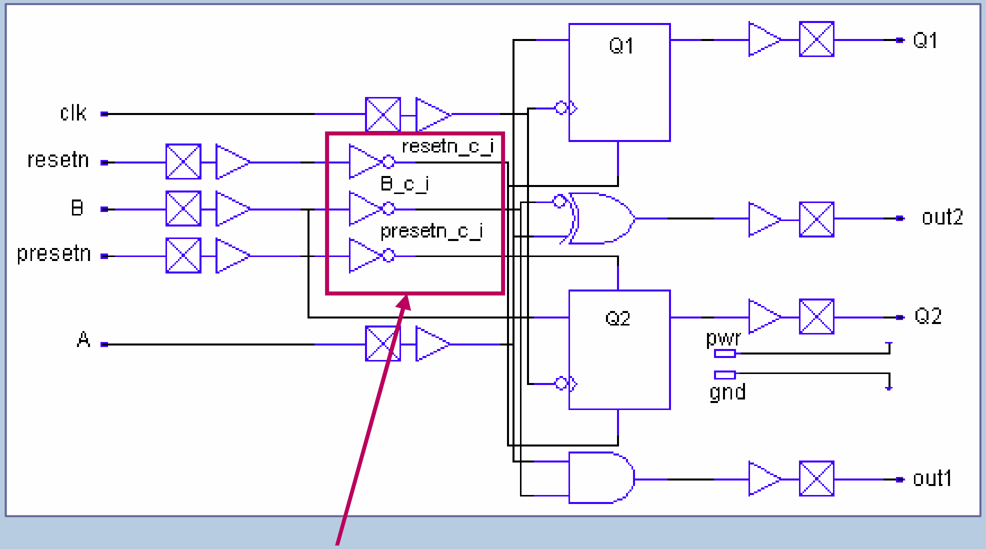
# Netlist Optimization Example
## *Flash Designs*

```
-- example to test APA optimization
library ieee;
use ieee.std_logic_1164.all;
entity test is
port (A, B, presetn, resetn, clk: in std_logic;
      out1, out2, Q1, Q2: out std_logic);
end test;

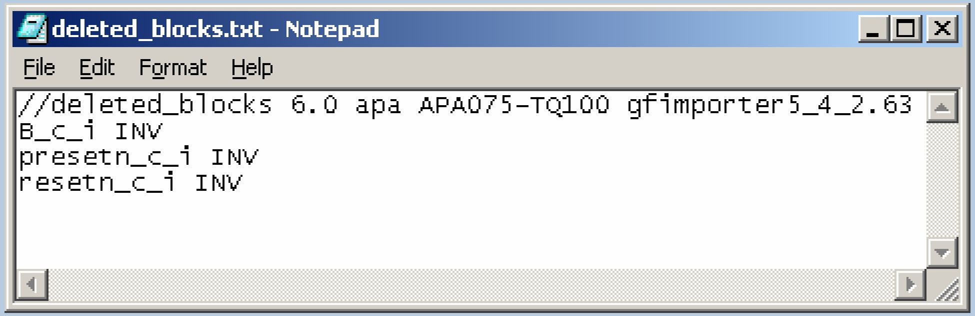
architecture RTL of test is
begin
process (clk, resetn)
begin
if (resetn = '0') then  Q1 <= '0';
elsif (clk 'event and clk = '0') then  Q1 <= A;
end if;
end process;

process (clk, resetn, presetn)
begin
if (resetn = '0') then    Q2 <= '0';
elsif (presetn = '0') then    Q2 <= '1';
elsif (clk 'event and clk = '0') then  Q2 <= B;
end if;
end process;

out1 <= A and not B;
out2 <= not A xor not B;
end RTL;
```

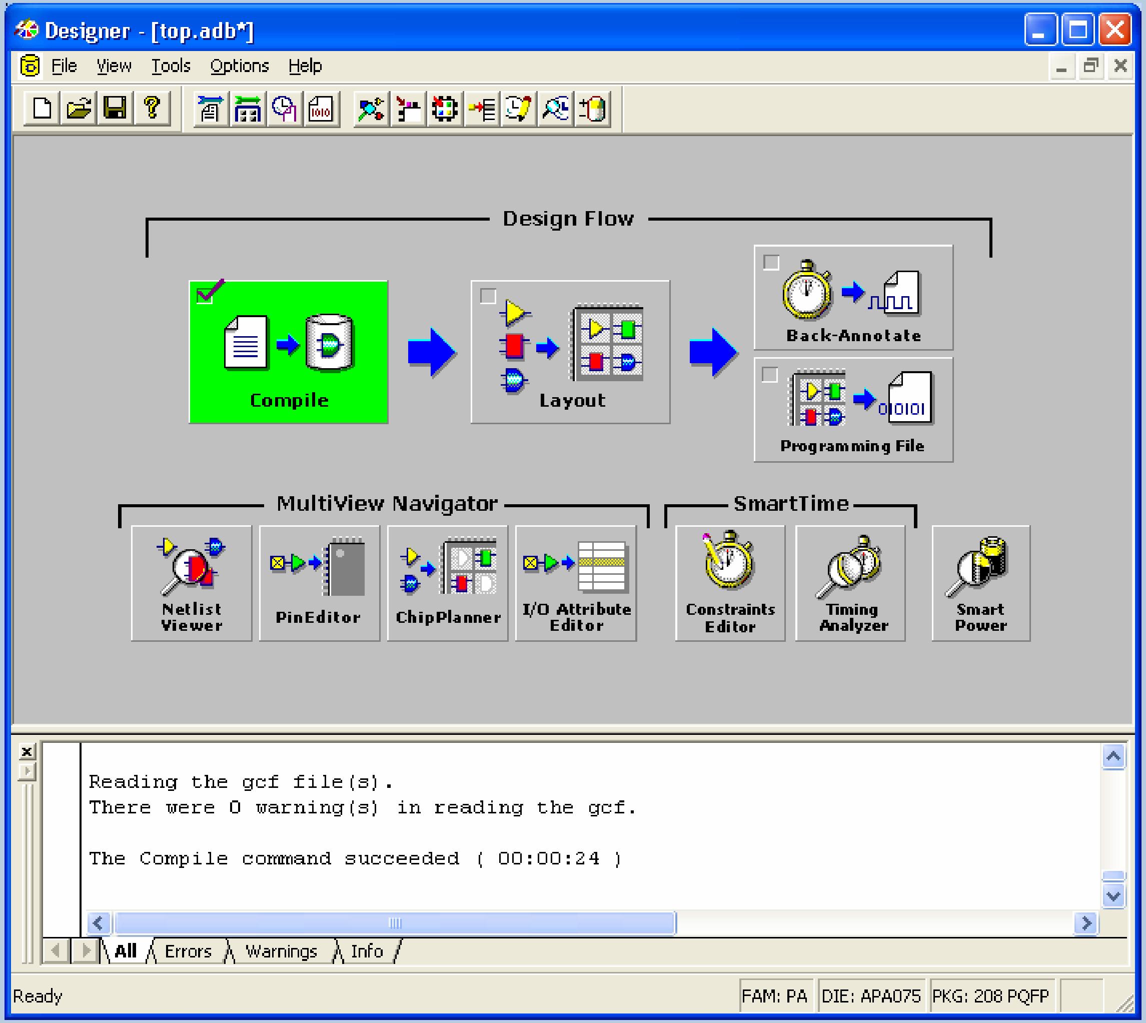


Deleted blocks



```
//deleted_blocks 6.0 apa APA075-TQ100 gfimporter5_4_2.63
B_c_i INV
presetn_c_i INV
resetn_c_i INV
```

# Successful Compile

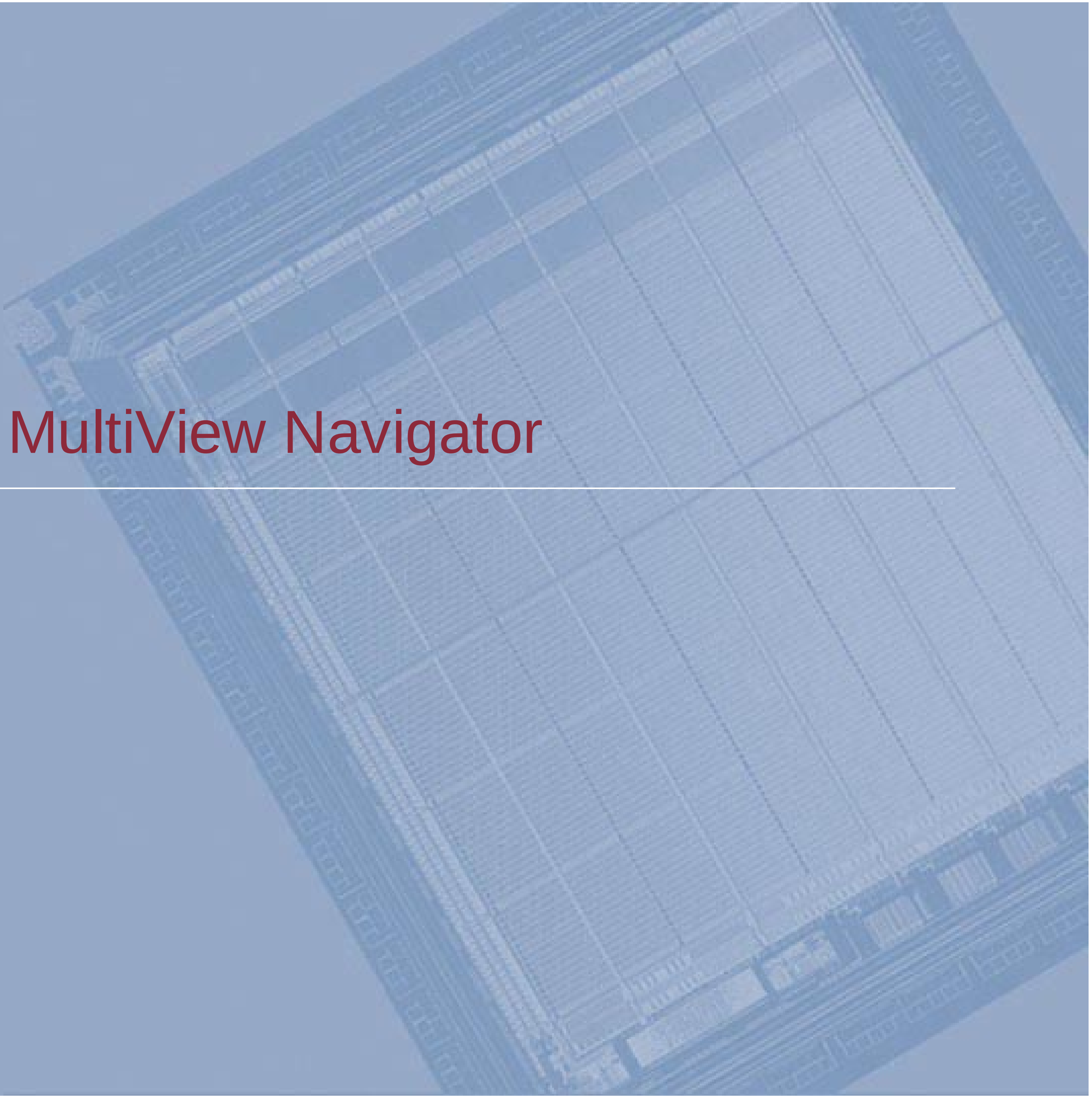


```
Reading the gcf file(s).
There were 0 warning(s) in reading the gcf.

The Compile command succeeded ( 00:00:24 )
```

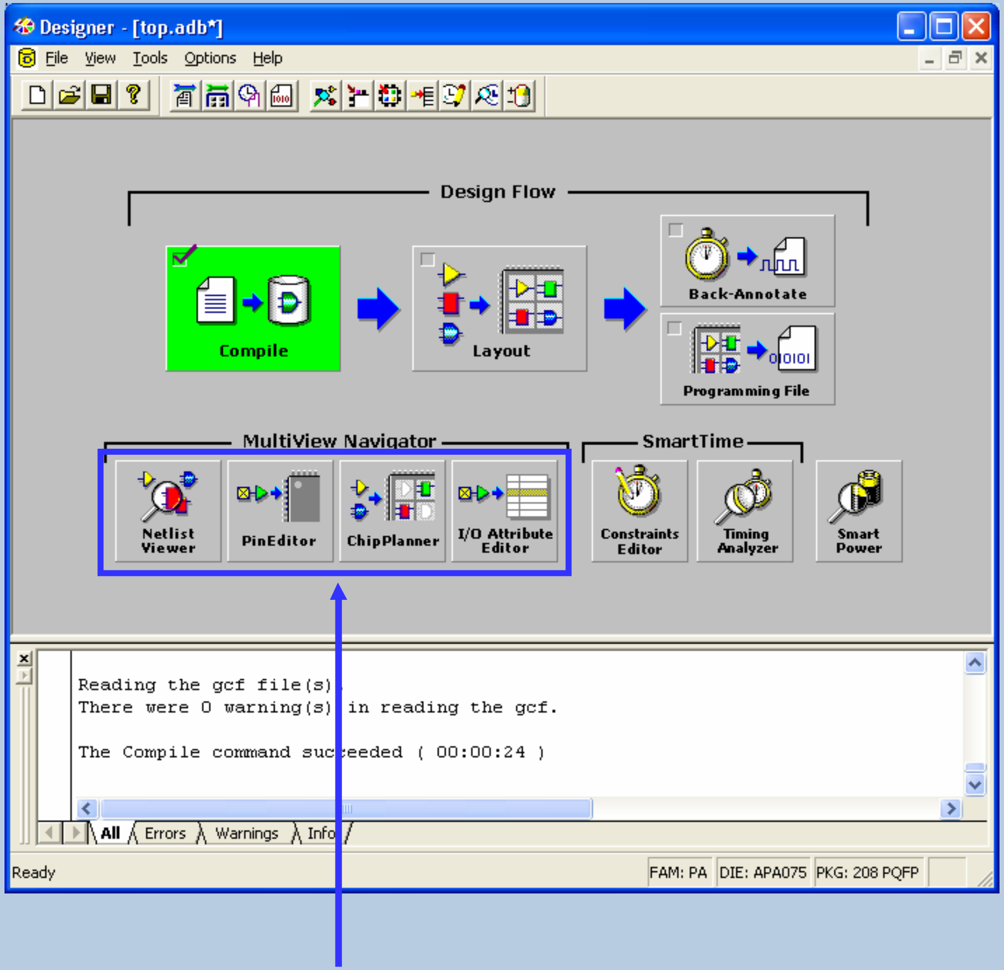
- Compile Button Turns Green if Compile Completes Successfully
  - **Errors Indicated in Designer Log Window**

# MultiView Navigator



# MultiView Navigator

- MultiView Navigator Includes the Following Tools:
  - **PinEditor, I/O Attribute Editor, NetlistViewer, and ChipPlanner**
- Supported for the following families:
  - **Fusion, ProASIC3\E, APA, A500K, AX, SX-A, SX-S, eX**
- Allows Cross-probing Among Different Designer Tools



```
Reading the gcf file(s)
There were 0 warning(s) in reading the gcf.

The Compile command succeeded ( 00:00:24 )
```

Click one of these buttons to open MVN

# MultiView Navigator

Zoom Controls

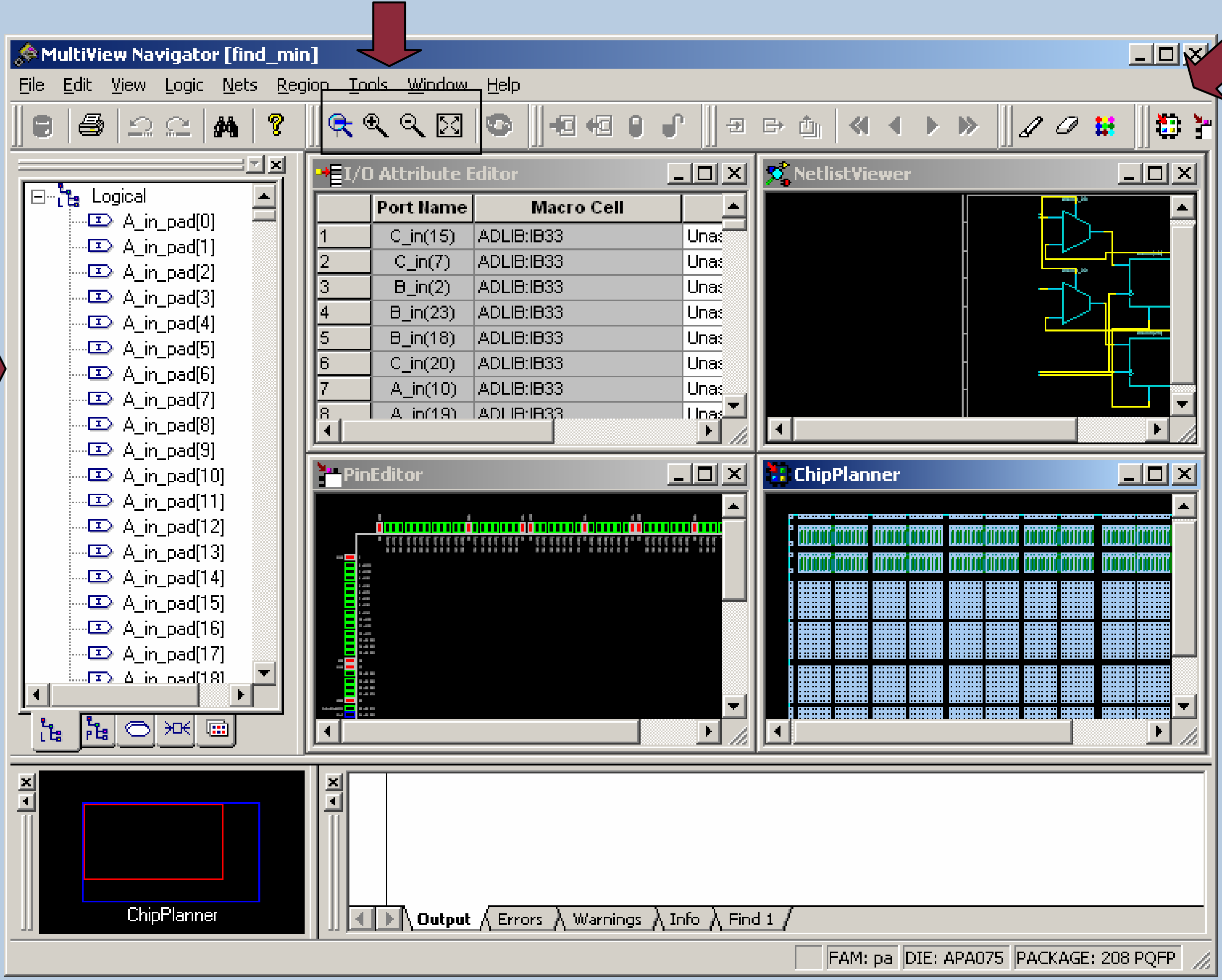
Toolbar Icons

Design Window

Working Area

World View Window

Log Window



- A_in_pad[0]
- A_in_pad[1]
- A_in_pad[2]
- A_in_pad[3]
- A_in_pad[4]
- A_in_pad[5]
- A_in_pad[6]
- A_in_pad[7]
- A_in_pad[8]
- A_in_pad[9]
- A_in_pad[10]
- A_in_pad[11]
- A_in_pad[12]
- A_in_pad[13]
- A_in_pad[14]
- A_in_pad[15]
- A_in_pad[16]
- A_in_pad[17]
- A_in_pad[18]

|  | Port Name | Macro Cell |  |
|---|---|---|---|
| 1 | C_in(15) | ADLIB:IB33 | Unas |
| 2 | C_in(7) | ADLIB:IB33 | Unas |
| 3 | B_in(2) | ADLIB:IB33 | Unas |
| 4 | B_in(23) | ADLIB:IB33 | Unas |
| 5 | B_in(18) | ADLIB:IB33 | Unas |
| 6 | C_in(20) | ADLIB:IB33 | Unas |
| 7 | A_in(10) | ADLIB:IB33 | Unas |
| 8 | A_in(19) | ADLIB:IB33 | Unas |

FAM: pa DIE: APA075 PACKAGE: 208 PQFP

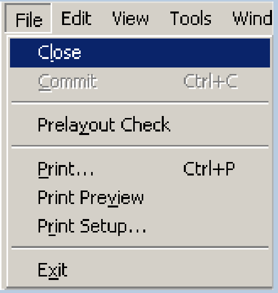
ONECHIP is all you need

# MultiView Navigator
*Windows*

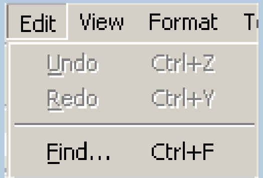
- Design Window
  - **View Design as Logical Blocks, Physical Elements, Ports, Nets, and Regions**
- World View Window
  - **Shows Position of Current Viewing Window Relative to Chip**
- Working Area Shows Current Active Tools
  - **Tile or Cascade Active Tools**
- Log Window Keeps Running Log of Activity
  - **Output – Shows All Messages**
  - **Errors – Shows Error Messages**
  - **Warnings – Shows Warning Messages**
  - **Info – Shows Informational Messages**
  - **Find Window – Keeps Result of Find Function for Later Usage**

# MultiView Navigator Toolbar

- File ->
  - Commit – Writes any Changes Made in Editors to Design
  - Prelayout Check – Verifies Placement Changes in Editors Are Legal



- Edit ->
  - Undo/Redo – Allows User to Undo a Mistake or Redo an Accidental Undo
  - Find – Enables Find Interface



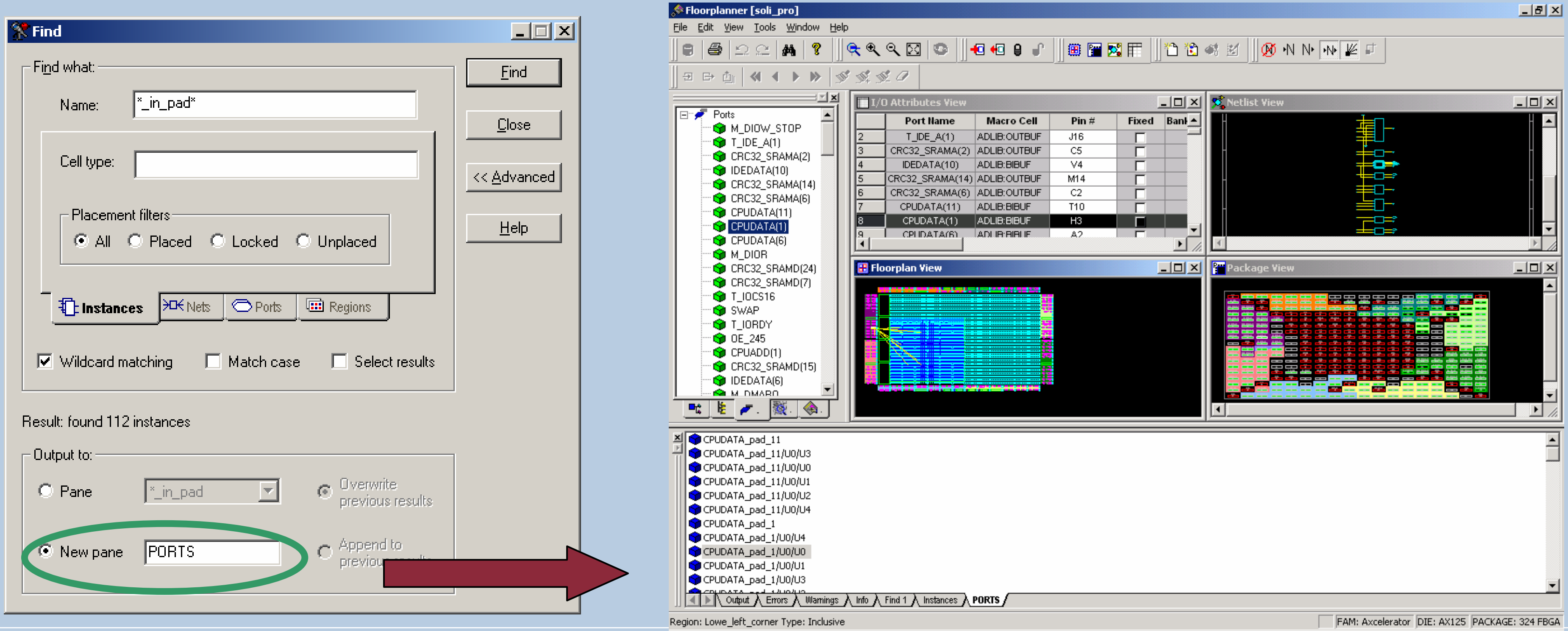
- Zoom Controls
  - Zoom Region, Zoom In, Zoom Out, Zoom to Fit
- Assignment Options
  - Place, Unplace, Lock (Fix), Unlock (Unfix)
- Tools Menu
  - ChipPlanner, PinEditor, NetlistViewer, I/O Attribute Editor
- “1 click" commands
  - Commit and Check
  - Lock All
  - Unlock All
  - Un-assign All from Location
  - Un-assign All from Region

# MultiView Navigator
## *Prelayout Checker*

- Infeasible Constraints Identified pre-Layout
  - Automatically Runs when You Commit from MVN
  - Users Can Run Using MVN Command Tools->DRC
- Enhanced Checks
  - Overlapping Region Checks
  - Resource Overbooking
  - I/O Technology Checks

# MultiView Navigator
## *Find / Search*

- Search for Instances, Nets or Ports
  - **Wildcard (*) Matching**
  - **Advanced Options - Choice of Log Window Pane for Search Results**
- Cross-probing from Find Tab to the other Four Windows



Find

Find what:

Name: *_in_pad*

Cell type:

Placement filters: ● All ○ Placed ○ Locked ○ Unplaced

☑ Wildcard matching □ Match case □ Select results

Result: found 112 instances

Output to:

○ Pane *_in_pad ● Overwrite previous results

● New pane PORTS ○ Append to previous results

Floorplanner [soli_pro]

Ports
- M_DIOW_STOP
- T_IDE_A(1)
- CRC32_SRAMA(2)
- IDEDATA(10)
- CRC32_SRAMA(14)
- CRC32_SRAMA(6)
- CPUDATA(11)
- CPUDATA(1)
- CPUDATA(6)
- M_DIOR
- CRC32_SRAMD(24)
- CRC32_SRAMD(7)
- T_IOCS16
- SWAP
- T_IORDY
- OE_245
- CPUADD(1)
- CRC32_SRAMD(15)
- IDEDATA(6)
- M_DMARQ

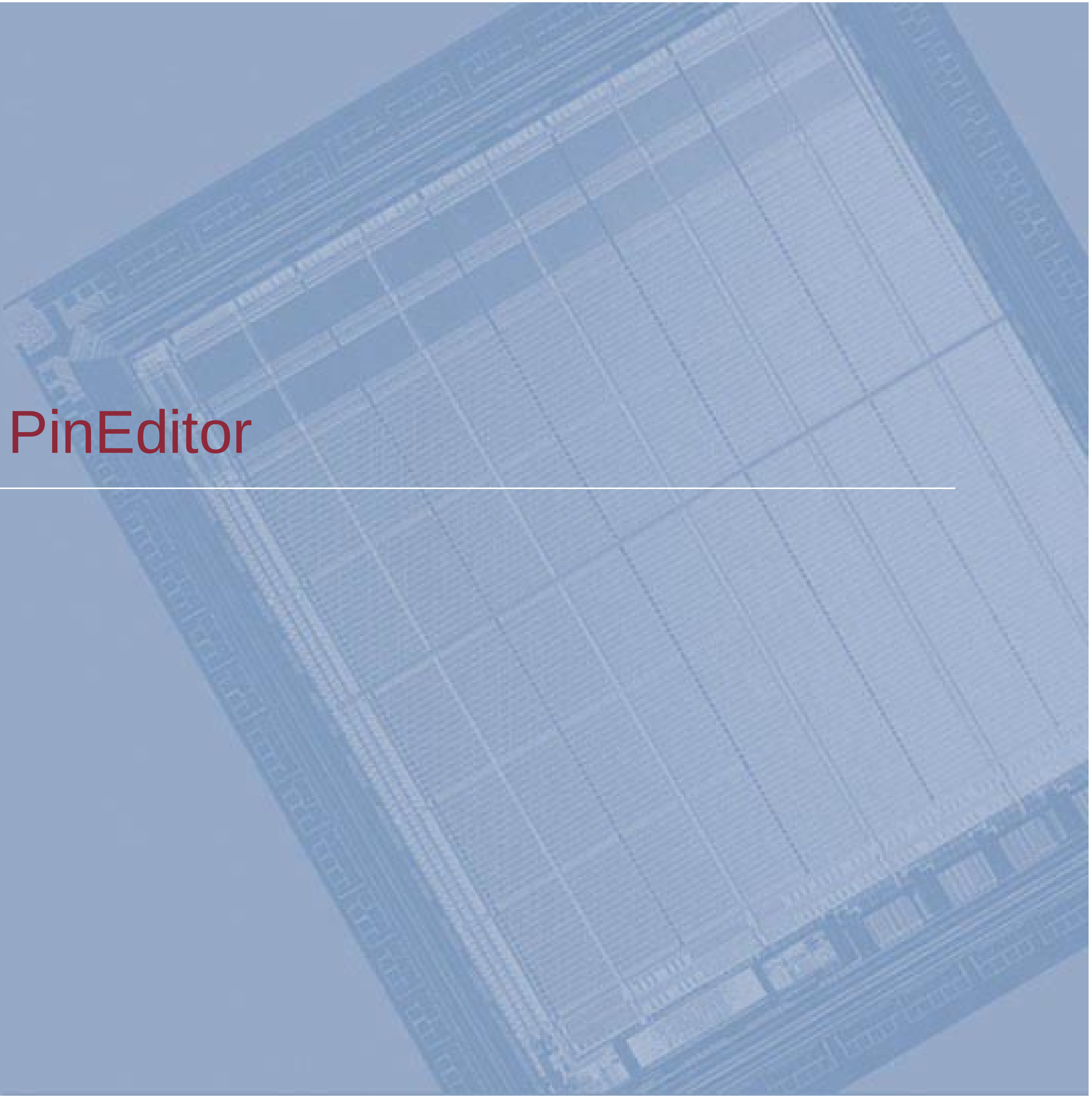
|  | Port Name | Macro Cell | Pin # | Fixed | Bank |
|---|---|---|---|---|---|
| 2 | T_IDE_A(1) | ADLIB:OUTBUF | J16 | □ |  |
| 3 | CRC32_SRAMA(2) | ADLIB:OUTBUF | C5 | □ |  |
| 4 | IDEDATA(10) | ADLIB:BIBUF | V4 | □ |  |
| 5 | CRC32_SRAMA(14) | ADLIB:OUTBUF | M14 | □ |  |
| 6 | CRC32_SRAMA(6) | ADLIB:OUTBUF | C2 | □ |  |
| 7 | CPUDATA(11) | ADLIB:BIBUF | T10 | □ |  |
| 8 | CPUDATA(1) | ADLIB:BIBUF | H3 | □ |  |
| 9 | CPUDATA(6) | ADLIB:BIBUF | A2 | □ |  |

```
CPUDATA_pad_11
CPUDATA_pad_11/U0/U3
CPUDATA_pad_11/U0/U0
CPUDATA_pad_11/U0/U1
CPUDATA_pad_11/U0/U2
CPUDATA_pad_11/U0/U4
CPUDATA_pad_1
CPUDATA_pad_1/U0/U4
CPUDATA_pad_1/U0/U0
CPUDATA_pad_1/U0/U1
CPUDATA_pad_1/U0/U3
```

Region: Lowe_left_corner Type: Inclusive

FAM: Axcelerator DIE: AX125 PACKAGE: 324 FBGA

# PinEditor



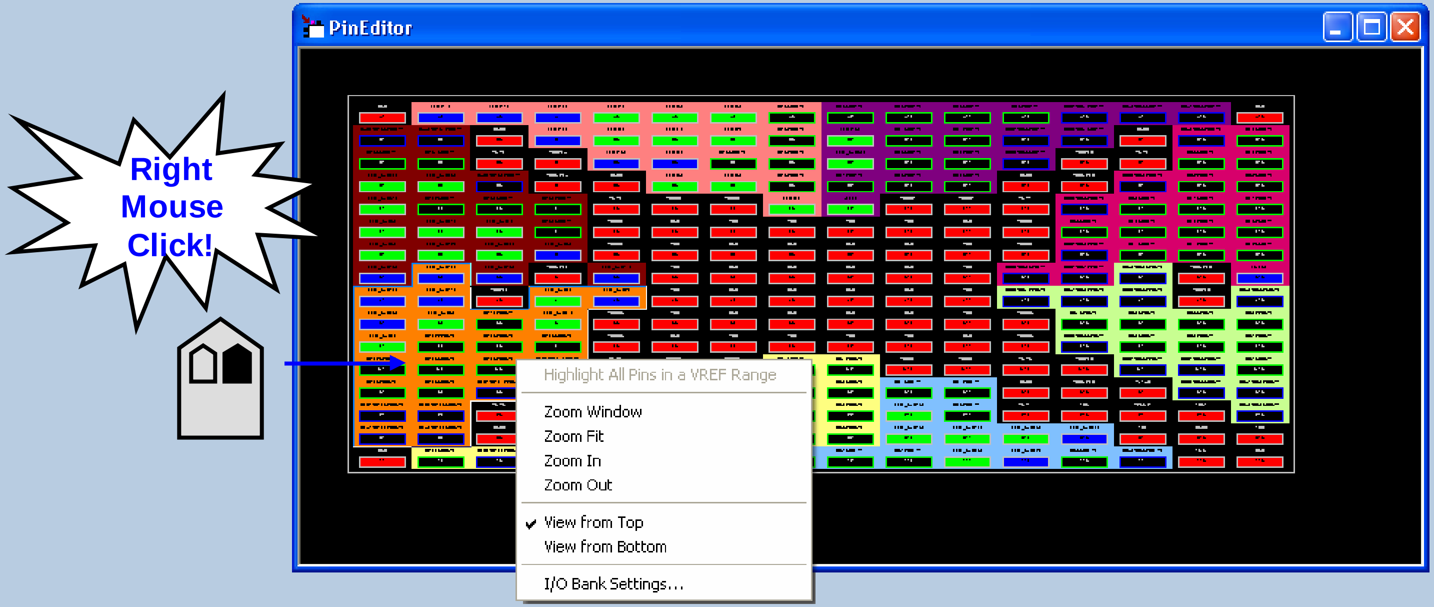
# Pin Assignment Options

- I/O Locations Can Be Assigned as Follows:
  - **Automatically by Designer Software during Layout**
  - **By Importing One of the Following:**
    - **. Gatefield Constraint File (.gcf) (ProASIC and ProASIC$^{\underline{PLUS}}$)**
    - **. PIN File (Antifuse Devices)**
    - **Physical Design Constraint (.pdc) (Axcelerator and ProASIC3/E)**
  - **Manually using PinEdit Tool in Designer**
    - **Pin Assignments May Be Exported for Later Use**

ONE CHIP is all you need

# MultiView Navigator
## *PinEditor*

- Graphical Pin Location Editor
  - **Drag and Drop Placement of Pins**
  - **Fix Pin Locations for Subsequent Place and Route Runs**
- Flip Display
  - **Enables Assignments as if Looking from Top or Bottom of Chip**
- Assign I/O Bank Properties for Axcelerator and ProASIC3E
- Pinout Can Be Printed for Documentation



# I/O Bank Configuration
*Axcelerator, ProASIC3E*

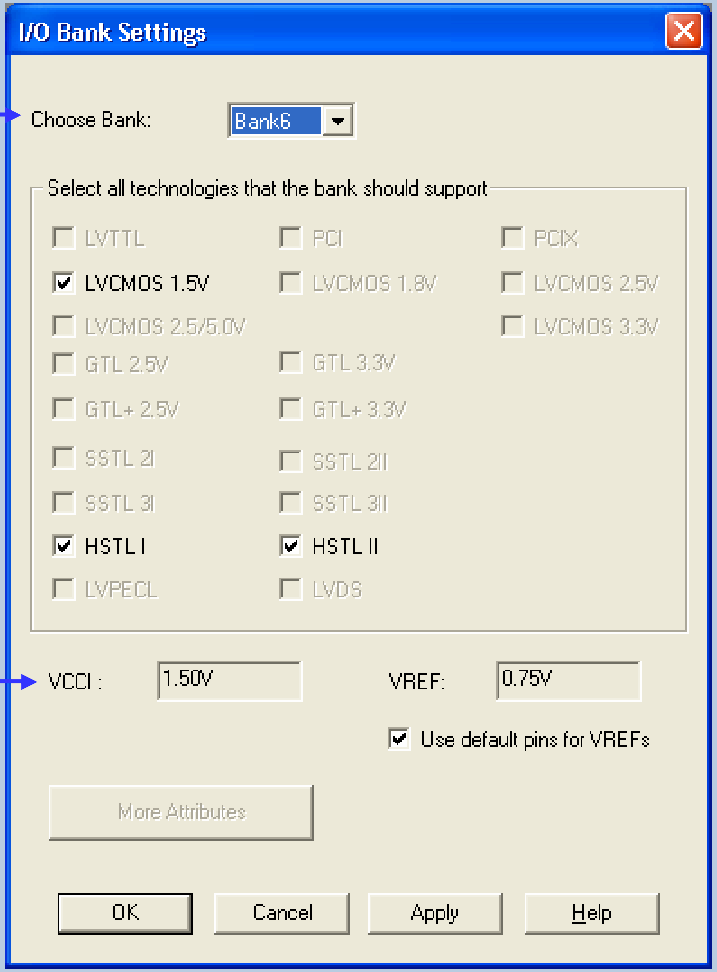
## I/O Bank Configuration

- Select Bank
- Select I/O Standards
  - Incompatible Options Disappear when Selecting I/O Standards
- Select Low-power Mode
- Select Input Delay

Select bank

I/O standards

I/O bank VCCI/VREF not editable



I/O Bank Settings

Choose Bank: Bank6

Select all technologies that the bank should support

| | | |
|---|---|---|
| ☐ LVTTL | ☐ PCI | ☐ PCIX |
| ☑ LVCMOS 1.5V | ☐ LVCMOS 1.8V | ☐ LVCMOS 2.5V |
| ☐ LVCMOS 2.5/5.0V | | ☐ LVCMOS 3.3V |
| ☐ GTL 2.5V | ☐ GTL 3.3V | |
| ☐ GTL+ 2.5V | ☐ GTL+ 3.3V | |
| ☐ SSTL 2I | ☐ SSTL 2II | |
| ☐ SSTL 3I | ☐ SSTL 3II | |
| ☑ HSTL I | ☑ HSTL II | |
| ☐ LVPECL | ☐ LVDS | |

VCCI : 1.50V

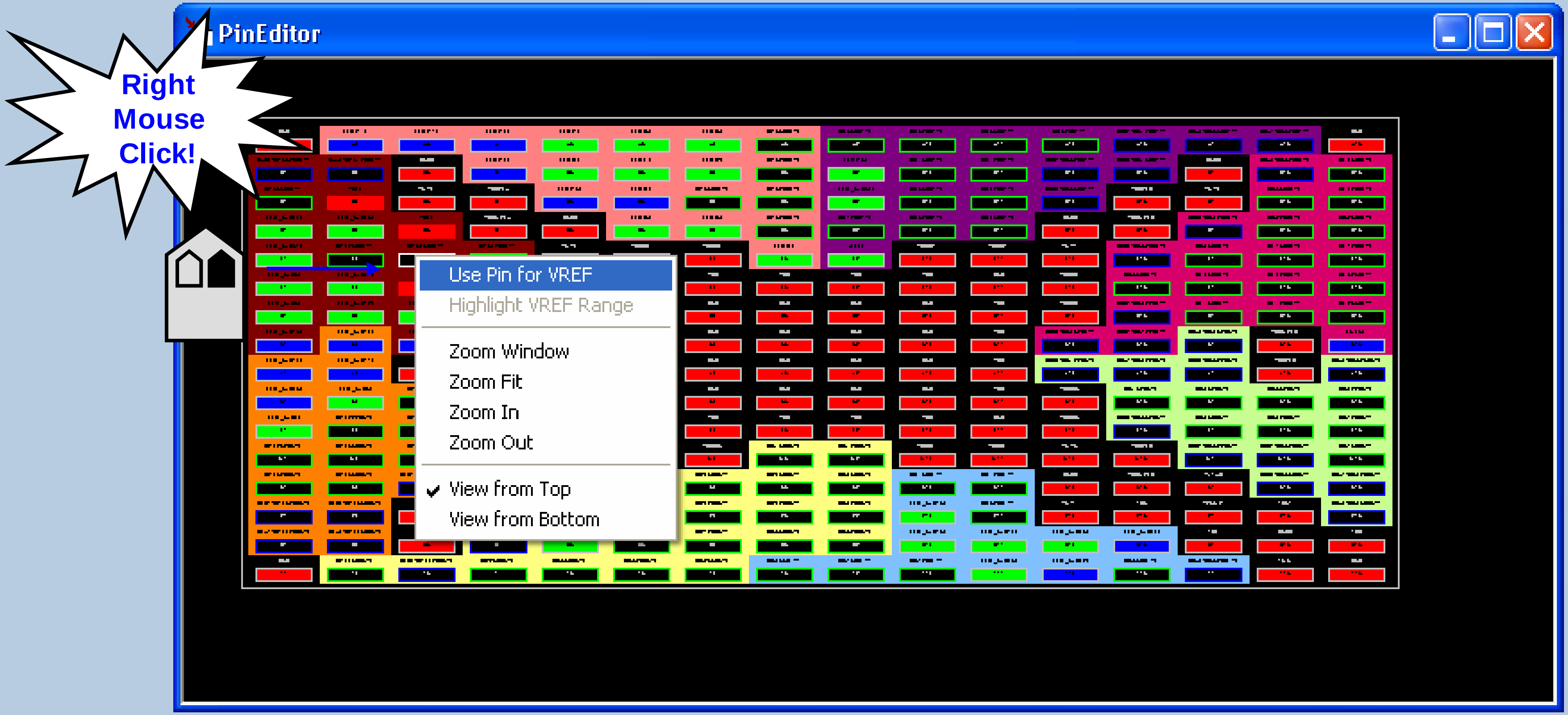
VREF: 0.75V

☑ Use default pins for VREFs

# VREF Pin Assignment
*Axcelerator and ProASIC3E*

## Select Package Pin And Click Right Mouse Button

- **Select "Use Pin for VREF"**



# Designer
## *Automatic I/O Bank Assignment*

- I/O Bank Assigner for A3P/E and AX
  - **Runs automatically during layout**
  - **Is available when at least one I/O bank is unassigned**
  - **Automatically assigns voltages to I/O banks that do not have I/Os assigned**
    - **Fills them with compatible I/Os**
  - **Assigns VREF pins if required**
  - **Respects manual assignment already in place**
  - **Maintains placement quality and performance**
    - **No impact on device performance**
  - **Can be controlled manually from within the MultiView Navigator**

# Pin Assignment Recommendations

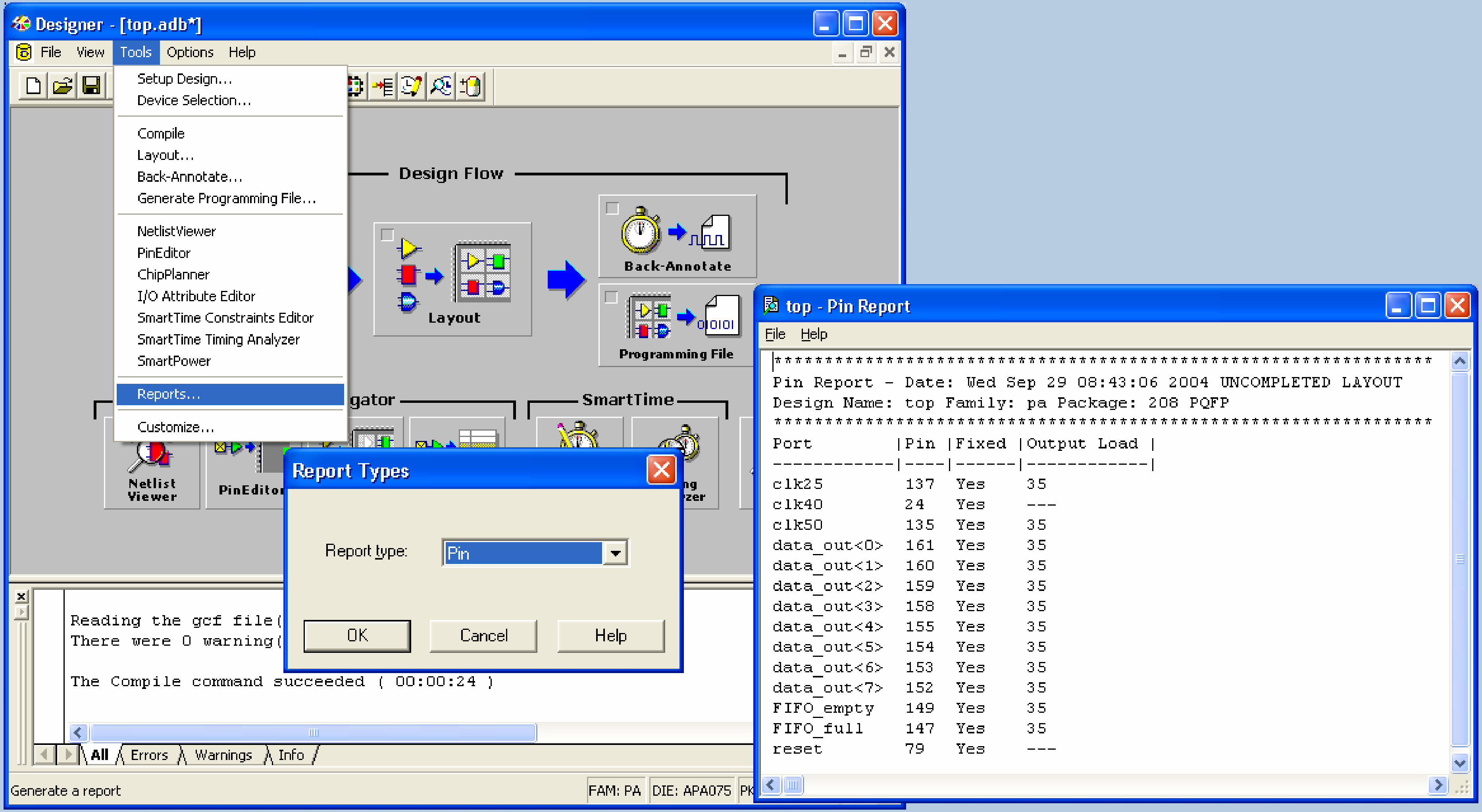
- Enter Design as Completely as Possible
  - **Don’t Worry about Functionality**
- Compile (Ignore Warnings) and Layout
- “Fix”All Pin Assignments

  **Edit > Select All then Edit > Fix**
- Send Pin Report to PCB Layout
- Continue Working Out Bugs
  - **Future Layouts Will Honor “Fixed” Assignments**

ONE CHIP is all you need

# Exporting Pin Report

## ■ Pin Report Can be Exported from Designer



Report type: Pin

```
Reading the gcf file(
There were 0 warning(

The Compile command succeeded ( 00:00:24 )
```

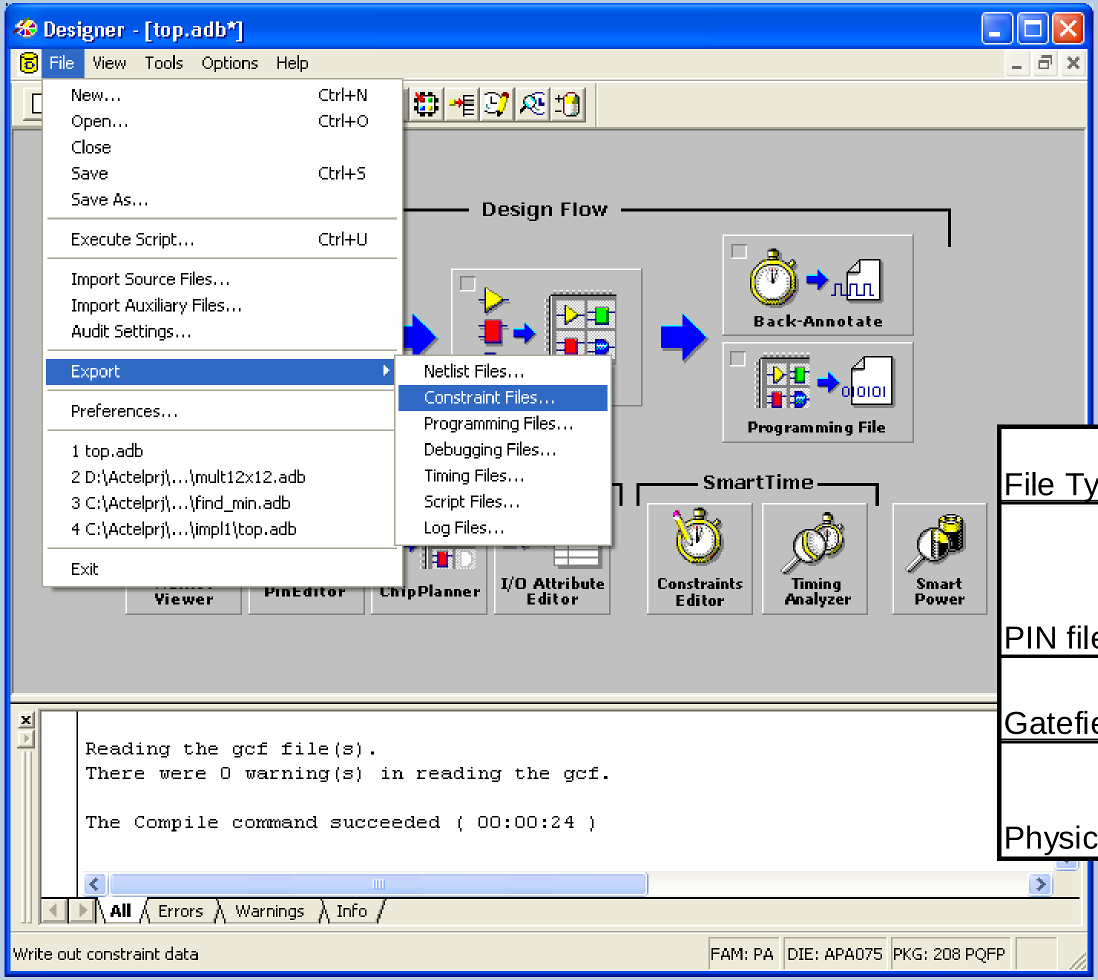
Generate a report

FAM: PA DIE: APA075 PK

```
**************************************************************************
Pin Report - Date: Wed Sep 29 08:43:06 2004 UNCOMPLETED LAYOUT
Design Name: top Family: pa Package: 208 PQFP
**************************************************************************
Port         |Pin |Fixed |Output Load |
-------------|----|------|------------|
clk25         137  Yes    35
clk40         24   Yes    ---
clk50         135  Yes    35
data_out<0>   161  Yes    35
data_out<1>   160  Yes    35
data_out<2>   159  Yes    35
data_out<3>   158  Yes    35
data_out<4>   155  Yes    35
data_out<5>   154  Yes    35
data_out<6>   153  Yes    35
data_out<7>   152  Yes    35
FIFO_empty    149  Yes    35
FIFO_full     147  Yes    35
reset         79   Yes    ---
```

# Exporting Pin Constraint File

- Pin Constraint File Can be Exported from Designer



```
Reading the gcf file(s).
There were 0 warning(s) in reading the gcf.

The Compile command succeeded ( 00:00:24 )
```

Write out constraint data

FAM: PA DIE: APA075 PKG: 208 PQFP

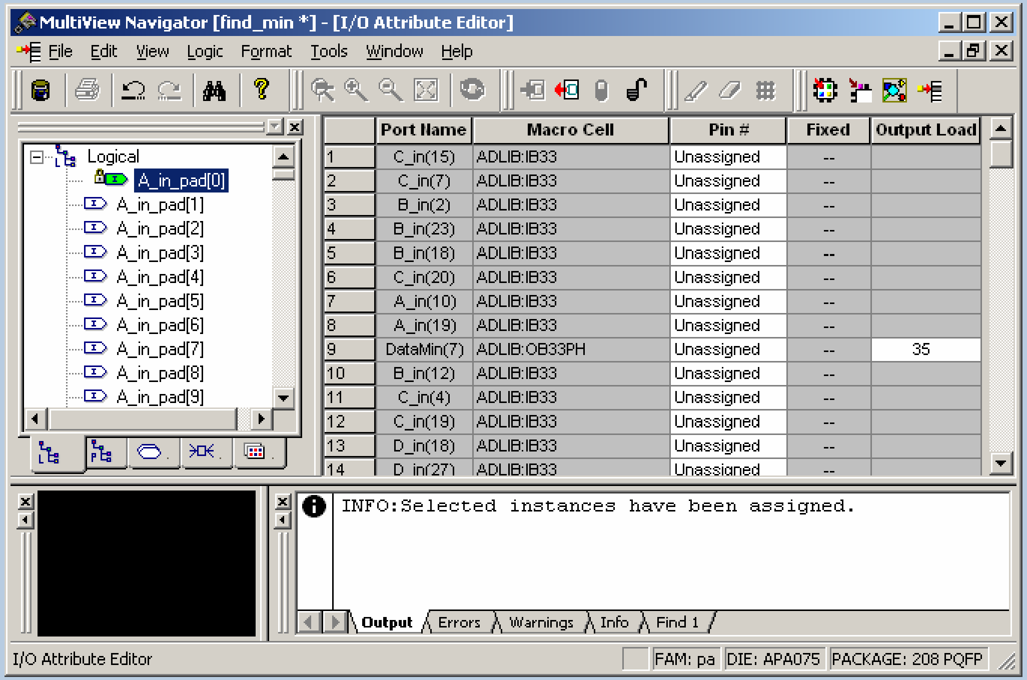
| File Type | File Extension | Family |
|---|---|---|
| PIN file | *.pin | ACT1, ACT2, ACT3, MX, XL, DX, SX, SX-A, eX |
| Gatefield Constraint file | *.gcf | ProASIC, ProASIC$^{PLUS}$ |
| Physical Design Constraint | *.pdc | Axcelerator, ProASIC3\E, Fusion |

ONECHIP is all you need

# I/O Attribute Editor

# MultiView Navigator
## *I/O Attribute Editor*

- Input/Output Attribute Editor
  - **Select (Varies by Family):**
    - **I/O Standard**
    - **I/O Threshold**
    - **Slew Rate**
    - **I/O Power-up State**
  - **Enter Load Capacitance of Load**
    - **Does Not Change SDF File Generation**
- Spreadsheet-like Sort, Copy, Paste



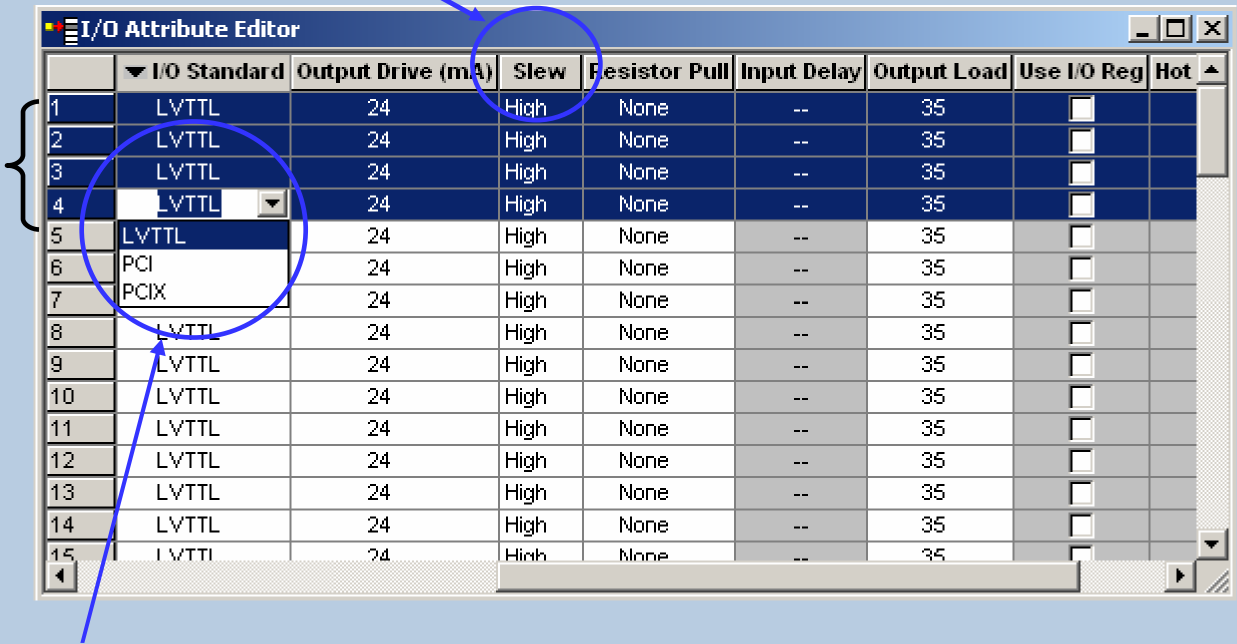
| | Port Name | Macro Cell | Pin # | Fixed | Output Load |
|---|---|---|---|---|---|
| 1 | C_in(15) | ADLIB:IB33 | Unassigned | -- | |
| 2 | C_in(7) | ADLIB:IB33 | Unassigned | -- | |
| 3 | B_in(2) | ADLIB:IB33 | Unassigned | -- | |
| 4 | B_in(23) | ADLIB:IB33 | Unassigned | -- | |
| 5 | B_in(18) | ADLIB:IB33 | Unassigned | -- | |
| 6 | C_in(20) | ADLIB:IB33 | Unassigned | -- | |
| 7 | A_in(10) | ADLIB:IB33 | Unassigned | -- | |
| 8 | A_in(19) | ADLIB:IB33 | Unassigned | -- | |
| 9 | DataMin(7) | ADLIB:OB33PH | Unassigned | -- | 35 |
| 10 | B_in(12) | ADLIB:IB33 | Unassigned | -- | |
| 11 | C_in(4) | ADLIB:IB33 | Unassigned | -- | |
| 12 | C_in(19) | ADLIB:IB33 | Unassigned | -- | |
| 13 | D_in(18) | ADLIB:IB33 | Unassigned | -- | |
| 14 | D_in(27) | ADLIB:IB33 | Unassigned | -- | |

```
INFO:Selected instances have been assigned.
```

# MultiView Navigator
## *I/O Attribute Editor (cont.)*

Double click on column to sort display by that column

Hold down CTRL key to select multiple rows



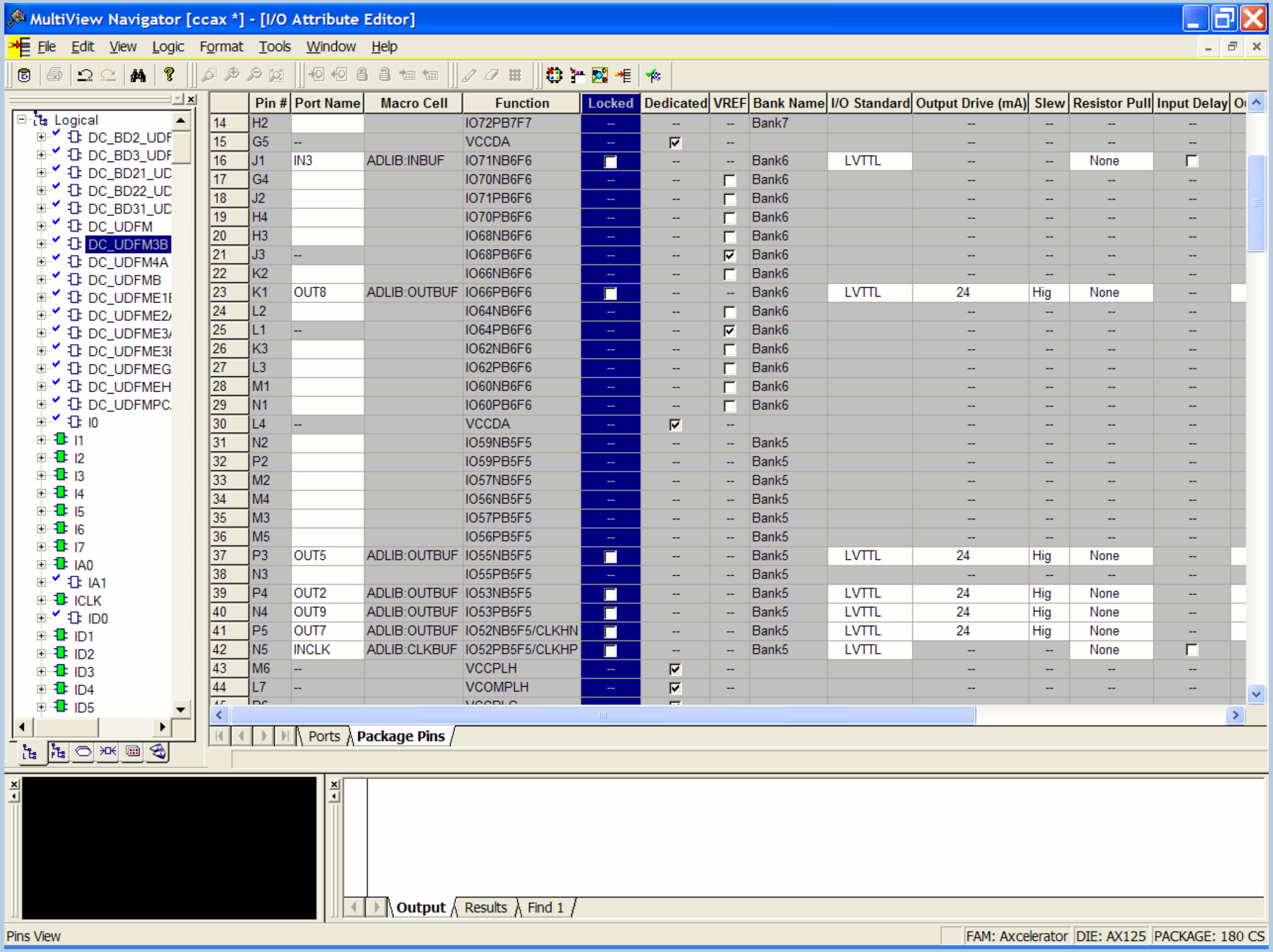
I/O Attribute Editor

|  | ▼ I/O Standard | Output Drive (mA) | Slew | Resistor Pull | Input Delay | Output Load | Use I/O Reg | Hot |
|---|---|---|---|---|---|---|---|---|
| 1 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 2 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 3 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 4 | LVTTL ▼ | 24 | High | None | -- | 35 | □ |  |
| 5 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 6 | PCI | 24 | High | None | -- | 35 | □ |  |
| 7 | PCIX | 24 | High | None | -- | 35 | □ |  |
| 8 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 9 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 10 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 11 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 12 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 13 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 14 | LVTTL | 24 | High | None | -- | 35 | □ |  |
| 15 | LVTTL | 24 | High | None | -- | 35 | □ |  |

With multiple rows selected, changing the value of a drop-down item with CTRL key pressed will change the value for all rows

# MultiView Navigator
## *Package Pins View*

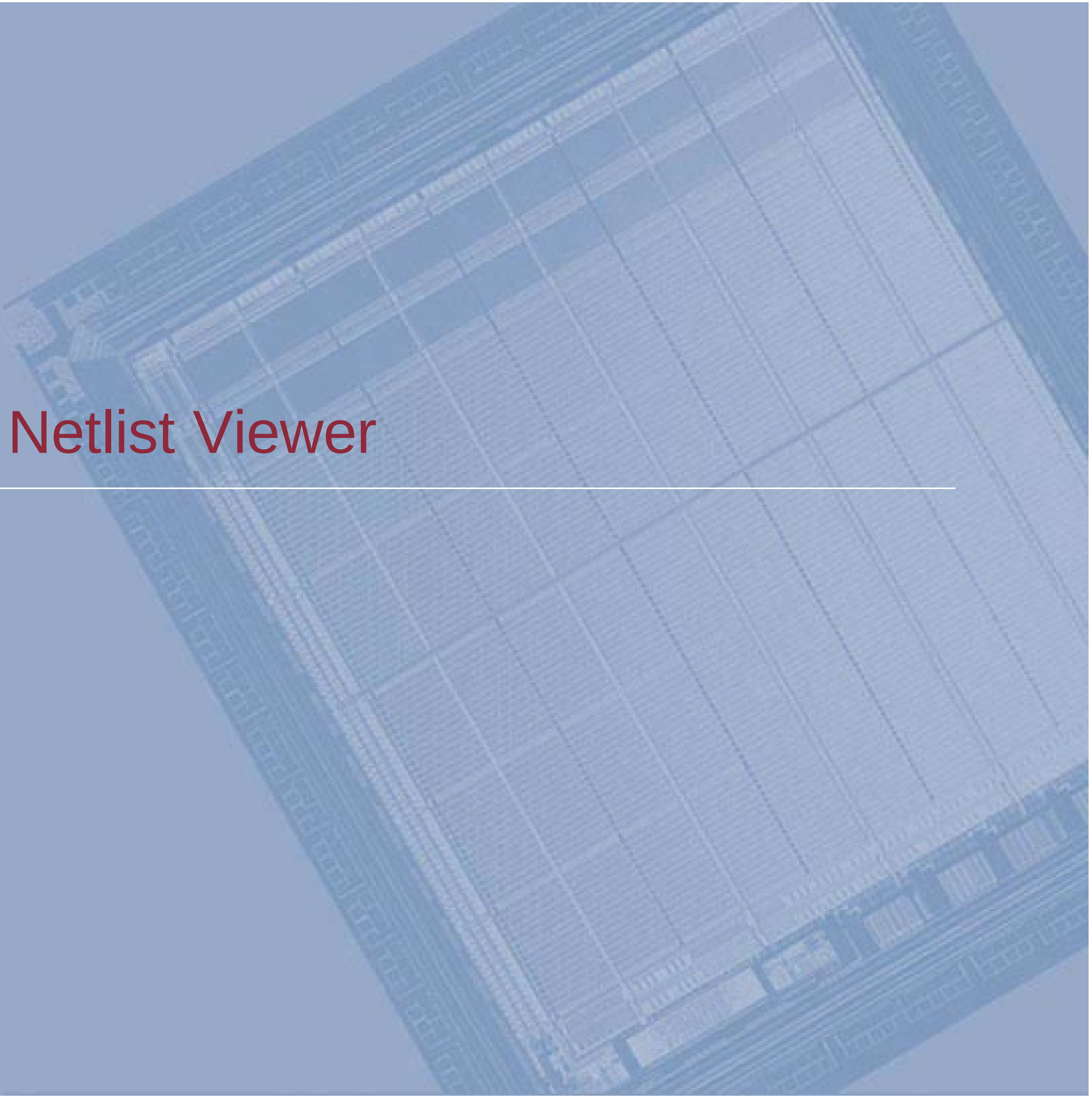
- Package Pins View Shows All Pins on Package



| | Pin # | Port Name | Macro Cell | Function | Locked | Dedicated | VREF | Bank Name | I/O Standard | Output Drive (mA) | Slew | Resistor Pull | Input Delay | O |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 14 | H2 | | | IO72PB7F7 | -- | -- | -- | Bank7 | | -- | -- | -- | -- | |
| 15 | G5 | -- | | VCCDA | -- | ☑ | -- | | | -- | -- | -- | -- | |
| 16 | J1 | IN3 | ADLIB:INBUF | IO71NB6F6 | □ | -- | -- | Bank6 | LVTTL | -- | -- | None | □ | |
| 17 | G4 | | | IO70NB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 18 | J2 | | | IO71PB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 19 | H4 | | | IO70PB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 20 | H3 | | | IO68NB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 21 | J3 | -- | | IO68PB6F6 | -- | -- | ☑ | Bank6 | | -- | -- | -- | -- | |
| 22 | K2 | | | IO66NB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 23 | K1 | OUT8 | ADLIB:OUTBUF | IO66PB6F6 | □ | -- | -- | Bank6 | LVTTL | 24 | Hig | None | -- | |
| 24 | L2 | | | IO64NB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 25 | L1 | -- | | IO64PB6F6 | -- | -- | ☑ | Bank6 | | -- | -- | -- | -- | |
| 26 | K3 | | | IO62NB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 27 | L3 | | | IO62PB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 28 | M1 | | | IO60NB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 29 | N1 | | | IO60PB6F6 | -- | -- | □ | Bank6 | | -- | -- | -- | -- | |
| 30 | L4 | -- | | VCCDA | -- | ☑ | -- | | | -- | -- | -- | -- | |
| 31 | N2 | | | IO59NB5F5 | -- | -- | -- | Bank5 | | -- | -- | -- | -- | |
| 32 | P2 | | | IO59PB5F5 | -- | -- | -- | Bank5 | | -- | -- | -- | -- | |
| 33 | M2 | | | IO57NB5F5 | -- | -- | -- | Bank5 | | -- | -- | -- | -- | |
| 34 | M4 | | | IO56NB5F5 | -- | -- | -- | Bank5 | | -- | -- | -- | -- | |
| 35 | M3 | | | IO57PB5F5 | -- | -- | -- | Bank5 | | -- | -- | -- | -- | |
| 36 | M5 | | | IO56PB5F5 | -- | -- | -- | Bank5 | | -- | -- | -- | -- | |
| 37 | P3 | OUT5 | ADLIB:OUTBUF | IO55NB5F5 | □ | -- | -- | Bank5 | LVTTL | 24 | Hig | None | -- | |
| 38 | N3 | | | IO55PB5F5 | -- | -- | -- | Bank5 | | -- | -- | -- | -- | |
| 39 | P4 | OUT2 | ADLIB:OUTBUF | IO53NB5F5 | □ | -- | -- | Bank5 | LVTTL | 24 | Hig | None | -- | |
| 40 | N4 | OUT9 | ADLIB:OUTBUF | IO53PB5F5 | □ | -- | -- | Bank5 | LVTTL | 24 | Hig | None | -- | |
| 41 | P5 | OUT7 | ADLIB:OUTBUF | IO52NB5F5/CLKHN | □ | -- | -- | Bank5 | LVTTL | 24 | Hig | None | -- | |
| 42 | N5 | INCLK | ADLIB:CLKBUF | IO52PB5F5/CLKHP | □ | -- | -- | Bank5 | LVTTL | -- | -- | None | □ | |
| 43 | M6 | -- | | VCCPLH | -- | ☑ | -- | | | -- | -- | -- | -- | |
| 44 | L7 | -- | | VCOMPLH | -- | ☑ | -- | | | -- | -- | -- | -- | |

Pins View

FAM: Axcelerator | DIE: AX125 | PACKAGE: 180 CS

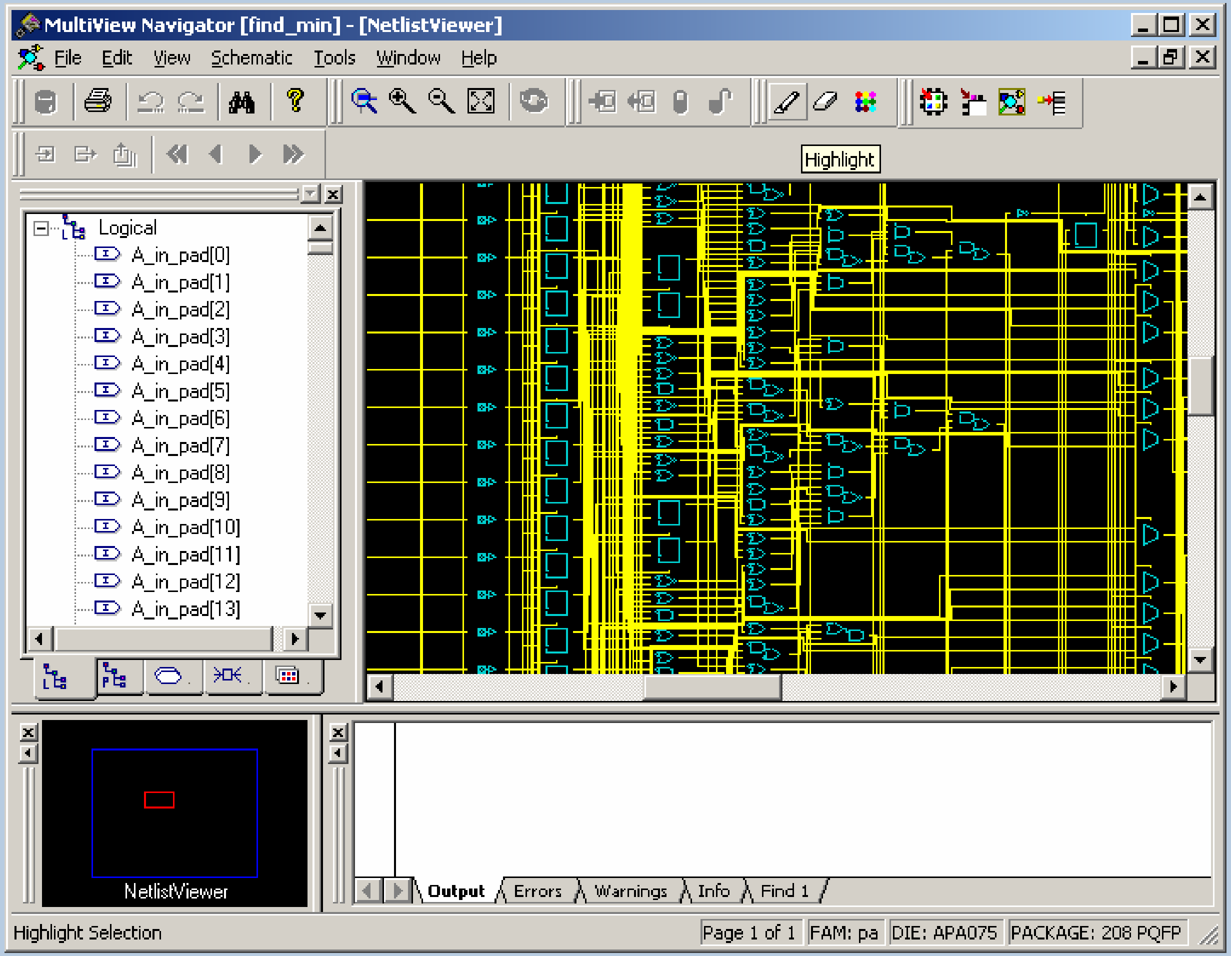


# Netlist Viewer

Actel

# MultiView Navigator
## *Netlist Viewer*

- Displays Netlist in Hierarchical Manner
  - **Explore each Level of Hierarchy and Trace Signals**



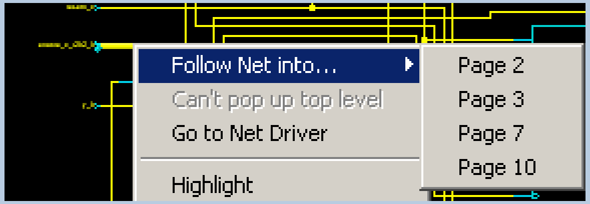
Schematic View Window – displays a graphical representation of the netlist

Search Window – shows results of searches

# MultiView Navigator
*Netlist Viewer (cont.)*

## Viewing Options

- **Push, Pop, Jump to Top**
- **Go to First Page, Go to Last Page, Go to Next Page, Go to Last Page**
- **Right-click on Net to Follow Net to Other Pages or Net Driver**



Follow Net into...
Can't pop up top level
Go to Net Driver
Highlight

Page 2
Page 3
Page 7
Page 10

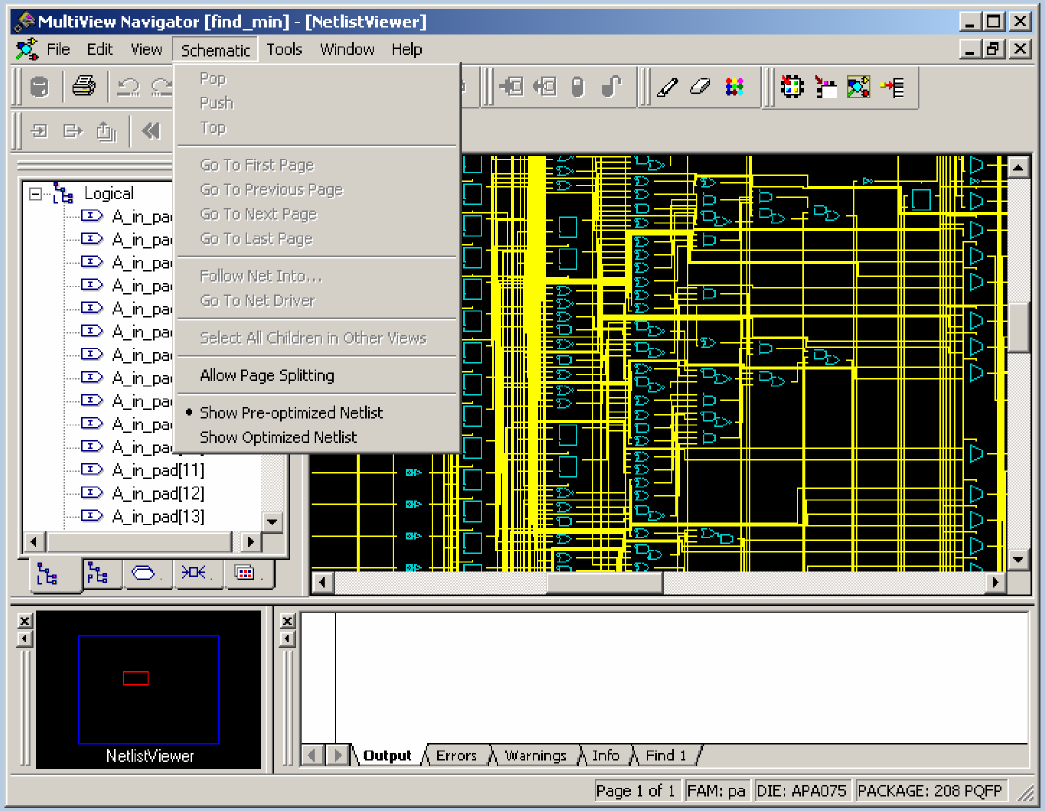
- **Highlight, Highlight Append, un-Highlight, un-Highlight All**
- **Allows Page Splitting**

✓ Allow Page Splitting

  - **Allows User to Decide if All Elements on that Level Are Shown as Single Page**

# MultiView Navigator
## *Netlist Viewer (cont.)*

- View Pre- and Optimized Netlists for ProASIC3\E, ProASIC$^{\underline{PLUS}}$ and Axcelerator
  - **Pre-optimized Netlist Is Original Hierarchical Netlist**
  - **Optimized Netlist is Flattened**
    - **Reflects what other Tools Use (ChipEdit, PinEdit)**



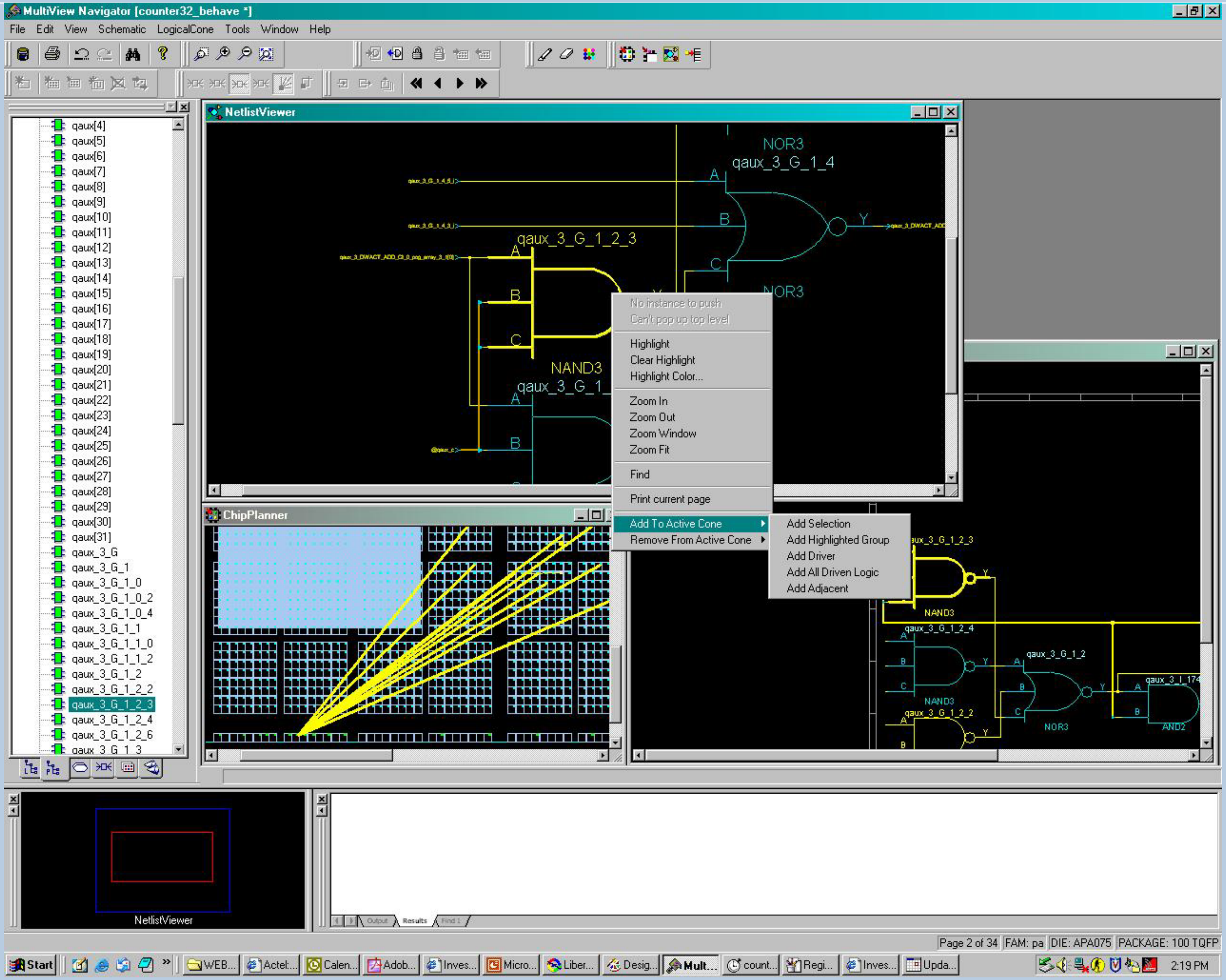
# MultiView Navigator
## *LogicalCone*

- Helps View Critical Portions of Netlist
  - Identify Critical Paths using SmartTime
  - Add this Logic to LogicalCone
  - Incrementally Add / Remove Logic from Cone
  - CrossProbe from / to LogicalCone
  - All NetlistView Features available in LogicalCone
  - New LogicalCone Tab in Hierarchy Window
  - New LogicalCone Menu Accessible from NetlistViewer
  - Can Simultaneously Create Multiple Cones
  - Set of Macros Can Be Highlighted, then Added to Cone
  - LogicalCone Data No Longer Valid after Recompile
  - Applies to All Families Supported by MVN

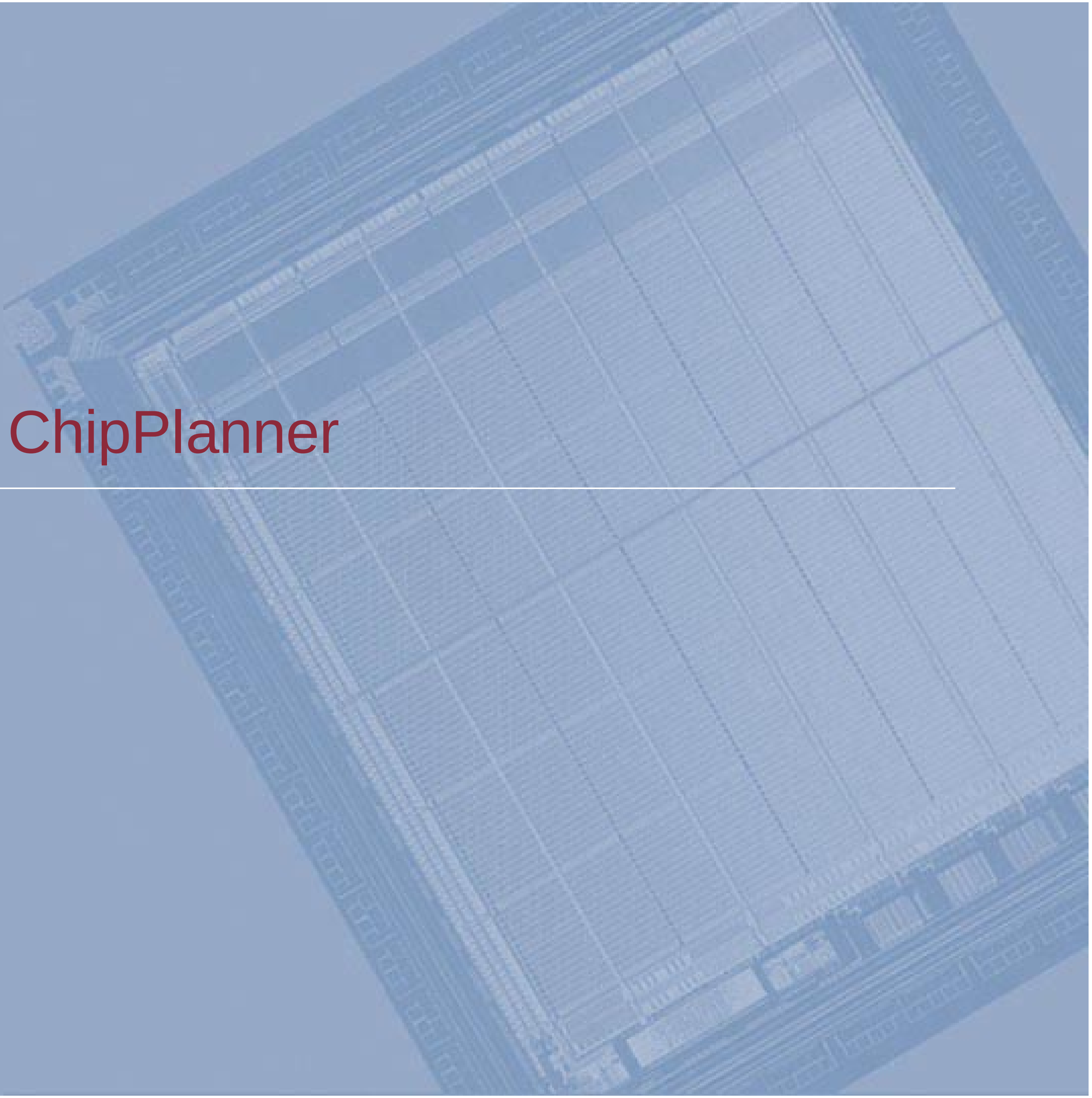
ONE CHIP is all you need

# LogicalCone

## *User Interface*



# ChipPlanner



# ChipPlanner

- Editing and Floorplanning Support for:
  - Fusion, ProASIC3\E, ProASIC$^{PLUS}$, ProASIC, Axcelerator, eX, SX-A and SX-S Families
  - Use ChipEditor for All other Actel FPGA Families
- ChipPlanner Capabilities:
  - Editing
    - Place, Unplace, or Move Logic and I/O
    - View Macro Placements Made during Layout
    - View Net Connections with Ratsnest or Route View
    - View Architectural Boundaries
    - View and Edit Silicon Features, such as I/O Banks
    - View Placement and Routing of Paths when Used with SmartTime
  - Floorplanning
    - Create and Assign Logic or Nets to Regions
  - Cross-probe with Silicon Explorer to Select Probes

# ChipPlanner Terminology

## Region

- **Defined sub-Portion of Die**
- **Shapes - Rectangular or Rectilinear (Union of Rectangles)**
- **Types:**
  - **Empty - No Logic Can Be Put into this Region**
  - **Inclusive - Assigned Logic *Must* Be Put into this Region**
    - ***Other Unassigned Logic Can Be Added to this Region by Layout***
  - **Exclusive - Only Assigned Logic Can Be Put into this Region**
    - ***Not Supported for APA or A500K***

## Assign

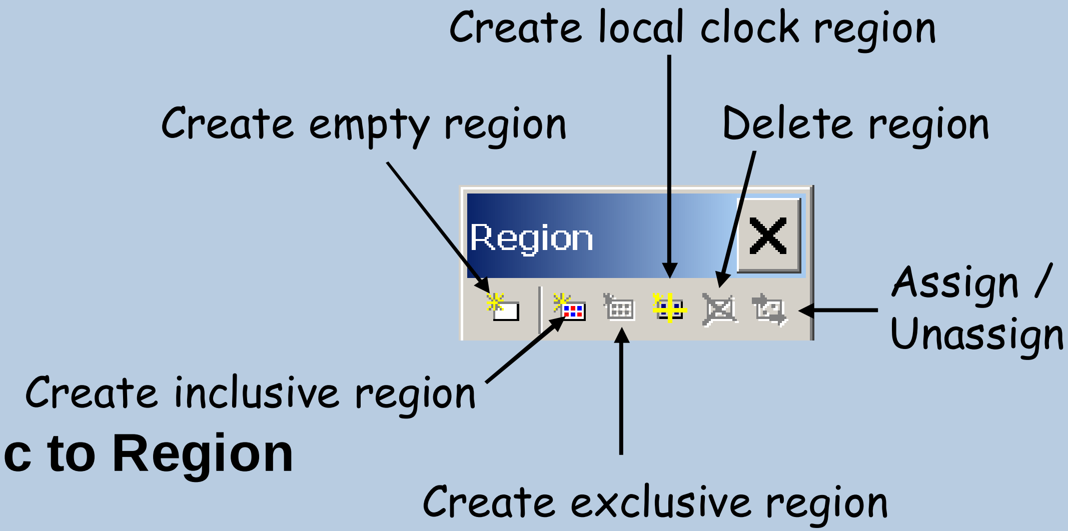
- **Place Logic into Particular Region or Location**
  - **Similar to "Place" in ChipEditor**

## Lock

- **Finalizes Allocation of Logic in Particular Location**
  - **Similar to "Fix" in ChipEditor**

# ChipPlanner
## *Editing and Floorplanning*

- Drag Logic or I/O to Desired Location
- ChipPlanner Floorplanning Functions
  - Create Logic Region
  - Create Empty Region
  - Select Region
  - Move Region
  - Delete Region
  - Resize Region
  - Assign/Unassign Logic to Region

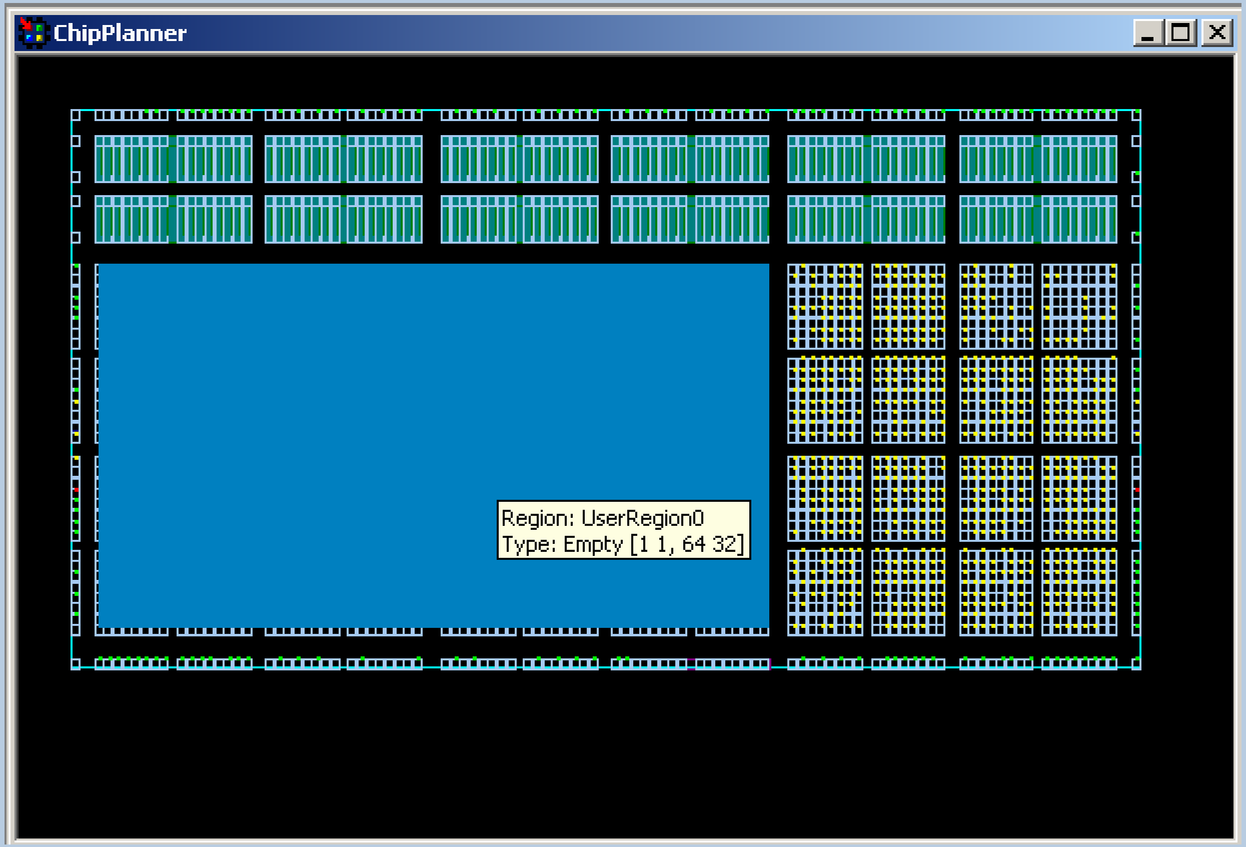


- Regions Can Span Logic, Memory Cells and I/O

# ChipPlanner
## *Empty Region*

## Region > Create Empty

- **No Logic Assigned to Empty Regions**

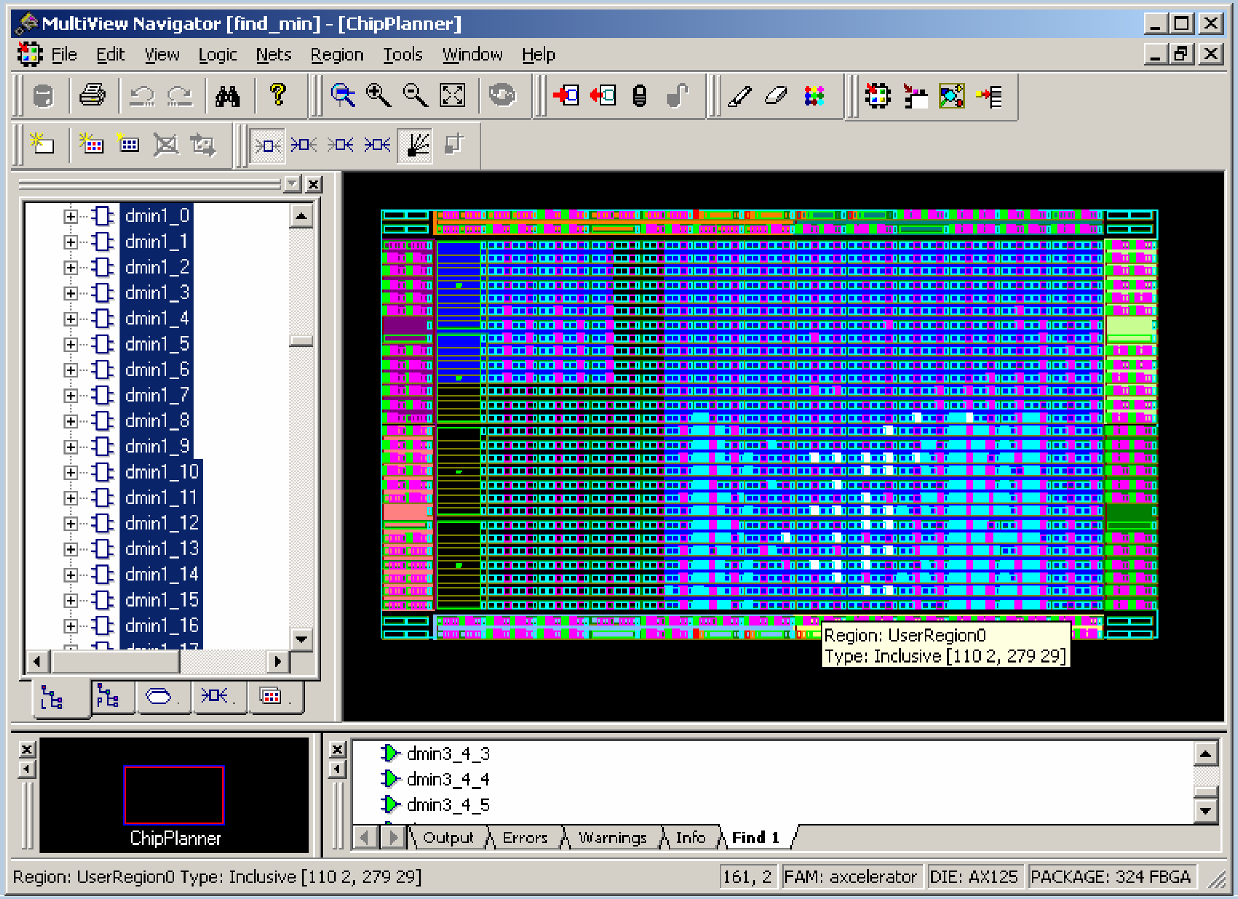


Region: UserRegion0
Type: Empty [1 1, 64 32]

# ChipPlanner
*Inclusive Region*

## Region > Create Inclusive

- Assigned Logic Put in Inclusive Region
  - Other Logic May also Be Put in this Region



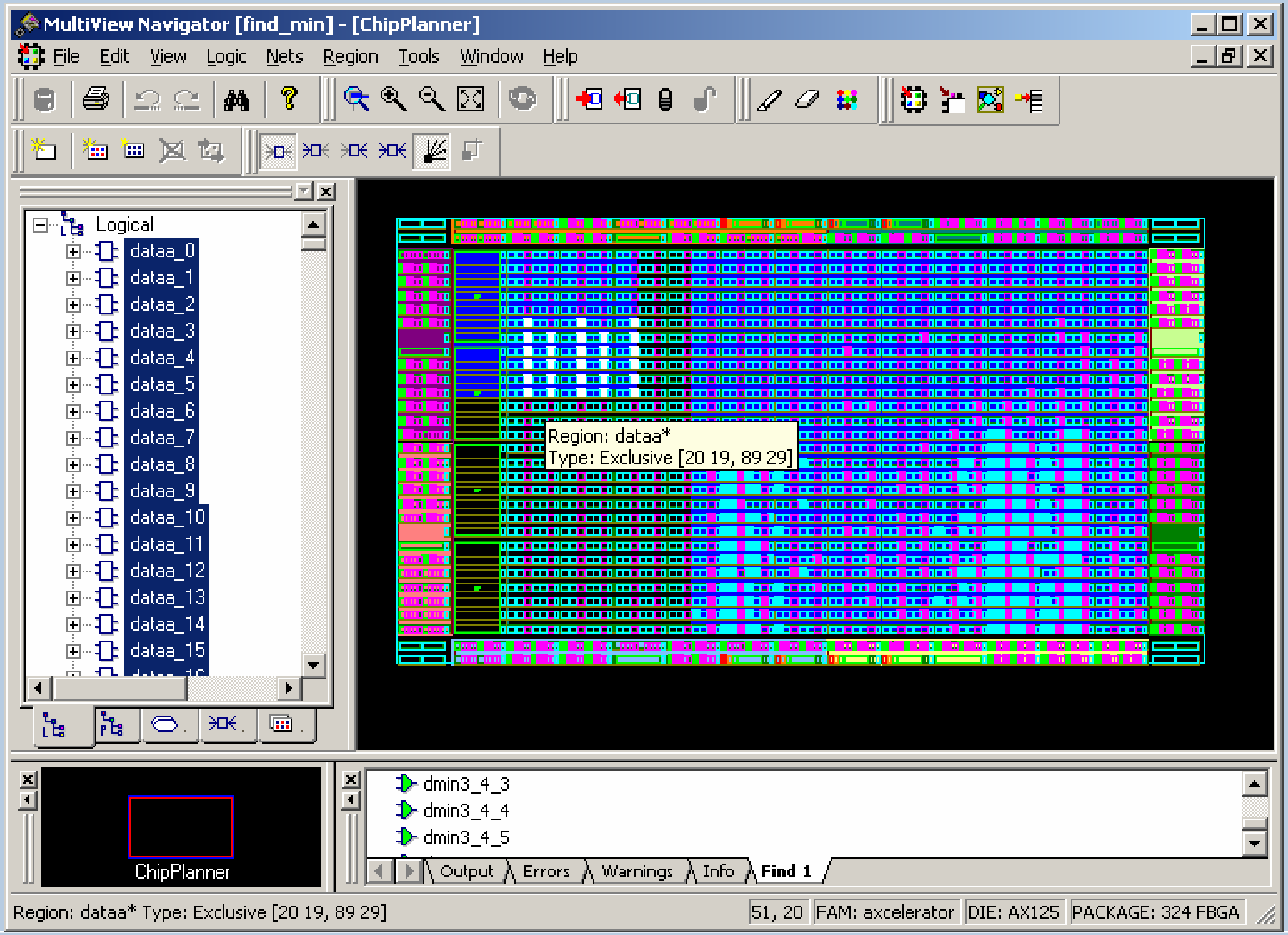
Region: UserRegion0
Type: Inclusive [110 2, 279 29]

Region: UserRegion0 Type: Inclusive [110 2, 279 29] | 161, 2 | FAM: axcelerator | DIE: AX125 | PACKAGE: 324 FBGA

# ChipPlanner
## *Exclusive Region (Axcelerator and ProASIC3/E)*

## ■ Region > Create Exclusive

- **Only assigned logic placed in exclusive region**



Region: dataa*
Type: Exclusive [20 19, 89 29]

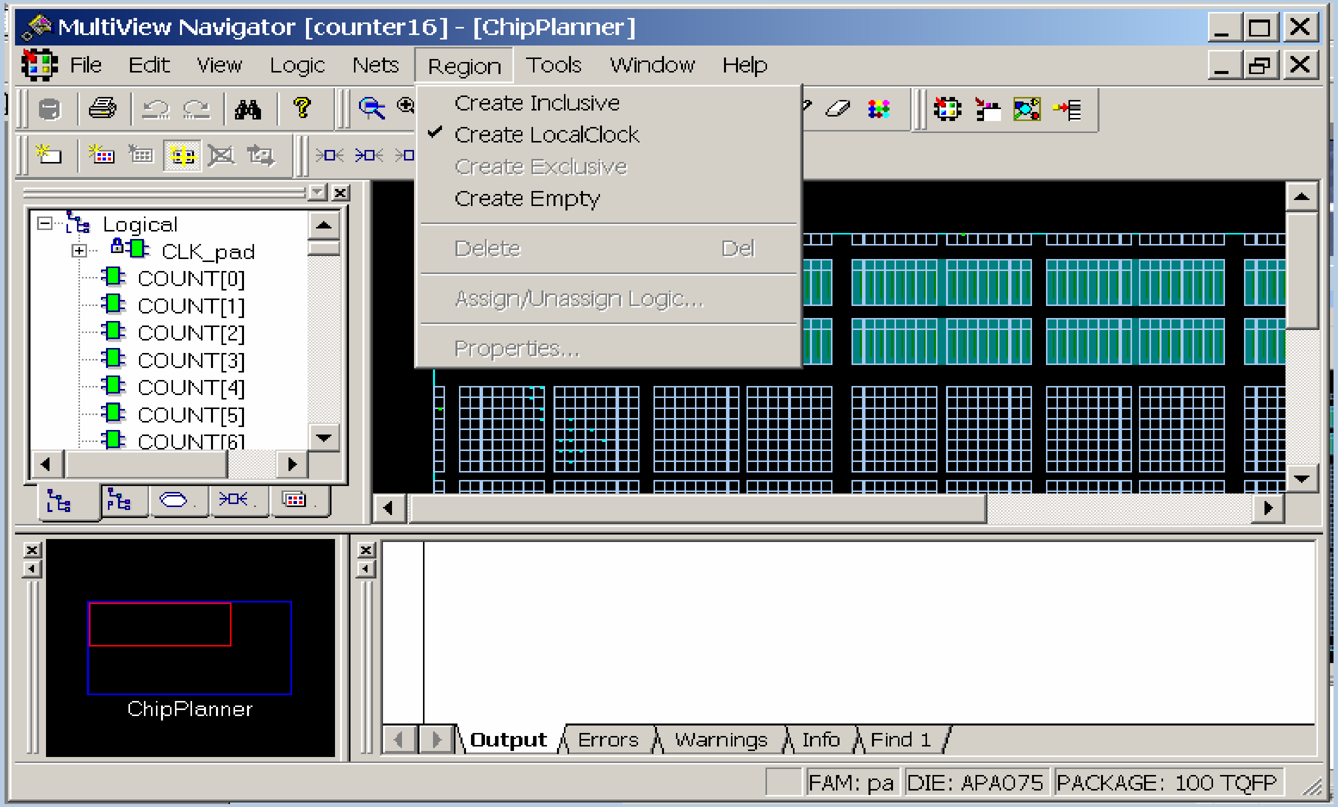
Region: dataa* Type: Exclusive [20 19, 89 29] 51, 20 FAM: axcelerator DIE: AX125 PACKAGE: 324 FBGA

# ChipPlanner

## *Local Clock Region (ProASIC$^{PLUS}$)*

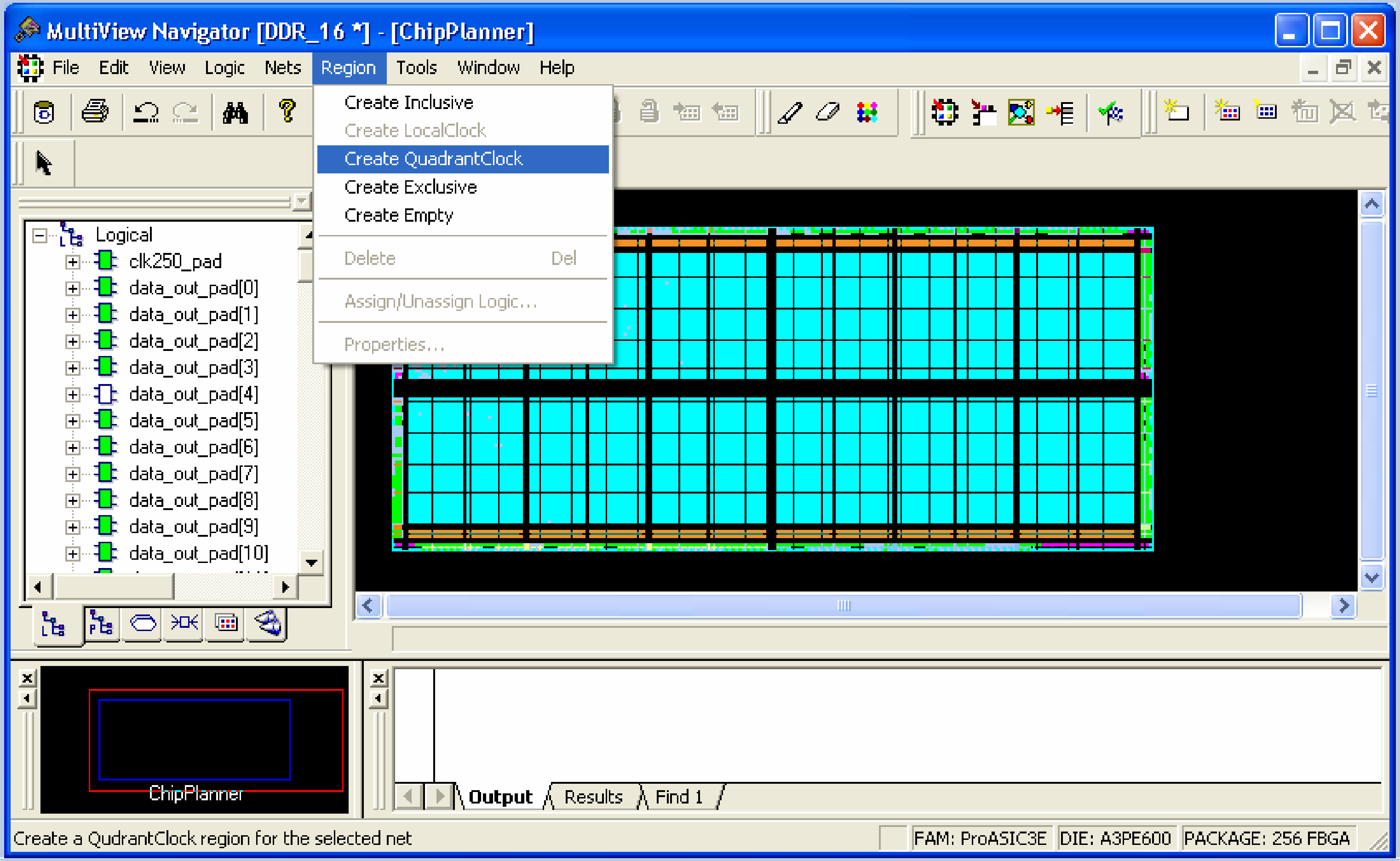
## Region > Create Local Clock

- Assign net to a spine region graphically
- All logic connected with the net will be assigned to the spine region



# ChipPlanner
## *Quadrant Clock Region (ProASIC3/E)*

- Region > Create QuadrantClock
  - **Graphically Assign net to a Quadrant Clock**



Create a QudrantClock region for the selected net

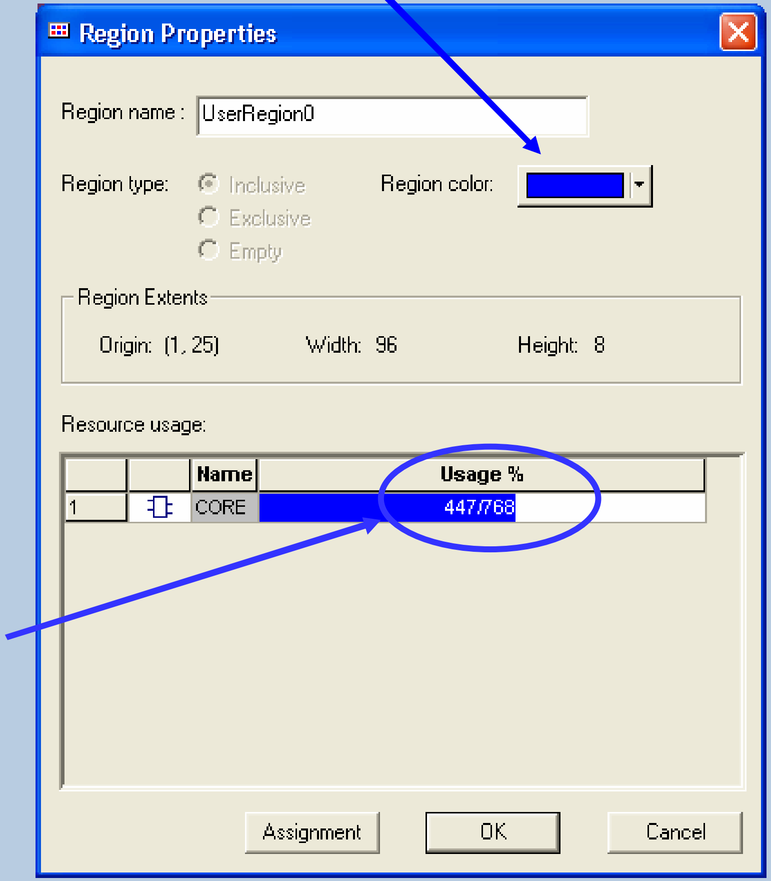
FAM: ProASIC3E DIE: A3PE600 PACKAGE: 256 FBGA

# ChipPlanner
## *Region Color Control*

- Individual Region Color Control
  - Regions Have Different Default Colors Based on Types
  - Can Change Each Region’s Default Color
  - Region Colors Saved in .adb File
  - Region Colors Reset to Defaults upon Recompile

# ChipPlanner
## *Region Properties*

- Region > Properties
- Indicates:
  - **Region Type**
  - **Region Width, Height and Origin**
  - **Region Usage**
- Shows Region Default Color
  - **Default Color Can be Changed**
- Also Provides Access to Assignment Window



Change region color

Region size and utilization

Region Properties

Region name : UserRegion0

Region type: ● Inclusive ○ Exclusive ○ Empty

Region color: 🟦

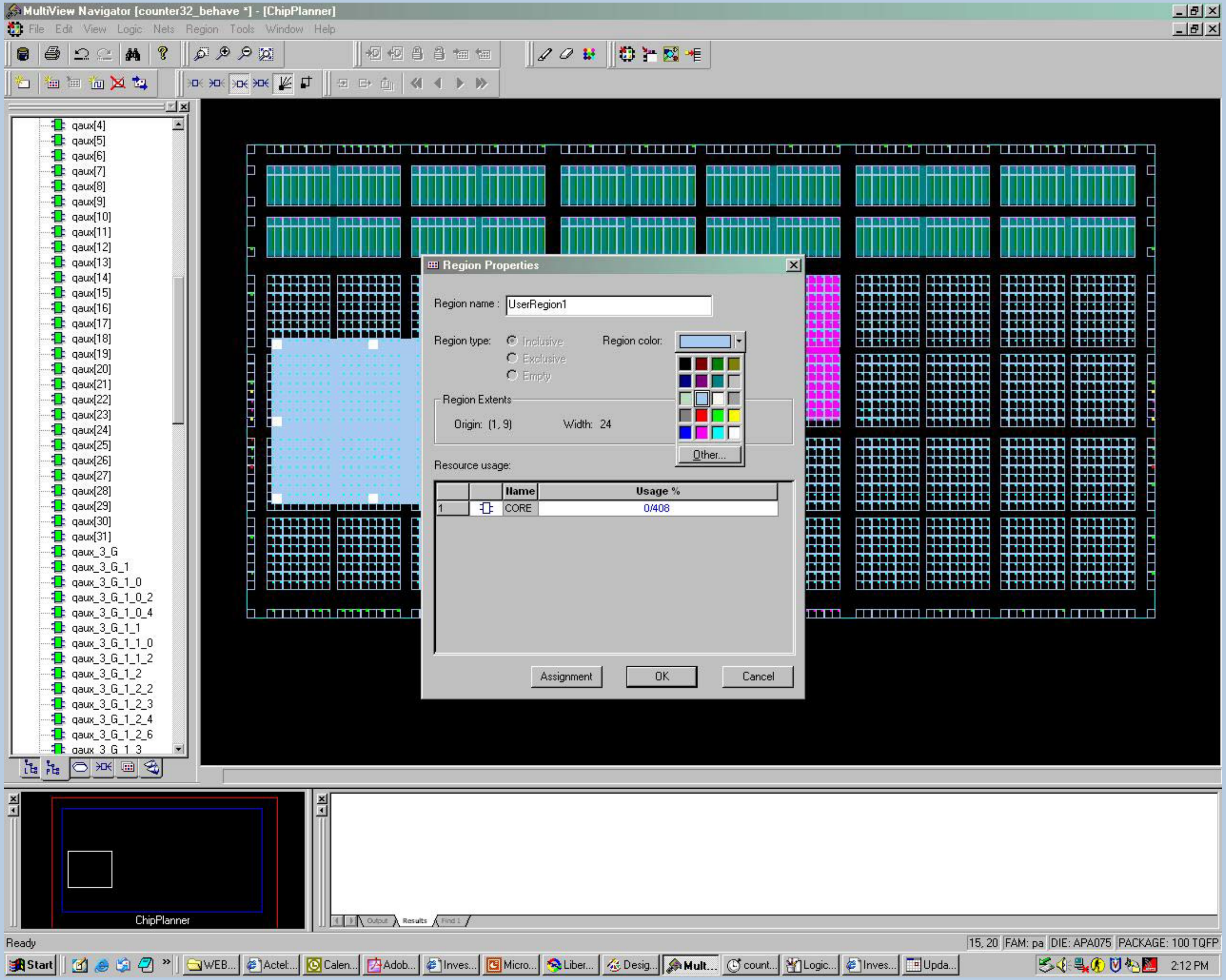
Region Extents

Origin: (1, 25) Width: 96 Height: 8

Resource usage:

| | | Name | Usage % |
|---|---|---|---|
| 1 | | CORE | 447/768 |

# MultiView Navigator
## *Region Color Control Example*



Region name : UserRegion1

Region type: ○ Inclusive ○ Exclusive ○ Empty

Region color:

Region Extents

Origin: (1, 9) Width: 24

Resource usage:

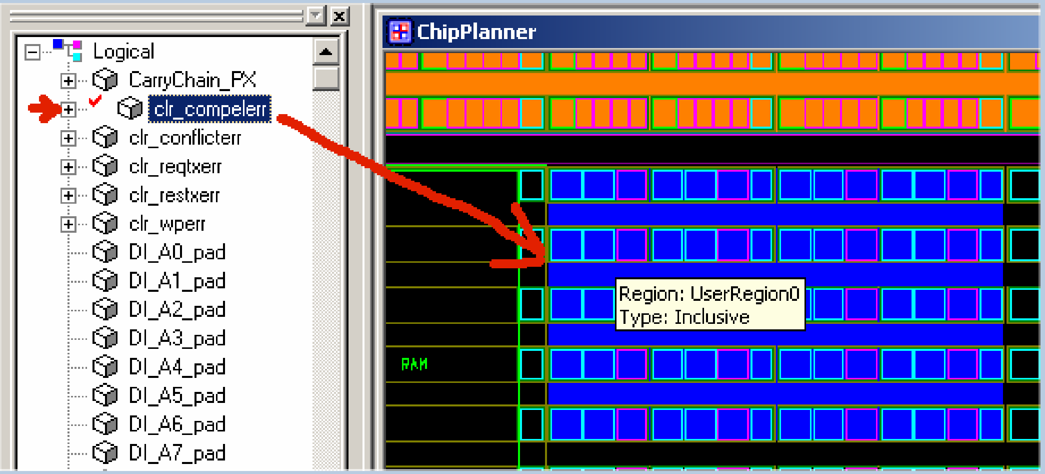
| | | Name | Usage % |
|---|---|---|---|
| 1 | | CORE | 0/408 |

Ready

15, 20 | FAM: pa | DIE: APA075 | PACKAGE: 100 TQFP

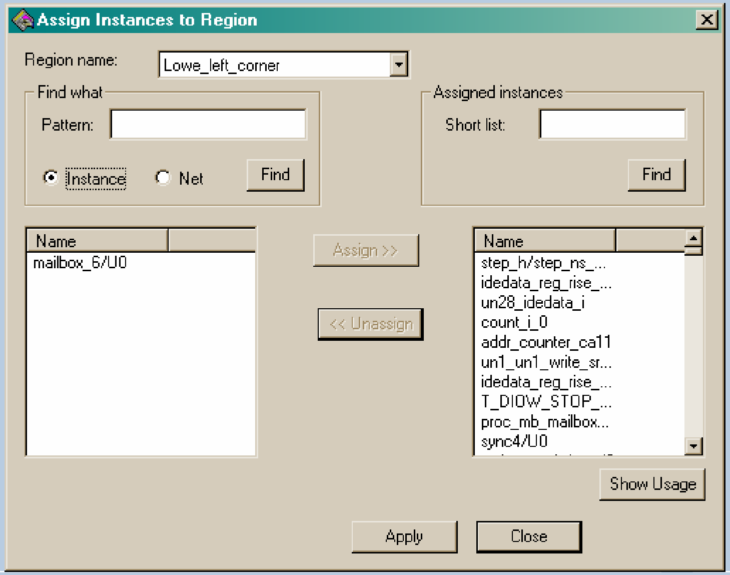
# ChipPlanner
## *Logic Assignment*

- Two Logic Assignment Methods
  - **Assignment Window (Region > Assign/Unassign Logic…)**
    - **Provides Search and Selection Capability**
    - **Also Available from Region Properties Dialog Box**
  - **Drag and Drop Logic into Region**
- Checkmark Indicates Assigned Logic



Logical
CarryChain_PX
✓ clr_compelerr
clr_conflicterr
clr_reqtxerr
clr_restxerr
clr_wperr
DI_A0_pad
DI_A1_pad
DI_A2_pad
DI_A3_pad
DI_A4_pad
DI_A5_pad
DI_A6_pad
DI_A7_pad

Region: UserRegion0
Type: Inclusive



Region name: Lowe_left_corner

Find what
Pattern:
● Instance ○ Net

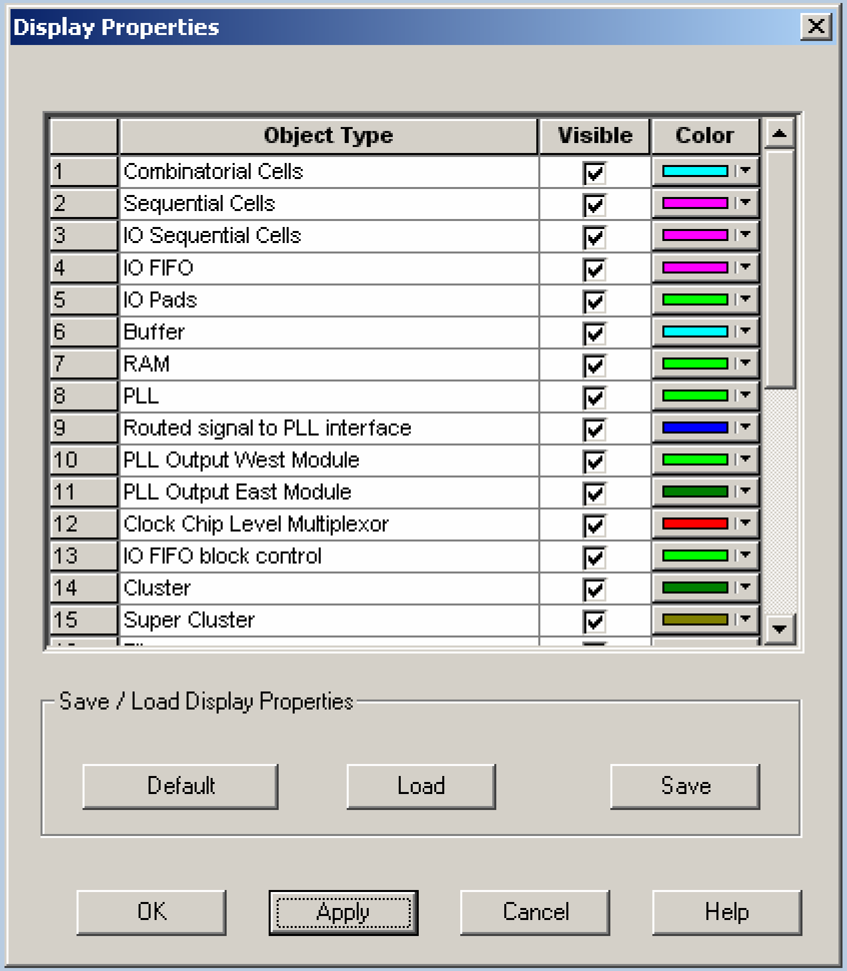
Assigned instances
Short list:

Name
mailbox_6/U0

Name
step_h/step_ns_...
idedata_reg_rise_...
un28_idedata_i
count_i_0
addr_counter_ca11
un1_un1_write_sr...
idedata_reg_rise_...
T_DIOW_STOP_...
proc_mb_mailbox...
sync4/U0

# ChipPlanner
## *Display Settings*

- Users Can Show/Hide Object and Assign Color to Resource
  - **View > Display Settings**



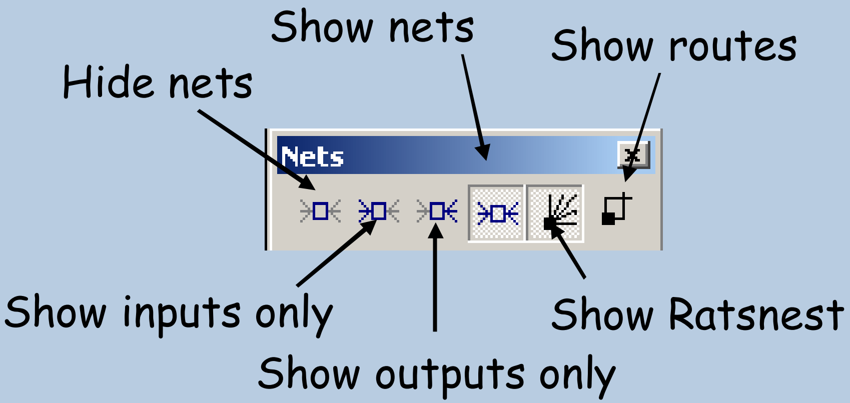
Display Properties

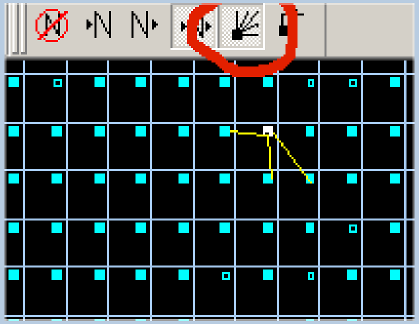
|  | Object Type | Visible | Color |
|---|---|---|---|
| 1 | Combinatorial Cells | ☑ | 🟦 |
| 2 | Sequential Cells | ☑ | 🟪 |
| 3 | IO Sequential Cells | ☑ | 🟪 |
| 4 | IO FIFO | ☑ | 🟪 |
| 5 | IO Pads | ☑ | 🟩 |
| 6 | Buffer | ☑ | 🟦 |
| 7 | RAM | ☑ | 🟩 |
| 8 | PLL | ☑ | 🟩 |
| 9 | Routed signal to PLL interface | ☑ | 🟦 |
| 10 | PLL Output West Module | ☑ | 🟩 |
| 11 | PLL Output East Module | ☑ | 🟩 |
| 12 | Clock Chip Level Multiplexor | ☑ | 🟥 |
| 13 | IO FIFO block control | ☑ | 🟩 |
| 14 | Cluster | ☑ | 🟩 |
| 15 | Super Cluster | ☑ | 🟫 |

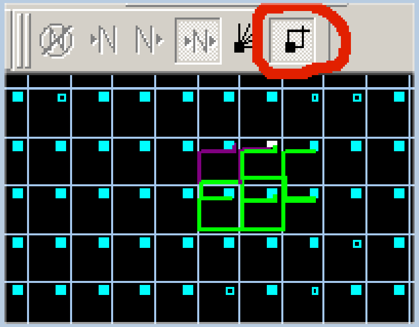
Save / Load Display Properties

# ChipPlanner
## *Viewing Nets*

- Select Net View Options from Nets Toolbar:
  - Display No Nets
  - Display Input Nets
  - Display Output Nets
  - Display Input and Output Nets
  - Display Ratsnest
  - Display Routes
    - Routes Option for ProASIC, ProASIC^PLUS, ProASIC3/E, Fusion

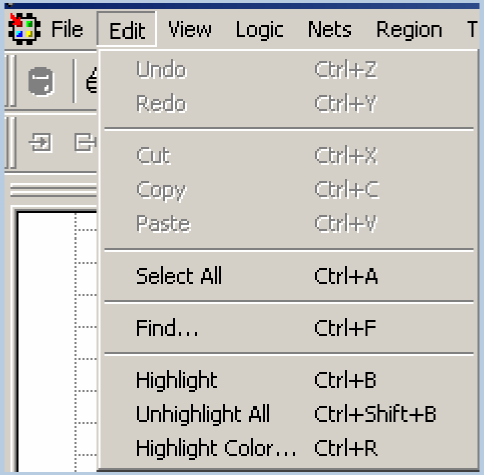


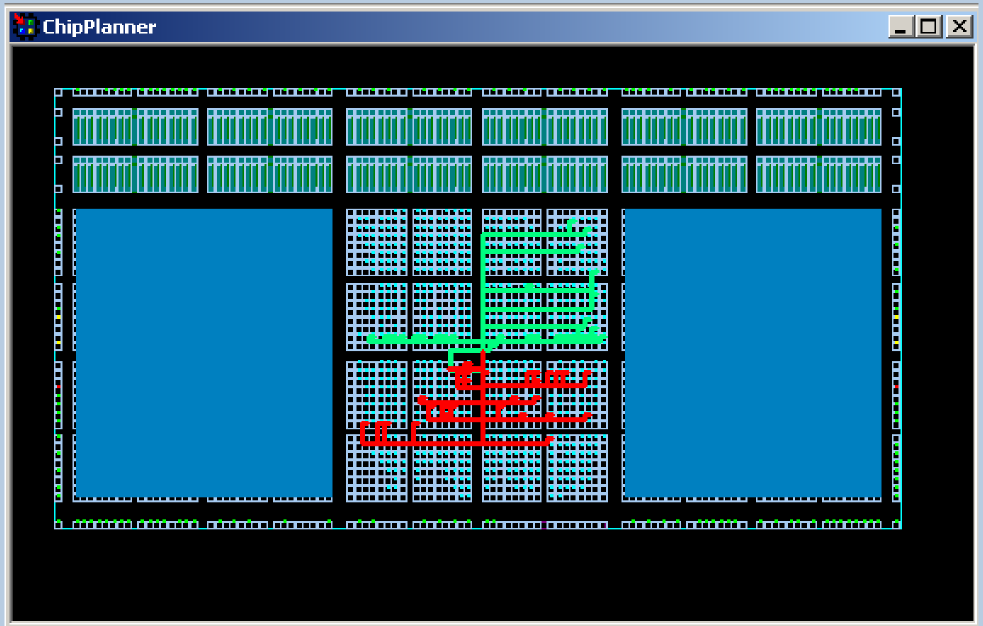

View Ratsnest

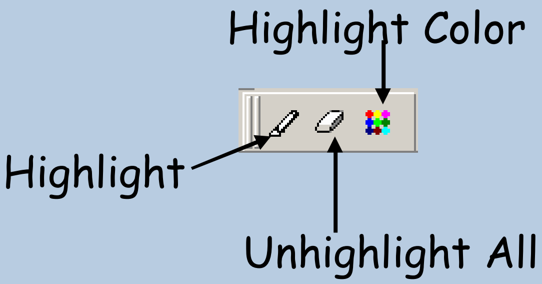

View Routes

# ChipPlanner
## *Highlighting Nets*

- Selected Nets Can Be Highlighted to Aid Analysis
  - **Select Net from Design Window Nets Tab or Search Results**
  - **Change Highlight Color from Toolbar or Edit Menu**







# ChipPlanner
## *ProASIC/ProASIC$^{PLUS}$*

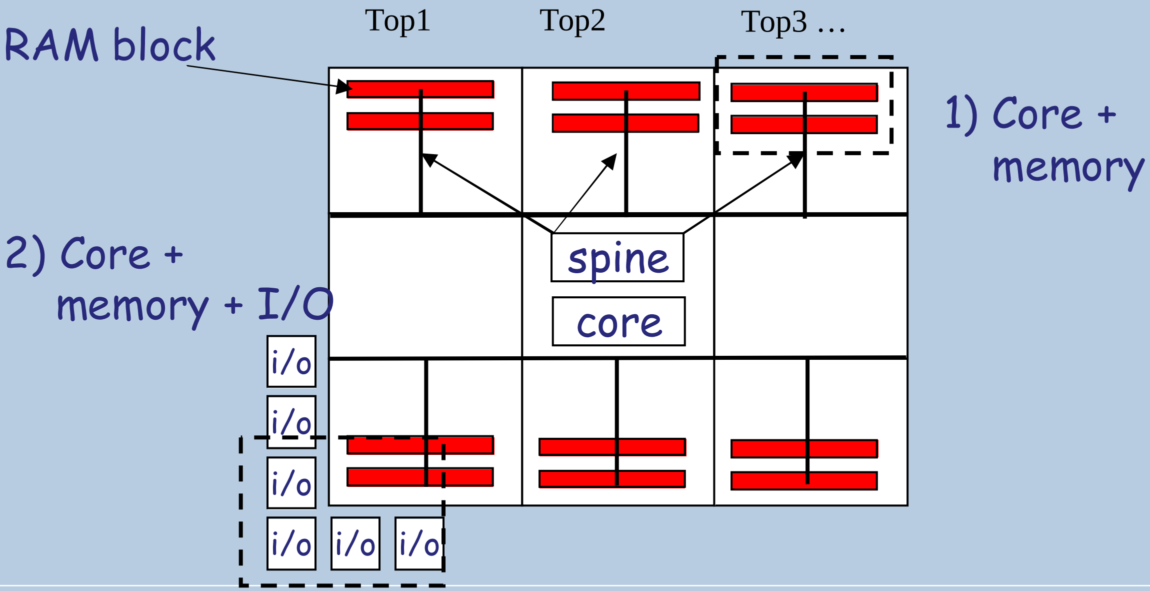
### Floorplanning Capabilities

- Define Rectangular Regions
  - x/y Location Displayed During Region Resize
  - Only Empty and Inclusive Regions Supported for APA and A500K
- Assign Logic, Regular I/O and Regular Nets to Region
  - Drag and Drop Assignments
  - Selection Highlighting and Color Selection
- Create Local Clock Region
- Multi-region Assignments Not Recommended
- I/O Assignments
- View Spines Created through GCF
- View Routing

# Silicon Support
*ProASIC/ProASIC^PLUS^*

## Multi-type Region Support

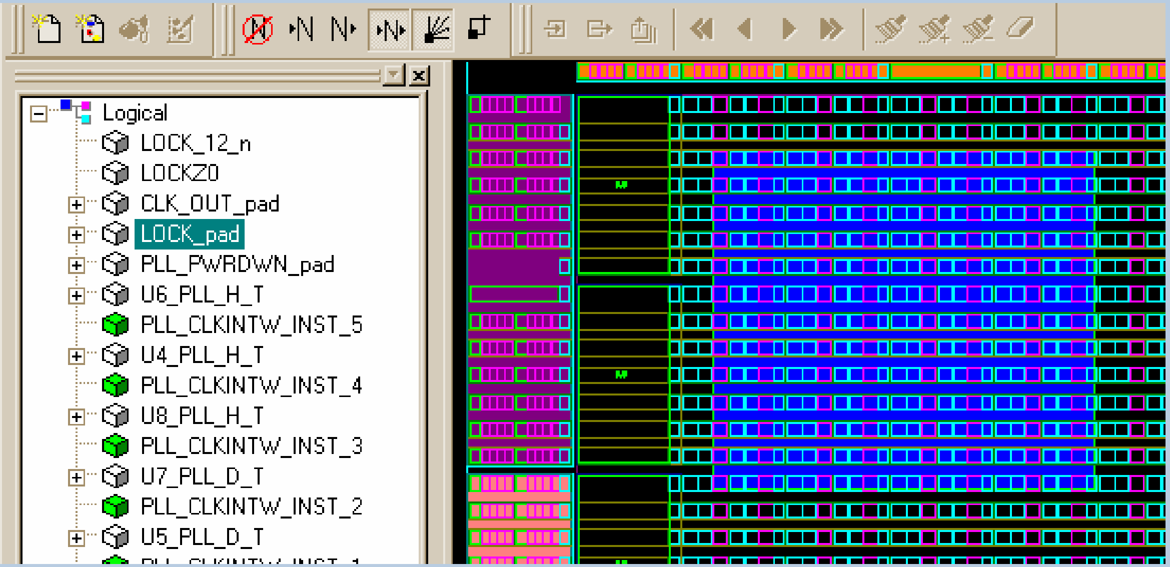
- Region Support for RAM
- LocalClock Regions Can Include RAM and I/O
  - Controlled by Compile Option (Designer -> Options -> Compile)
  - Need to Recompile after Modifying Option
  - Default is ON for New Designs from Designer 6.0 on



# ChipPlanner
*Axcelerator*

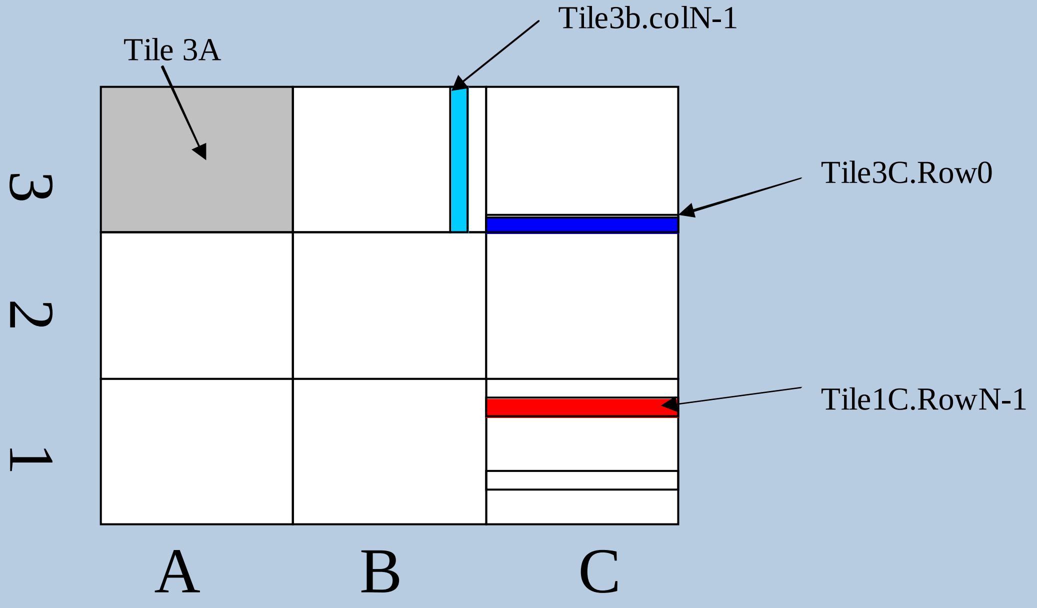
## Floorplanning Capabilities

- **Define Rectangular Regions**
  - **Empty, Exclusive and Inclusive Region Support for Axcelerator**
  - **Modify Region types (Inclusive / Exclusive)**
- **Assign Logic and Nets to Region**
  - **I/O Assignments**
  - **PLL and RAM Assignments**
- **Drag and Drop Assignments**
- **Multi-region Assignments NOT Recommended**



## ■ LocalClock Region Support

- **Created through PDC only**
- **PDC Syntax**
  - ***assign_local_clock –type routing_resource_type –net netname <local_clock_region> [local_clock_region] [local_clock_region] …***
  - ***routing_resource_type*** is either hclk or rclk
  - ***local_clock_region*** is Hierarchical Resource Name of Specific Clock Region



# ChipPlanner
## *Scripting Support*

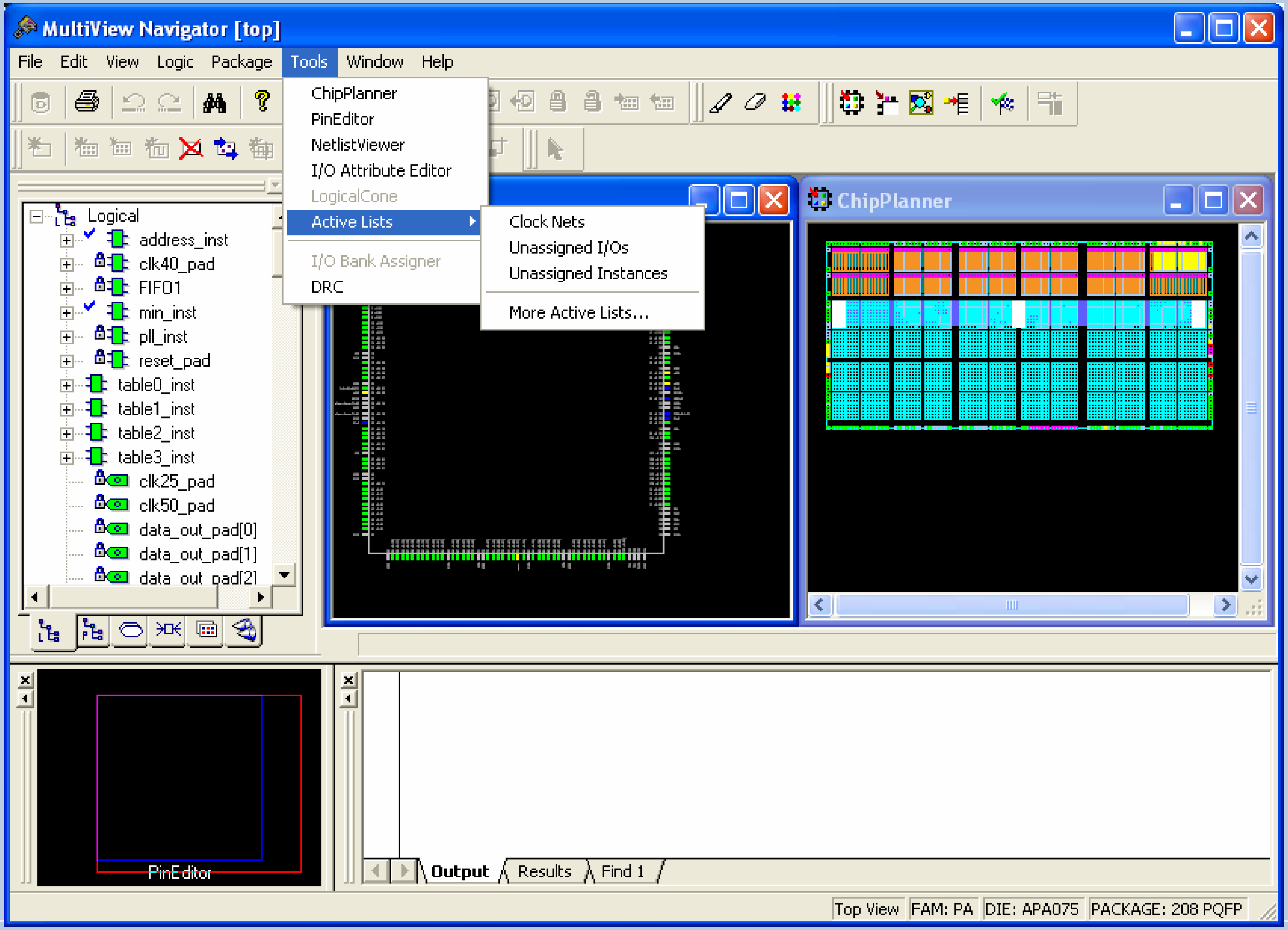
- ProASIC/ProASIC$^{\underline{\text{PLUS}}}$
  - Existing GCF Format and Capabilities
  - GCF Enhancement to Support Partial I/O Regions
- Axcelerator
  - PDC Commands for Floorplanning
    - Define and un-Define Region
      - *Rectangular*
      - *Rectilinear (Currently Only Supported in PDC)*
    - Region Types
      - *Empty*
      - *Inclusive*
      - *Exclusive*
    - Assign and Unassign Resources
      - *Macros*
      - *Nets*
    - Reset Floorplan

# MultiView Navigator
## *Active Lists*

- “Enables User To Compile Lists Of Important Resources
  - **Instances**
  - **Nets**
  - **Macros**
  - **Regions**
- Default Lists
  - **Unassigned Instances**
  - **Unassigned Pins**
  - **Clock Nets**
- Navigate Thru Design To Find Status Of Important Design Resources

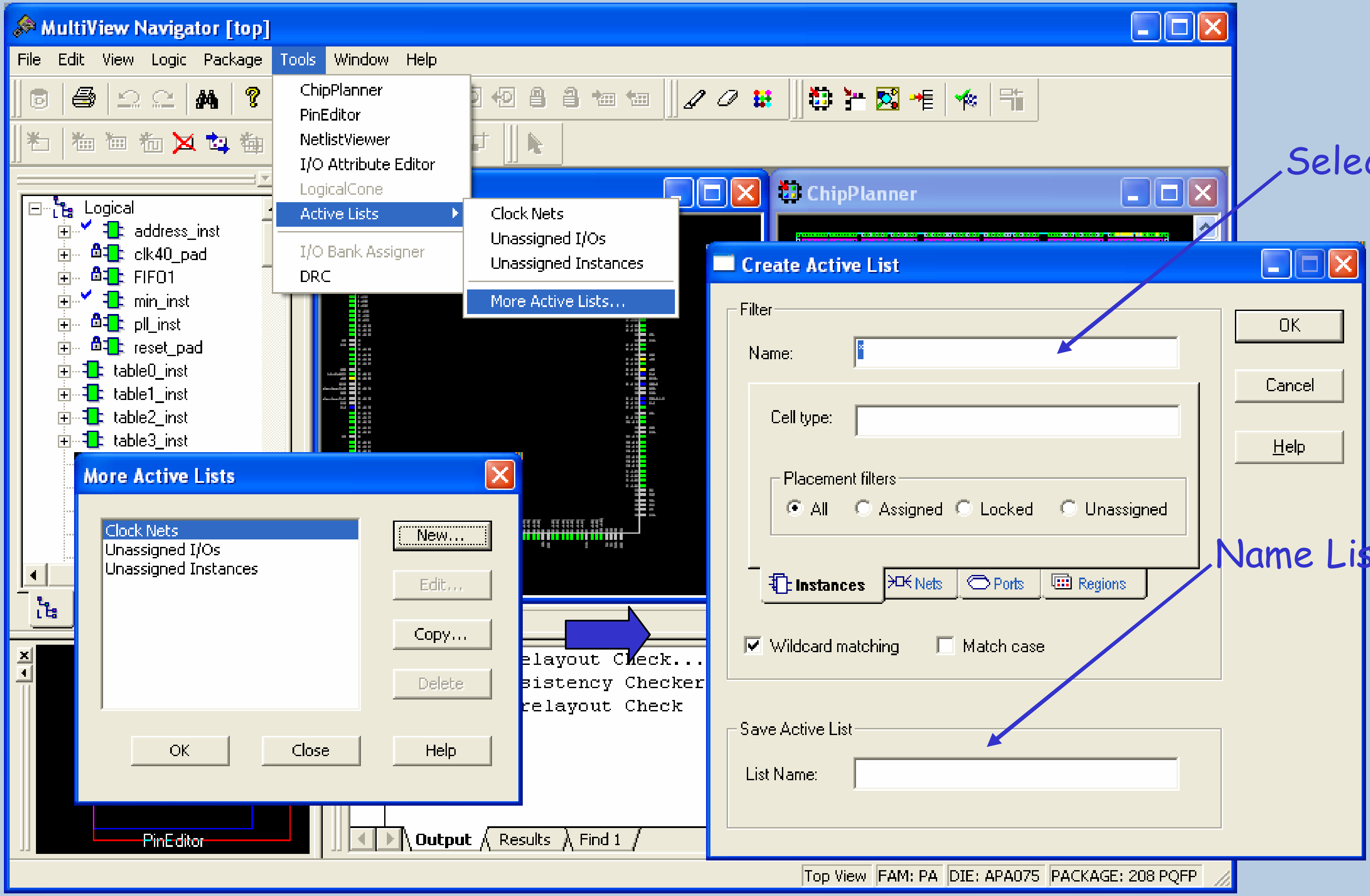
# MultiView Navigator
## *Viewing Active Lists*

- Open Default Active Lists from MVN Tools Menu



# MultiView Navigator
## *Creating Active Lists*

## ■ Users Can Create New Active Lists



Create Active List

Filter

Name:

Cell type:

Placement filters

● All ○ Assigned ○ Locked ○ Unassigned

Instances | Nets | Ports | Regions

☑ Wildcard matching ☐ Match case

Save Active List

List Name:

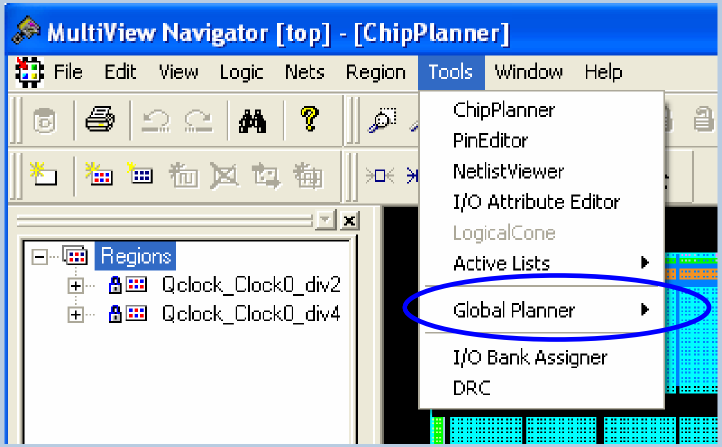
OK | Cancel | Help

Select instances

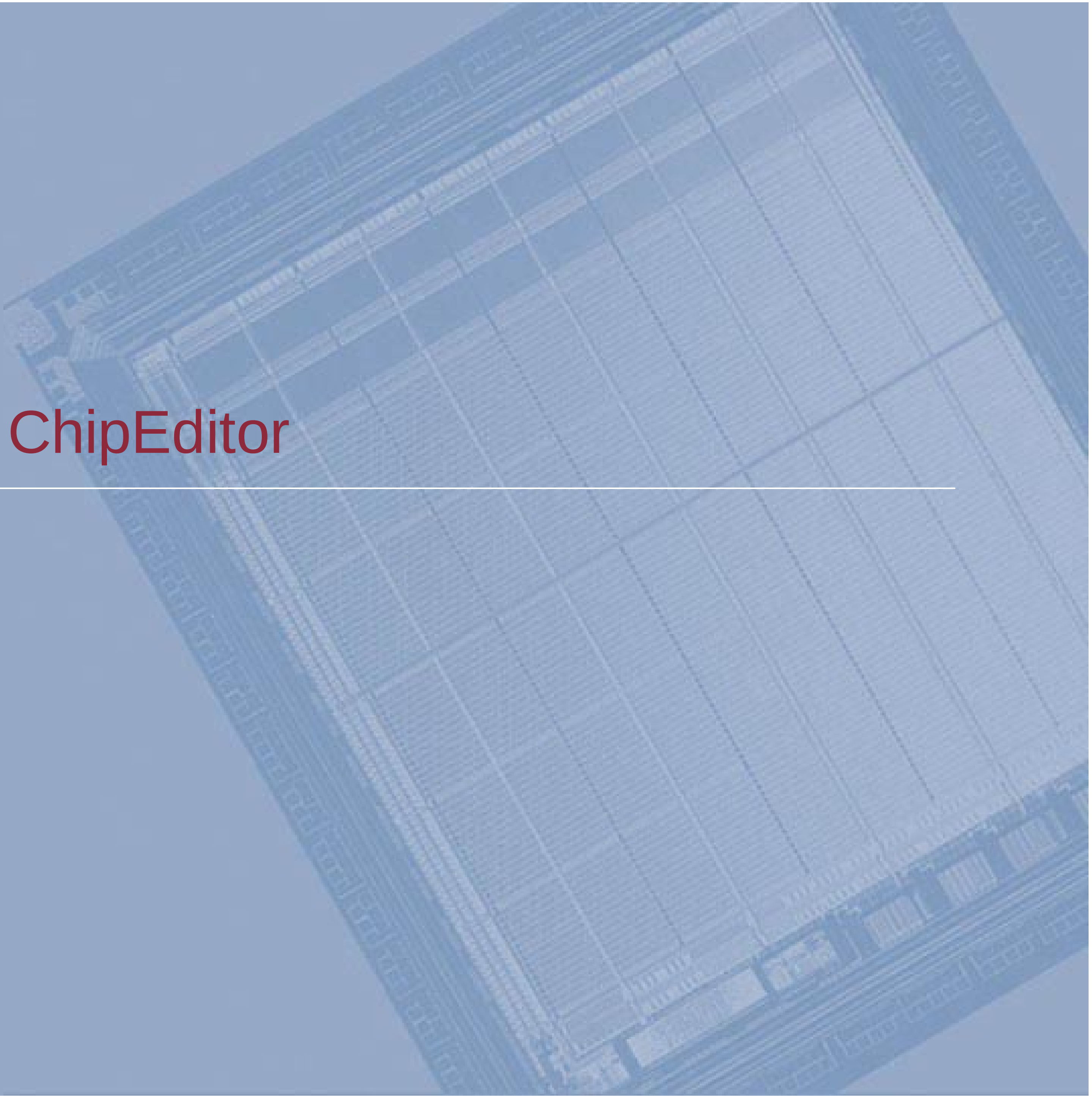
Name List

# MVN v7.2 Enhancements

- Global Planner Function Within the MVN Tools Can Be Used To Place Global Nets Automatically



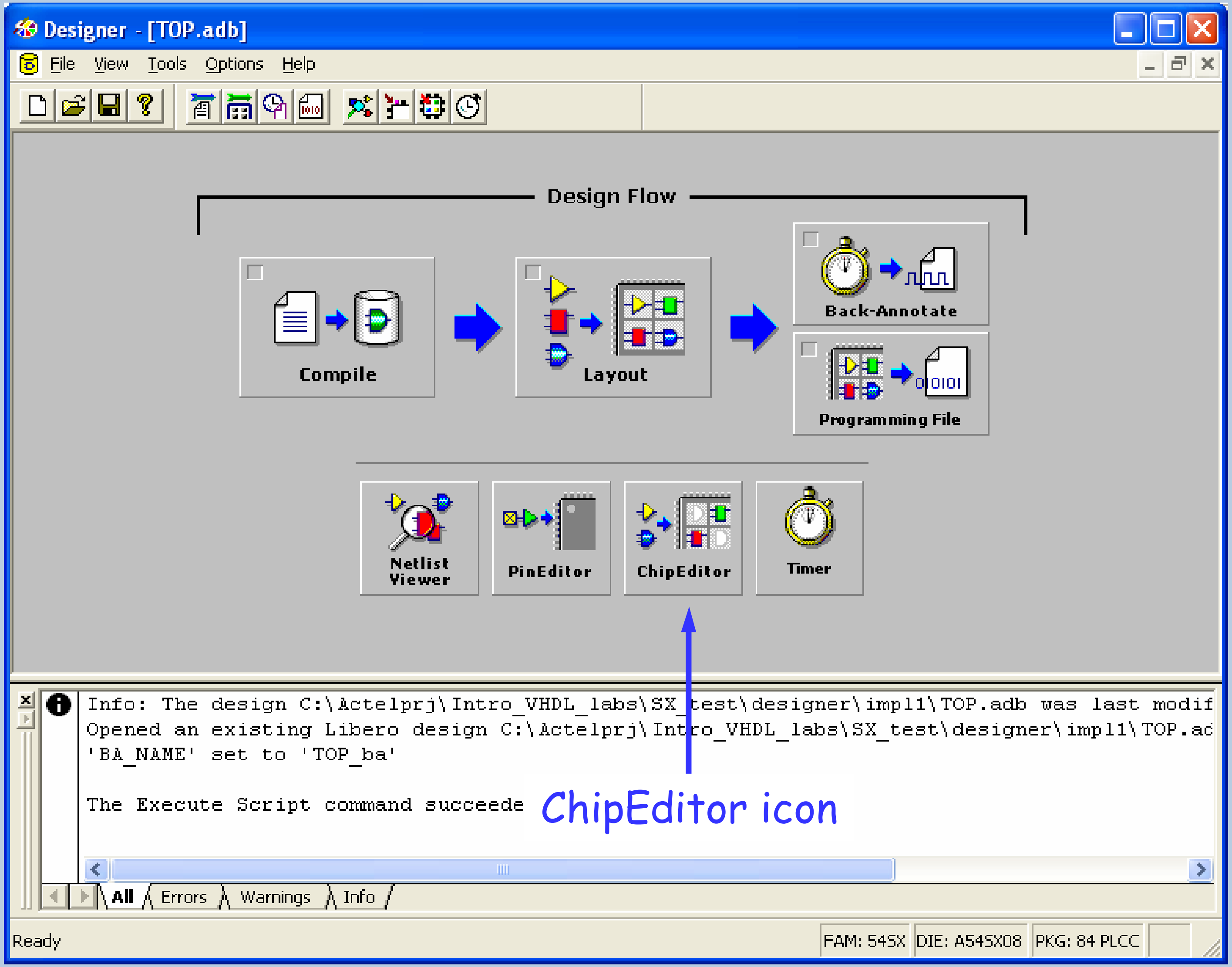
- Global Planner Can Distinguish Between Locked And Non-locked Quadrant Clock Regions
  - **Each Quadrant Clock region can be marked as locked**
  - **New capabilities:**
    - **Each Quadrant Clock region can be locked manually using a PDC file or through the MVN**
    - **Each locked Quadrant Clock region is not changed; Non-locked Quadrant Clock regions are deleted and recreated each time the Global Planner is executed**



# ChipEditor

Actel

# ChipEditor
*ACT1,2,3, MX, SX*



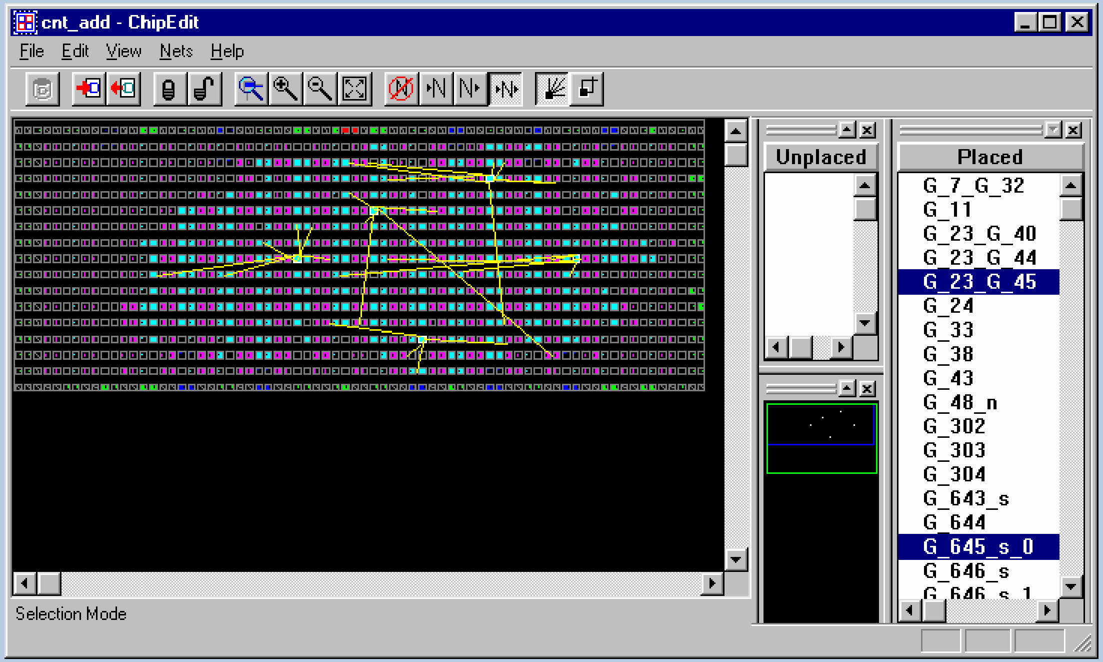
```
Info: The design C:\Actelprj\Intro_VHDL_labs\SX_test\designer\impl1\TOP.adb was last modif
Opened an existing Libero design C:\Actelprj\Intro_VHDL_labs\SX_test\designer\impl1\TOP.ad
'BA_NAME' set to 'TOP_ba'

The Execute Script command succeede
```

ChipEditor icon

# ChipEditor

## *ACT1,2,3, MX, SX*

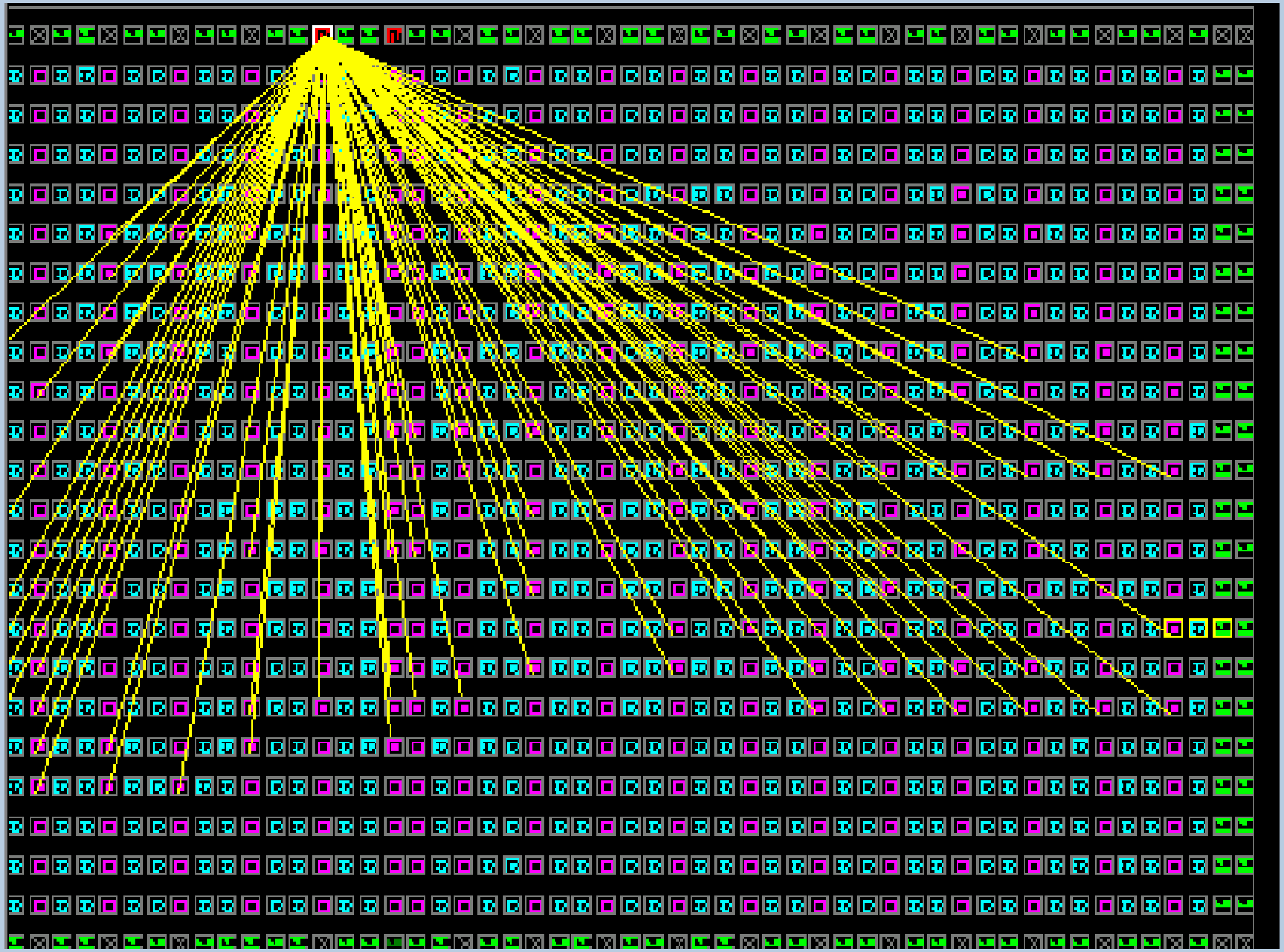


G_7_G_32
G_11
G_23_G_40
G_23_G_44
G_23_G_45
G_24
G_33
G_38
G_43
G_48_n
G_302
G_303
G_304
G_643_s
G_644
G_645_s_0
G_646_s
G_646_s_1

- Graphical Placement Editor
  - Place Logic Modules and I/O
- ChipEdit Shows Routing Congestion with “Rats Nest” Views
- Gives More Control to Power User

# ChipEditor
## *Viewing Routing*

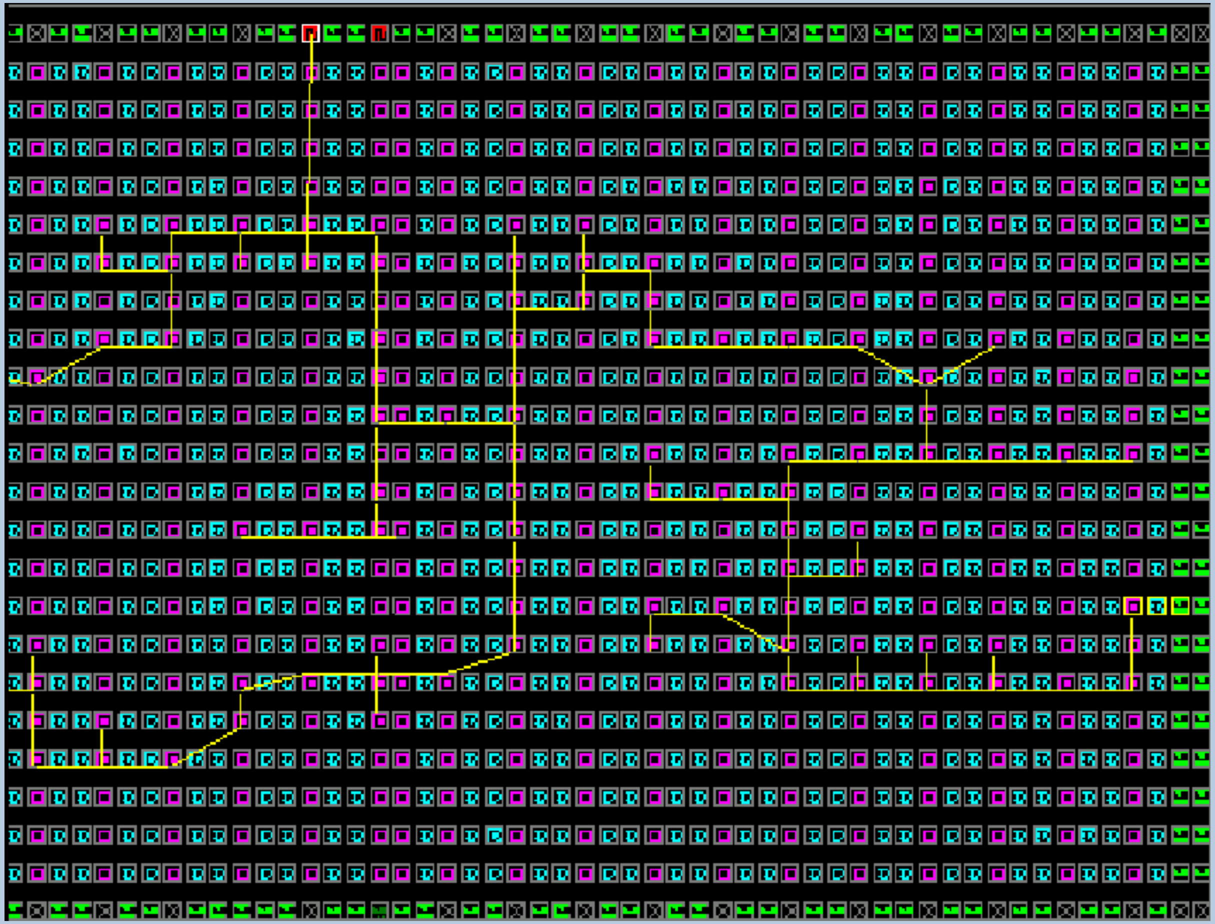
- Rats Nest View Shows Connectivity
  - **Example – CLKBUF Connected to Several Registers**

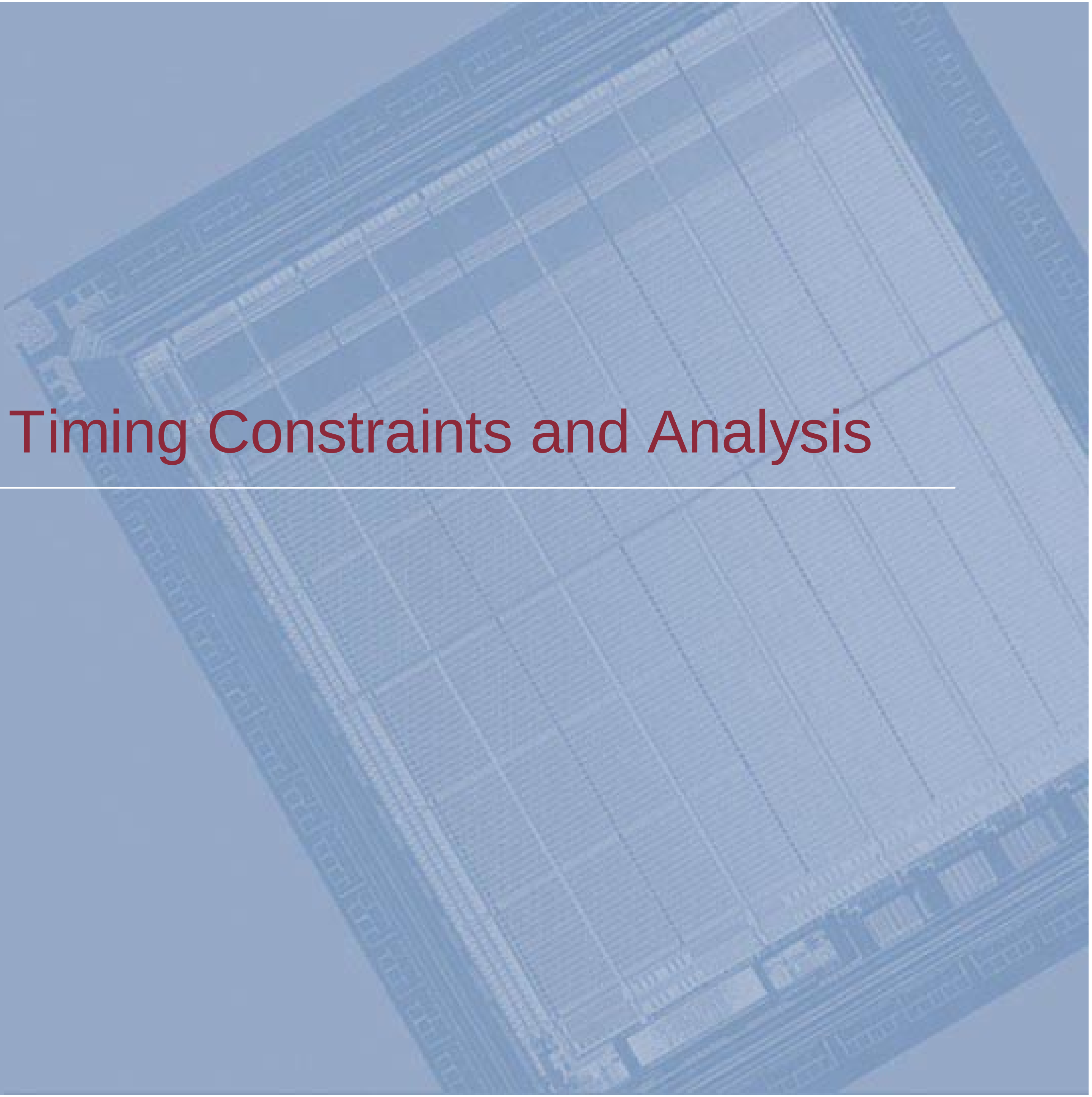


# ChipEditor
*Viewing Routing (cont.)*

## Minimum Spanning Tree Mode

- **Shows Connectivity between Selected Macros**





# Timing Constraints and Analysis

Actel

# SmartTime Overview

- SmartTime is Actel’s New Static Timing Analysis Tool
- SmartTime Replaces the Original Timer for:
  - **SX-A, RTSX-S, eX, AX, RTAX-S**
  - **500K, APA, ProASIC3\E and Fusion**
  - **All Future Products**

# SmartTime Features

- Graphical Constraint Entry
- SDC Constraint Support
- SDC Constraint Checker
- Analysis
  - **Cross-clock Domain Analysis**
  - **Flexibility in Clock Domain Selection**
- Improved Ease-of-Use
  - **Separate Constraint & Analysis Views**
    - **Separate Maximum & Minimum Analysis Views**
    - **Clock Domain Browser for the Analysis View**
  - **Visual Constraint Dialogs**
  - **Customizable Timing Information for the Paths List**
  - **Constraint Entry from the Analysis Window**
  - **Customizable Timing Reports**
  - **Filtering Capabilities**
  - **Persistence of User Settings**

# SmartTime
## *SDC Constraint Support*

- Constraints
  - SDC `create_clock`
  - SDC `create_generated_clock`
  - SDC `set_input_delay`
  - SDC `set_output_delay`
- Exceptions
  - SDC `set_false_path –from –through –to`
  - SDC `set_multicycle_path –from –through –to`

# SDC Constraint Support by Family

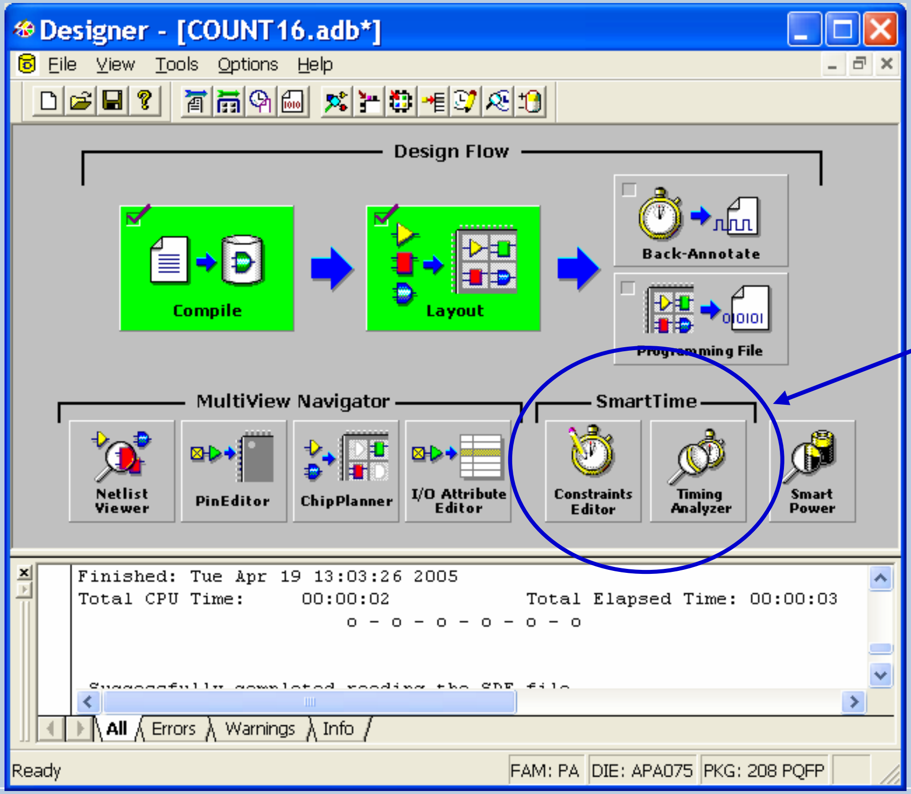
| SDC Constraint | Fusion | ProASIC3E | ProASIC3 | Axcelerator | ProASIC$^{PLUS}$ | A500K | eX | A54SXA | A54SX | 42MX | 3200DX | ACT3 | ACT2 / 1200XL | ACT1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| create_clock | ✓ | ✓ | ✓ | ✓ | ✓ | ✓[1] | ✓ | ✓ | | | | | | |
| create_generated_clock | ✓ | ✓ | ✓ | ✓ | ✓ | ✓[1] | ✓ | ✓ | | | | | | |
| set_input_delay | ✓ | ✓ | ✓ | ✓ | ✓ | ✓[1] | ✓[1] | ✓[1] | | | | | | |
| set_output_delay | ✓ | ✓ | ✓ | ✓ | ✓ | ✓[1] | ✓[1] | ✓[1] | | | | | | |
| set_false_path | ✓ | ✓ | ✓ | ✓ | ✓ | ✓[1] | ✓[2] | ✓[2] | | | | | | |
| set_multicycle_path | ✓ | ✓ | ✓ | ✓ | ✓ | ✓[1] | ✓[1] | ✓[1] | | | | | | |
| set_maximum_delay | ✓ | ✓ | ✓ | ✓ | ✓ | ✓[1] | ✓[2] | ✓[2] | | | | | | |

[1] Supported for analysis only

[2] Only -through option supported for layout

# SmartTime Windows

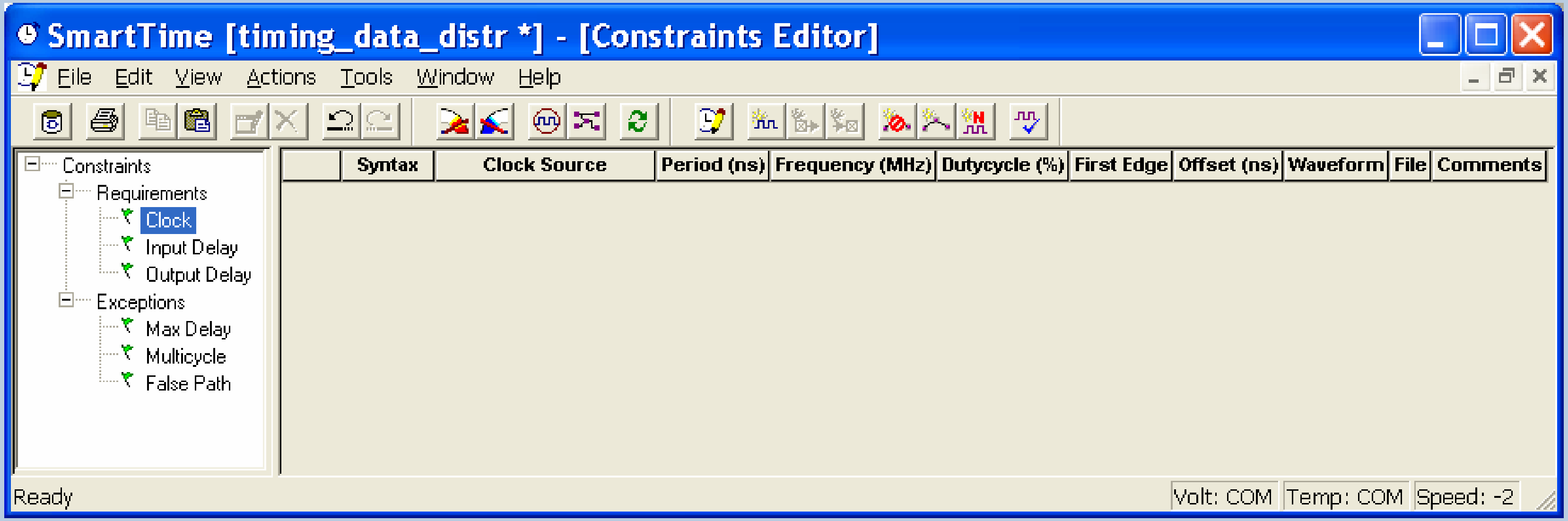
- SmartTime Includes of Separate Constraint Editor and Timing Analysis Windows
  - Constraint Editor – GUI Based Constraint Entry
  - Timing Analyzer Provides Delay Information



```
Finished: Tue Apr 19 13:03:26 2005
Total CPU Time:      00:00:02              Total Elapsed Time: 00:00:03
                                  o - o - o - o - o - o
```

Click to launch SmartTime Constraint Editor or Analysis Views

# SmartTime
## *Constraints Editor*

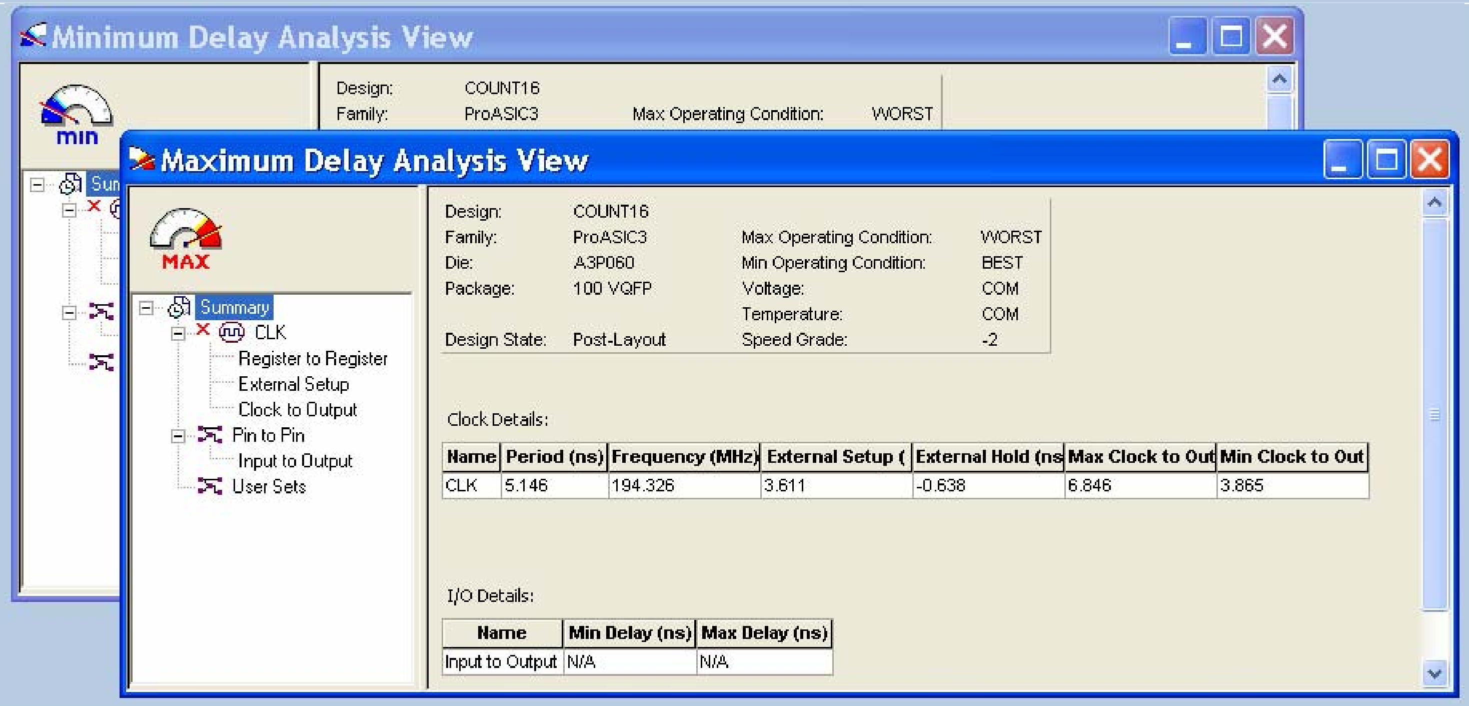


| | Syntax | Clock Source | Period (ns) | Frequency (MHz) | Dutycycle (%) | First Edge | Offset (ns) | Waveform | File | Comments |
|---|---|---|---|---|---|---|---|---|---|---|

- Use Constraints Editor to:
  - Enter or Edit Timing Requirements:
    - Clock Frequency, Input and Output Delays
  - Enter or Edit Timing Exceptions:
    - Max Delay, Multicycle Paths, False Paths
  - Browse Clock Domains

# SmartTime

## *Timing Analysis View*



| | | | |
|---|---|---|---|
| Design: | COUNT16 | | |
| Family: | ProASIC3 | Max Operating Condition: | WORST |
| Die: | A3P060 | Min Operating Condition: | BEST |
| Package: | 100 VQFP | Voltage: | COM |
| | | Temperature: | COM |
| Design State: | Post-Layout | Speed Grade: | -2 |

Clock Details:

| Name | Period (ns) | Frequency (MHz) | External Setup ( | External Hold (ns | Max Clock to Out | Min Clock to Out |
|---|---|---|---|---|---|---|
| CLK | 5.146 | 194.326 | 3.611 | -0.638 | 6.846 | 3.865 |

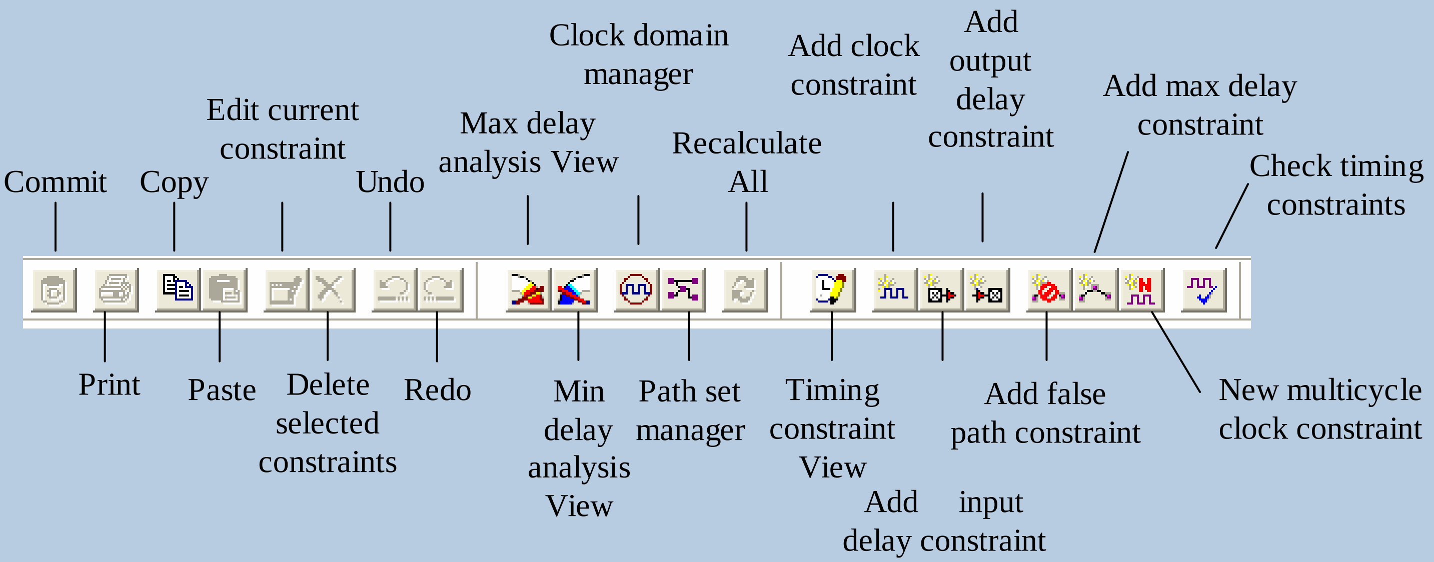
I/O Details:

| Name | Min Delay (ns) | Max Delay (ns) |
|---|---|---|
| Input to Output | N/A | N/A |

- **Determine Maximum Operating Frequency**
- **Verify Setup and Hold Requirements**
- **Identify Timing Violations**
- **Browse Clock Domains**
- **Set Constraints on Specific Pins or Sets of Paths**
- **Copy, Print, Expand or Cross-Probe Sets of Paths**

# SmartTime Toolbar

- The SmartTime Toolbar Contains Commands for Performing Common Operations.
  - **Tool Tips Are Available for Each Button.**



# SmartTime Constraint Entry

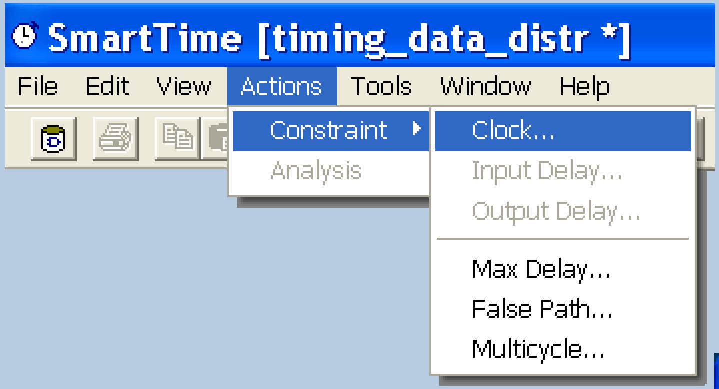
- Clock Constraints
- Input and Output Delay Constraints
- Clock Exceptions

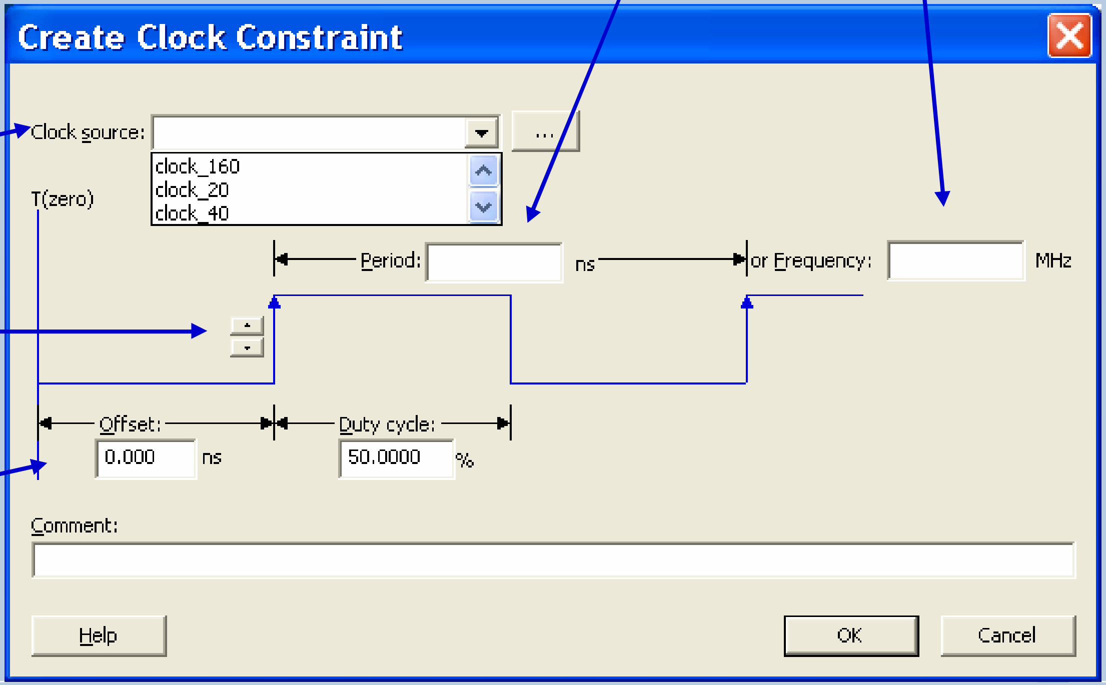
# SmartTime
## *Clock Domains*

- SmartTime Detects Possible Clocks by Tracing Back from the Clock Pins of all Sequential Components Until it Finds:
  - **An Input Port**
  - **The Output of Another Sequential Element, or**
  - **The Output of a PLL**
- SmartTime Classifies Clock Sources Into Three Types:
  - **Explicit Clocks**
  - **Potential Clocks**
  - **Clock Network**
- Each Clock Domain Contains at Least 3 Path Sets:
  - **Register to Register**
  - **External Setup or Hold**
  - **Clock to Out**

# SmartTime
## *Entering Clock Constraints*

- Visual Constraint Dialog Box Simplifies Constraint Entry





Clock source:

clock_160
clock_20
clock_40

Period:

or Frequency:

Offset: 0.000 ns

Duty cycle: 50.0000 %

Comment:

Enter Period or Frequency

Select Clock Source from pull-down Menu

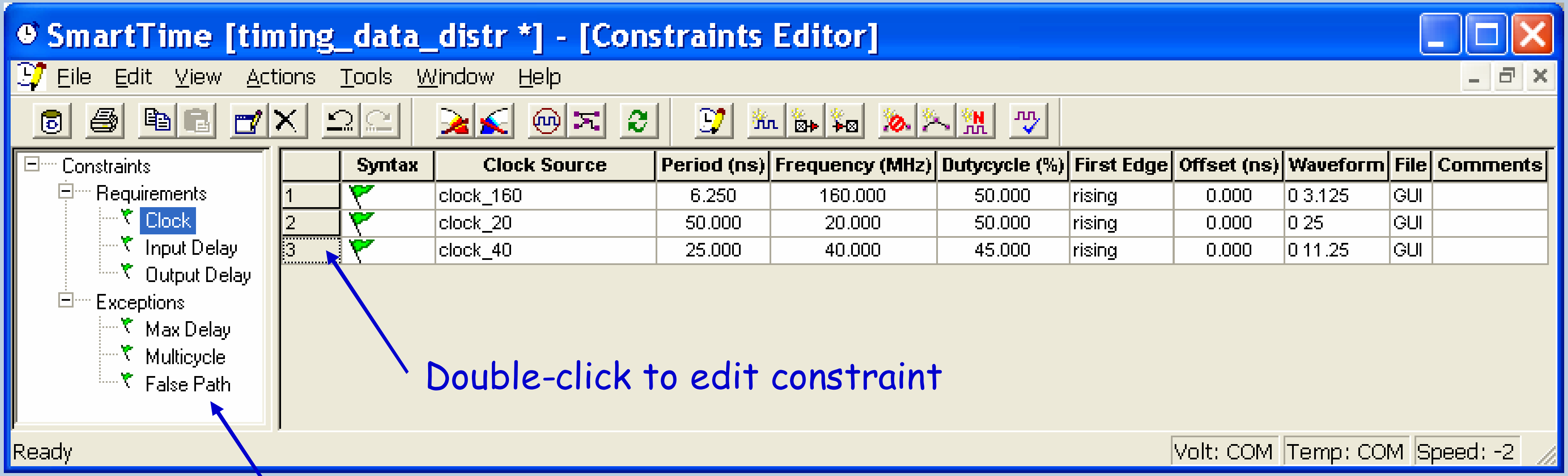
Select Starting Edge

Enter Offset and Duty Cycle

# SmartTime Clock Constraints

## Clock Constraints in Constraint Editor

- **Select Constraint to Add, Edit or Delete**



SmartTime [timing_data_distr *] - [Constraints Editor]

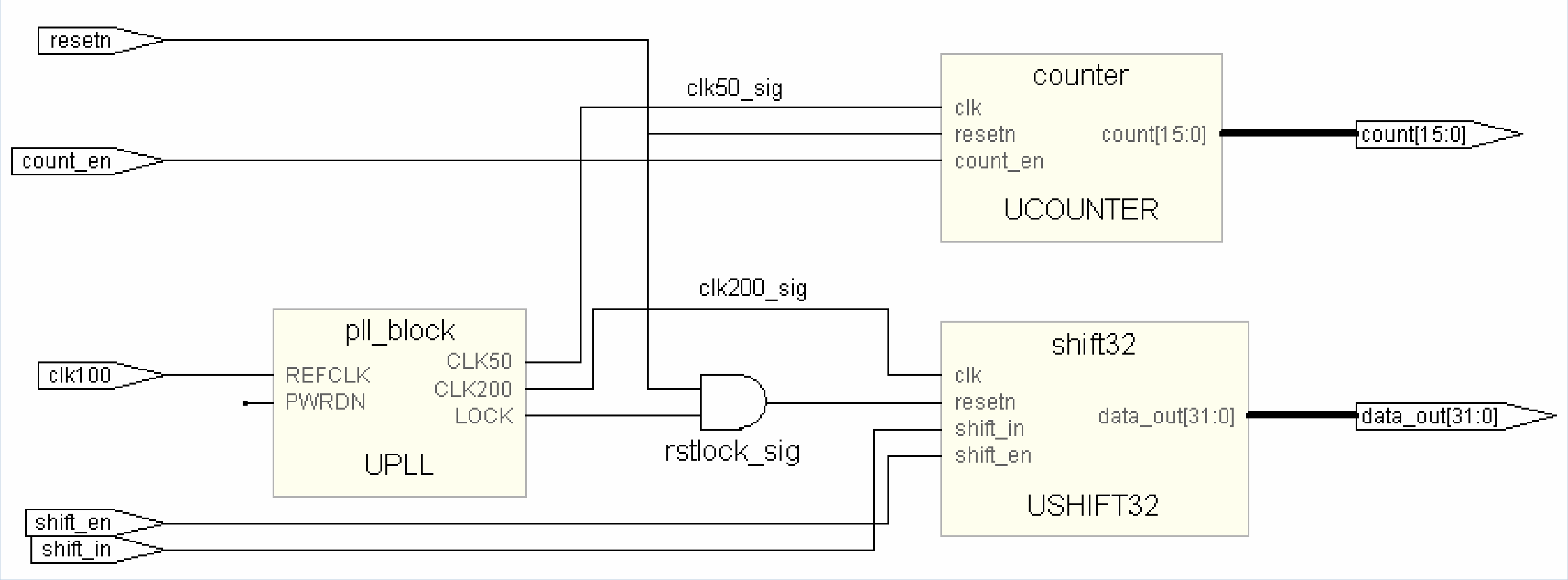
| | Syntax | Clock Source | Period (ns) | Frequency (MHz) | Dutycycle (%) | First Edge | Offset (ns) | Waveform | File | Comments |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | clock_160 | 6.250 | 160.000 | 50.000 | rising | 0.000 | 0 3.125 | GUI | |
| 2 | | clock_20 | 50.000 | 20.000 | 50.000 | rising | 0.000 | 0 25 | GUI | |
| 3 | | clock_40 | 25.000 | 40.000 | 45.000 | rising | 0.000 | 0 11.25 | GUI | |

Double-click to edit constraint

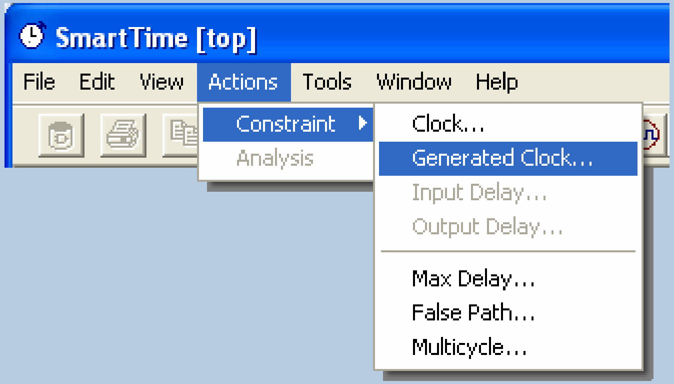
Double-click constraint type to add constraint

# SmartTime
## *Generated Clock Constraints*

- Constraints For Internally Generated Clock Can Be Specified Using Generated Clock Constraints
  - **Useful For Constraining PLL Outputs**

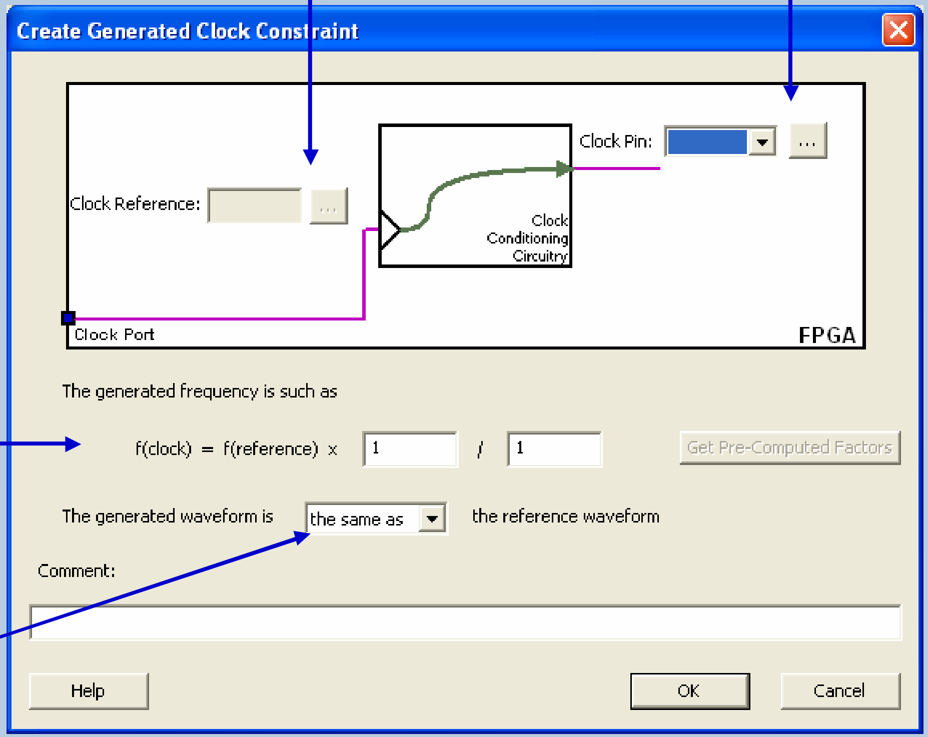


# SmartTime
## *Entering Generated Clock Constraints*



Specify clock reference

Select pin for generated clock


Create Generated Clock Constraint
Clock Conditioning Circuitry
Clock Port
FPGA
Get Pre-Computed Factors
Help
OK
Cancel

Clock Reference:

Clock Pin:

The generated frequency is such as

f(clock) = f(reference) x 1 / 1

The generated waveform is the same as the reference waveform

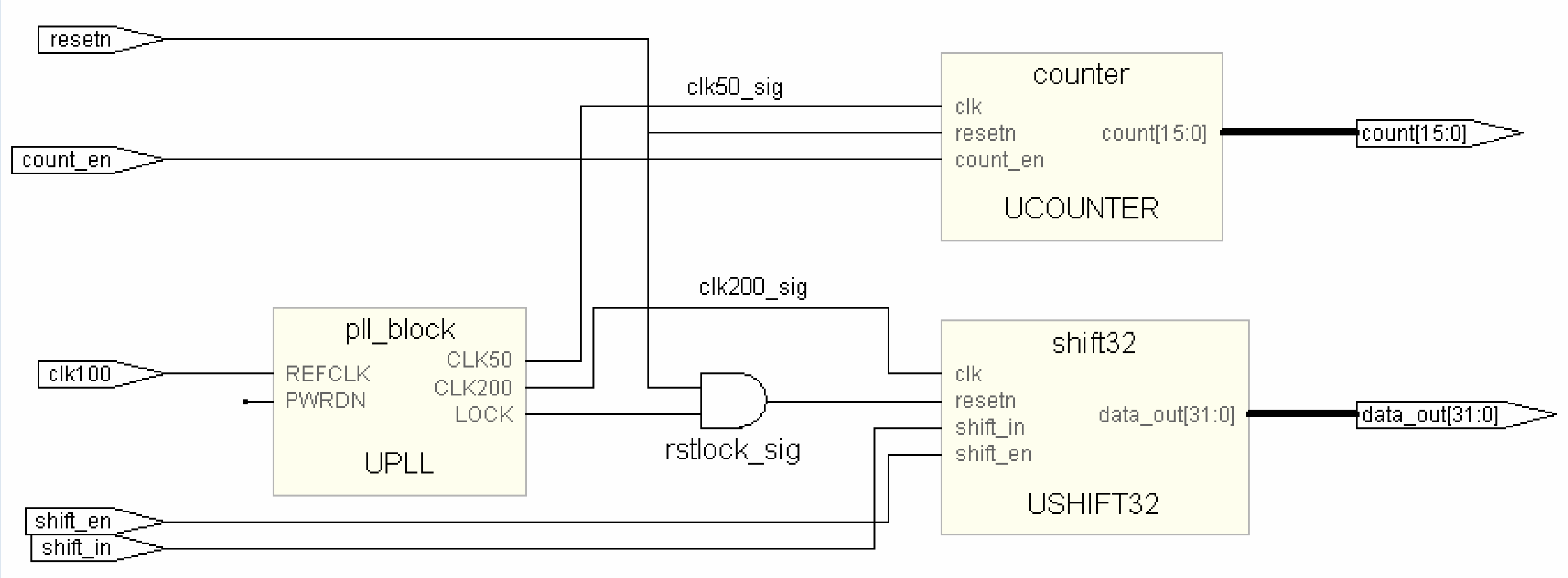
Comment:

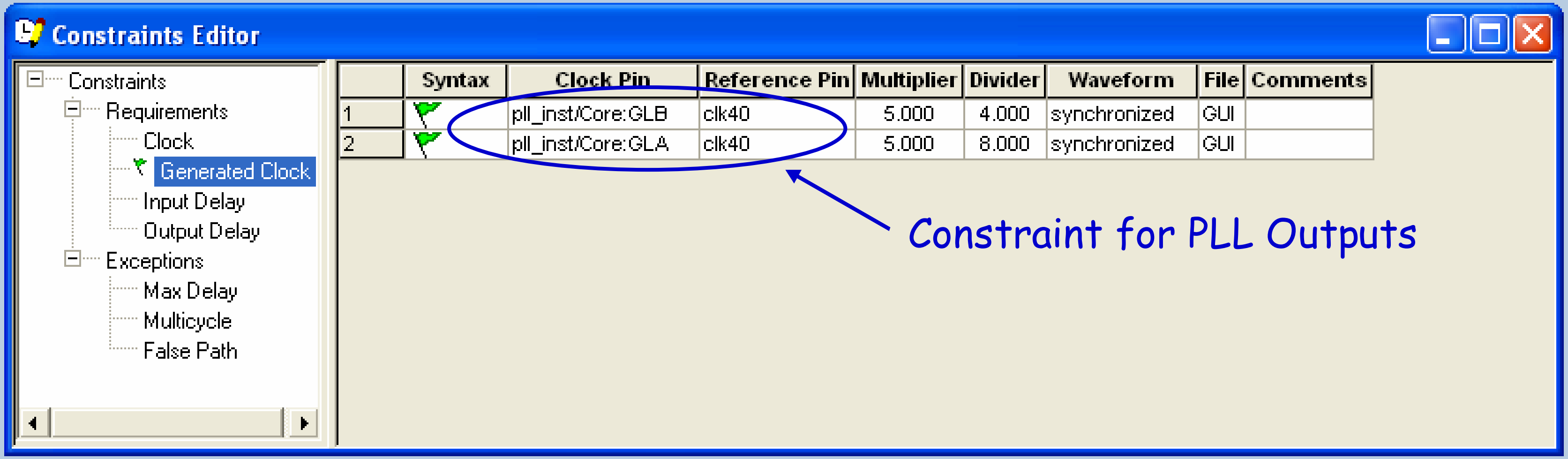
Enter multiplication and division factors to generate frequency

Specify edge relationship to reference clock

# SmartTime

## *Generated Clocks - PLL Outputs*





| | Syntax | Clock Pin | Reference Pin | Multiplier | Divider | Waveform | File | Comments |
|---|---|---|---|---|---|---|---|---|
| 1 | ✓ | pll_inst/Core:GLB | clk40 | 5.000 | 4.000 | synchronized | GUI | |
| 2 | ✓ | pll_inst/Core:GLA | clk40 | 5.000 | 8.000 | synchronized | GUI | |

Constraint for PLL Outputs

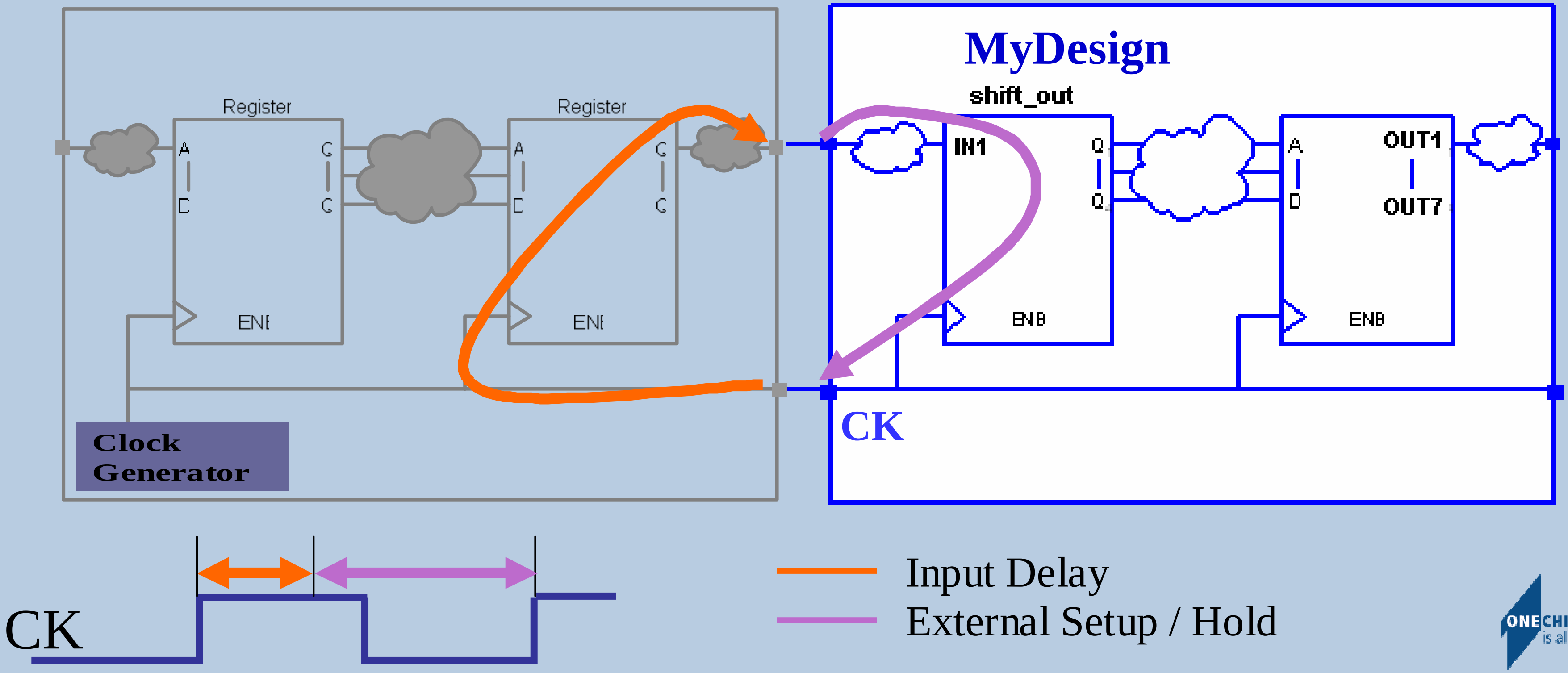
# SmartTime Constraint Entry

- Clock Constraints
- Input and Output Delay Constraints
- Clock Exceptions

ONECHIP is all you need

# SmartTime
*Input Constraints*

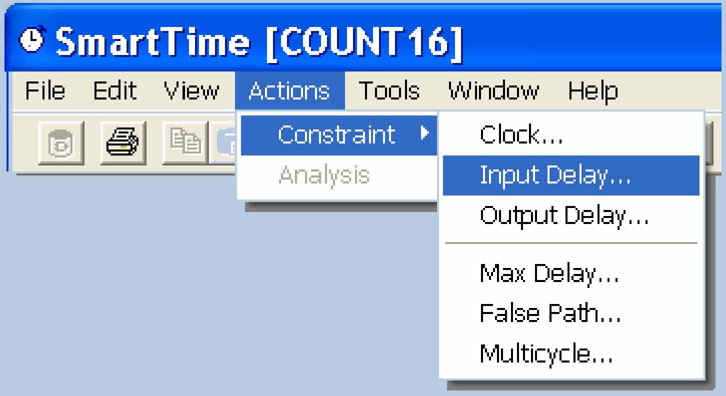
- Input Constraints can be Entered as Input Delay or External Setup/Hold
  - **Input Delay – Enter Input Delay in Terms of Delay Budget *Outside* FPGA**
    - **SDC Format**
  - **External Setup / Hold – Specify Input Delay Budget *Inside* FPGA**
    - **Used by Previous Actel Timer**

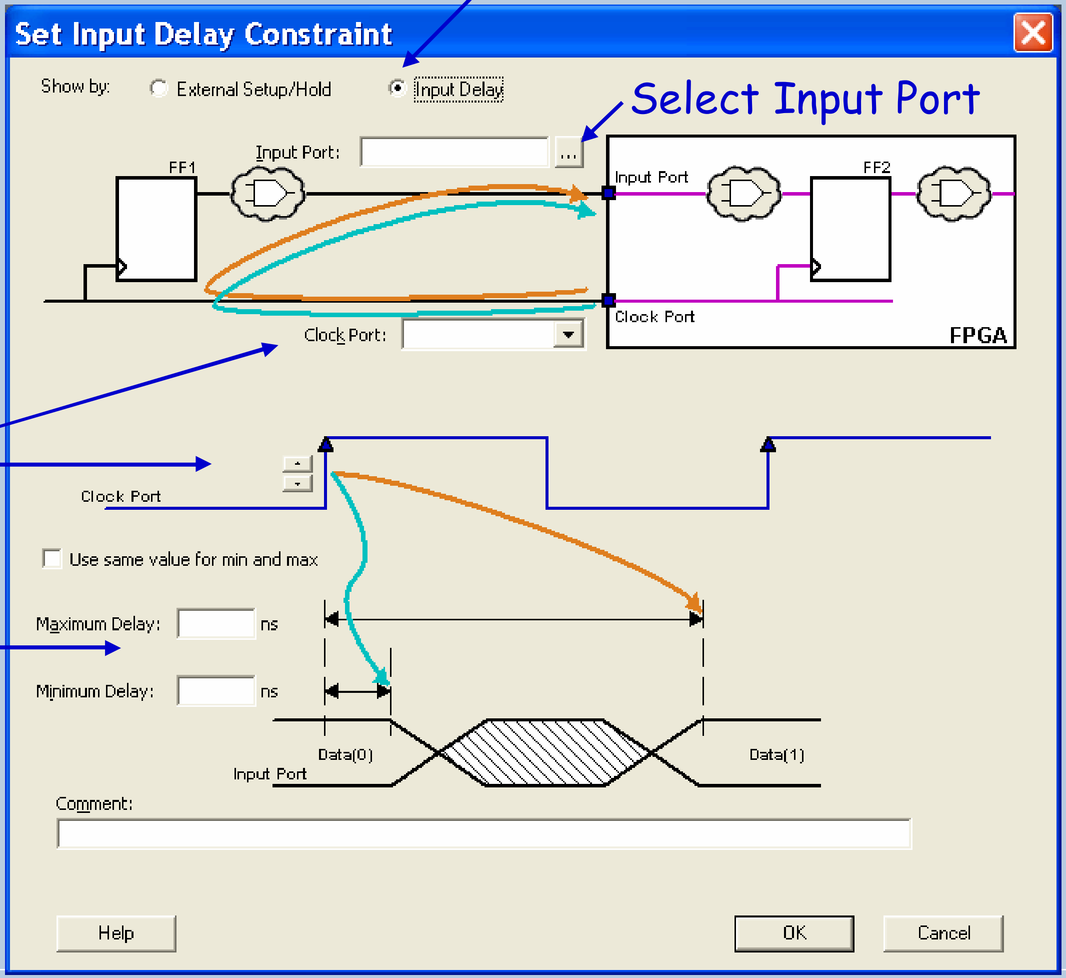


Input Delay
External Setup / Hold

# Input Constraints
## *Input Delay*

- Visual Constraint Dialog Box Simplifies Constraint Entry




Set Input Delay Constraint

Show by: ○ External Setup/Hold ● Input Delay

Input Port:

Clock Port:

☐ Use same value for min and max

Maximum Delay: ns

Minimum Delay: ns

Comment:

Select Input Delay

Select Input Port

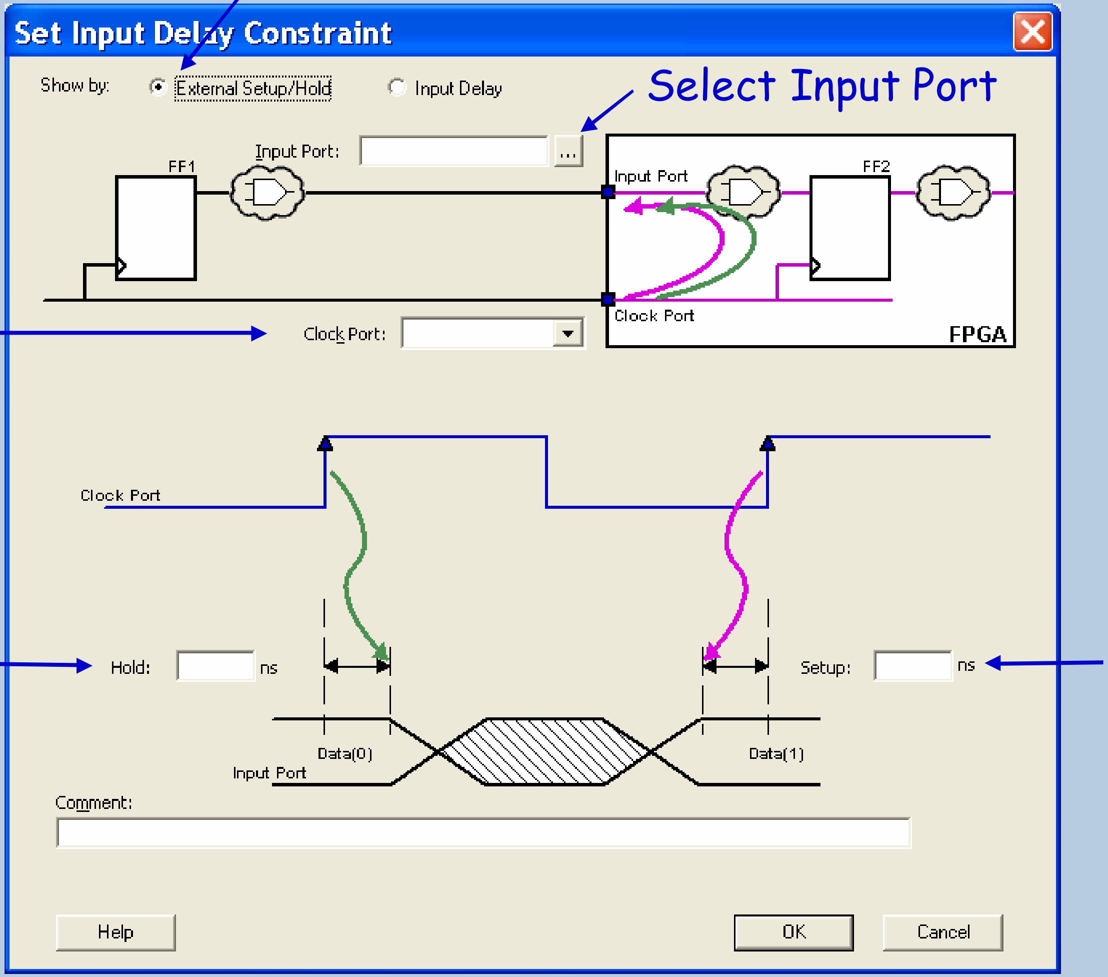
Select Clock Port and Reference Edge

Enter Min and Max delay or same value for both

Minimum Delay for analysis only

# Input Constraints
## *External Setup / Hold*

Select External Setup/Hold



Set Input Delay Constraint

Show by: ● External Setup/Hold ○ Input Delay

Input Port:

Clock Port:

Hold: ns

Setup: ns

Comment:

Select Input Port

Select Clock Port

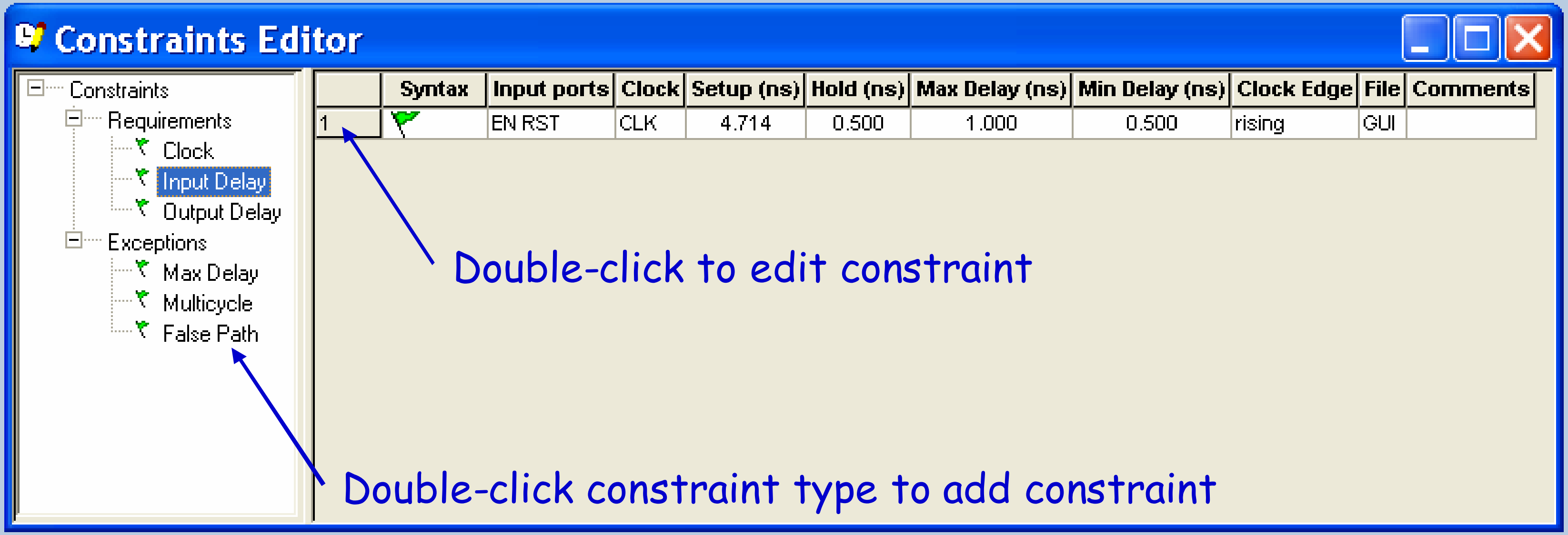
Enter Hold Requirement

Enter Setup Requirement

# SmartTime
*Input Constraints*

## Input Delay Constraints in Constraint Editor

- **Constraint Displayed as External Setup / Hold and Input Delay**



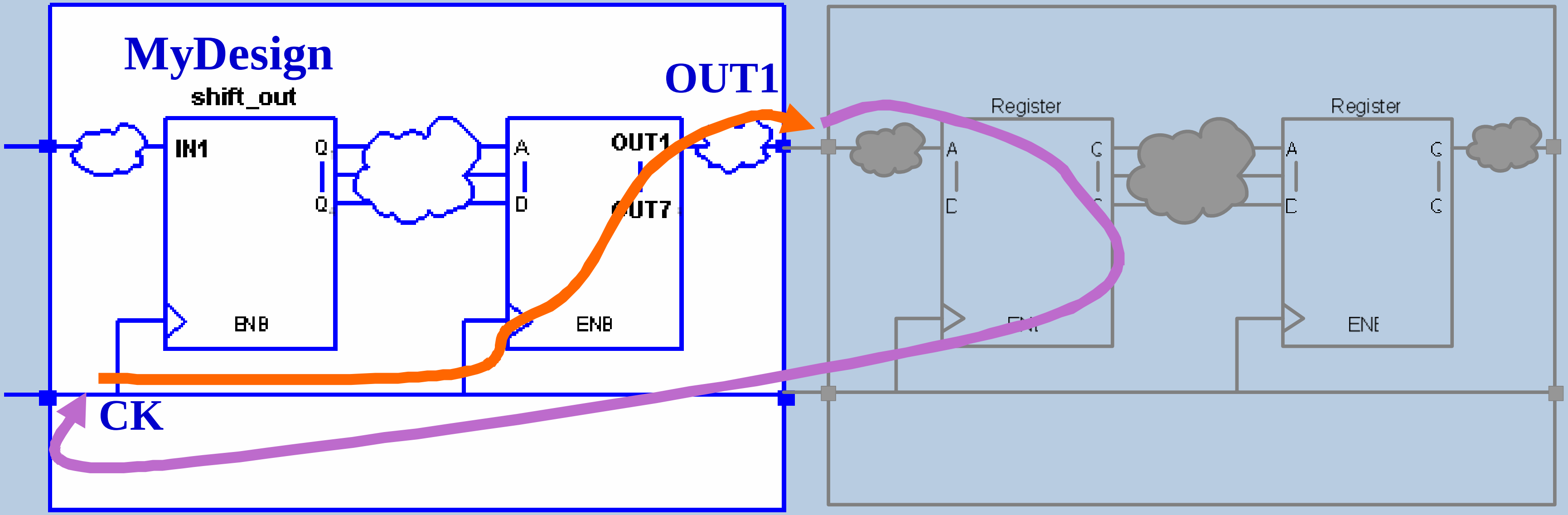
|  | Syntax | Input ports | Clock | Setup (ns) | Hold (ns) | Max Delay (ns) | Min Delay (ns) | Clock Edge | File | Comments |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 |  | EN RST | CLK | 4.714 | 0.500 | 1.000 | 0.500 | rising | GUI |  |

Double-click to edit constraint

Double-click constraint type to add constraint

# SmartTime
## *Output Constraints*

- Output Constraints Define the Delay of an Output Relative to a Clock
- Output Constraints can be Entered as Clock-to-Output or Output Delay
  - **Clock-to-Output: Specifies the Output Delay by Specifying the Timing Budget *Inside* the FPGA (default)**
  - **Output Delay: Specifies Output Delay Constraint by Specifying the Timing Budget *Outside* the FPGA**
    - **SDC Format**



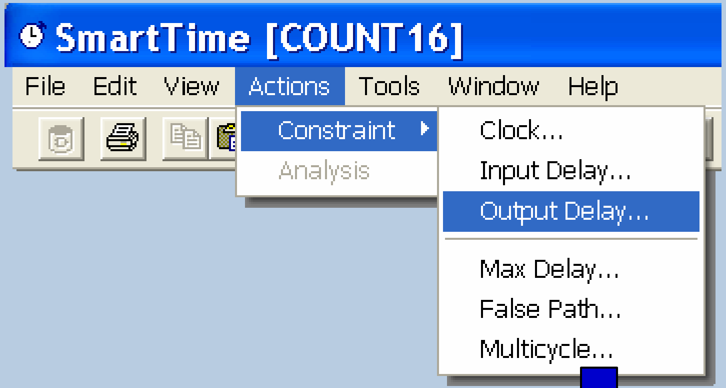
— Clock-to-Output — Output Delay

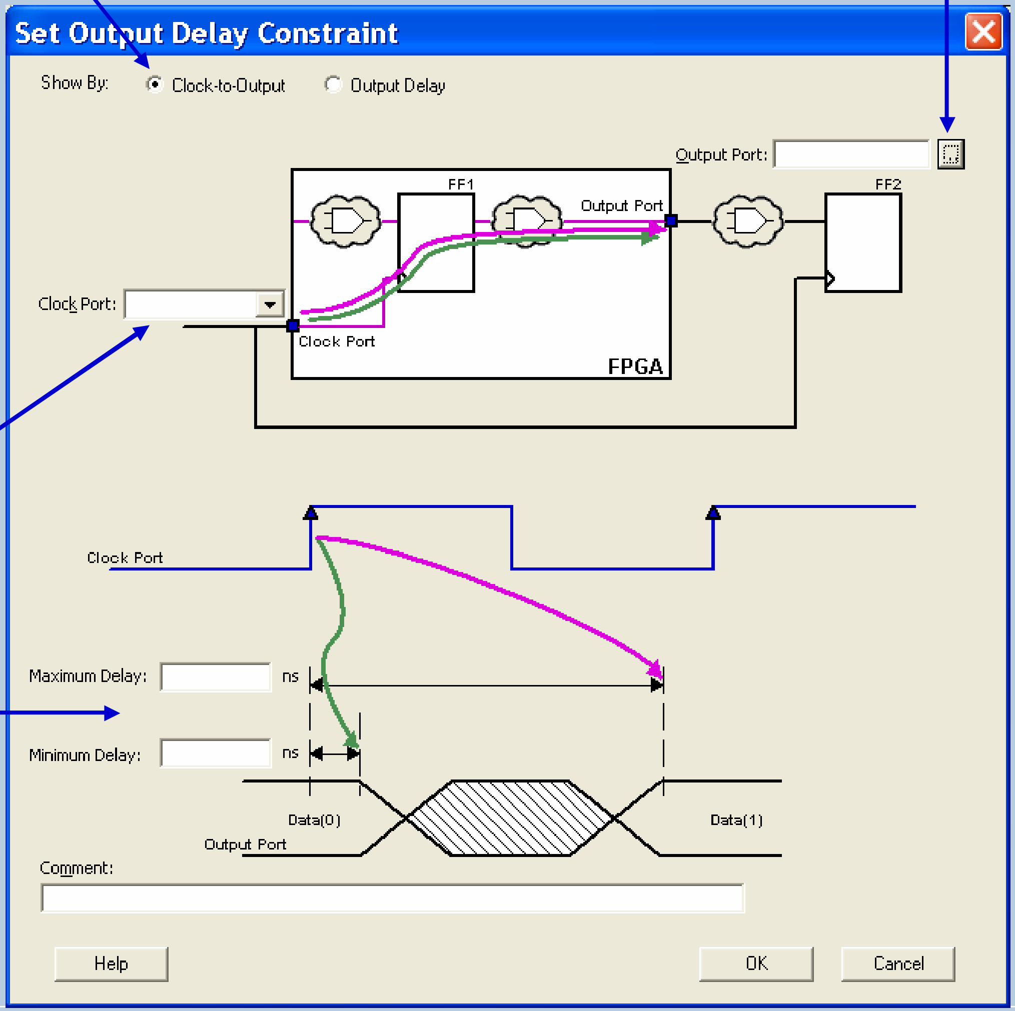
# Output Constraints
*Clock-to-Output*

- Visual Constraint Dialog Box Simplifies Constraint Entry

Select Clock-to-Output

Select Output Port





Show By: ● Clock-to-Output ○ Output Delay

Output Port:

Clock Port:

Maximum Delay: ns

Minimum Delay: ns

Comment:

Select Clock Port

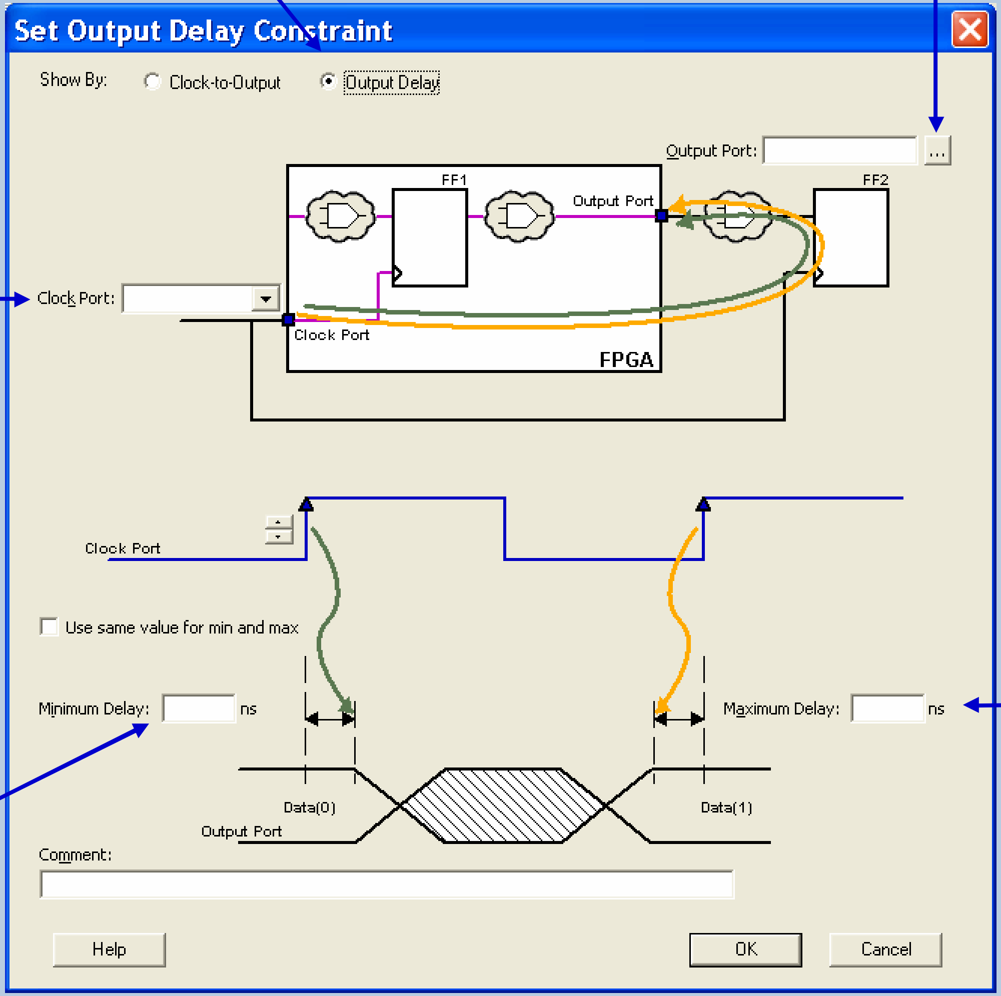
Enter Min and Max delay
Minimum Delay for analysis only

# Output Constraints
*Output Delay*

Select Output Delay

Select Output Port

Select Clock Port



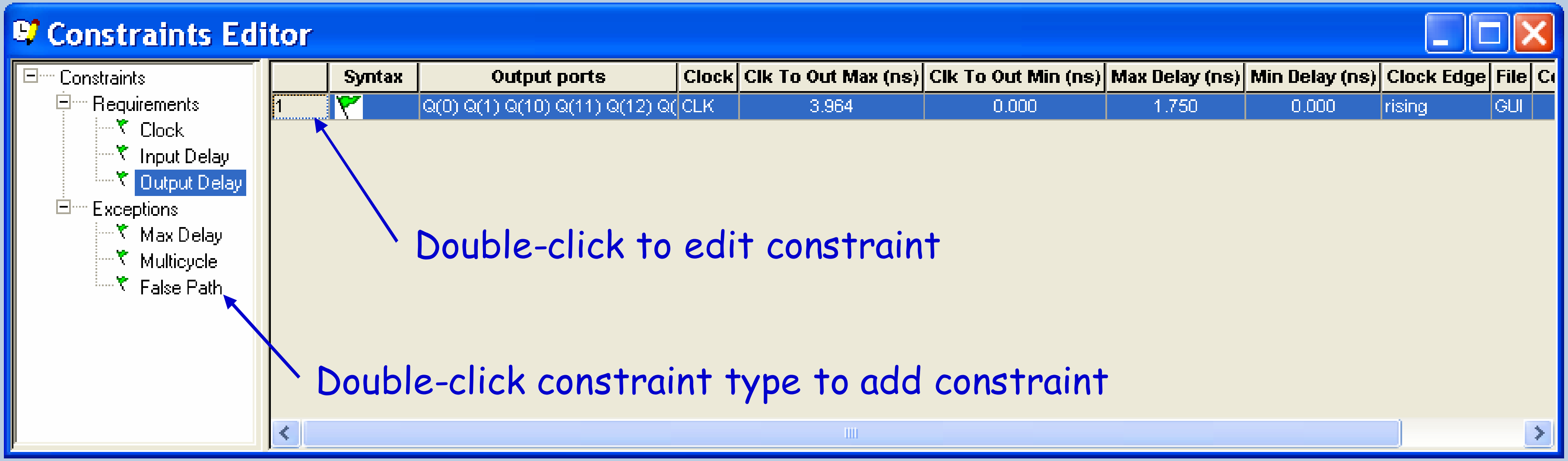
Maximum Delay

Minimum Delay

# SmartTime
## *Output Delay Constraints*

## Output Constraints in Constraint Editor

- **Displayed as Clock-to-Output and Output Delay**
- **Select Constraint to Add, Edit or Delete**



Constraints Editor

| | Syntax | Output ports | Clock | Clk To Out Max (ns) | Clk To Out Min (ns) | Max Delay (ns) | Min Delay (ns) | Clock Edge | File | Co |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | Q(0) Q(1) Q(10) Q(11) Q(12) Q( | CLK | 3.964 | 0.000 | 1.750 | 0.000 | rising | GUI | |

Double-click to edit constraint

Double-click constraint type to add constraint

# SmartTime Constraint Entry

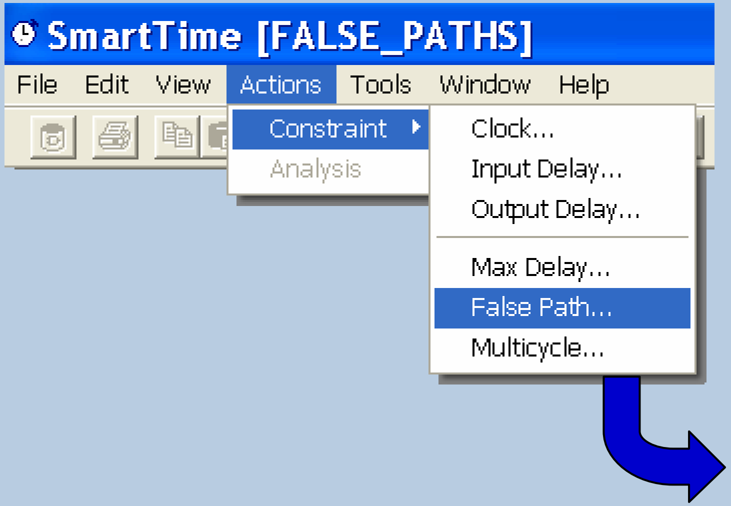
- Clock Constraints
- Input and Output Delay Constraints
- Clock Exceptions

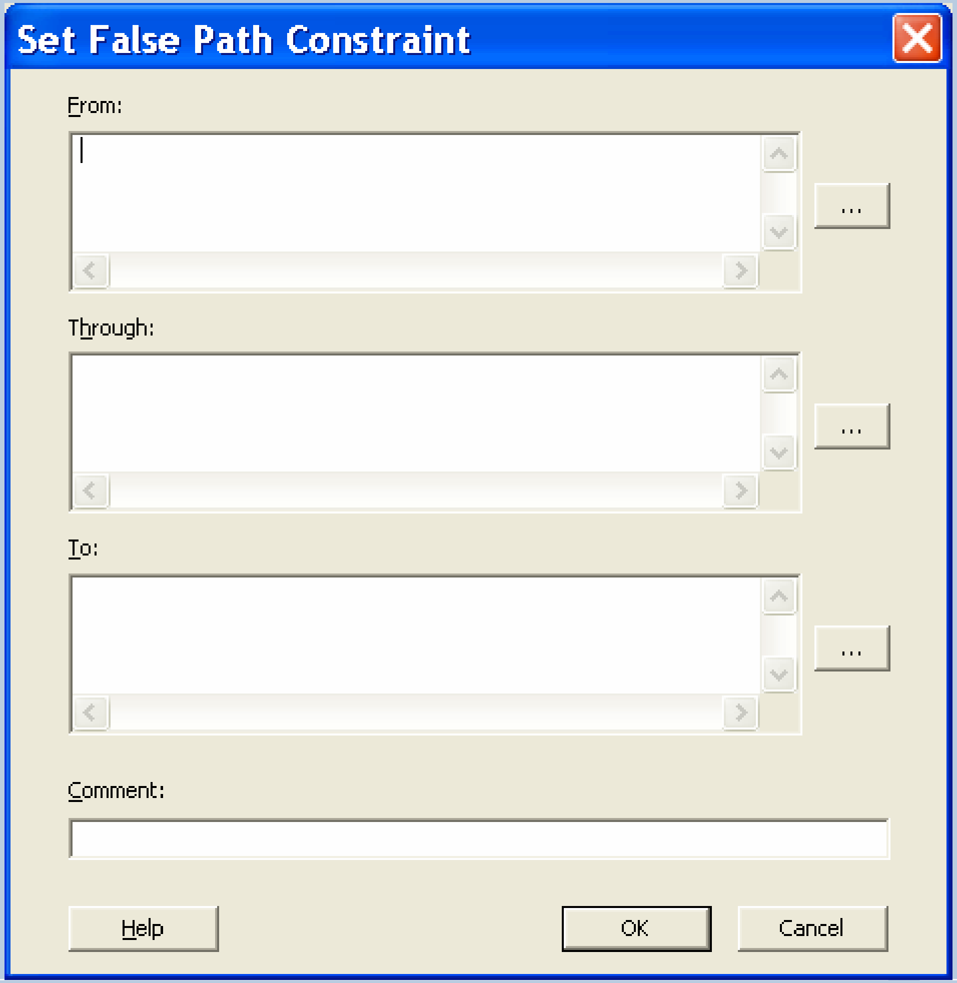
# Timing Exceptions
## *False Paths*

- The False Path Constraint Removes Timing Requirements on Specified Paths
  - Starting Points Are Input Ports or Register Clock Pins
  - Ending Points Are the Register Data Pins or Output Ports
- False Paths Are Not Considered During the Timing Analysis
- False Path Constraints Take Precedence Over Multiple Cycle Path Constraints and Overrides Maximum Delay Constraints

# SmartTime
## *Entering False Path Constraints*

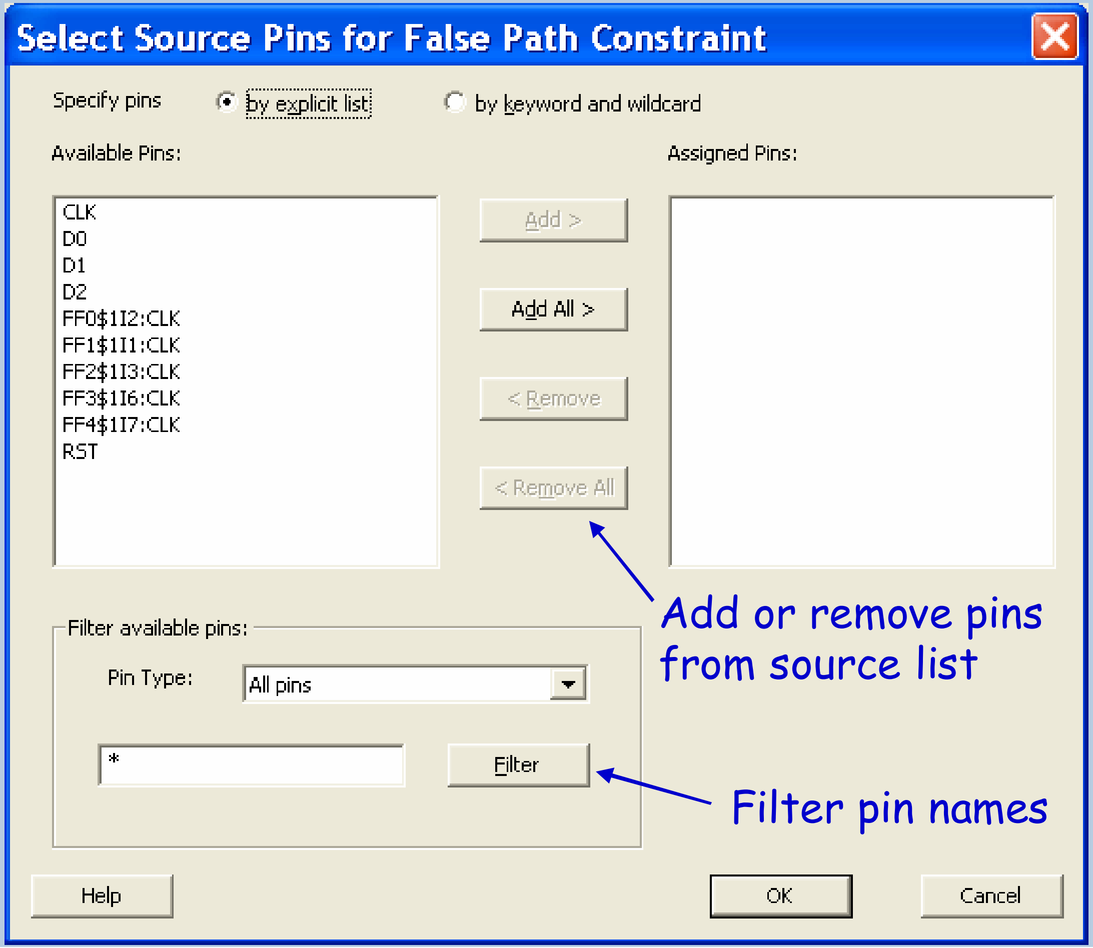
- Specify From, To, Through Pins





# False Path Constraint
*Source Pins*

## Specify Starting Point for False Path



Select Source Pins for False Path Constraint

Specify pins ● by explicit list ○ by keyword and wildcard

Available Pins:

- CLK
- D0
- D1
- D2
- FF0$1I2:CLK
- FF1$1I1:CLK
- FF2$1I3:CLK
- FF3$1I6:CLK
- FF4$1I7:CLK
- RST

Assigned Pins:

Filter available pins:

Pin Type: All pins

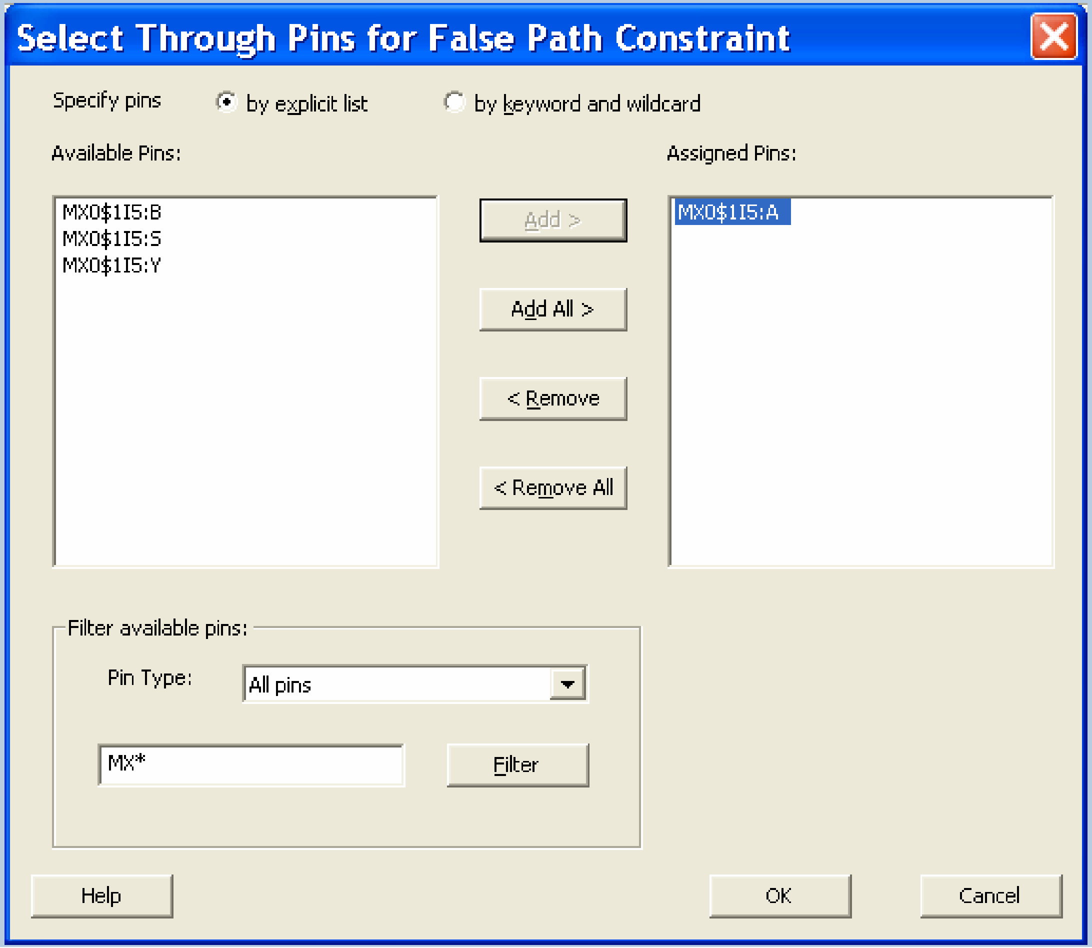
*

Add or remove pins from source list

Filter pin names

# False Path Constraint
*Through Pins*

- Select a List of Pins or Nets for the False Path Passes Through



Select Through Pins for False Path Constraint

Specify pins ● by explicit list ○ by keyword and wildcard

Available Pins:

MX0$1I5:B
MX0$1I5:S
MX0$1I5:Y

Assigned Pins:

MX0$1I5:A

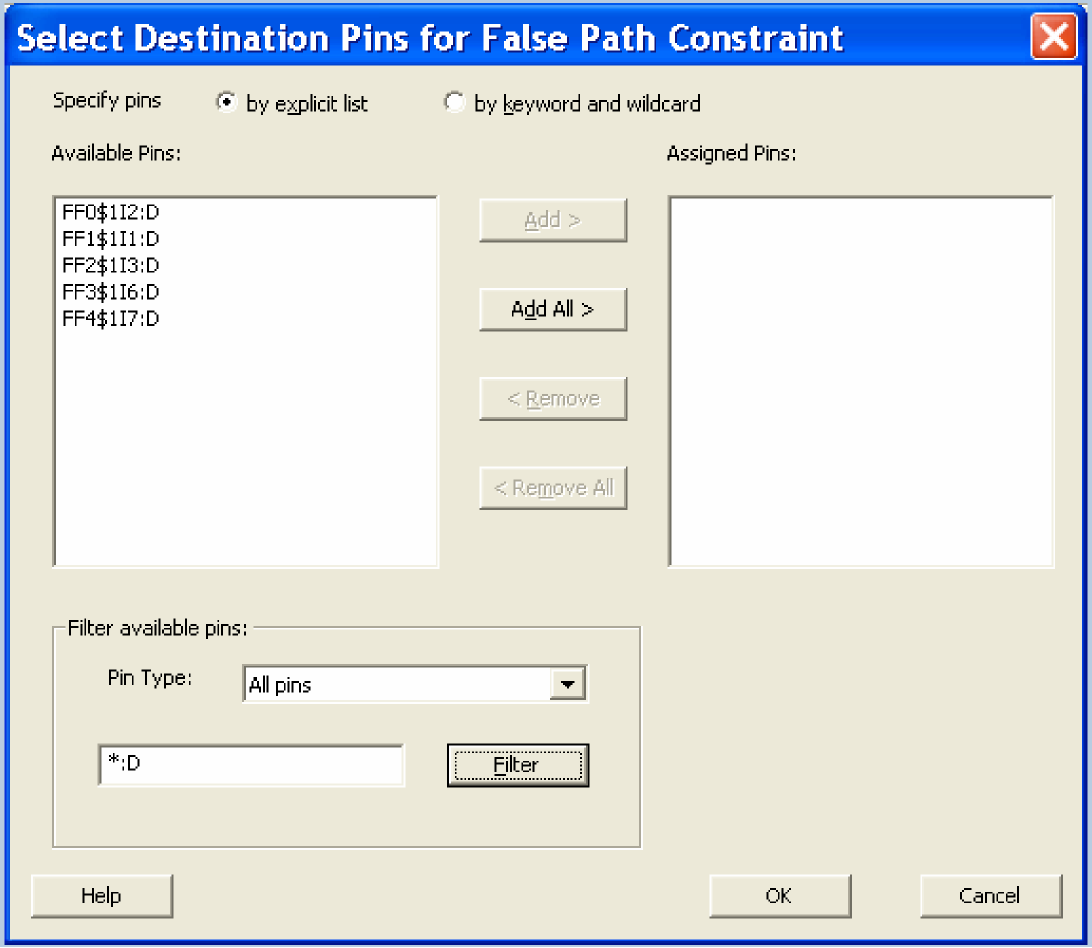
Filter available pins:

Pin Type: All pins

MX*

# False Path Constraint
## *Destination Pins*

- Specify the End Points for the False Path



Select Destination Pins for False Path Constraint

Specify pins ● by explicit list ○ by keyword and wildcard

Available Pins:

FF0$1I2:D
FF1$1I1:D
FF2$1I3:D
FF3$1I6:D
FF4$1I7:D

Assigned Pins:

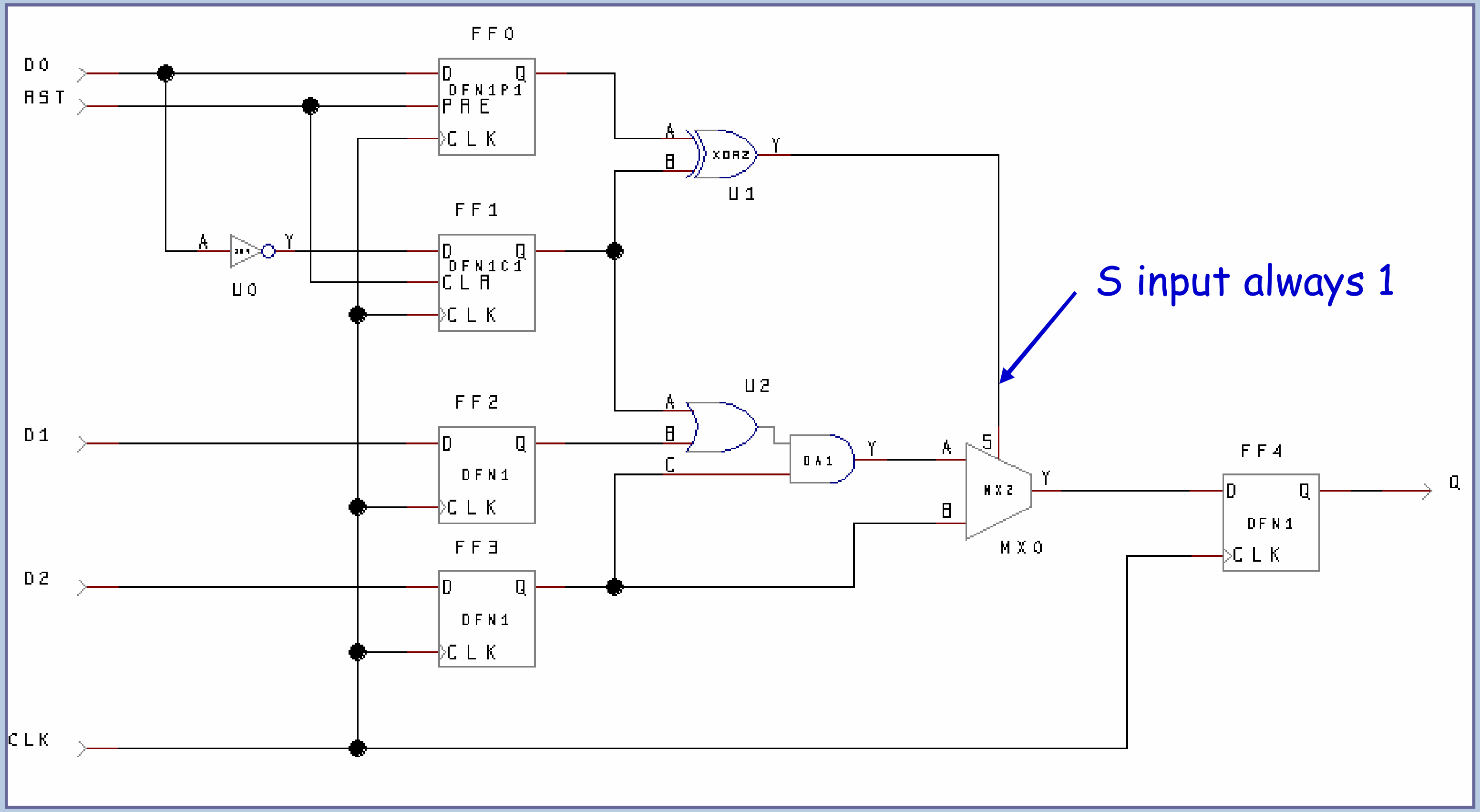
Filter available pins:

Pin Type: All pins

*:D

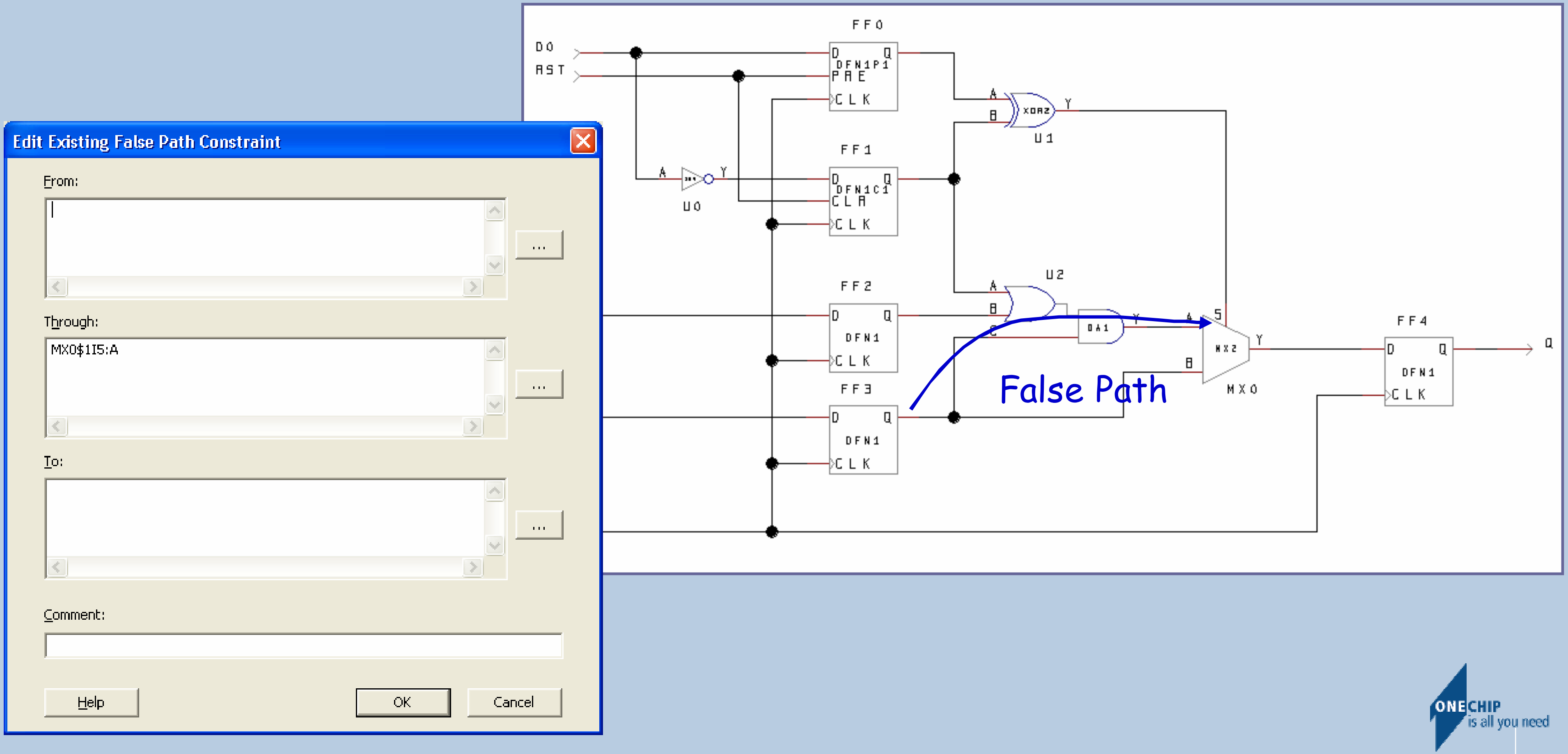
# False Path Example

- Multiplexer S Input Never Changes
  - **FF1, FF2 and FF3 to FF4 through MX0:A are False Paths**



# False Path Example (cont.)

- False Path Constraint Through MX0:A



Edit Existing False Path Constraint

From:

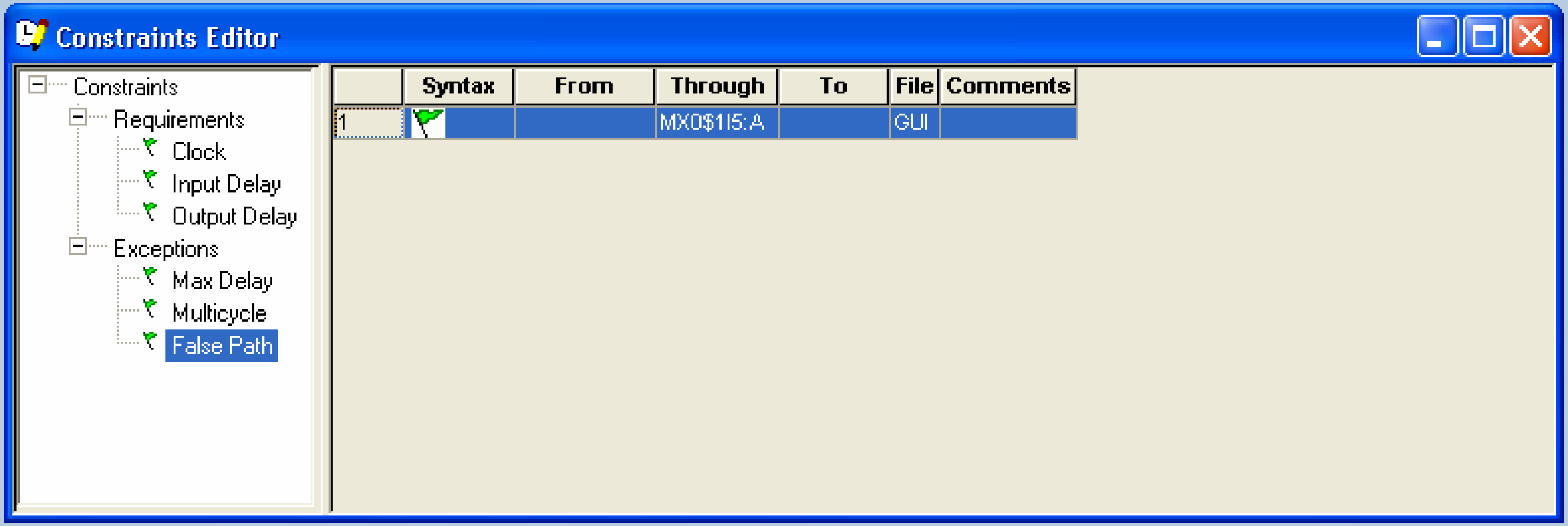
Through: MX0$1I5:A

To:

Comment:

# False Paths in Constraint Editor

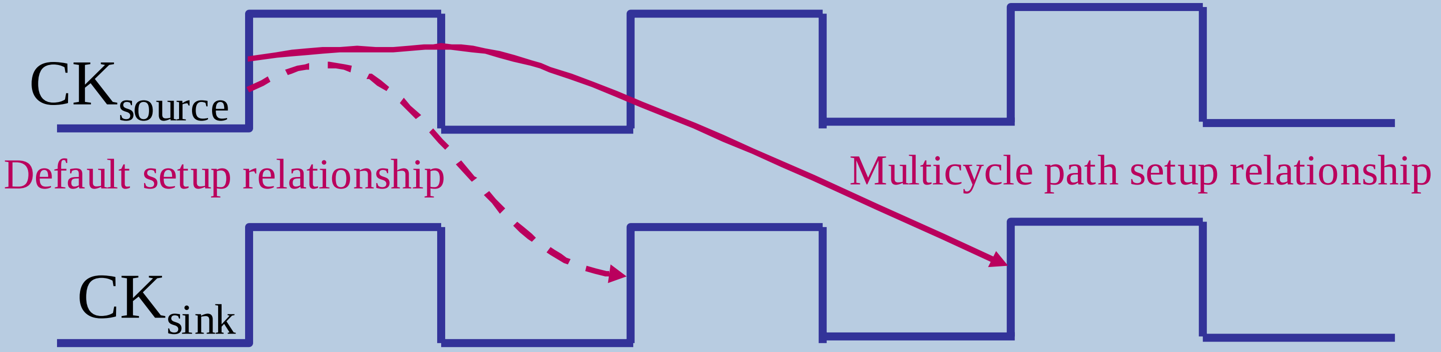
- False Path Constraint in Constraint Editor
  - **Select Constraint to Add, Edit or Delete**



| | Syntax | From | Through | To | File | Comments |
|---|---|---|---|---|---|---|
| 1 | ✓ | | MX0$1I5:A | | GUI | |

# Timing Exceptions
## *Multicycle Paths*

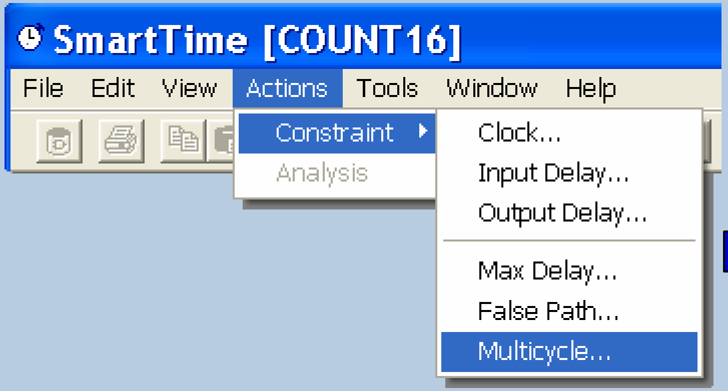
- The Multicycle Path Constraint Overrides the Single Cycle Timing Requirement Between Sequential Elements
  - **The Number of Clock Cycles for Setup or Hold Check Is Specified in the Constraint**
- False Path Constraints Take Precedence Over Multicycle Path Constraints

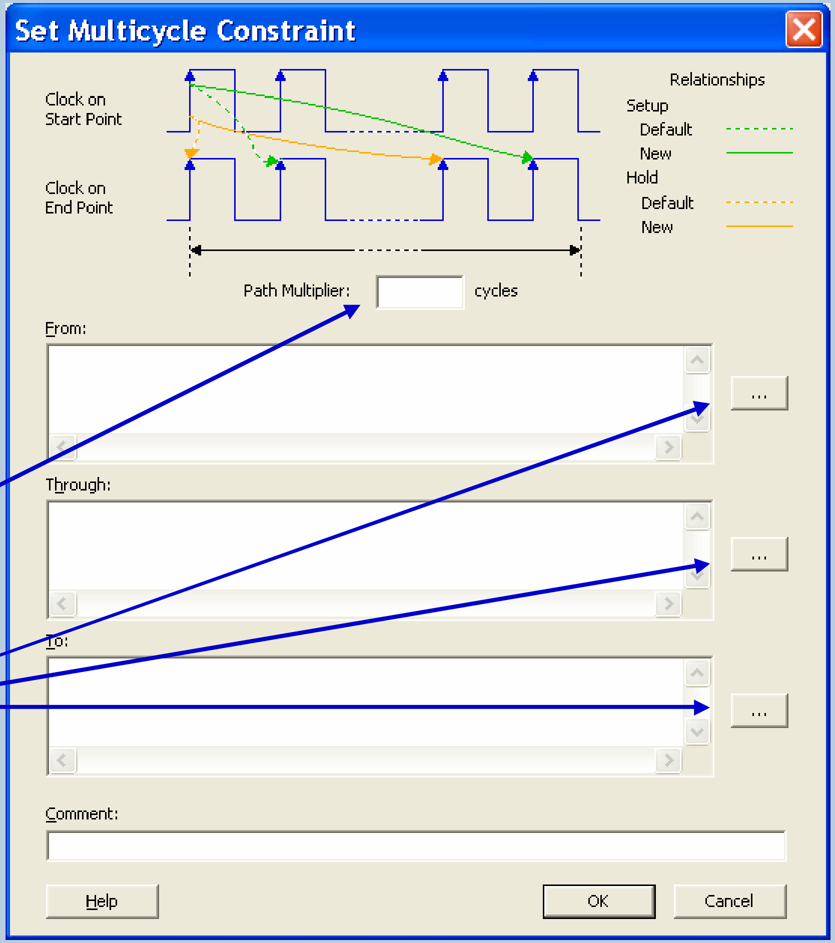


$CK_{source}$
Default setup relationship
Multicycle path setup relationship
$CK_{sink}$

# SmartTime
## *Entering Multicycle Path Constraints*

- Specify Path Multiplier and From, To, Through Pins
- Add Path Multiplier





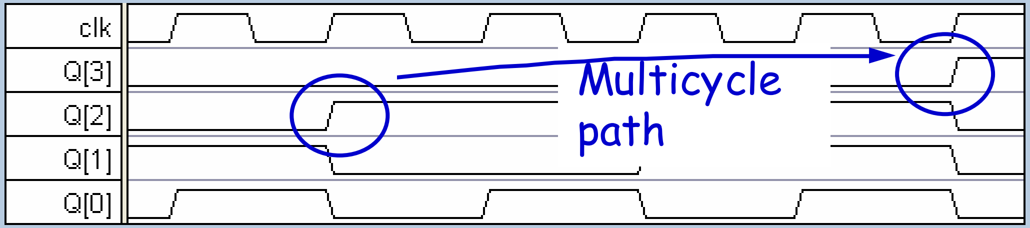
Enter path multiplier

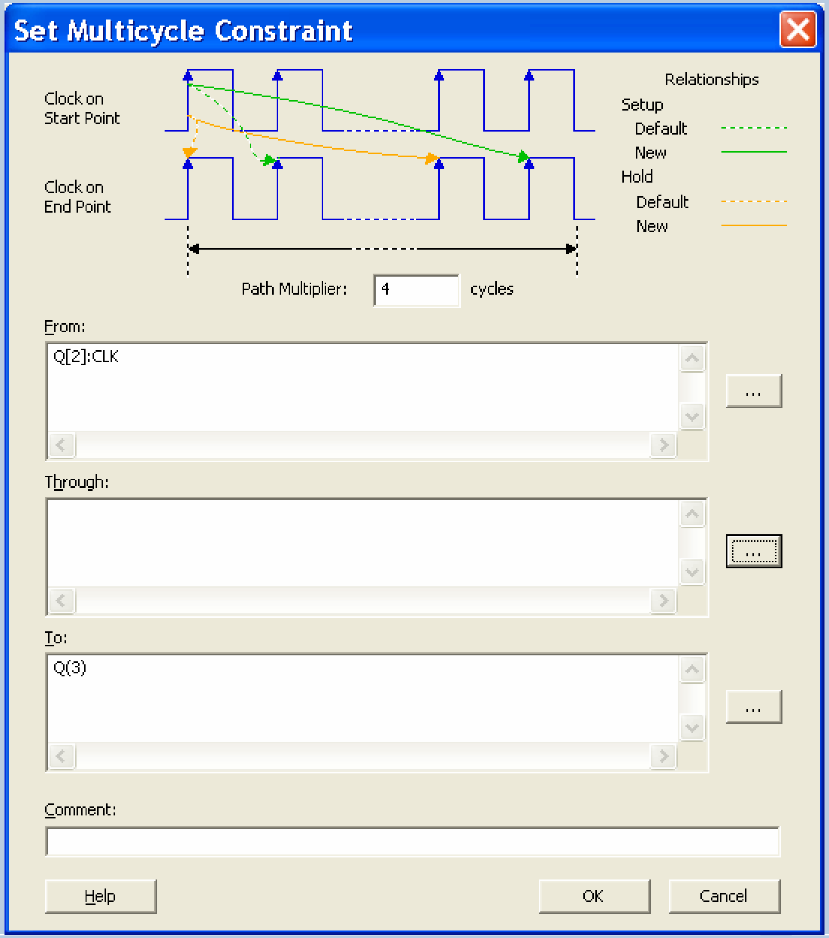
Browse for From, Through or To pins

# Multicycle Path Example
*Binary counter*

## Binary Counters Contain Multicycle Paths

- **Enter Multicycle Constraint to Obtain Proper Timing Analysis**





Path Multiplier: 4 cycles

From:
Q[2]:CLK

Through:

To:
Q(3)

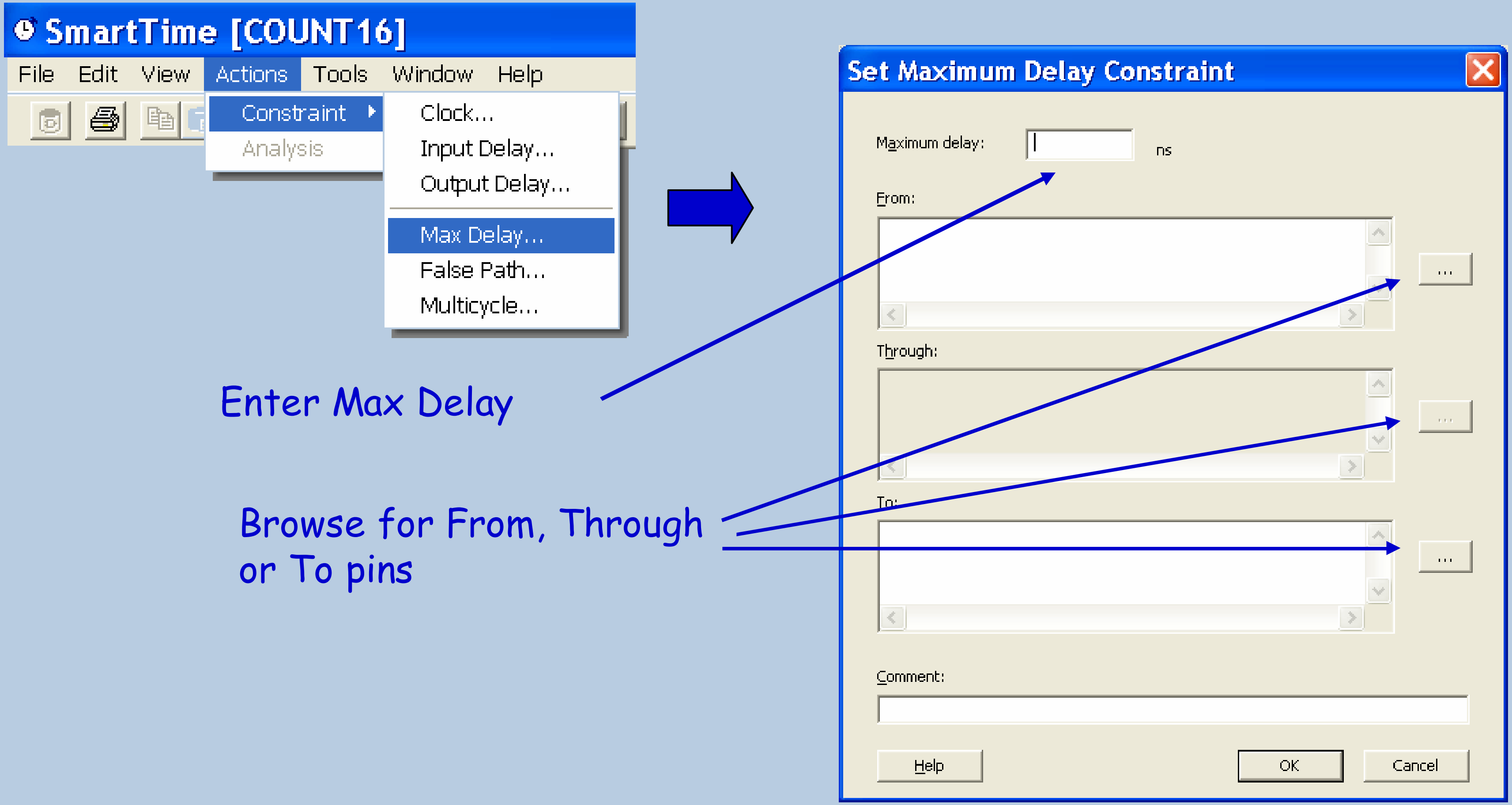
Comment:

# Timing Exceptions
## *Maximum Delay*

- The Max Delay Constraint Is Used To Specify The Maximum Delay For Timing Paths In The Design
- Max Delay Is A Timing Exception And Overrides The Timing Requirement Between Sequential Elements
- Max Delay Can Also Be Used To Constrain Input To Output Paths In Combinatorial Designs

# Timing Exceptions
## *Maximum Delay*

- Maximum Delay Constraint Overrides Clock Constraint



Enter Max Delay

Browse for From, Through or To pins

# SmartTime 7.2
## *New Features*

- Clock Source Latency
- Asynchronous Checks
- Datasheet Generation
- Tcl Commands
- Additional Ease-of-Use Features
  - **User sets management (editing, adding exceptions…)**
  - **Clock network details in expand path**
  - **Automatic creation of generated-clocks on PLLs**
  - **Multicycle with hold specifier**
  - **Expanding parallel paths**
  - **Reports in spreadsheet format**
  - **Logic stage count column in analysis window**
  - **Clock constraints in summary window**
  - **Select all in add path set dialog**
  - **Path aware exceptions**
  - **Improved auto-TDPR constraint setting**

# SmartTime 7.2
## *New Constraint Entry Features*

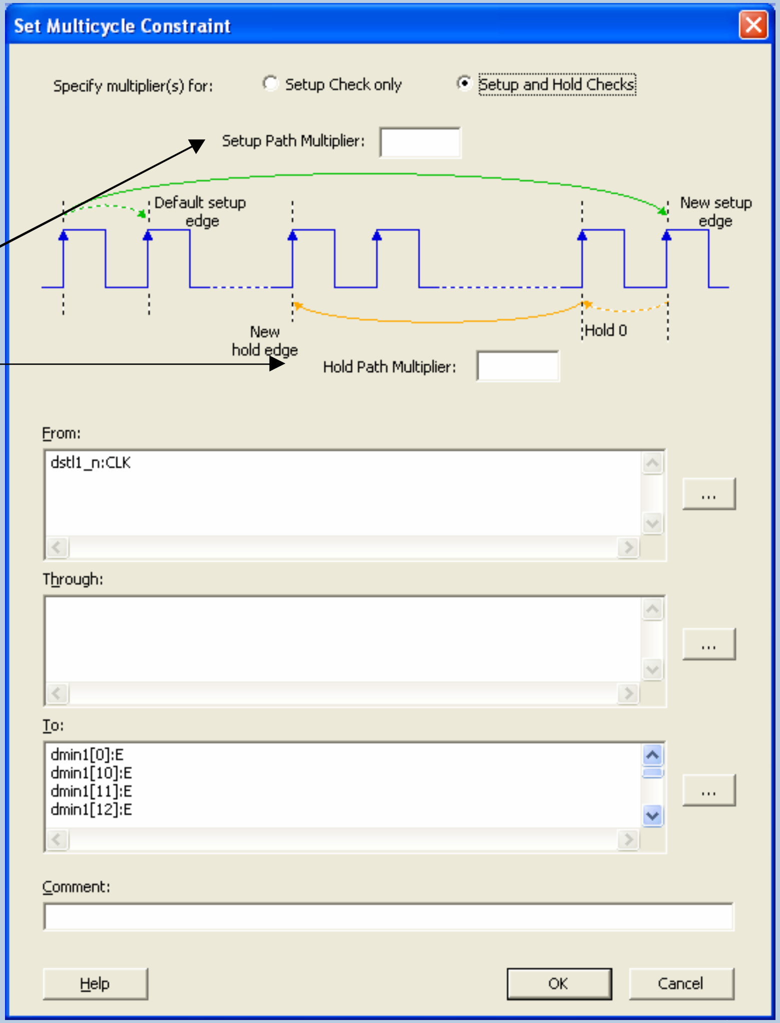
- Specify Multicycle Path Constraint for Setup, Hold or Both
  - **Supported in GUI and SDC Commands**
- Specify Clock Source Latency
  - **Use to Model Clock Insertion Delay when Clock Generation is not part of the Design**
- Specify Early and Late Clock Arrival Times
  - **Analyze Performance for Clock Jitter**
- Automatic Creation of Generated Clocks
- New TCL Commands

# SmartTime 7.2

## *Multicyle Path Constraints*

- Specify Whether Multicycle Path Applies to Setup Check, Hold Check or Both

Specify different multiplier for setup analysis and hold analysis



Set Multicycle Constraint

Specify multiplier(s) for: ○ Setup Check only ● Setup and Hold Checks

Setup Path Multiplier:

Hold Path Multiplier:

From:

dstl1_n:CLK

Through:

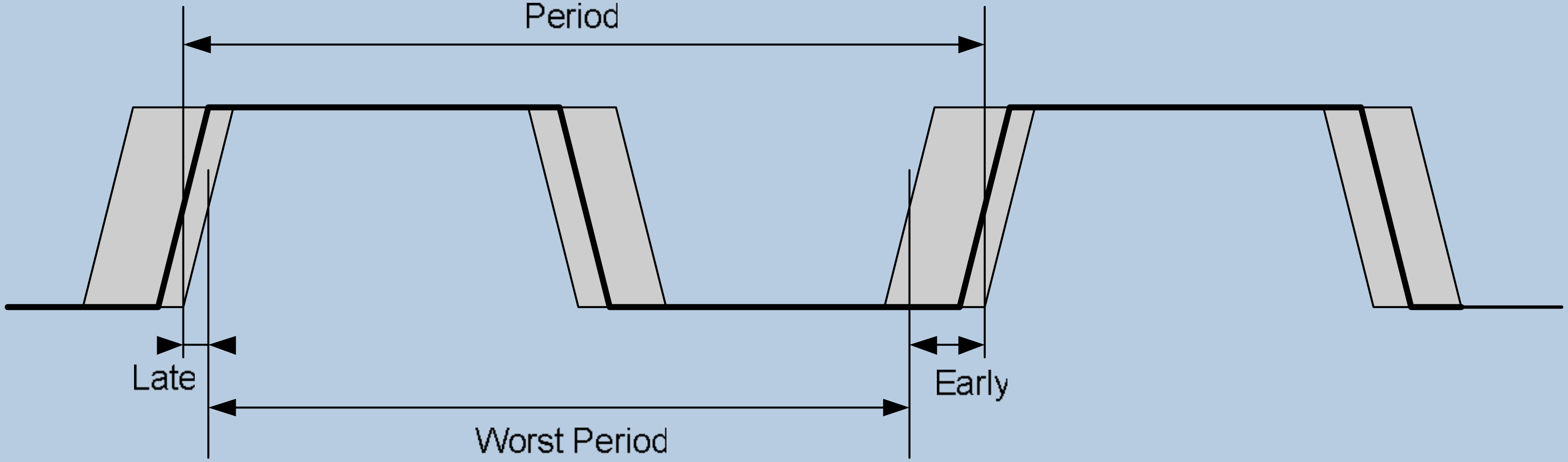
To:

dmin1[0]:E
dmin1[10]:E
dmin1[11]:E
dmin1[12]:E

Comment:

# Clock Source Latency:
*Definition*

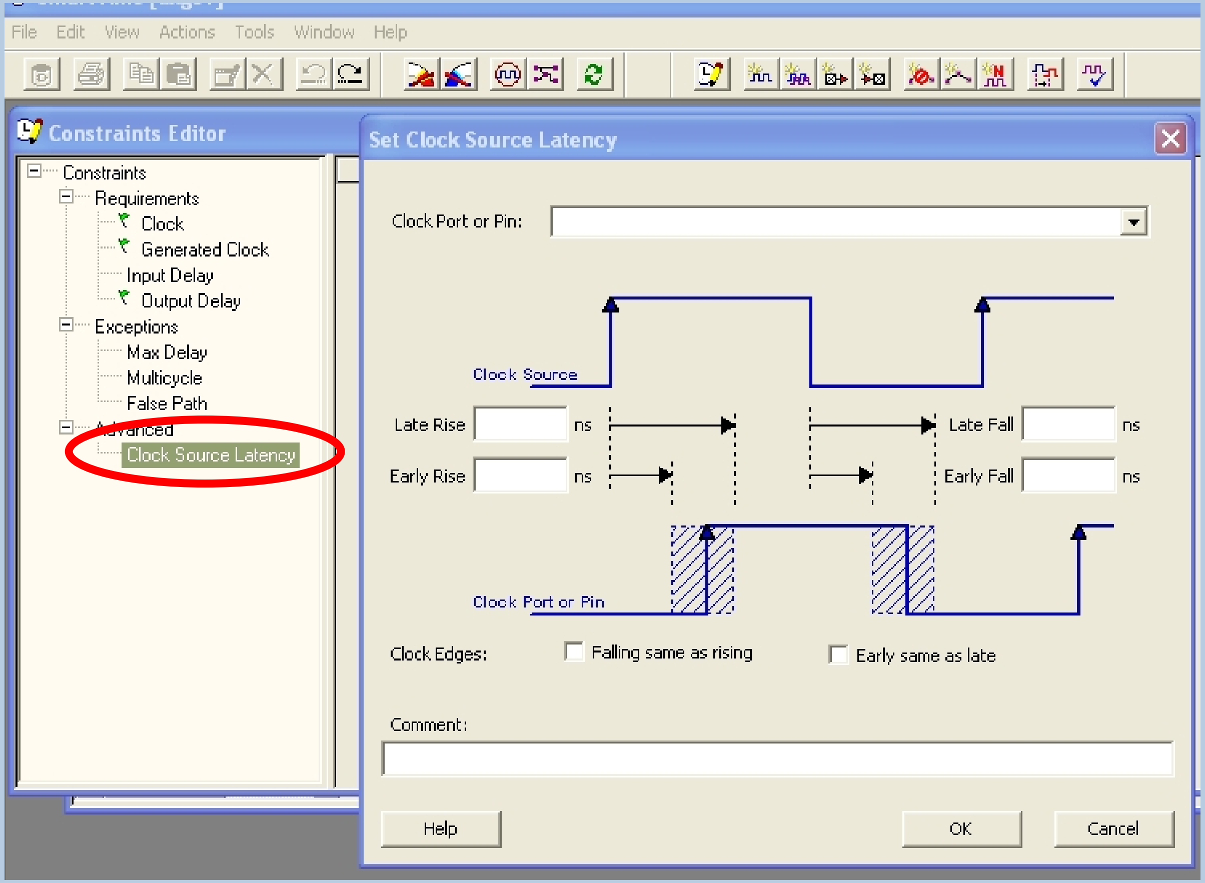
- Specify delay when clock is generated outside the design
- Specify clock jitter



- Clock Source Latency can be attached to any clock constraint (internal or external)

# Clock Source Latency: *Constraints Specification*

- Specify Clock Insertion Delay
- Specify Early and Late Times for Rising and Falling Edges
- SDC Constraint: **`set_clock_latency`**



Clock Port or Pin:

Late Rise ns

Early Rise ns

Late Fall ns

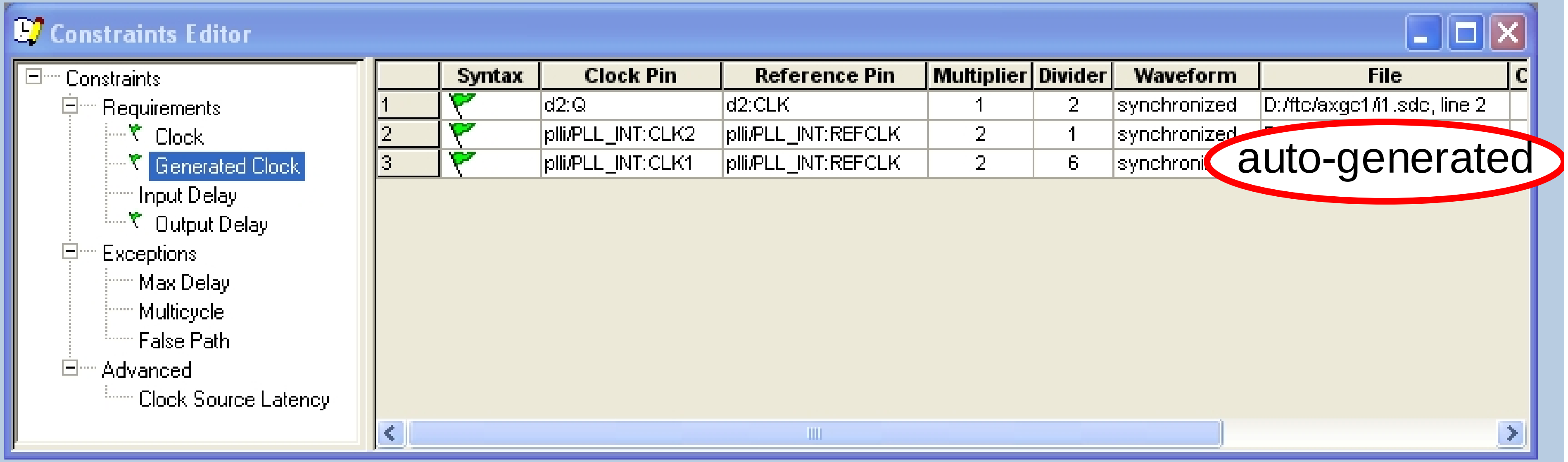
Early Fall ns

Clock Edges: □ Falling same as rising □ Early same as late

Comment:

# SmartTime 7.2
## *Automatic Creation of Generated Clocks*

- Automatic Creation Of Generated Clock Constraint Based On Static Configuration of PLLs for AX, RTAX-S, Fusion, ProASIC3/E
- No Effect Unless The Clock Reference Has A Clock Constraint



| | Syntax | Clock Pin | Reference Pin | Multiplier | Divider | Waveform | File | C |
|---|---|---|---|---|---|---|---|---|
| 1 | ✓ | d2:Q | d2:CLK | 1 | 2 | synchronized | D:/ftc/axgc1/i1.sdc, line 2 | |
| 2 | ✓ | plli/PLL_INT:CLK2 | plli/PLL_INT:REFCLK | 2 | 1 | synchronized | | |
| 3 | ✓ | plli/PLL_INT:CLK1 | plli/PLL_INT:REFCLK | 2 | 6 | synchroni | | |

auto-generated

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# SmartTime 7.2
## *New TCL Commands*

- `st_create_set` - Creates A Set Of Paths To Be Analyzed
- `st_edit_set` - Modify The Paths In A User Set
- `st_remove_set` - Deletes A User Set From The Design
- `st_commit` - Saves The Changes Made In SmartTime To The Design .adb File
- `st_restore` - Restores Constraints Previously Committed In SmartTime
- `st_expand_path` - Displays Expanded Path Information For Paths
- `st_set_options` - Sets options for timing analysis
- `st_list_paths` - Displays the list of paths in the same tabular format shown in SmartTime

# Timing Analysis with SmartTime

Actel

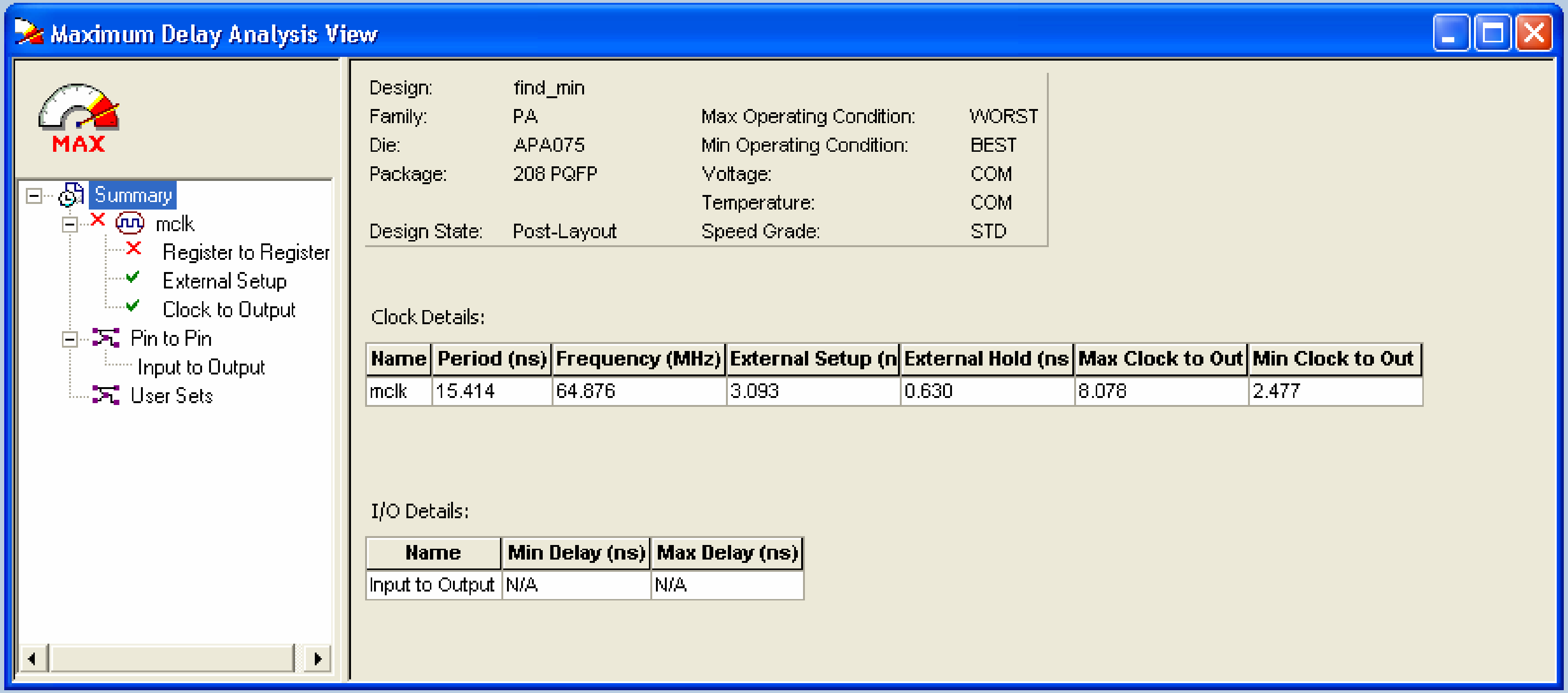
# Timing Analysis with SmartTime

- Design Summary
- Setup and Hold Checks
- Cross Clock Domain Analysis
- Adding User Sets and Filtering
- Customizing the Analysis View
- Cross-Probing with MVN Tools

ONE CHIP is all you need

# SmartTime Analysis View
*Design Summary*

- Performance Summary is Displayed in Maximum and Minimum Delay Analysis View
  - √ - **Indicates Timing Requirements Met for That Domain**
  - X – **Indicates There Are Violations Within the Domain**



| | | | |
|---|---|---|---|
| Design: | find_min | | |
| Family: | PA | Max Operating Condition: | WORST |
| Die: | APA075 | Min Operating Condition: | BEST |
| Package: | 208 PQFP | Voltage: | COM |
| | | Temperature: | COM |
| Design State: | Post-Layout | Speed Grade: | STD |

Clock Details:

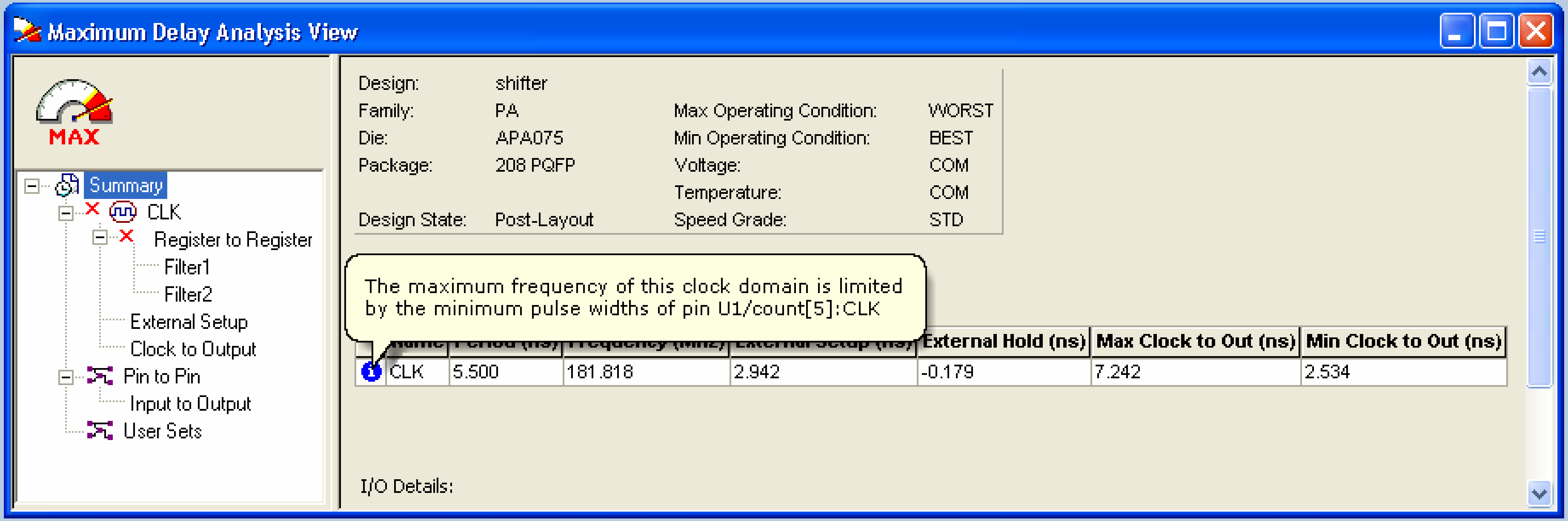
| Name | Period (ns) | Frequency (MHz) | External Setup (n | External Hold (ns | Max Clock to Out | Min Clock to Out |
|---|---|---|---|---|---|---|
| mclk | 15.414 | 64.876 | 3.093 | 0.630 | 8.078 | 2.477 |

I/O Details:

| Name | Min Delay (ns) | Max Delay (ns) |
|---|---|---|
| Input to Output | N/A | N/A |

# SmartTime
## *Design Summary*

- Minimum pulse width check performed on paths in design
  - Information is used to determine the maximum operating frequency reported in the SmartTime Design Summary



Design: shifter
Family: PA
Die: APA075
Package: 208 PQFP
Design State: Post-Layout

Max Operating Condition: WORST
Min Operating Condition: BEST
Voltage: COM
Temperature: COM
Speed Grade: STD

The maximum frequency of this clock domain is limited by the minimum pulse widths of pin U1/count[5]:CLK

| Name | Period (ns) | Frequency (MHz) | External Setup (ns) | External Hold (ns) | Max Clock to Out (ns) | Min Clock to Out (ns) |
|---|---|---|---|---|---|---|
| CLK | 5.500 | 181.818 | 2.942 | -0.179 | 7.242 | 2.534 |

I/O Details:

# Timing Analysis with SmartTime

- Design Summary
- Setup and Hold Checks
- Cross Clock Domain Analysis
- Adding User Sets and Filtering
- Customizing the Analysis View
- Cross-Probing with MVN Tools

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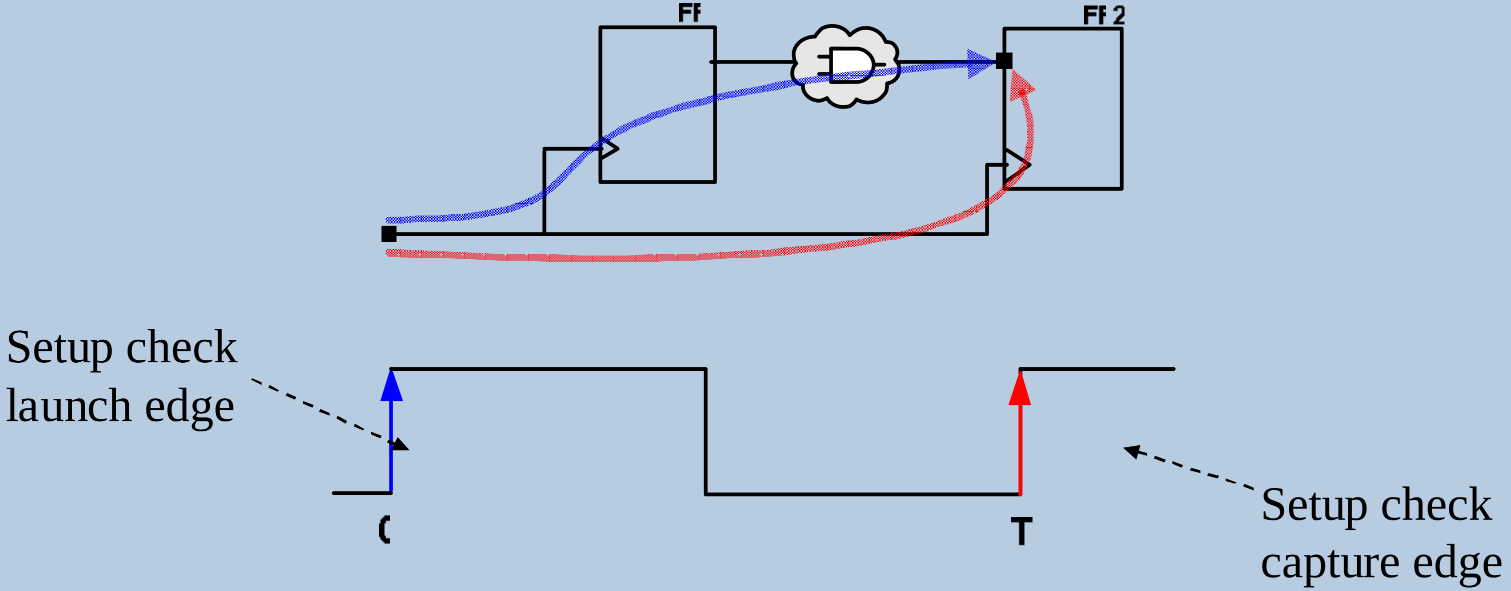
# SmartTime
## *Setup Check*

- Setup Check is Displayed in Maximum Delay Analysis View

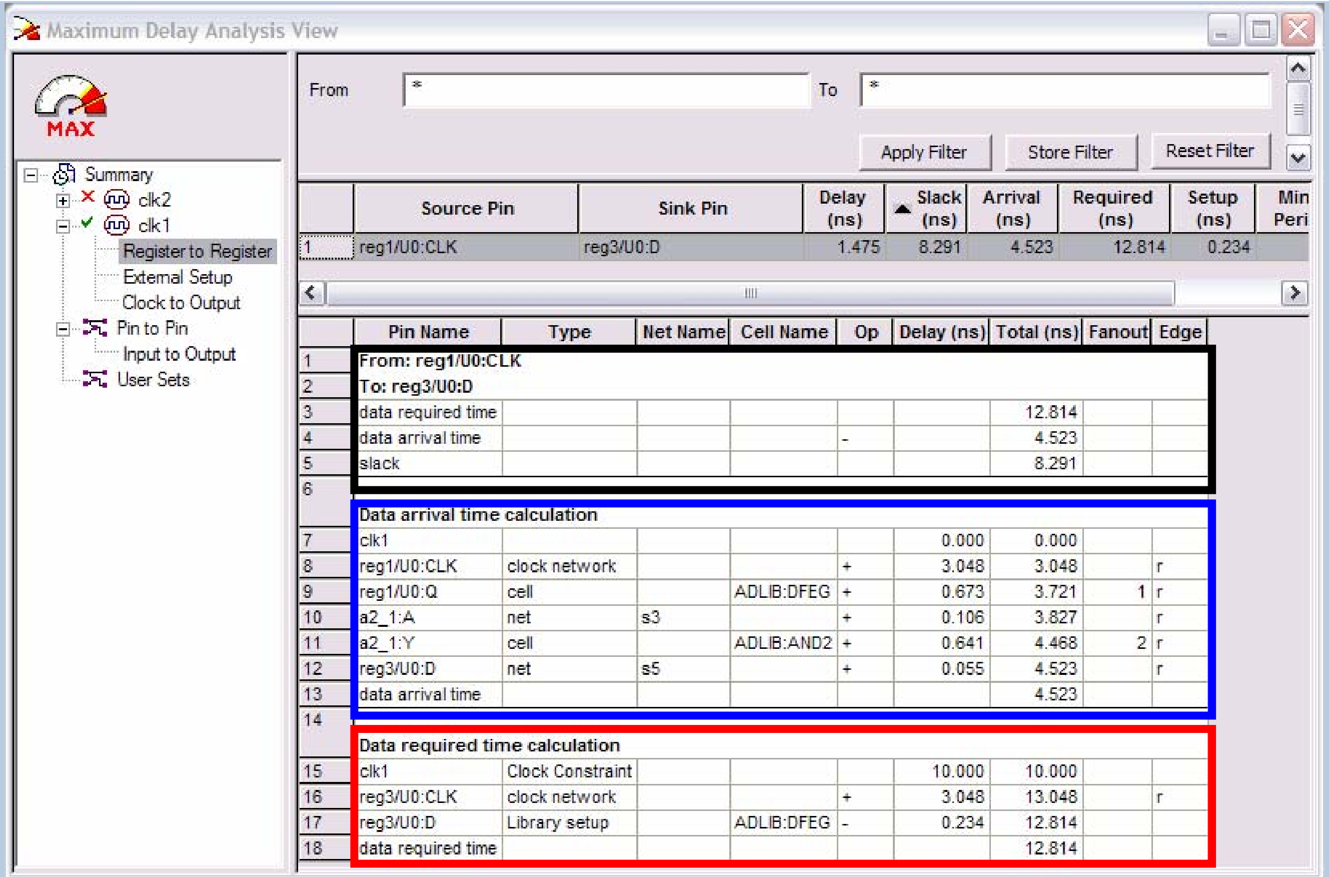


Setup check launch edge

Setup check capture edge

- Setup Check Calculation
  - **Arrival time = Launch edge (0) + max Clock to FF1 + max Data path**
  - **Required time = Capture edge (T) + min Clock to FF2 – Setup of FF2**
  - **Slack = Required – Arrival = Violation if < 0**

# Setup Check in SmartTime



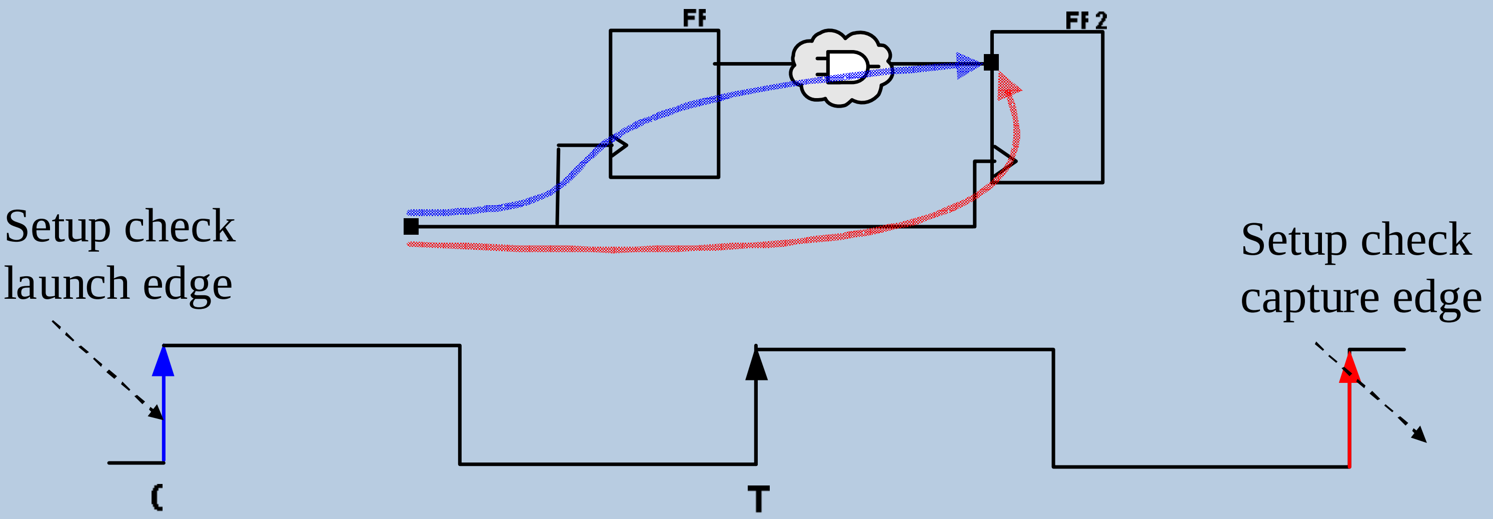
| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) | Min Peri |
|---|---|---|---|---|---|---|---|---|
| 1 | reg1/U0:CLK | reg3/U0:D | 1.475 | 8.291 | 4.523 | 12.814 | 0.234 | |

| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | From: reg1/U0:CLK | | | | | | | | |
| 2 | To: reg3/U0:D | | | | | | | | |
| 3 | data required time | | | | | | 12.814 | | |
| 4 | data arrival time | | | | - | | 4.523 | | |
| 5 | slack | | | | | | 8.291 | | |
| 6 | | | | | | | | | |
| | Data arrival time calculation | | | | | | | | |
| 7 | clk1 | | | | | 0.000 | 0.000 | | |
| 8 | reg1/U0:CLK | clock network | | | + | 3.048 | 3.048 | | r |
| 9 | reg1/U0:Q | cell | | ADLIB:DFEG | + | 0.673 | 3.721 | 1 | r |
| 10 | a2_1:A | net | s3 | | + | 0.106 | 3.827 | | r |
| 11 | a2_1:Y | cell | | ADLIB:AND2 | + | 0.641 | 4.468 | 2 | r |
| 12 | reg3/U0:D | net | s5 | | + | 0.055 | 4.523 | | r |
| 13 | data arrival time | | | | | | 4.523 | | |
| 14 | | | | | | | | | |
| | Data required time calculation | | | | | | | | |
| 15 | clk1 | Clock Constraint | | | | 10.000 | 10.000 | | |
| 16 | reg3/U0:CLK | clock network | | | + | 3.048 | 13.048 | | r |
| 17 | reg3/U0:D | Library setup | | ADLIB:DFEG | - | 0.234 | 12.814 | | |
| 18 | data required time | | | | | | 12.814 | | |

- Setup Check
  - **Arrival time = Launch edge (0) + max Clock to FF1 + max Data path**
  - **Required time = Capture edge (T) + min Clock to FF2 – Setup of FF2**
  - **Slack = Required – Arrival = Violation if < 0**

# Setup Check w/ Multicycle Path

- SmartTime Uses Multicycle Path Constraint in Setup Check

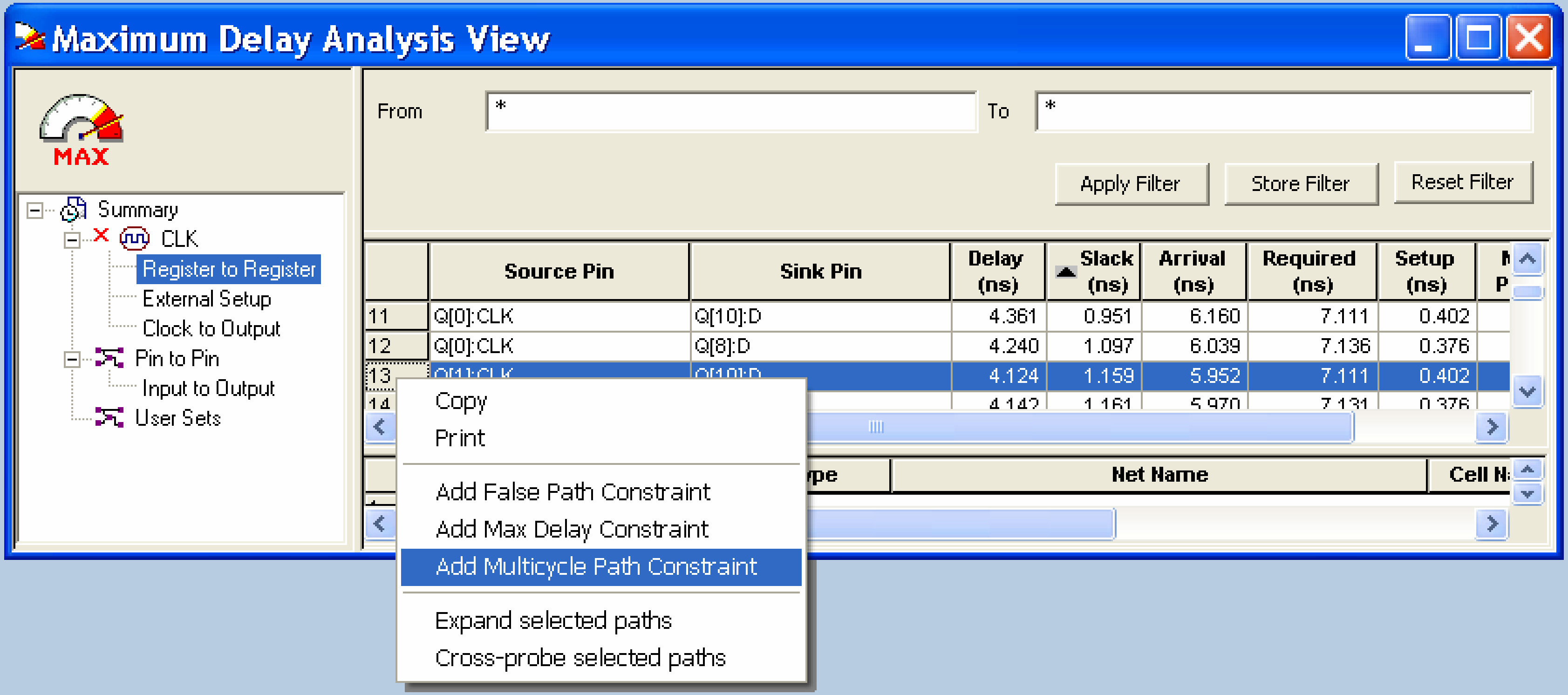


- Setup Check Calculation
  - **Arrival time = Launch edge (0) + max Clock to FF1 + max Data path**
  - **Required time = Capture edge (2T) + min Clock to FF2 – Setup of FF2**
  - **Slack = Required – Arrival = Violation if < 0**

# Setup Check w/ Multicycle Path

## Add Multicycle Exception from Analysis View

- **Right-click on the Path in the Analysis Window**



From *

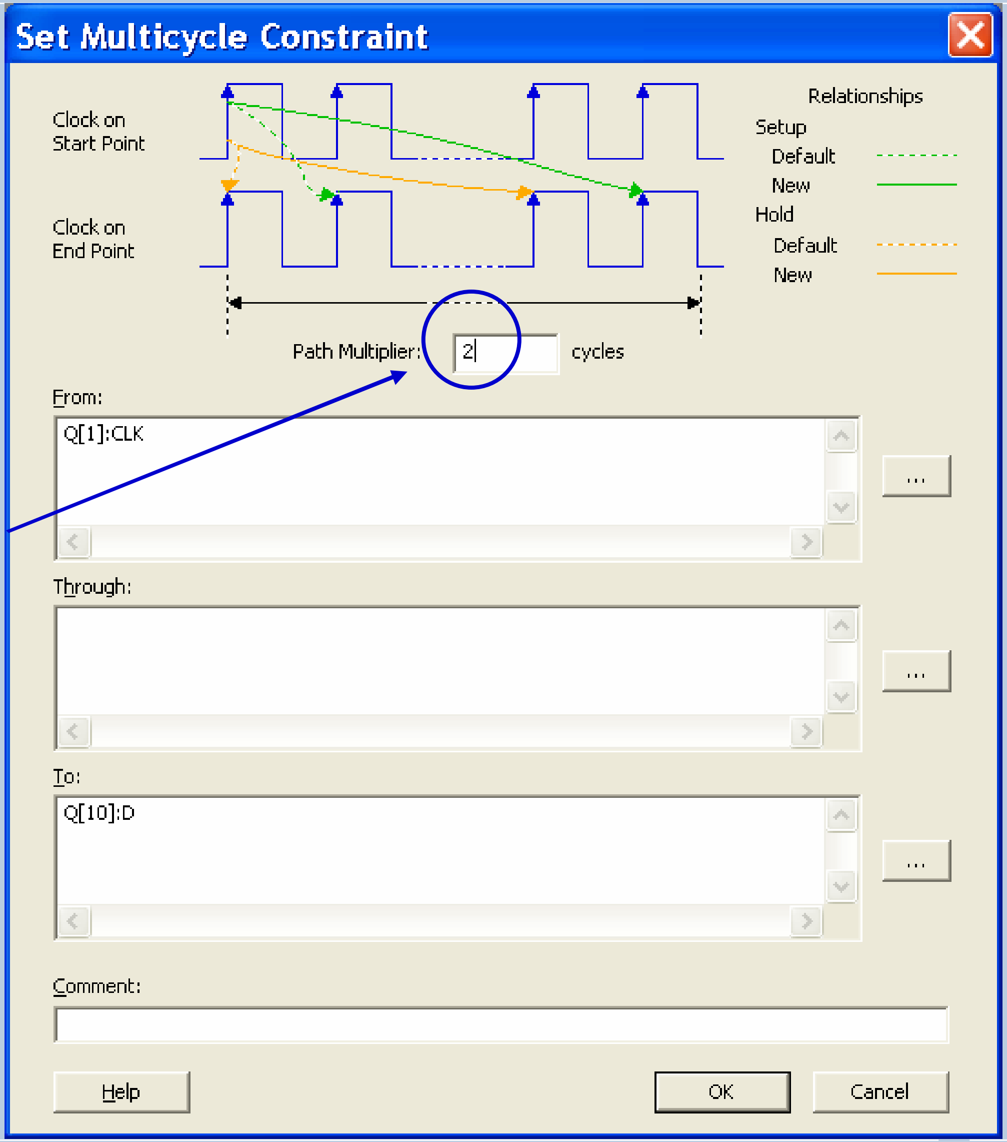
To *

| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) |
|---|---|---|---|---|---|---|---|
| 11 | Q[0]:CLK | Q[10]:D | 4.361 | 0.951 | 6.160 | 7.111 | 0.402 |
| 12 | Q[0]:CLK | Q[8]:D | 4.240 | 1.097 | 6.039 | 7.136 | 0.376 |
| 13 | Q[1]:CLK | Q[10]:D | 4.124 | 1.159 | 5.952 | 7.111 | 0.402 |
| 14 | | | 4.142 | 1.161 | 5.970 | 7.131 | 0.376 |

# Setup Check w/ Multicycle Path

- Add Multicycle Exception
  - Fields are pre-filled with the path information

Path multiplier = 2



Path Multiplier: 2 cycles

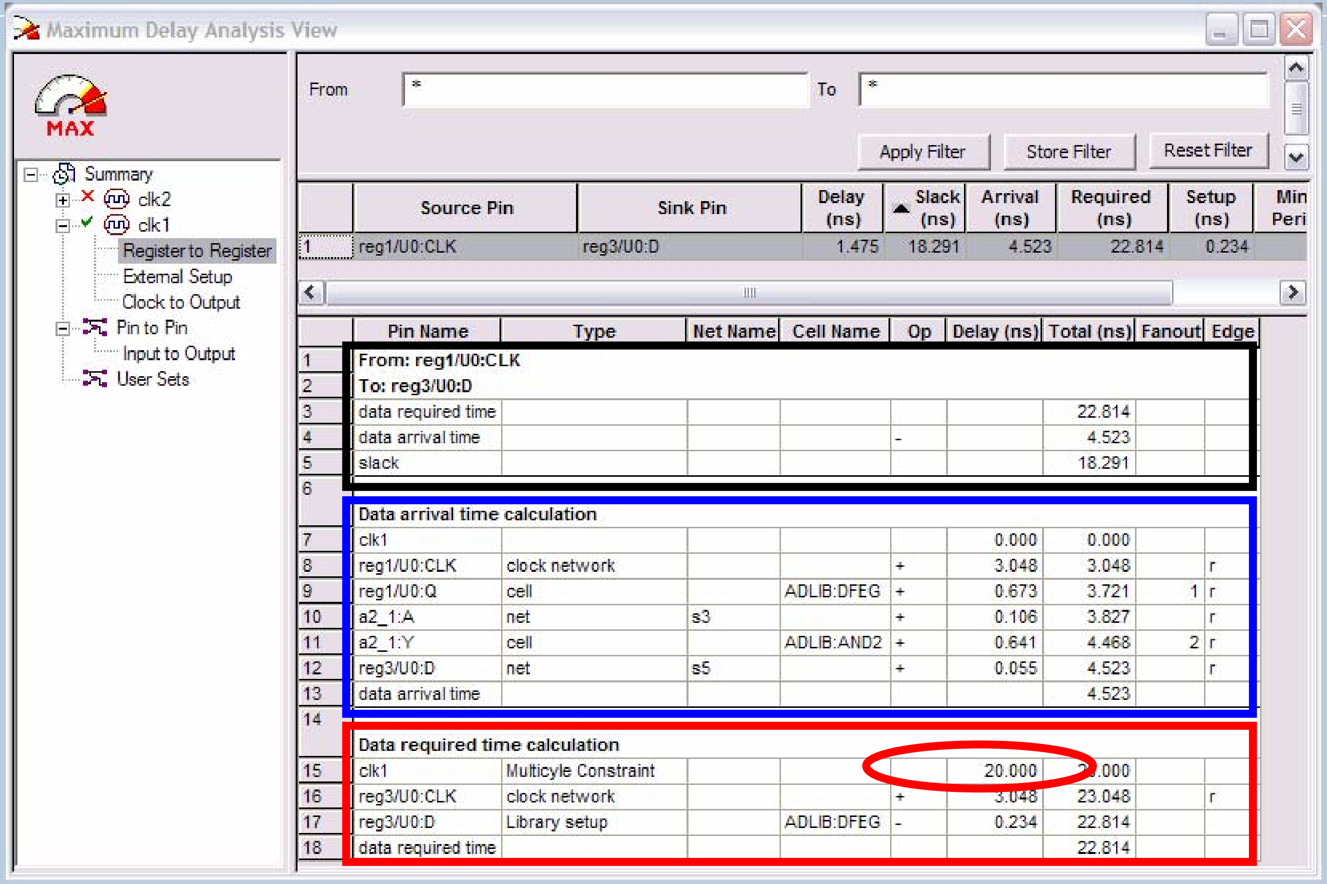
From: Q[1]:CLK

Through:

To: Q[10]:D

Comment:

# Setup Check w/ Multicycle Path



- Summary
  - clk2
  - clk1
    - Register to Register
    - External Setup
    - Clock to Output
  - Pin to Pin
    - Input to Output
  - User Sets

From *  To *

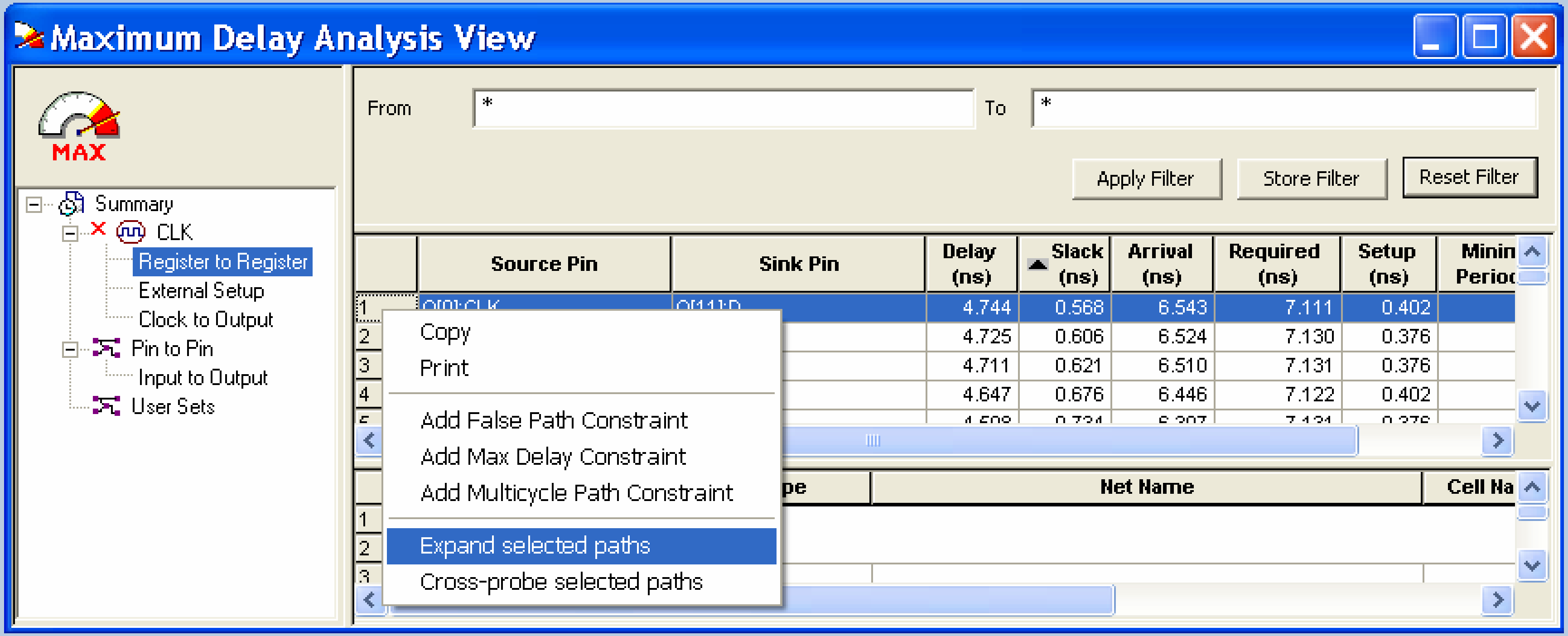
|  | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) | Min Peri |
|---|---|---|---|---|---|---|---|---|
| 1 | reg1/U0:CLK | reg3/U0:D | 1.475 | 18.291 | 4.523 | 22.814 | 0.234 |  |

|  | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | From: reg1/U0:CLK |  |  |  |  |  |  |  |  |
| 2 | To: reg3/U0:D |  |  |  |  |  |  |  |  |
| 3 | data required time |  |  |  |  |  | 22.814 |  |  |
| 4 | data arrival time |  |  |  | - |  | 4.523 |  |  |
| 5 | slack |  |  |  |  |  | 18.291 |  |  |
| 6 |  |  |  |  |  |  |  |  |  |
| 7 | Data arrival time calculation |  |  |  |  |  |  |  |  |
| 7 | clk1 |  |  |  |  | 0.000 | 0.000 |  |  |
| 8 | reg1/U0:CLK | clock network |  |  | + | 3.048 | 3.048 |  | r |
| 9 | reg1/U0:Q | cell |  | ADLIB:DFEG | + | 0.673 | 3.721 | 1 | r |
| 10 | a2_1:A | net | s3 |  | + | 0.106 | 3.827 |  | r |
| 11 | a2_1:Y | cell |  | ADLIB:AND2 | + | 0.641 | 4.468 | 2 | r |
| 12 | reg3/U0:D | net | s5 |  | + | 0.055 | 4.523 |  | r |
| 13 | data arrival time |  |  |  |  |  | 4.523 |  |  |
| 14 |  |  |  |  |  |  |  |  |  |
|  | Data required time calculation |  |  |  |  |  |  |  |  |
| 15 | clk1 | Multicycle Constraint |  |  |  | 20.000 | 20.000 |  |  |
| 16 | reg3/U0:CLK | clock network |  |  | + | 3.048 | 23.048 |  | r |
| 17 | reg3/U0:D | Library setup |  | ADLIB:DFEG | - | 0.234 | 22.814 |  |  |
| 18 | data required time |  |  |  |  |  | 22.814 |  |  |

- Setup Check
  - **Arrival time = Launch edge (0) + max Clock to FF1 + max Data path**
  - **Required time = Capture edge (2T) + min Clock to FF2 – Setup of FF2**
  - **Slack = Required – Arrival = Violation if < 0**

# SmartTime
## *Expanded Path Timing Information*

- Right-click a Path in the Path List Displays the Expanded Path in a Separate Window



From *

To *

|  | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) | Minin Perioc |
|---|---|---|---|---|---|---|---|---|
| 1 | Q[0]:CLK | Q[11]:D | 4.744 | 0.568 | 6.543 | 7.111 | 0.402 |  |
| 2 |  |  | 4.725 | 0.606 | 6.524 | 7.130 | 0.376 |  |
| 3 |  |  | 4.711 | 0.621 | 6.510 | 7.131 | 0.376 |  |
| 4 |  |  | 4.647 | 0.676 | 6.446 | 7.122 | 0.402 |  |
| 5 |  |  | 4.598 | 0.734 | 6.397 | 7.131 | 0.376 |  |

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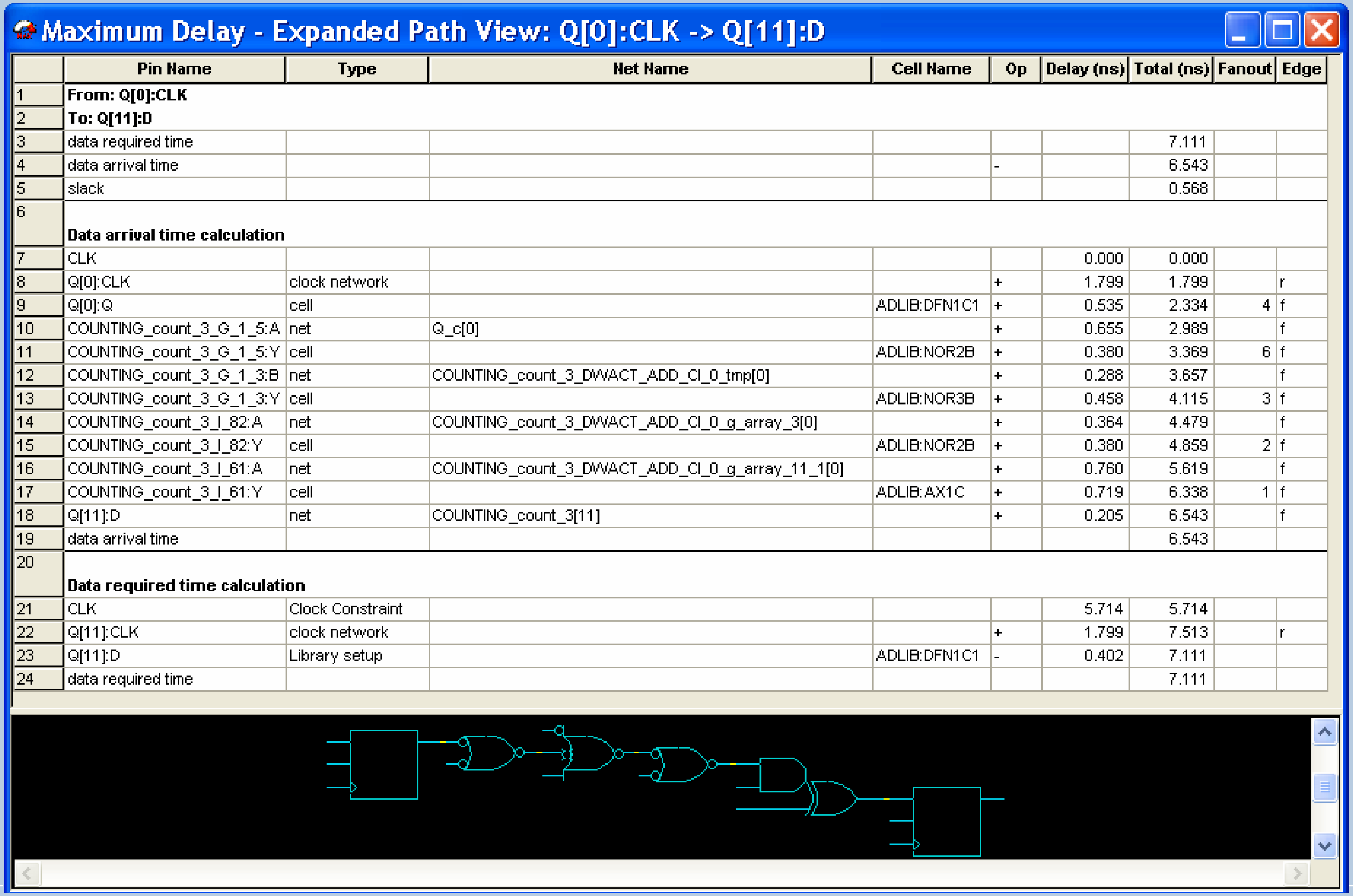
# SmartTime
## *Expanded Path (cont.)*

- Expanded Path View Includes a Schematic of the Path



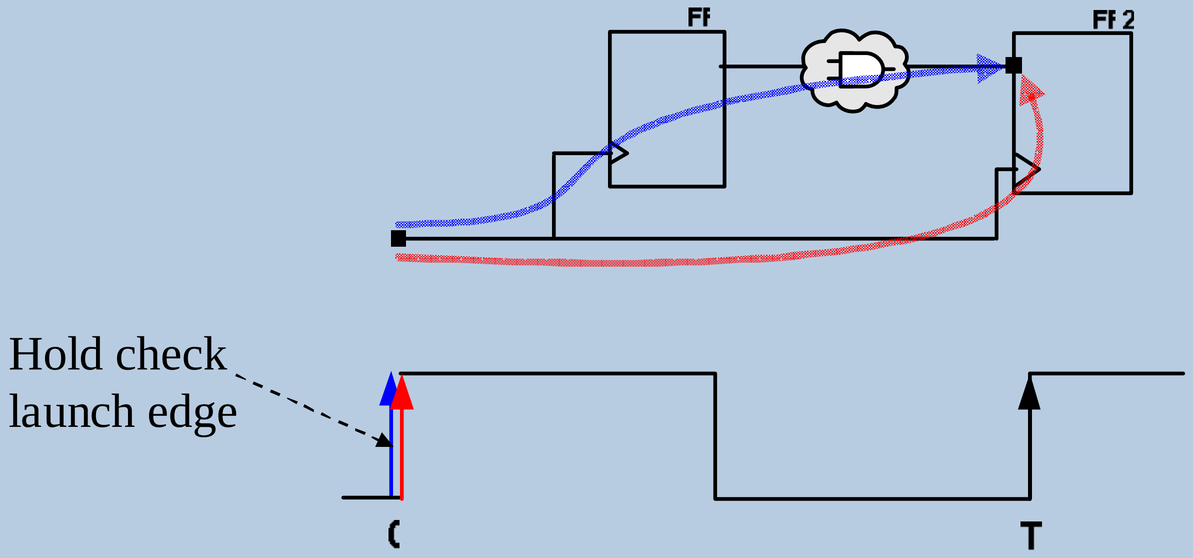
Maximum Delay - Expanded Path View: Q[0]:CLK -> Q[11]:D

| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **From: Q[0]:CLK** | | | | | | | | |
| 2 | **To: Q[11]:D** | | | | | | | | |
| 3 | data required time | | | | | | 7.111 | | |
| 4 | data arrival time | | | | - | | 6.543 | | |
| 5 | slack | | | | | | 0.568 | | |
| 6 | <br>**Data arrival time calculation** | | | | | | | | |
| 7 | CLK | | | | | 0.000 | 0.000 | | |
| 8 | Q[0]:CLK | clock network | | | + | 1.799 | 1.799 | | r |
| 9 | Q[0]:Q | cell | | ADLIB:DFN1C1 | + | 0.535 | 2.334 | 4 | f |
| 10 | COUNTING_count_3_G_1_5:A | net | Q_c[0] | | + | 0.655 | 2.989 | | f |
| 11 | COUNTING_count_3_G_1_5:Y | cell | | ADLIB:NOR2B | + | 0.380 | 3.369 | 6 | f |
| 12 | COUNTING_count_3_G_1_3:B | net | COUNTING_count_3_DWACT_ADD_CI_0_tmp[0] | | + | 0.288 | 3.657 | | f |
| 13 | COUNTING_count_3_G_1_3:Y | cell | | ADLIB:NOR3B | + | 0.458 | 4.115 | 3 | f |
| 14 | COUNTING_count_3_I_82:A | net | COUNTING_count_3_DWACT_ADD_CI_0_g_array_3[0] | | + | 0.364 | 4.479 | | f |
| 15 | COUNTING_count_3_I_82:Y | cell | | ADLIB:NOR2B | + | 0.380 | 4.859 | 2 | f |
| 16 | COUNTING_count_3_I_61:A | net | COUNTING_count_3_DWACT_ADD_CI_0_g_array_11_1[0] | | + | 0.760 | 5.619 | | f |
| 17 | COUNTING_count_3_I_61:Y | cell | | ADLIB:AX1C | + | 0.719 | 6.338 | 1 | f |
| 18 | Q[11]:D | net | COUNTING_count_3[11] | | + | 0.205 | 6.543 | | f |
| 19 | data arrival time | | | | | | 6.543 | | |
| 20 | <br>**Data required time calculation** | | | | | | | | |
| 21 | CLK | Clock Constraint | | | | 5.714 | 5.714 | | |
| 22 | Q[11]:CLK | clock network | | | + | 1.799 | 7.513 | | r |
| 23 | Q[11]:D | Library setup | | ADLIB:DFN1C1 | - | 0.402 | 7.111 | | |
| 24 | data required time | | | | | | 7.111 | | |

Right click in window to zoom

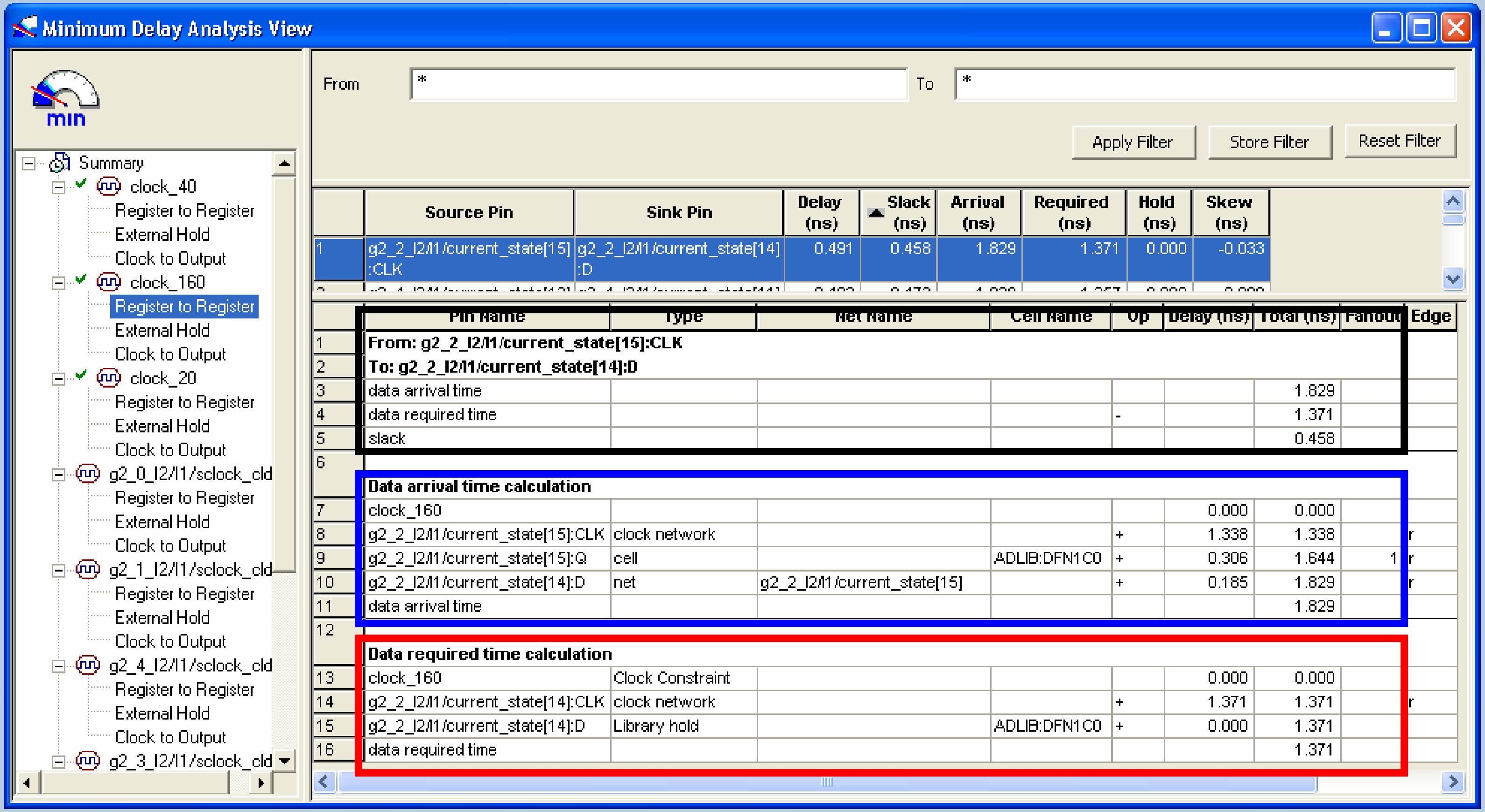
# SmartTime
## *Hold Check*

- Hold Check is Displayed in the Minimum Delay Analysis View



- Hold Check Calculation
  - Arrival time = Launch edge (0) + min Clock to FF1 + min Data path
  - Required time = Launch edge (0) + max Clock to FF2 + Hold of FF2
  - Slack = Arrival – Required = Violation if < 0

# SmartTime
## *Hold Check (cont.)*



- Summary
  - ✓ clock_40
    - Register to Register
    - External Hold
    - Clock to Output
  - ✓ clock_160
    - Register to Register
    - External Hold
    - Clock to Output
  - ✓ clock_20
    - Register to Register
    - External Hold
    - Clock to Output
  - g2_0_I2/I1/sclock_cld
    - Register to Register
    - External Hold
    - Clock to Output
  - g2_1_I2/I1/sclock_cld
    - Register to Register
    - External Hold
    - Clock to Output
  - g2_4_I2/I1/sclock_cld
    - Register to Register
    - External Hold
    - Clock to Output
  - g2_3_I2/I1/sclock_cld

From: *
To: *

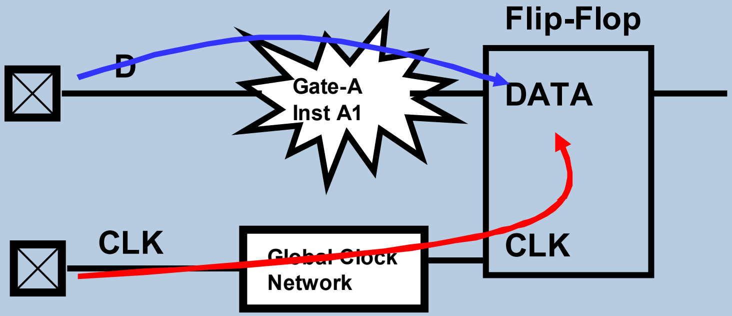
| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Hold (ns) | Skew (ns) |
|---|---|---|---|---|---|---|---|---|
| 1 | g2_2_I2/I1/current_state[15]:CLK | g2_2_I2/I1/current_state[14]:D | 0.491 | 0.458 | 1.829 | 1.371 | 0.000 | -0.033 |

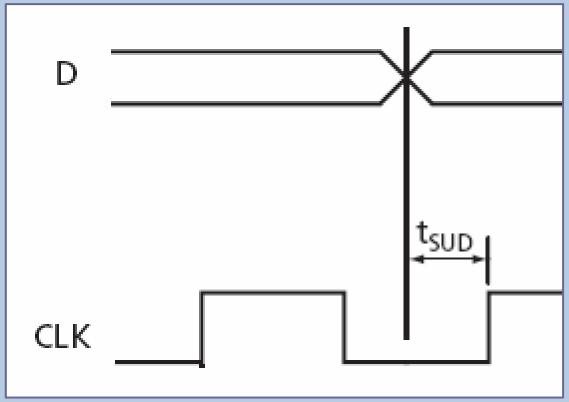
| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | From: g2_2_I2/I1/current_state[15]:CLK | | | | | | | | |
| 2 | To: g2_2_I2/I1/current_state[14]:D | | | | | | | | |
| 3 | data arrival time | | | | | | 1.829 | | |
| 4 | data required time | | | | - | | 1.371 | | |
| 5 | slack | | | | | | 0.458 | | |
| 6 | | | | | | | | | |
| | Data arrival time calculation | | | | | | | | |
| 7 | clock_160 | | | | | 0.000 | 0.000 | | |
| 8 | g2_2_I2/I1/current_state[15]:CLK | clock network | | | + | 1.338 | 1.338 | | r |
| 9 | g2_2_I2/I1/current_state[15]:Q | cell | | ADLIB:DFN1C0 | + | 0.306 | 1.644 | 1 | r |
| 10 | g2_2_I2/I1/current_state[14]:D | net | g2_2_I2/I1/current_state[15] | | + | 0.185 | 1.829 | | r |
| 11 | data arrival time | | | | | | 1.829 | | |
| 12 | | | | | | | | | |
| | Data required time calculation | | | | | | | | |
| 13 | clock_160 | Clock Constraint | | | | 0.000 | 0.000 | | |
| 14 | g2_2_I2/I1/current_state[14]:CLK | clock network | | | + | 1.371 | 1.371 | | r |
| 15 | g2_2_I2/I1/current_state[14]:D | Library hold | | ADLIB:DFN1C0 | + | 0.000 | 1.371 | | |
| 16 | data required time | | | | | | 1.371 | | |

- Hold Check
  - Arrival time = Launch edge (0) + min Clock to FF1 + min Data path
  - Required time = Capture edge (0) + max Clock to FF2 + Hold of FF2
  - Slack = Arrival – Required = Violation if < 0

# SmartTime
## *External Setup Check*

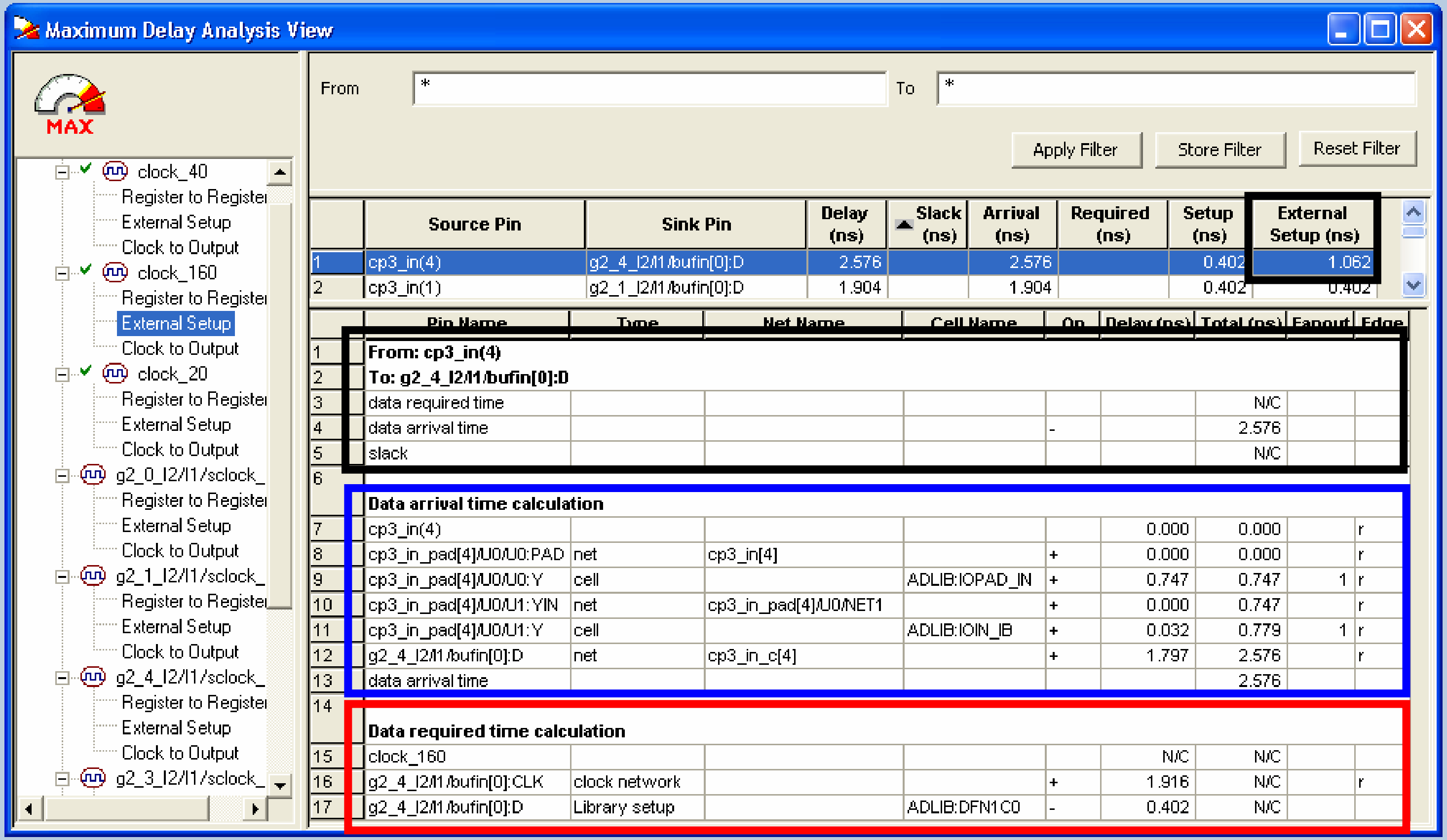
- External Setup Defines the Timing Requirements at the Input Pins
- External Setup Check is Displayed in the Maximum Delay Analysis View for Each Clock Domain





- External Setup Check Calculation
  - **Arrival time = max Input Pad to FF1**
  - **Required time = min Clock to FF1 - Setup of FF1**
  - **External Hold = Arrival - Required**

# SmartTime
## *External Setup Check*



From *

To *

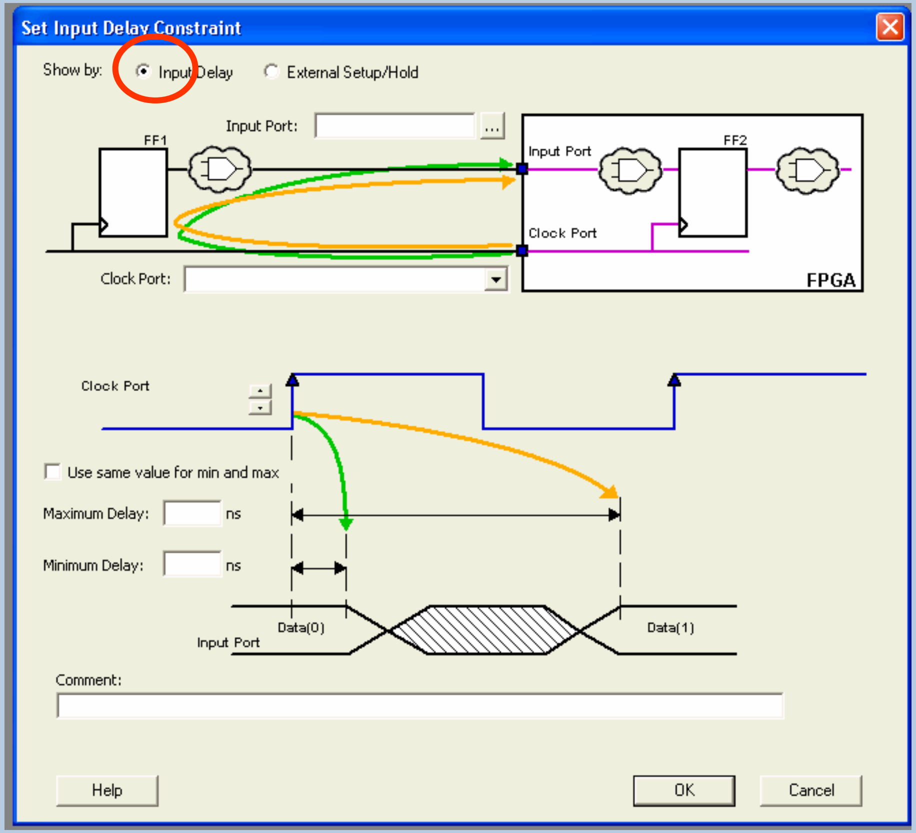
| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) | External Setup (ns) |
|---|---|---|---|---|---|---|---|---|
| 1 | cp3_in(4) | g2_4_I2/I1/bufin[0]:D | 2.576 | | 2.576 | | 0.402 | 1.062 |
| 2 | cp3_in(1) | g2_1_I2/I1/bufin[0]:D | 1.904 | | 1.904 | | 0.402 | 0.402 |

| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **From: cp3_in(4)** | | | | | | | | |
| 2 | **To: g2_4_I2/I1/bufin[0]:D** | | | | | | | | |
| 3 | data required time | | | | | | N/C | | |
| 4 | data arrival time | | | | - | | 2.576 | | |
| 5 | slack | | | | | | N/C | | |
| 6 | | | | | | | | | |
| | **Data arrival time calculation** | | | | | | | | |
| 7 | cp3_in(4) | | | | | 0.000 | 0.000 | | r |
| 8 | cp3_in_pad[4]/U0/U0:PAD | net | cp3_in[4] | | + | 0.000 | 0.000 | | r |
| 9 | cp3_in_pad[4]/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 0.747 | 0.747 | 1 | r |
| 10 | cp3_in_pad[4]/U0/U1:YIN | net | cp3_in_pad[4]/U0/NET1 | | + | 0.000 | 0.747 | | r |
| 11 | cp3_in_pad[4]/U0/U1:Y | cell | | ADLIB:IOIN_IB | + | 0.032 | 0.779 | 1 | r |
| 12 | g2_4_I2/I1/bufin[0]:D | net | cp3_in_c[4] | | + | 1.797 | 2.576 | | r |
| 13 | data arrival time | | | | | | 2.576 | | |
| 14 | | | | | | | | | |
| | **Data required time calculation** | | | | | | | | |
| 15 | clock_160 | | | | | N/C | N/C | | |
| 16 | g2_4_I2/I1/bufin[0]:CLK | clock network | | | + | 1.916 | N/C | | r |
| 17 | g2_4_I2/I1/bufin[0]:D | Library setup | | ADLIB:DFN1C0 | - | 0.402 | N/C | | |

- External Setup Check
  - **Arrival time = max Input Pad to FF1**
  - **Required time = min Clock to FF1 - Setup of FF1**
  - **External Setup = Arrival - Required**

# External Setup Check w/ Input Delay Constraint

- Enter Constraint as Input Delay



Set Input Delay Constraint

Show by: [✓ ● Input Delay] ○ External Setup/Hold

Input Port:

Clock Port:

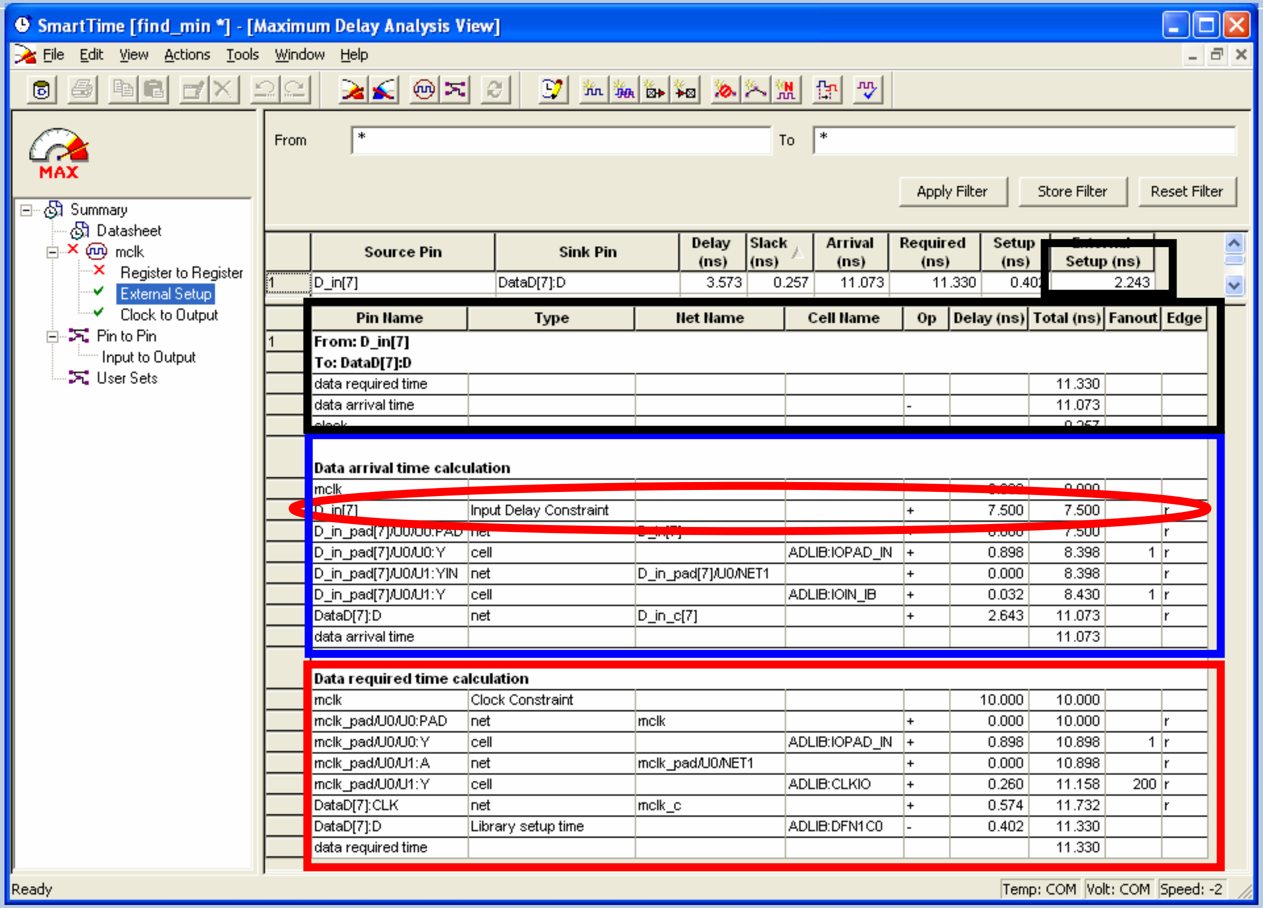
□ Use same value for min and max

Maximum Delay: ns

Minimum Delay: ns

Comment:

# External Setup Check w/ Input Delay Constraint



From: *

To: *

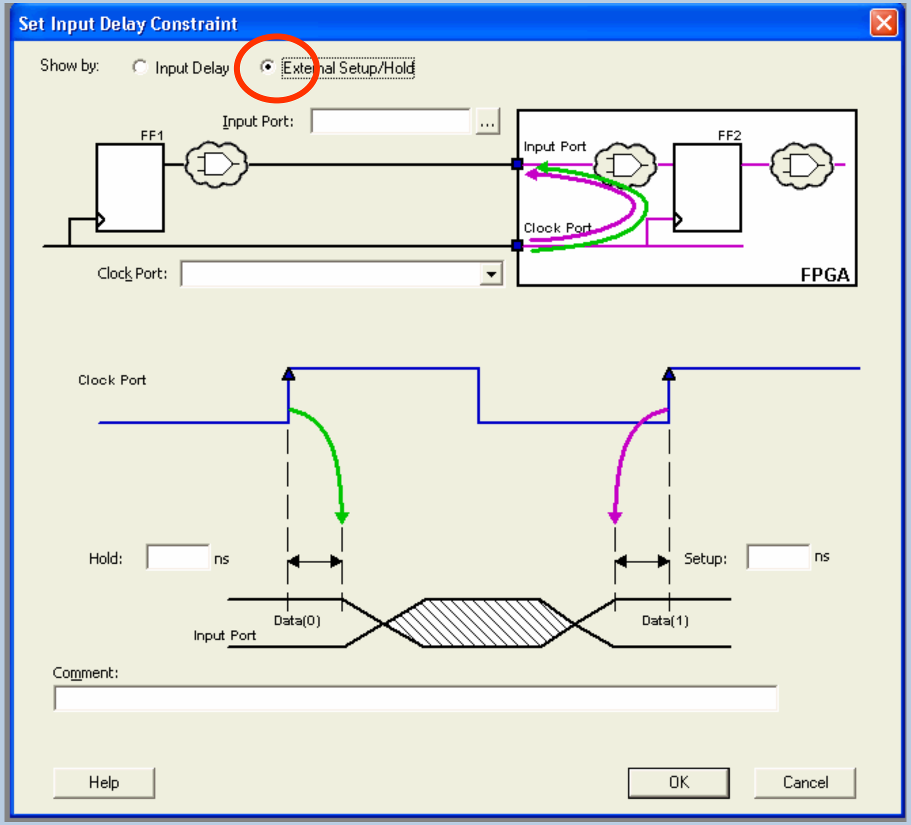
| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) | External Setup (ns) |
|---|---|---|---|---|---|---|---|---|
| 1 | D_in[7] | DataD[7]:D | 3.573 | 0.257 | 11.073 | 11.330 | 0.402 | 2.243 |

| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **From: D_in[7]** | | | | | | | | |
| | **To: DataD[7]:D** | | | | | | | | |
| | data required time | | | | | | 11.330 | | |
| | data arrival time | | | | - | | 11.073 | | |
| | slack | | | | | | 0.257 | | |
| | | | | | | | | | |
| | **Data arrival time calculation** | | | | | | | | |
| | mclk | | | | | 0.000 | 0.000 | | |
| | D_in[7] | Input Delay Constraint | | | + | 7.500 | 7.500 | | r |
| | D_in_pad[7]/U0/U0:PAD | net | D_in[7] | | + | 0.000 | 7.500 | | r |
| | D_in_pad[7]/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 0.898 | 8.398 | 1 | r |
| | D_in_pad[7]/U0/U1:YIN | net | D_in_pad[7]/U0/NET1 | | + | 0.000 | 8.398 | | r |
| | D_in_pad[7]/U0/U1:Y | cell | | ADLIB:IOIN_IB | + | 0.032 | 8.430 | 1 | r |
| | DataD[7]:D | net | D_in_c[7] | | + | 2.643 | 11.073 | | r |
| | data arrival time | | | | | | 11.073 | | |
| | | | | | | | | | |
| | **Data required time calculation** | | | | | | | | |
| | mclk | Clock Constraint | | | | 10.000 | 10.000 | | |
| | mclk_pad/U0/U0:PAD | net | mclk | | + | 0.000 | 10.000 | | r |
| | mclk_pad/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 0.898 | 10.898 | 1 | r |
| | mclk_pad/U0/U1:A | net | mclk_pad/U0/NET1 | | + | 0.000 | 10.898 | | r |
| | mclk_pad/U0/U1:Y | cell | | ADLIB:CLKIO | + | 0.260 | 11.158 | 200 | r |
| | DataD[7]:CLK | net | mclk_c | | + | 0.574 | 11.732 | | r |
| | DataD[7]:D | Library setup time | | ADLIB:DFN1C0 | - | 0.402 | 11.330 | | |
| | data required time | | | | | | 11.330 | | |

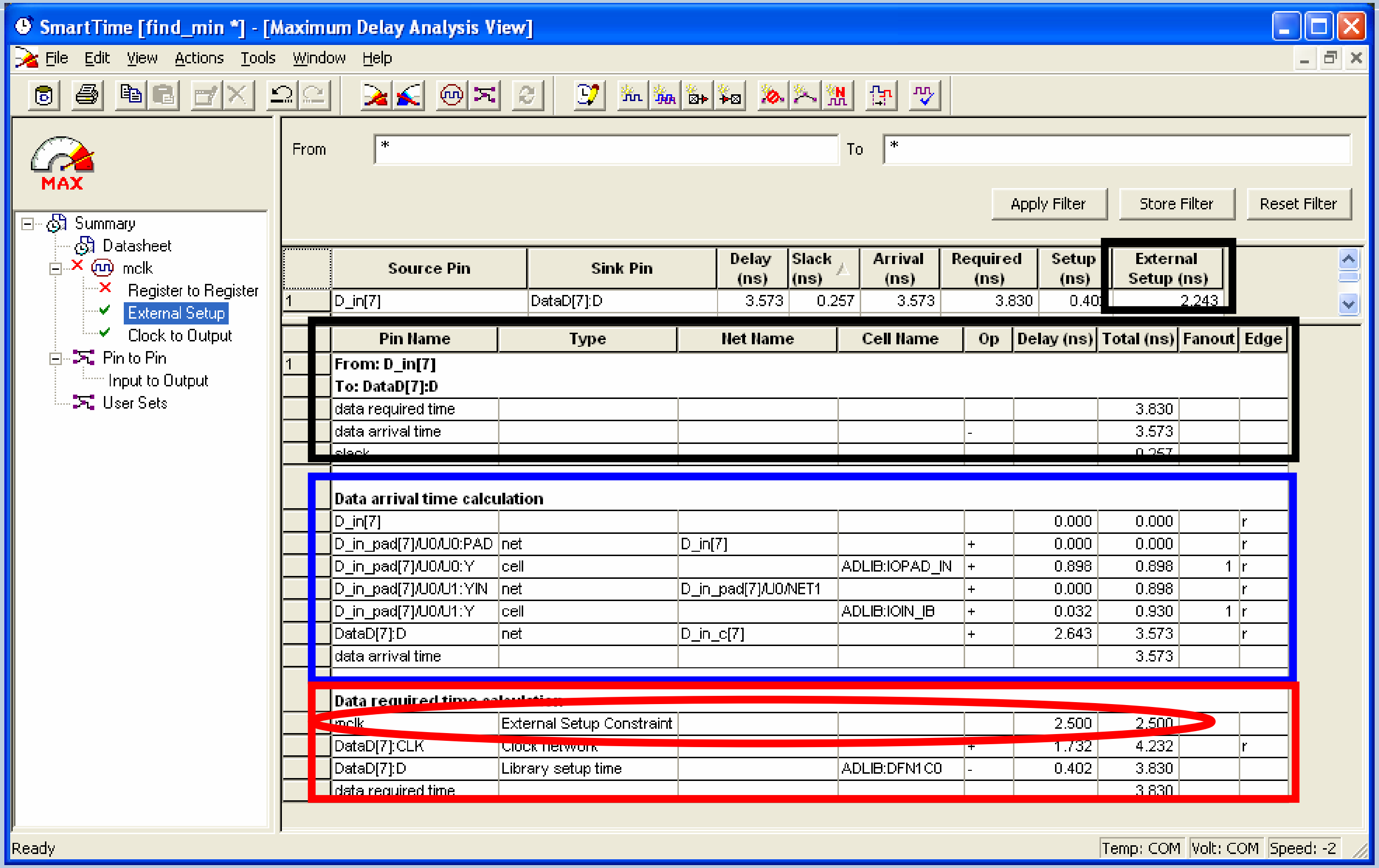
- External Setup Check Calculation
  - **Arrival time = Launch edge (0) + max input delay + max Data path**
  - **Required time = Capture edge (T) + min Clock to FF1 – Setup of FF1**
  - **Slack = Required – Arrival = Violation if < 0**

# External Setup Check w/ External Setup Constraint

- Enter Constraint as External Setup/Hold



# External Setup Check w/ External Setup Constraint



| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) | External Setup (ns) |
|---|---|---|---|---|---|---|---|---|
| 1 | D_in[7] | DataD[7]:D | 3.573 | 0.257 | 3.573 | 3.830 | 0.40 | 2.243 |

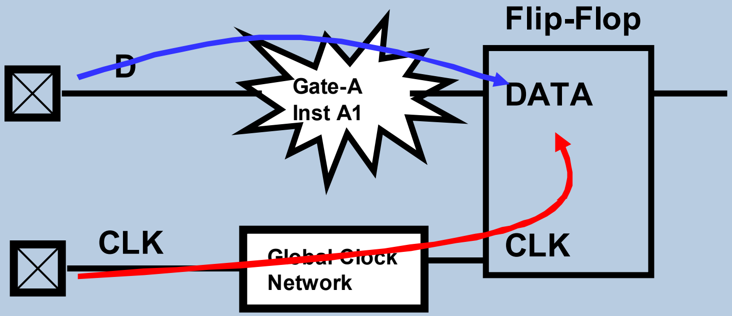
| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **From: D_in[7]** | | | | | | | | |
| | **To: DataD[7]:D** | | | | | | | | |
| | data required time | | | | | | 3.830 | | |
| | data arrival time | | | | - | | 3.573 | | |
| | slack | | | | | | 0.257 | | |
| | | | | | | | | | |
| | **Data arrival time calculation** | | | | | | | | |
| | D_in[7] | | | | | 0.000 | 0.000 | | r |
| | D_in_pad[7]/U0/U0:PAD | net | D_in[7] | | + | 0.000 | 0.000 | | r |
| | D_in_pad[7]/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 0.898 | 0.898 | 1 | r |
| | D_in_pad[7]/U0/U1:YIN | net | D_in_pad[7]/U0/NET1 | | + | 0.000 | 0.898 | | r |
| | D_in_pad[7]/U0/U1:Y | cell | | ADLIB:IOIN_IB | + | 0.032 | 0.930 | 1 | r |
| | DataD[7]:D | net | D_in_c[7] | | + | 2.643 | 3.573 | | r |
| | data arrival time | | | | | | 3.573 | | |
| | | | | | | | | | |
| | **Data required time calculation** | | | | | | | | |
| | mclk | External Setup Constraint | | | | 2.500 | 2.500 | | |
| | DataD[7]:CLK | Clock network | | | + | 1.732 | 4.232 | | r |
| | DataD[7]:D | Library setup time | | ADLIB:DFN1C0 | - | 0.402 | 3.830 | | |
| | data required time | | | | | | 3.830 | | |

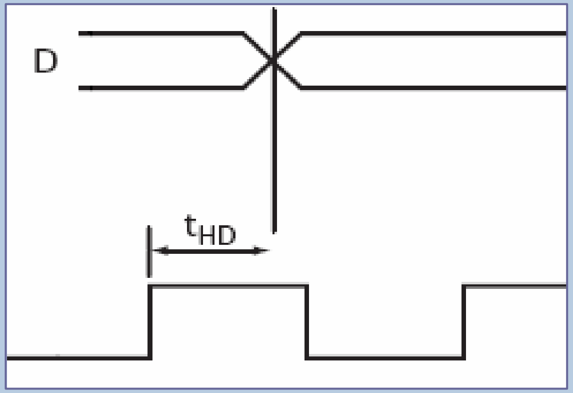
- External Setup Check Calculation
  - **Arrival time = Launch edge (0) + max input delay + max Data path**
  - **Required time = Capture edge (T) + min Clock to FF1 – Setup of FF1**
  - **Slack = Required – Arrival = Violation if < 0**

ONE CHIP is all you need

# SmartTime
## *External Hold Check*

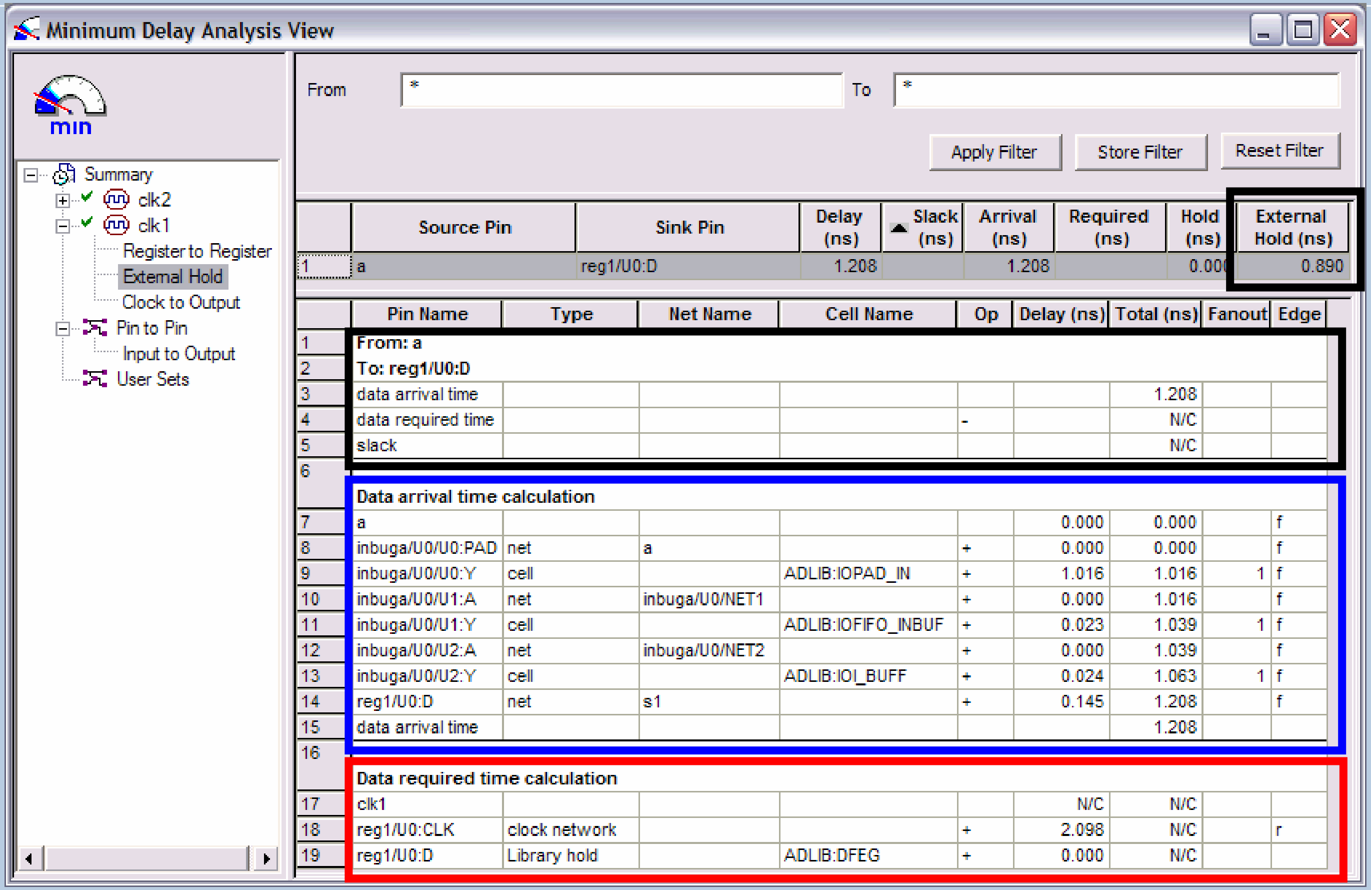
- External Hold Defines the Timing Requirements at the Input Pins
- External Hold Check is Displayed in the Minimum Delay Analysis View for Each Clock Domain





- External Hold Check Calculation
  - Arrival time = min Input Pad to FF1
  - Required time = max Clock to FF1 - Hold of FF1
  - External Hold = Arrival - Required

# SmartTime
## *External Hold Check*



Minimum Delay Analysis View

- Summary
  - clk2
  - clk1
    - Register to Register
    - External Hold
    - Clock to Output
  - Pin to Pin
    - Input to Output
  - User Sets

From: *    To: *

Apply Filter | Store Filter | Reset Filter

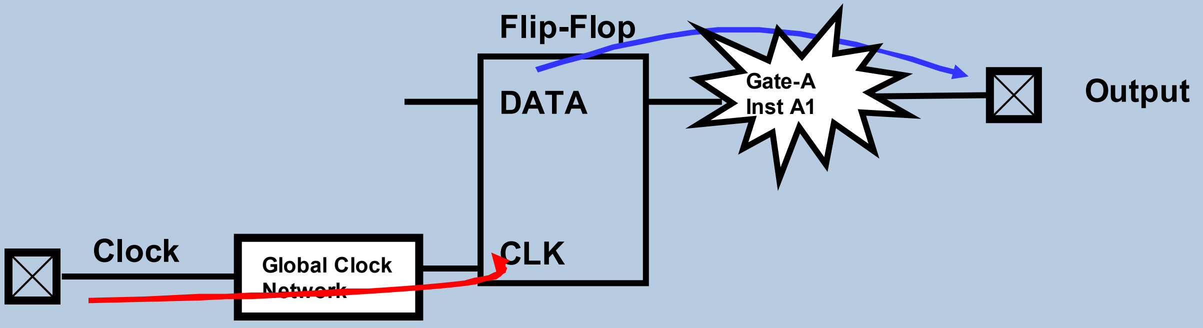
| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Hold (ns) | External Hold (ns) |
|---|---|---|---|---|---|---|---|---|
| 1 | a | reg1/U0:D | 1.208 | | 1.208 | | 0.00 | 0.890 |

| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **From: a** | | | | | | | | |
| 2 | **To: reg1/U0:D** | | | | | | | | |
| 3 | data arrival time | | | | | | 1.208 | | |
| 4 | data required time | | | | - | | N/C | | |
| 5 | slack | | | | | | N/C | | |
| 6 | | | | | | | | | |
| | **Data arrival time calculation** | | | | | | | | |
| 7 | a | | | | | 0.000 | 0.000 | | f |
| 8 | inbuga/U0/U0:PAD | net | a | | + | 0.000 | 0.000 | | f |
| 9 | inbuga/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 1.016 | 1.016 | 1 | f |
| 10 | inbuga/U0/U1:A | net | inbuga/U0/NET1 | | + | 0.000 | 1.016 | | f |
| 11 | inbuga/U0/U1:Y | cell | | ADLIB:IOFIFO_INBUF | + | 0.023 | 1.039 | 1 | f |
| 12 | inbuga/U0/U2:A | net | inbuga/U0/NET2 | | + | 0.000 | 1.039 | | f |
| 13 | inbuga/U0/U2:Y | cell | | ADLIB:IOI_BUFF | + | 0.024 | 1.063 | 1 | f |
| 14 | reg1/U0:D | net | s1 | | + | 0.145 | 1.208 | | f |
| 15 | data arrival time | | | | | | 1.208 | | |
| 16 | | | | | | | | | |
| | **Data required time calculation** | | | | | | | | |
| 17 | clk1 | | | | | N/C | N/C | | |
| 18 | reg1/U0:CLK | clock network | | | + | 2.098 | N/C | | r |
| 19 | reg1/U0:D | Library hold | | ADLIB:DFEG | + | 0.000 | N/C | | |

- External Hold Check – Minimum Delay Analysis View
  - **Arrival time = min Input Pad to FF1**
  - **Required time = max Clock to FF1 + Hold of FF1**
  - **Slack = Arrival – Required = Violation if < 0**

# SmartTime
## *Clock to Output Check*

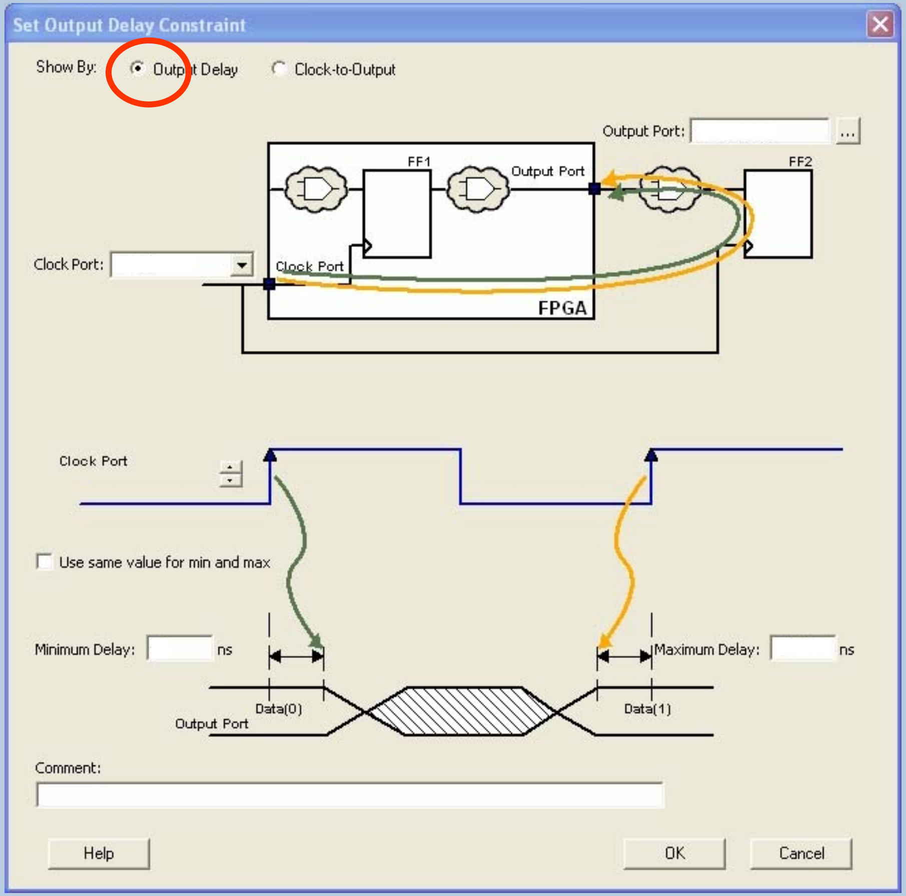
- Clock to Output is Displayed in the Maximum Delay Analysis View for Each Clock Domain



- Clock to Output Calculation
  - **Arrival time = Launch edge (0) + max Data path**
  - **Required time = Capture edge (T)**
  - **Slack = Required – Arrival = Violation if < 0**

# Clock to Output Check w/ Output Delay Constraint

- Enter Constraint as Output Delay



Set Output Delay Constraint

Show By: ● Output Delay ○ Clock-to-Output

Output Port:

Clock Port:

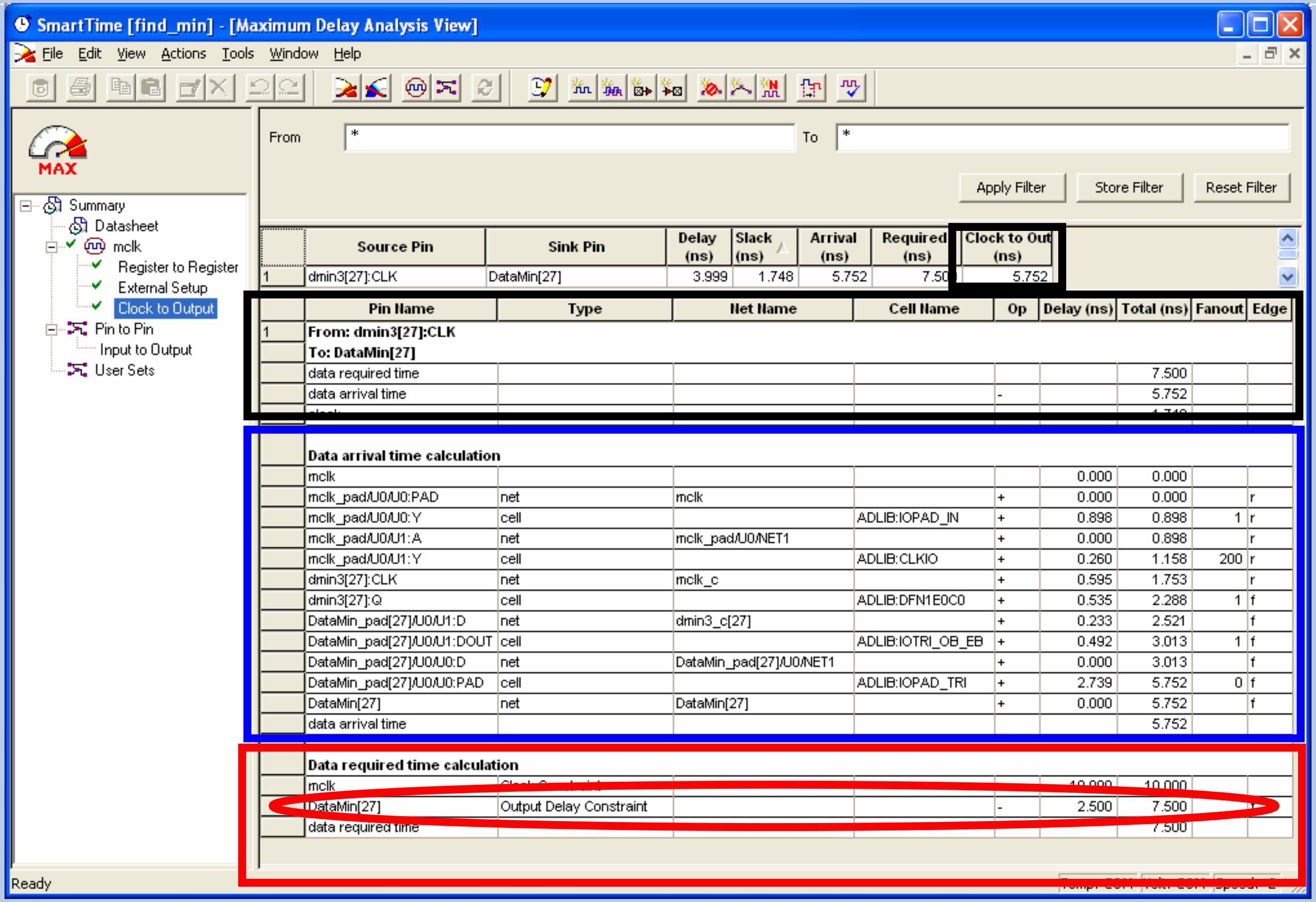
□ Use same value for min and max

Minimum Delay: ns

Maximum Delay: ns

Comment:

# Clock to Output Check w/ Output Delay Constraint



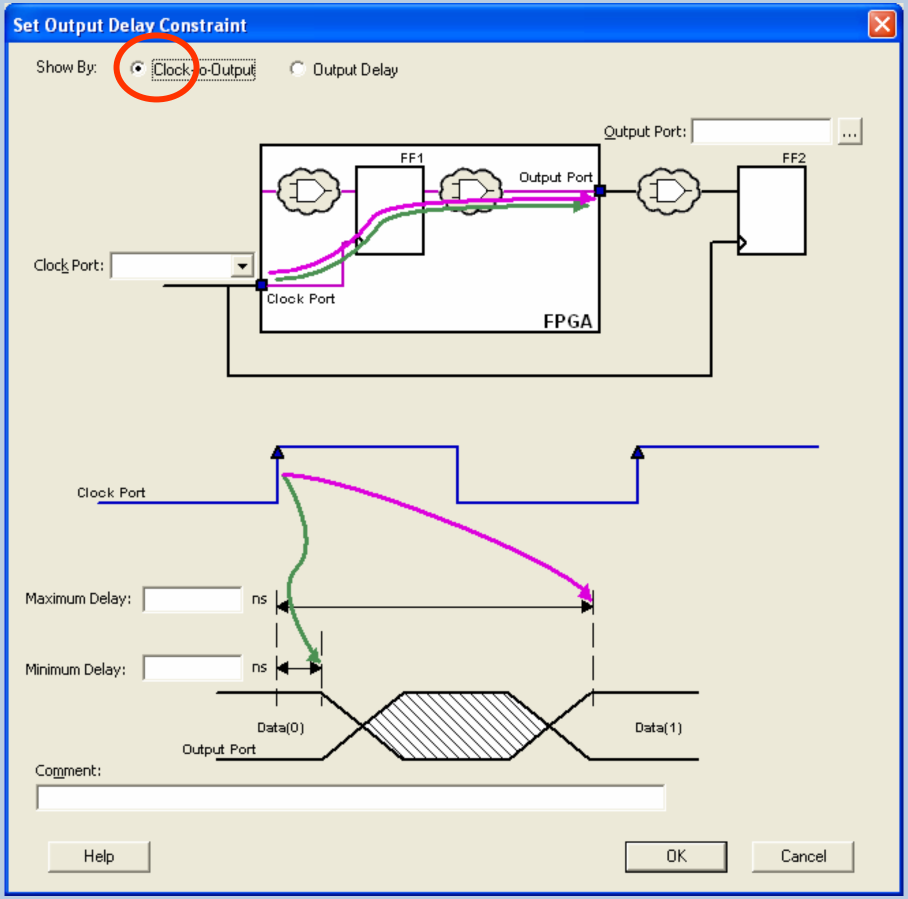
| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Clock to Out (ns) |
|---|---|---|---|---|---|---|---|
| 1 | dmin3[27]:CLK | DataMin[27] | 3.999 | 1.748 | 5.752 | 7.50 | 5.752 |

| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **From: dmin3[27]:CLK** | | | | | | | | |
| | **To: DataMin[27]** | | | | | | | | |
| | data required time | | | | | | 7.500 | | |
| | data arrival time | | | | - | | 5.752 | | |
| | slack | | | | | | 1.748 | | |
| | | | | | | | | | |
| | **Data arrival time calculation** | | | | | | | | |
| | mclk | | | | | 0.000 | 0.000 | | |
| | mclk_pad/U0/U0:PAD | net | mclk | | + | 0.000 | 0.000 | | r |
| | mclk_pad/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 0.898 | 0.898 | 1 | r |
| | mclk_pad/U0/U1:A | net | mclk_pad/U0/NET1 | | + | 0.000 | 0.898 | | r |
| | mclk_pad/U0/U1:Y | cell | | ADLIB:CLKIO | + | 0.260 | 1.158 | 200 | r |
| | dmin3[27]:CLK | net | mclk_c | | + | 0.595 | 1.753 | | r |
| | dmin3[27]:Q | cell | | ADLIB:DFN1E0C0 | + | 0.535 | 2.288 | 1 | f |
| | DataMin_pad[27]/U0/U1:D | net | dmin3_c[27] | | + | 0.233 | 2.521 | | f |
| | DataMin_pad[27]/U0/U1:DOUT | cell | | ADLIB:IOTRI_OB_EB | + | 0.492 | 3.013 | 1 | f |
| | DataMin_pad[27]/U0/U0:D | net | DataMin_pad[27]/U0/NET1 | | + | 0.000 | 3.013 | | f |
| | DataMin_pad[27]/U0/U0:PAD | cell | | ADLIB:IOPAD_TRI | + | 2.739 | 5.752 | 0 | f |
| | DataMin[27] | net | DataMin[27] | | + | 0.000 | 5.752 | | f |
| | data arrival time | | | | | | 5.752 | | |
| | | | | | | | | | |
| | **Data required time calculation** | | | | | | | | |
| | mclk | Clock Constraint | | | | 10.000 | 10.000 | | |
| | DataMin[27] | Output Delay Constraint | | | - | 2.500 | 7.500 | | f |
| | data required time | | | | | | 7.500 | | |

- Setup Check
  - Arrival time = Launch edge (0) + max Data path
  - Required time = Capture edge (T) – Output Delay
  - Slack = Required – Arrival = Violation if < 0

# Clock to Output Check w/ Clock to Output Constraint

- Enter Constraint as Clock-to-Out



Set Output Delay Constraint

Show By: ● Clock-to-Output ○ Output Delay

Output Port:

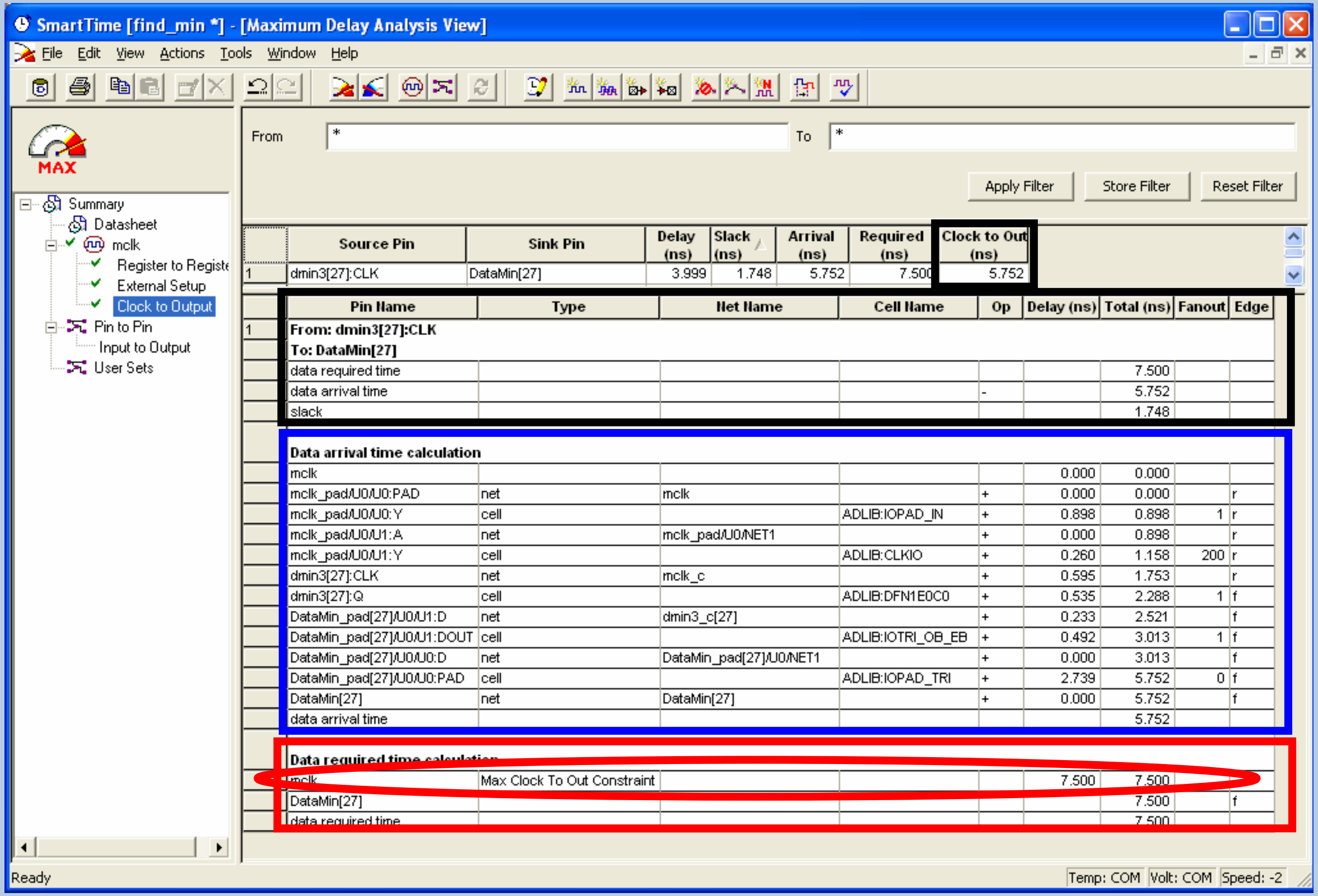
Clock Port:

Maximum Delay: ns

Minimum Delay: ns

Comment:

# Clock to Output Check w/ Output Delay Constraint



| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Clock to Out (ns) |
|---|---|---|---|---|---|---|---|
| 1 | dmin3[27]:CLK | DataMin[27] | 3.999 | 1.748 | 5.752 | 7.500 | 5.752 |

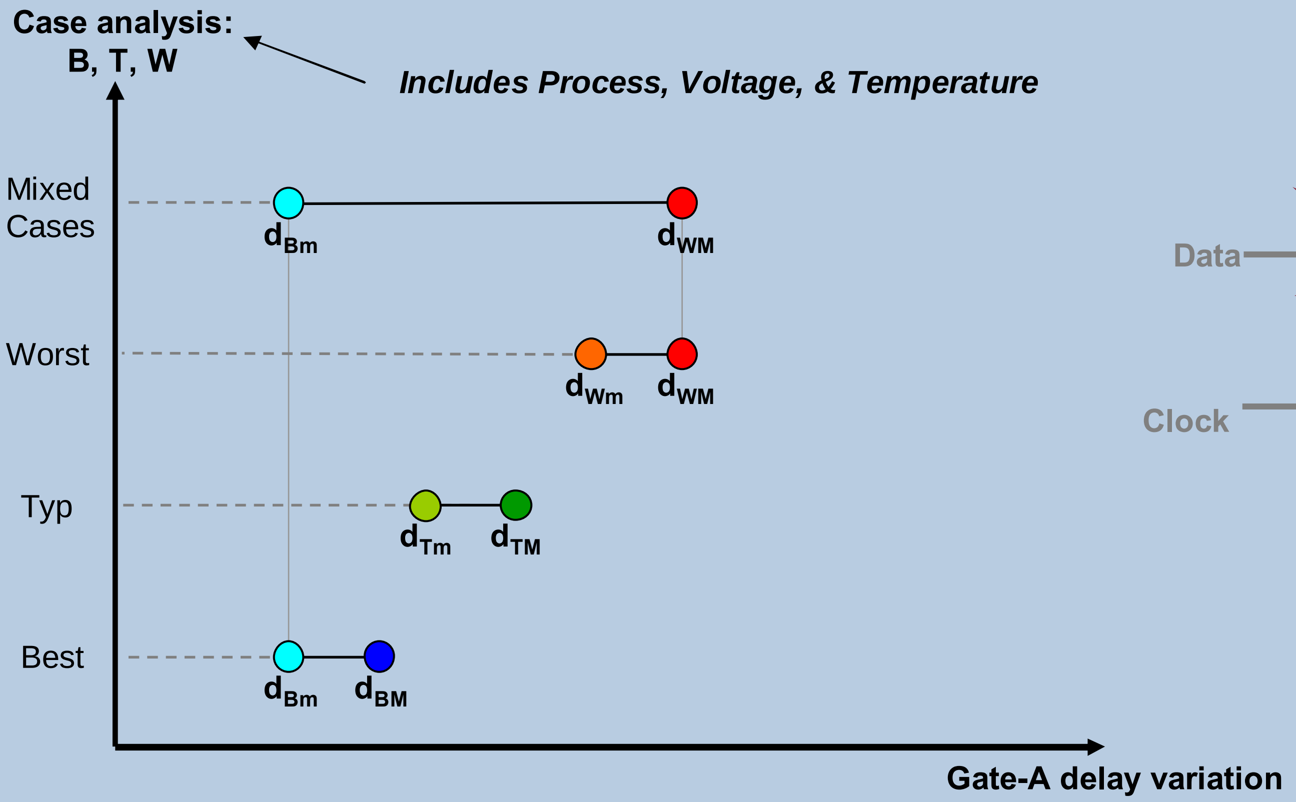
| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | From: dmin3[27]:CLK | | | | | | | | |
| | To: DataMin[27] | | | | | | | | |
| | data required time | | | | | | 7.500 | | |
| | data arrival time | | | | - | | 5.752 | | |
| | slack | | | | | | 1.748 | | |
| | Data arrival time calculation | | | | | | | | |
| | mclk | | | | | 0.000 | 0.000 | | |
| | mclk_pad/U0/U0:PAD | net | mclk | | + | 0.000 | 0.000 | | r |
| | mclk_pad/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 0.898 | 0.898 | 1 | r |
| | mclk_pad/U0/U1:A | net | mclk_pad/U0/NET1 | | + | 0.000 | 0.898 | | r |
| | mclk_pad/U0/U1:Y | cell | | ADLIB:CLKIO | + | 0.260 | 1.158 | 200 | r |
| | dmin3[27]:CLK | net | mclk_c | | + | 0.595 | 1.753 | | r |
| | dmin3[27]:Q | cell | | ADLIB:DFN1E0C0 | + | 0.535 | 2.288 | 1 | f |
| | DataMin_pad[27]/U0/U1:D | net | dmin3_c[27] | | + | 0.233 | 2.521 | | f |
| | DataMin_pad[27]/U0/U1:DOUT | cell | | ADLIB:IOTRI_OB_EB | + | 0.492 | 3.013 | 1 | f |
| | DataMin_pad[27]/U0/U0:D | net | DataMin_pad[27]/U0/NET1 | | + | 0.000 | 3.013 | | f |
| | DataMin_pad[27]/U0/U0:PAD | cell | | ADLIB:IOPAD_TRI | + | 2.739 | 5.752 | 0 | f |
| | DataMin[27] | net | DataMin[27] | | + | 0.000 | 5.752 | | f |
| | data arrival time | | | | | | 5.752 | | |
| | Data required time calculation | | | | | | | | |
| | mclk | Max Clock To Out Constraint | | | | 7.500 | 7.500 | | |
| | DataMin[27] | | | | | | 7.500 | | f |
| | data required time | | | | | | 7.500 | | |

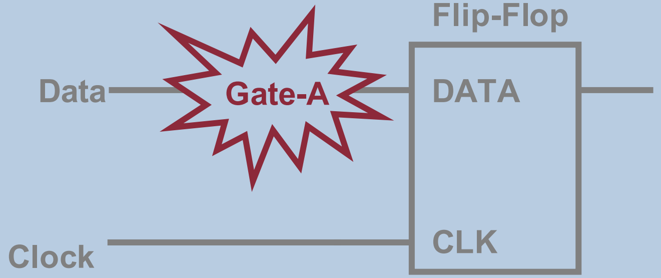
- Setup Check
  - Arrival time = Launch edge (0) + max Data path
  - Required time = Capture edge (T) – Output Delay
  - Slack = Required – Arrival = Violation if < 0

# SmartTime
## *Enhanced Min Delay*

- Provides more accurate min delay evaluation
  - Precise hold-time analysis
  - Silicon characterization-based approach
    - Based on the spread of the characterization curve
  - Endorsed on all paths in a clock domain when the clock is using a global network
  - Viewed in the SmartTime “Minimum Delay View”

# The Min-Delay Problem:
## *Gate delays Case Study*

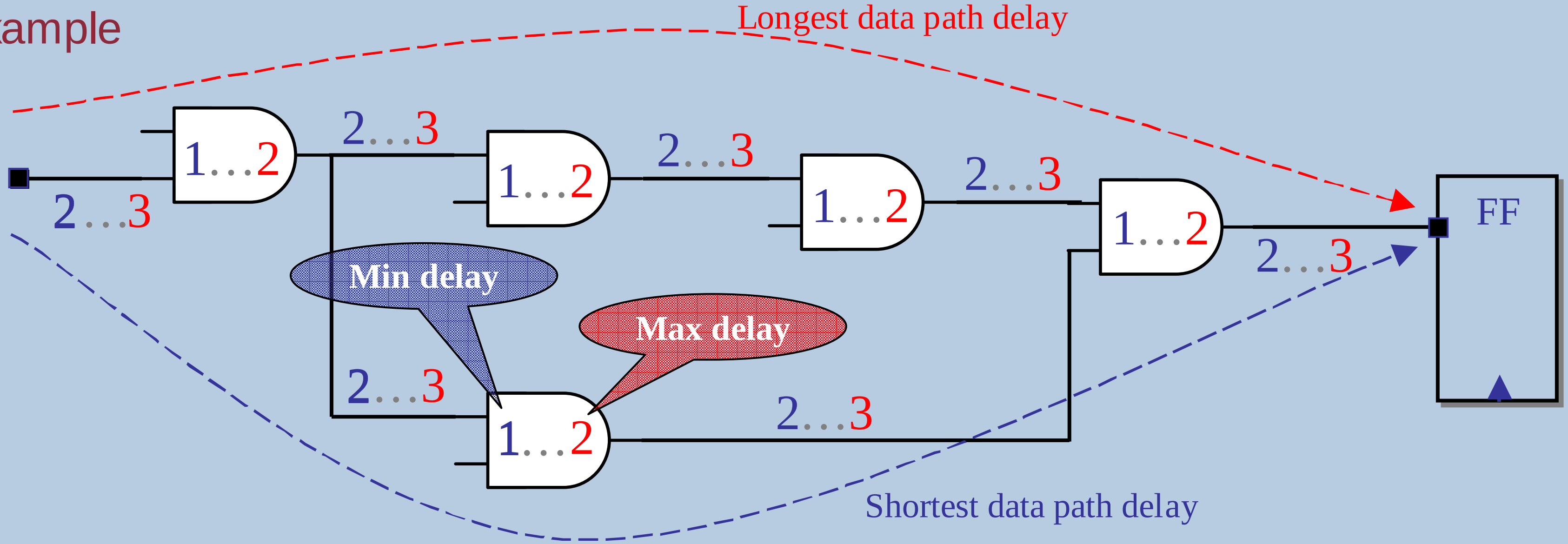




- SETUP Check requires the longest data path:
  - $d_{WM}$, $d_{TM}$, or $d_{BM}$ of Gate-A depending on the case under analysis
- HOLD Check requires the shortest data path:
  - $d_{Wm}$, $d_{Tm}$, or $d_{Bm}$ of Gate-A depending on the case under analysis

# The Min-Delay Problem:
## *An Example*

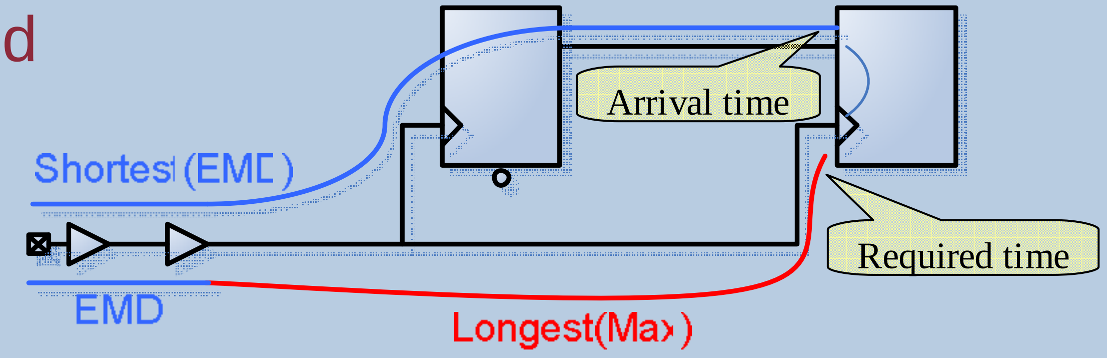
- Example



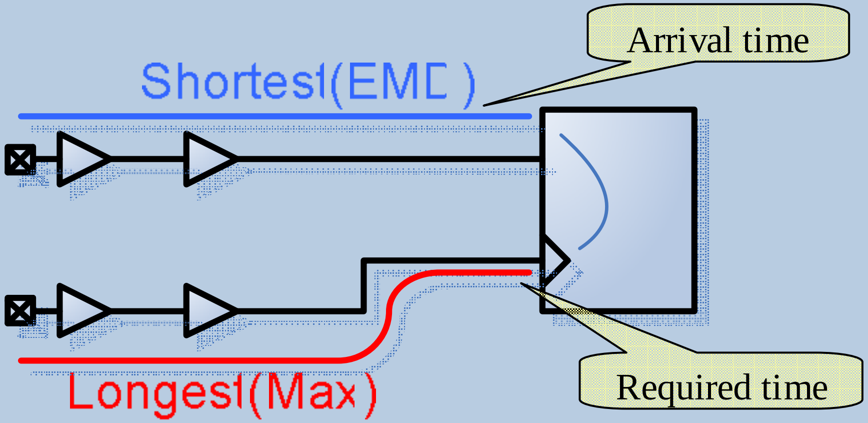
- Theoretically
  - **Setup check uses longest data path delay = Max ( ∑ (Max($\text{Gate}_i$)) ) = 23**
  - **Hold check uses shortest data path delay = Min ( ∑ (Min($\text{Gate}_i$)) ) = 11**
- So far, we had no Min(Gate) delay, so we use Max(Gate) delay
  - **Shortest data path delay = Min ( ∑ (Max($\text{Gate}_i$)) ) = 18**
- Therefore, we were overestimating the minimum data path delay

# Enhanced Min-Delay (EMD)
*Application*

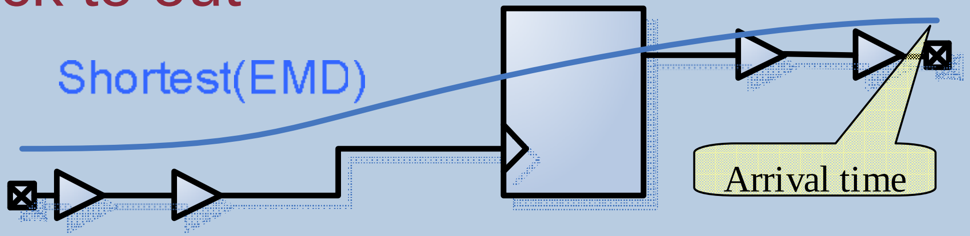
- Register-to-Register hold



- External hold



- Clock to out



# Enhanced Min-Delay (EMD)
## *Support & Limitations*

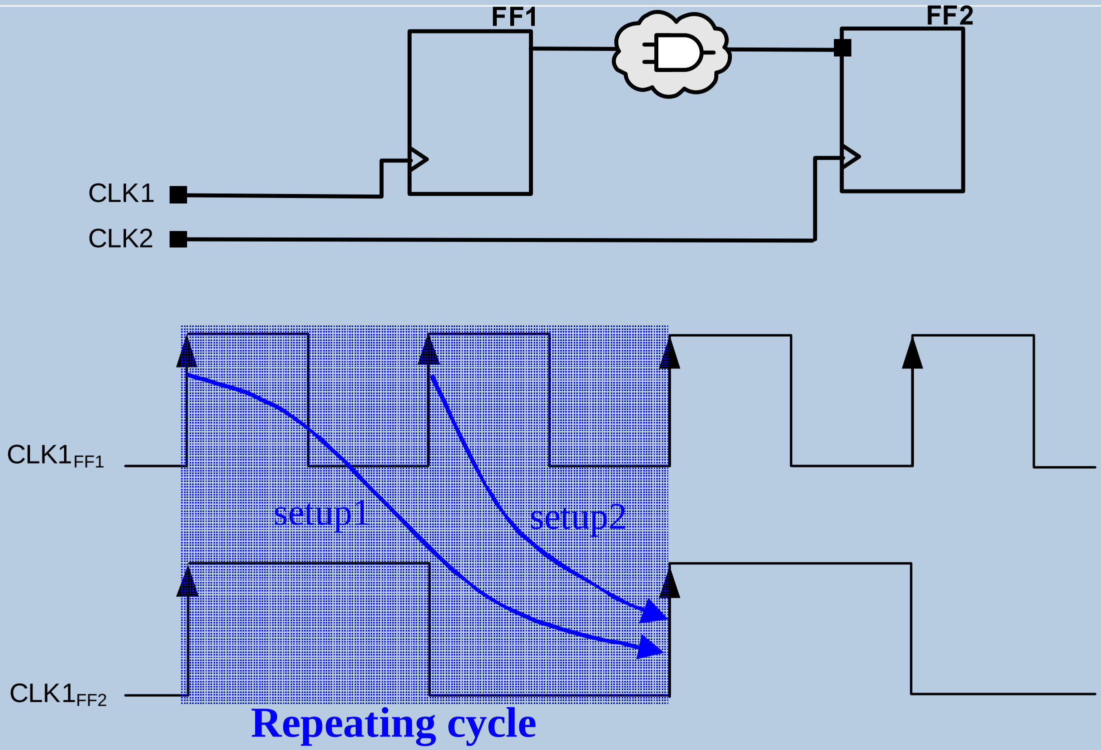
- Supported Products
  - Release 6.3: APA, AX, RTAX-S
  - Future: A3P/E and all future products
- New versus Existing Designs
  - EMD only activated for designs started in 6.3 and beyond
- Resources
  - EMD is endorsed on all paths in a clock domain when the clock is using a global network
- Other Limitations
  - No SDF(min) export
  - No TDPR support in addressing min-delay violations

ONE CHIP is all you need

# Timing Analysis with SmartTime

- Design Summary
- Setup and Hold Checks
- Cross Clock Domain Analysis
- Adding User Sets and Filtering
- Customizing the Analysis View
- Cross-Probing with MVN Tools

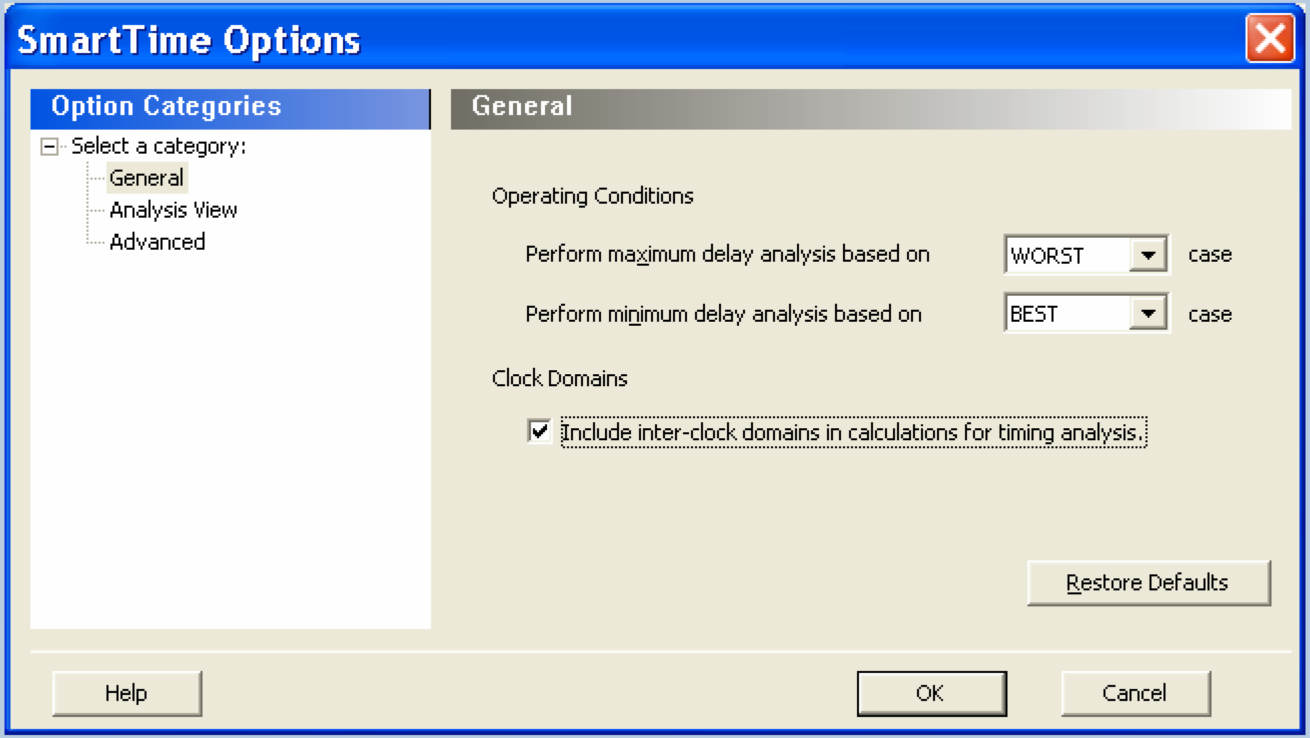
# SmartTime
## *Cross-Clock Domains*



- SmartTime Performs Setup Check Across Clock Domains
  - **SmartTime Looks at the Relationship Between the Active Clock Edges Over a Full Repeating Cycle, Equal to the Least Common Multiple of the Two Clock Periods**
  - **For Each Capture Edge at the Destination Flip-flop, SmartTime Assumes That the Corresponding Launch Edge Is the Nearest Source Clock Edge Occurring Before the Capture Edge**

# SmartTime
## *Activating Cross-Clock Domain Analysis*

- Activate Cross-clock Domain Analysis for a Particular Clock Domain
  - **SmartTime Automatically Detects All Other Clock Domains With Paths Ending at Selected Clock Domain**



SmartTime Options

Option Categories

Select a category:
- General
- Analysis View
- Advanced

General

Operating Conditions

Perform maximum delay analysis based on WORST case

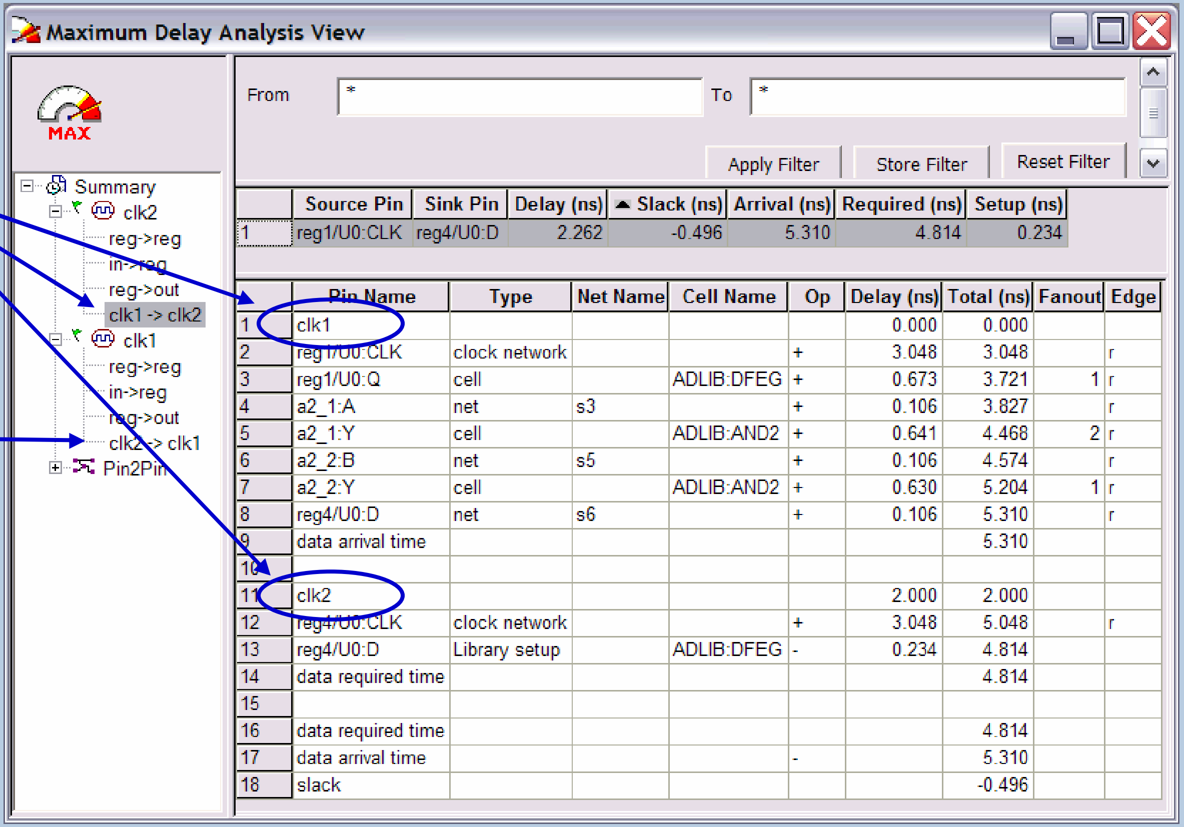
Perform minimum delay analysis based on BEST case

Clock Domains

☑ Include inter-clock domains in calculations for timing analysis.

# SmartTime

## *Cross-Clock Domains in SmartTime*



From * To *

| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) |
|---|---|---|---|---|---|---|---|
| 1 | reg1/U0:CLK | reg4/U0:D | 2.262 | -0.496 | 5.310 | 4.814 | 0.234 |

| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | clk1 | | | | | 0.000 | 0.000 | | |
| 2 | reg1/U0:CLK | clock network | | | + | 3.048 | 3.048 | | r |
| 3 | reg1/U0:Q | cell | | ADLIB:DFEG | + | 0.673 | 3.721 | 1 | r |
| 4 | a2_1:A | net | s3 | | + | 0.106 | 3.827 | | r |
| 5 | a2_1:Y | cell | | ADLIB:AND2 | + | 0.641 | 4.468 | 2 | r |
| 6 | a2_2:B | net | s5 | | + | 0.106 | 4.574 | | r |
| 7 | a2_2:Y | cell | | ADLIB:AND2 | + | 0.630 | 5.204 | 1 | r |
| 8 | reg4/U0:D | net | s6 | | + | 0.106 | 5.310 | | r |
| 9 | data arrival time | | | | | | 5.310 | | |
| 10 | | | | | | | | | |
| 11 | clk2 | | | | | 2.000 | 2.000 | | |
| 12 | reg4/U0:CLK | clock network | | | + | 3.048 | 5.048 | | r |
| 13 | reg4/U0:D | Library setup | | ADLIB:DFEG | - | 0.234 | 4.814 | | |
| 14 | data required time | | | | | | 4.814 | | |
| 15 | | | | | | | | | |
| 16 | data required time | | | | | | 4.814 | | |
| 17 | data arrival time | | | | - | | 5.310 | | |
| 18 | slack | | | | | | -0.496 | | |

Inter clock domain clk1 to clk2

Inter clock domain clk2 to clk1

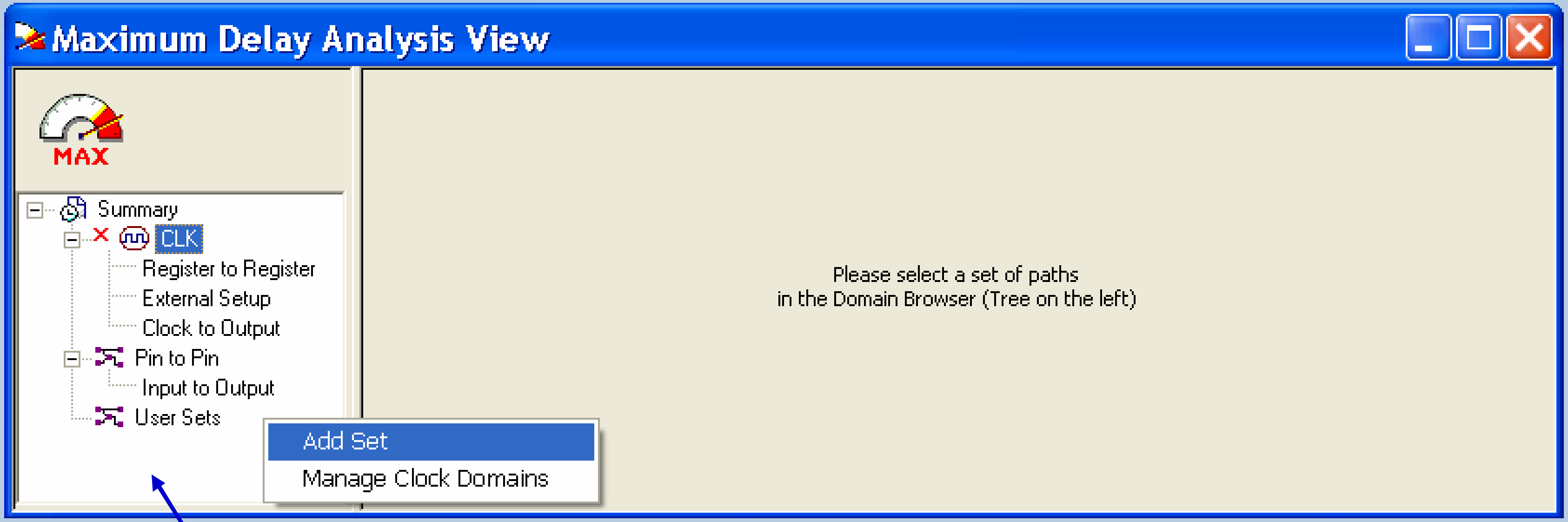
# Timing Analysis with SmartTime

- Design Summary
- Setup and Hold Checks
- Cross Clock Domain Analysis
- Adding User Sets and Filtering
- Customizing the Analysis View
- Cross-Probing with MVN Tools

ONE CHIP is all you need

# SmartTime
## *Adding Path Sets*

- Users Can Create and Manage Custom Path Sets for Timing Analysis
  - **Custom Path Sets Appear Under User Sets in Domain Browser**



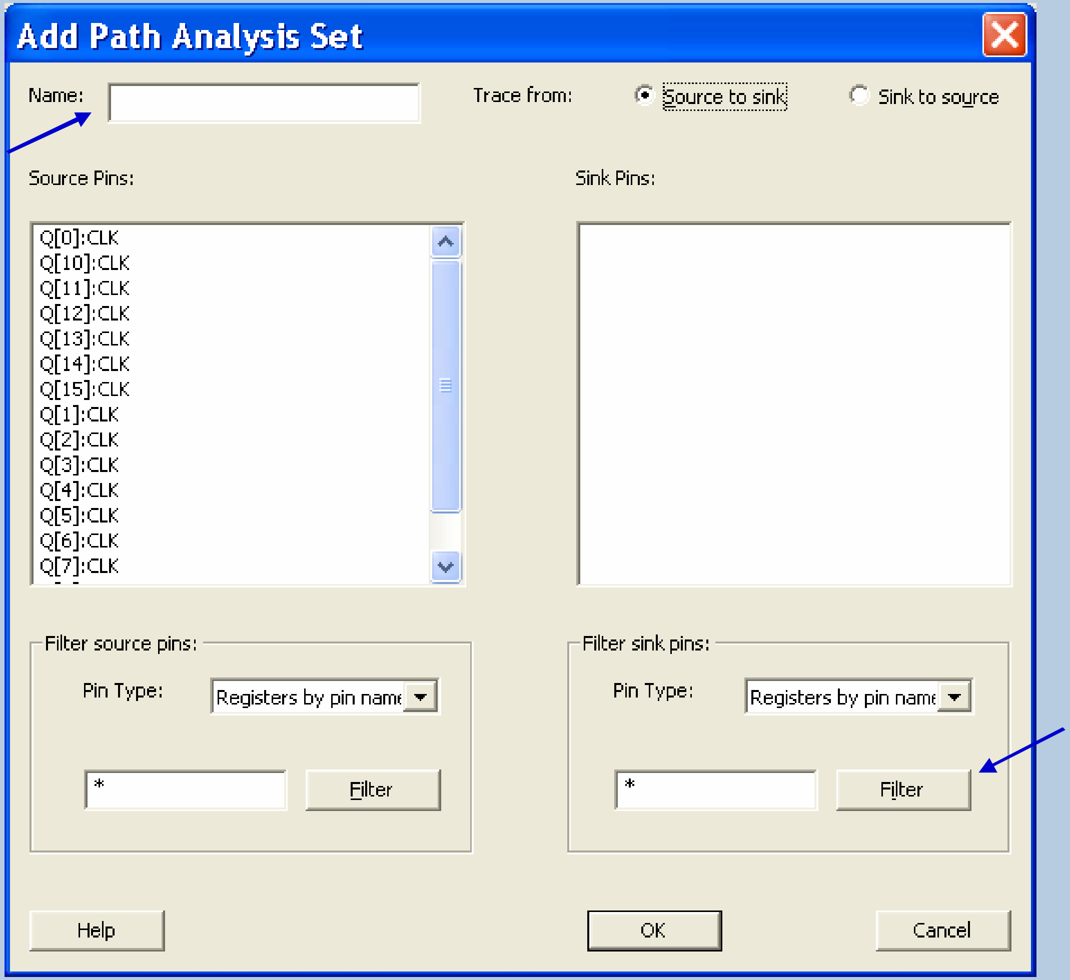
Please select a set of paths in the Domain Browser (Tree on the left)

Right click in domain browser area

# SmartTime

## *Adding Path Sets (cont.)*

- Enter Path Set Name and Select Source and Sink Pins



Add Path Analysis Set

Name:

Trace from: ● Source to sink ○ Sink to source

Source Pins:

Q[0]:CLK
Q[10]:CLK
Q[11]:CLK
Q[12]:CLK
Q[13]:CLK
Q[14]:CLK
Q[15]:CLK
Q[1]:CLK
Q[2]:CLK
Q[3]:CLK
Q[4]:CLK
Q[5]:CLK
Q[6]:CLK
Q[7]:CLK

Sink Pins:

Filter source pins:

Pin Type: Registers by pin name

*

Filter sink pins:

Pin Type: Registers by pin name

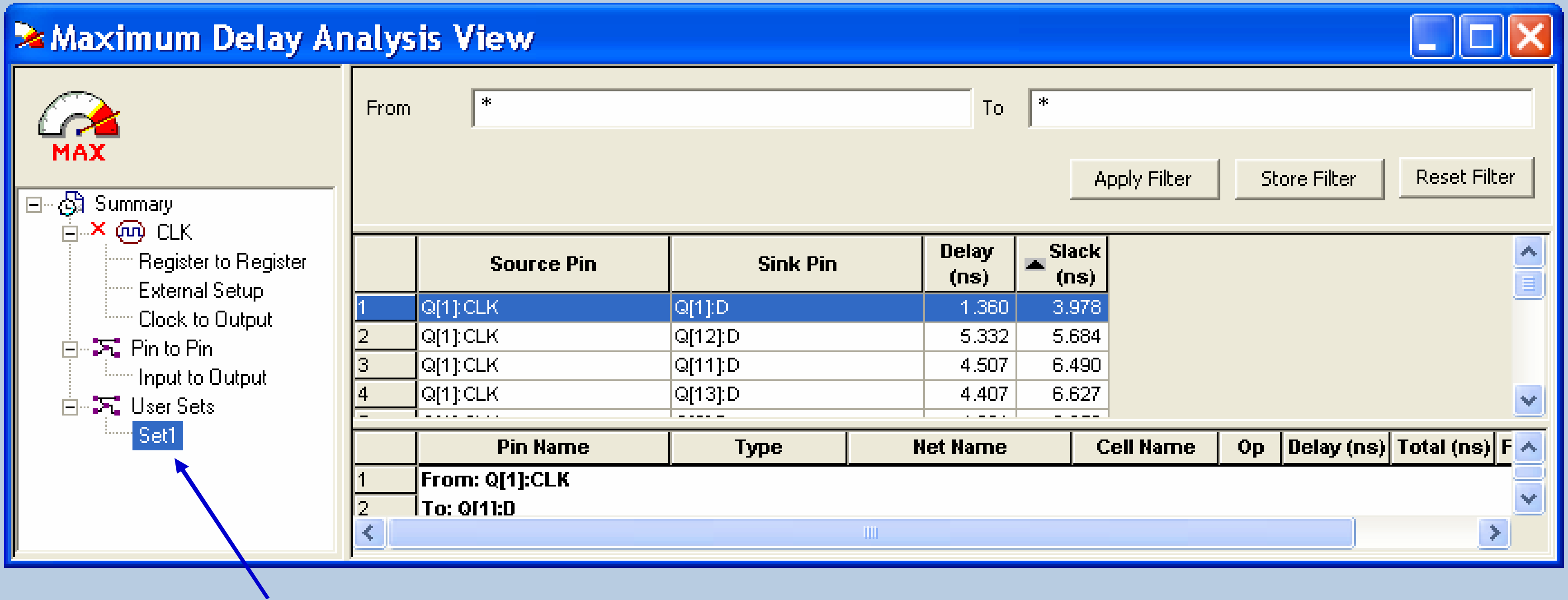
*

Enter path set name

Filtering for source and sink pins

# SmartTime
## *Adding Path Sets (cont.)*

- Maximum Delay Analysis View With Added Path Set



| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) |
|---|---|---|---|---|
| 1 | Q[1]:CLK | Q[1]:D | 1.360 | 3.978 |
| 2 | Q[1]:CLK | Q[12]:D | 5.332 | 5.684 |
| 3 | Q[1]:CLK | Q[11]:D | 4.507 | 6.490 |
| 4 | Q[1]:CLK | Q[13]:D | 4.407 | 6.627 |

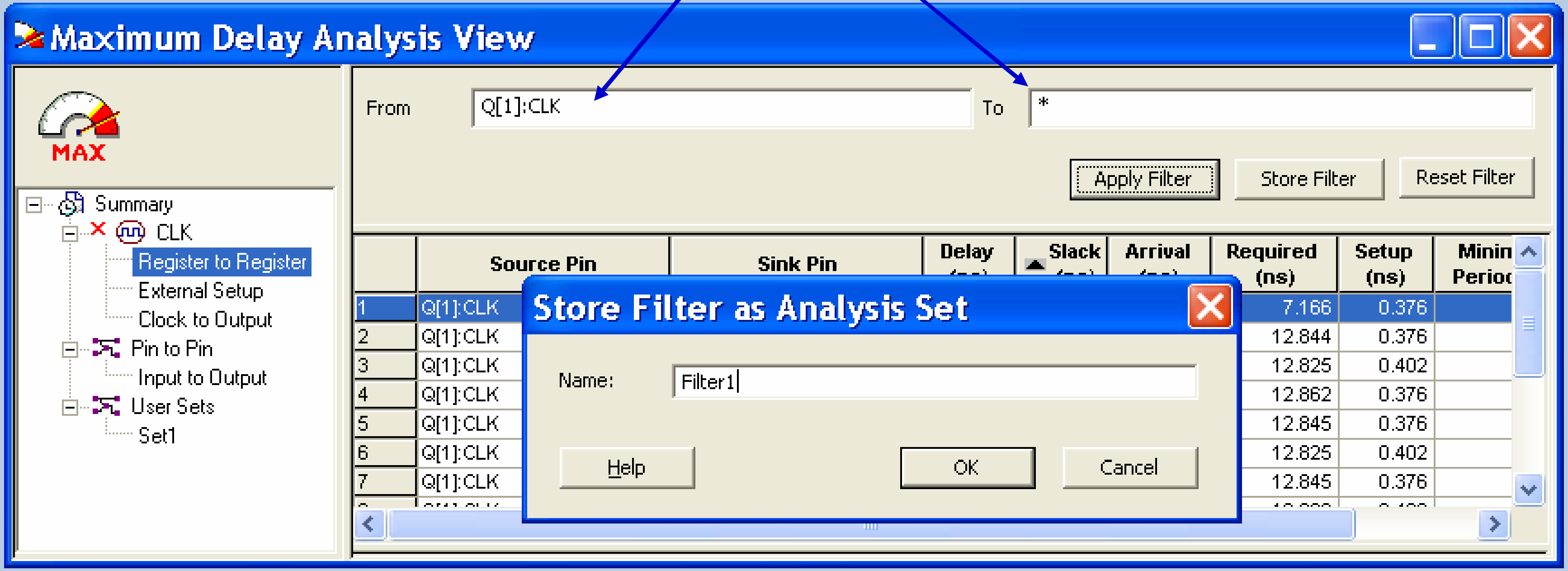
| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | F |
|---|---|---|---|---|---|---|---|---|
| 1 | **From: Q[1]:CLK** | | | | | | | |
| 2 | **To: Q[1]:D** | | | | | | | |

Custom Path Set

# SmartTime
*Filtering Management*

- Filters Can Be Used to Limit Path Set Content
  - **Filters Are Displayed Below Set Under Which It Was Created**
  - **Filters Can Be Nested**

Enter source and sink pins for filter



From: Q[1]:CLK

To: *

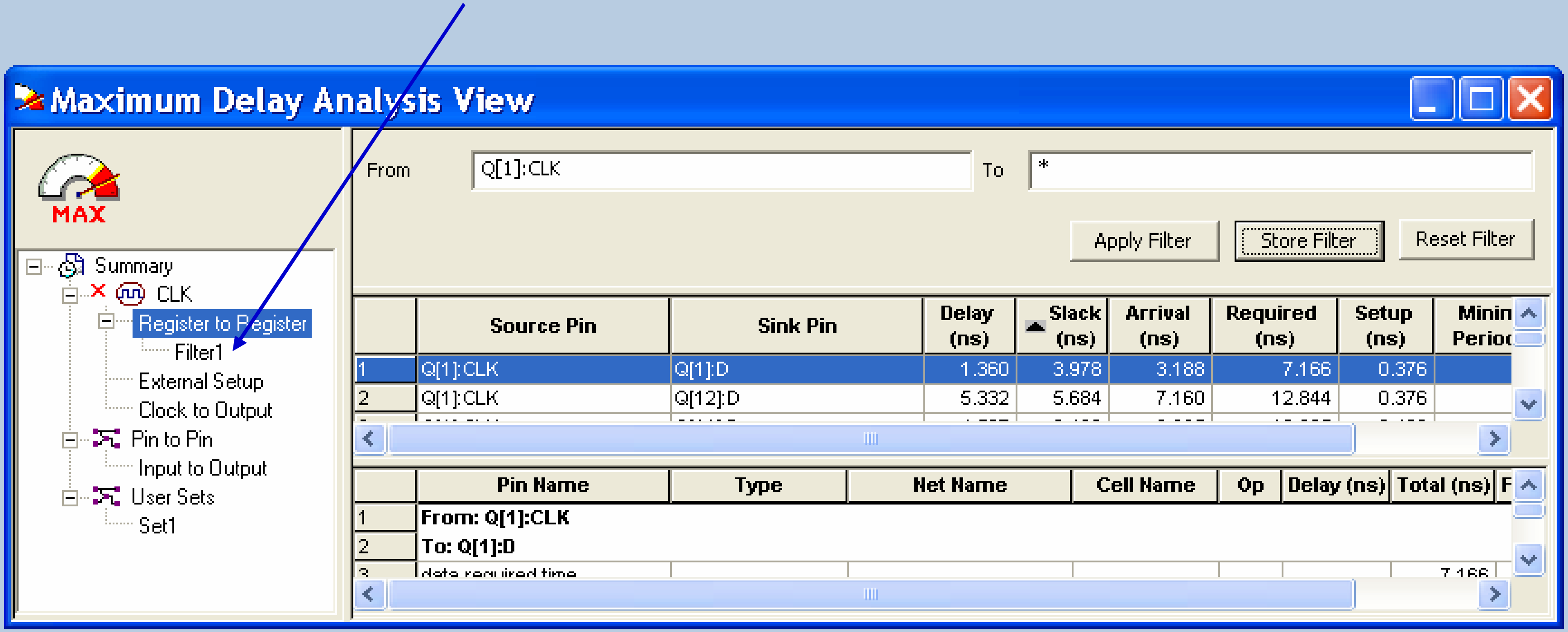
| | Source Pin | Sink Pin | Delay | Slack | Arrival | Required (ns) | Setup (ns) | Minin Perioc |
|---|---|---|---|---|---|---|---|---|
| 1 | Q[1]:CLK | | | | | 7.166 | 0.376 | |
| 2 | Q[1]:CLK | | | | | 12.844 | 0.376 | |
| 3 | Q[1]:CLK | | | | | 12.825 | 0.402 | |
| 4 | Q[1]:CLK | | | | | 12.862 | 0.376 | |
| 5 | Q[1]:CLK | | | | | 12.845 | 0.376 | |
| 6 | Q[1]:CLK | | | | | 12.825 | 0.402 | |
| 7 | Q[1]:CLK | | | | | 12.845 | 0.376 | |

Store Filter as Analysis Set

Name: Filter1

# SmartTime
## *Filtering Management (cont.)*

Stored Filter



From: Q[1]:CLK

To: *

|  | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) | Minin Perioc |
|---|---|---|---|---|---|---|---|---|
| 1 | Q[1]:CLK | Q[1]:D | 1.360 | 3.978 | 3.188 | 7.166 | 0.376 |  |
| 2 | Q[1]:CLK | Q[12]:D | 5.332 | 5.684 | 7.160 | 12.844 | 0.376 |  |

|  | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | F |
|---|---|---|---|---|---|---|---|---|
| 1 | From: Q[1]:CLK |  |  |  |  |  |  |  |
| 2 | To: Q[1]:D |  |  |  |  |  |  |  |
| 3 | data required time |  |  |  |  |  | 7.166 |  |

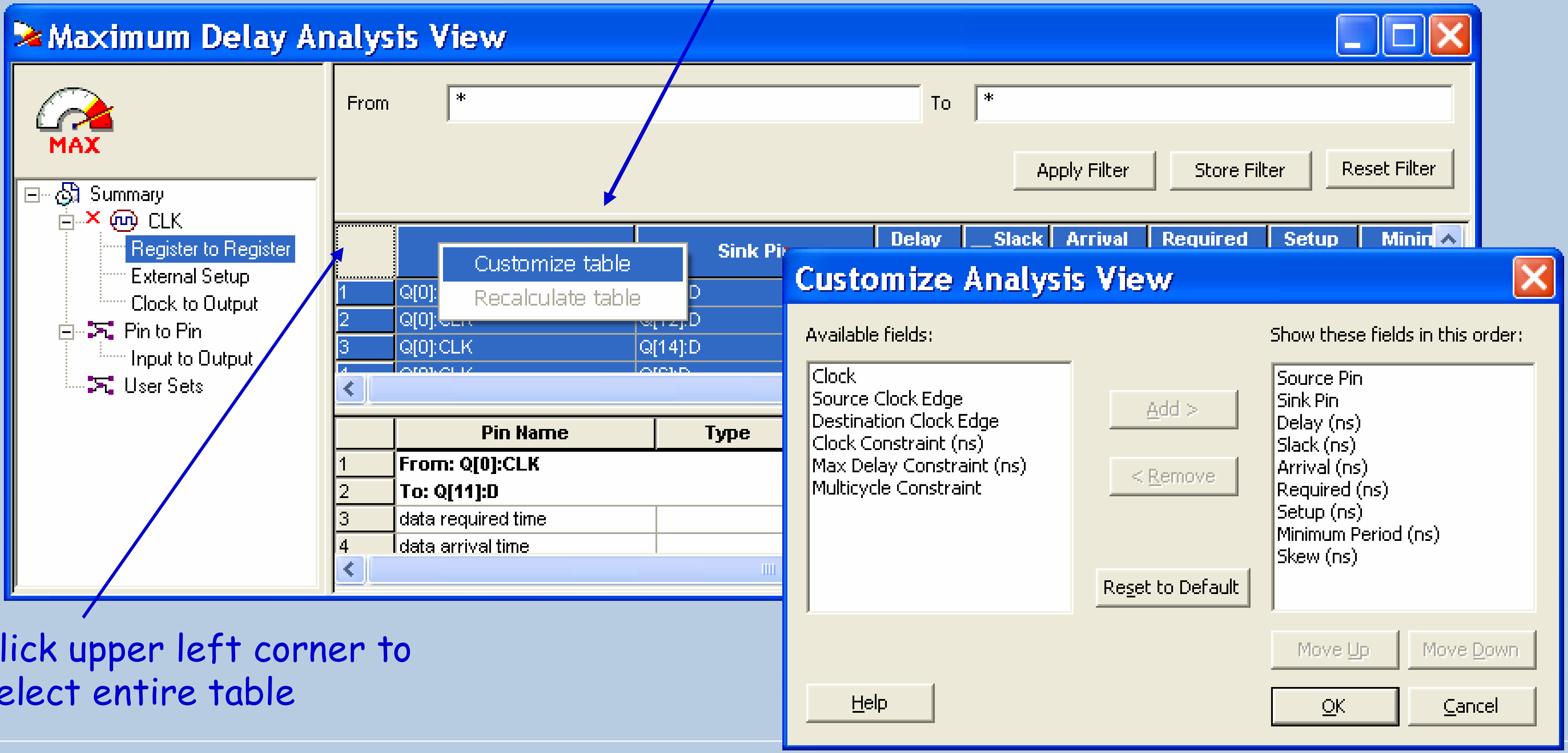
# Timing Analysis with SmartTime

- Design Summary
- Setup and Hold Checks
- Cross Clock Domain Analysis
- Adding User Sets and Filtering
- Customizing the Analysis View
- Cross-Probing with MVN Tools

# SmartTime
## *Customizing Analysis View*

- Timing Information in Path List Is Customizable
  - **Add or Remove Columns for Each Type of Path Set**

Right-click in Table Header and Select "Customize Table"



From: *
To: *

| | | Sink Pin |
|---|---|---|
| 1 | Q[0]: | D |
| 2 | Q[0]:CLK | Q[12]:D |
| 3 | Q[0]:CLK | Q[14]:D |
| 4 | Q[0]:CLK | Q[6]:D |

| | Pin Name | Type |
|---|---|---|
| 1 | **From: Q[0]:CLK** | |
| 2 | **To: Q[11]:D** | |
| 3 | data required time | |
| 4 | data arrival time | |

Available fields:

- Clock
- Source Clock Edge
- Destination Clock Edge
- Clock Constraint (ns)
- Max Delay Constraint (ns)
- Multicycle Constraint

Show these fields in this order:

- Source Pin
- Sink Pin
- Delay (ns)
- Slack (ns)
- Arrival (ns)
- Required (ns)
- Setup (ns)
- Minimum Period (ns)
- Skew (ns)

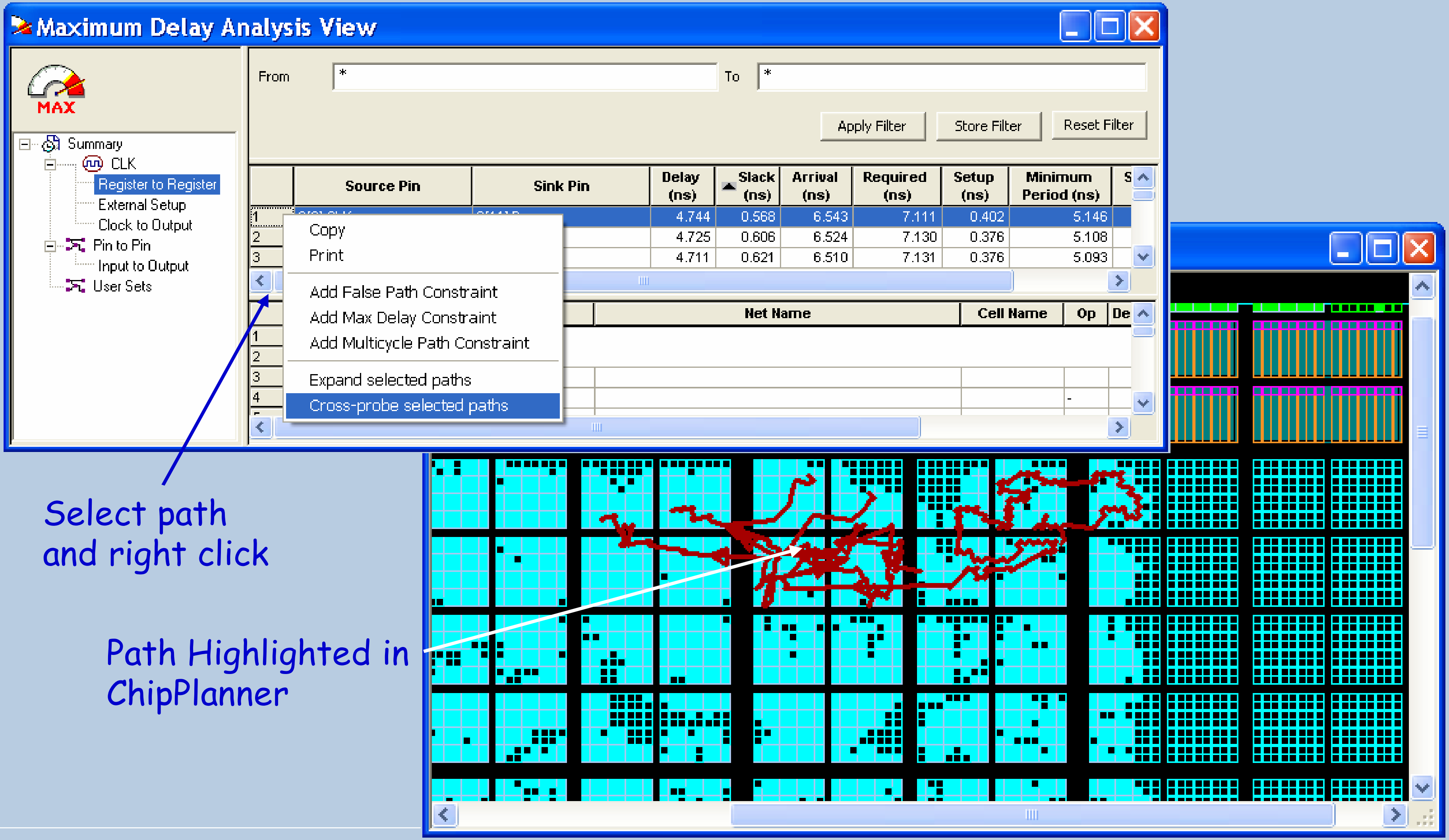
Click upper left corner to select entire table

# Timing Analysis with SmartTime

- Design Summary
- Setup and Hold Checks
- Cross Clock Domain Analysis
- Adding User Sets and Filtering
- Customizing the Analysis View
- Cross-Probing with MVN Tools

# SmartTime
## *Cross-Probing with MultiView Navigator*

## Cross-probe between SmartTime and MVN Tools

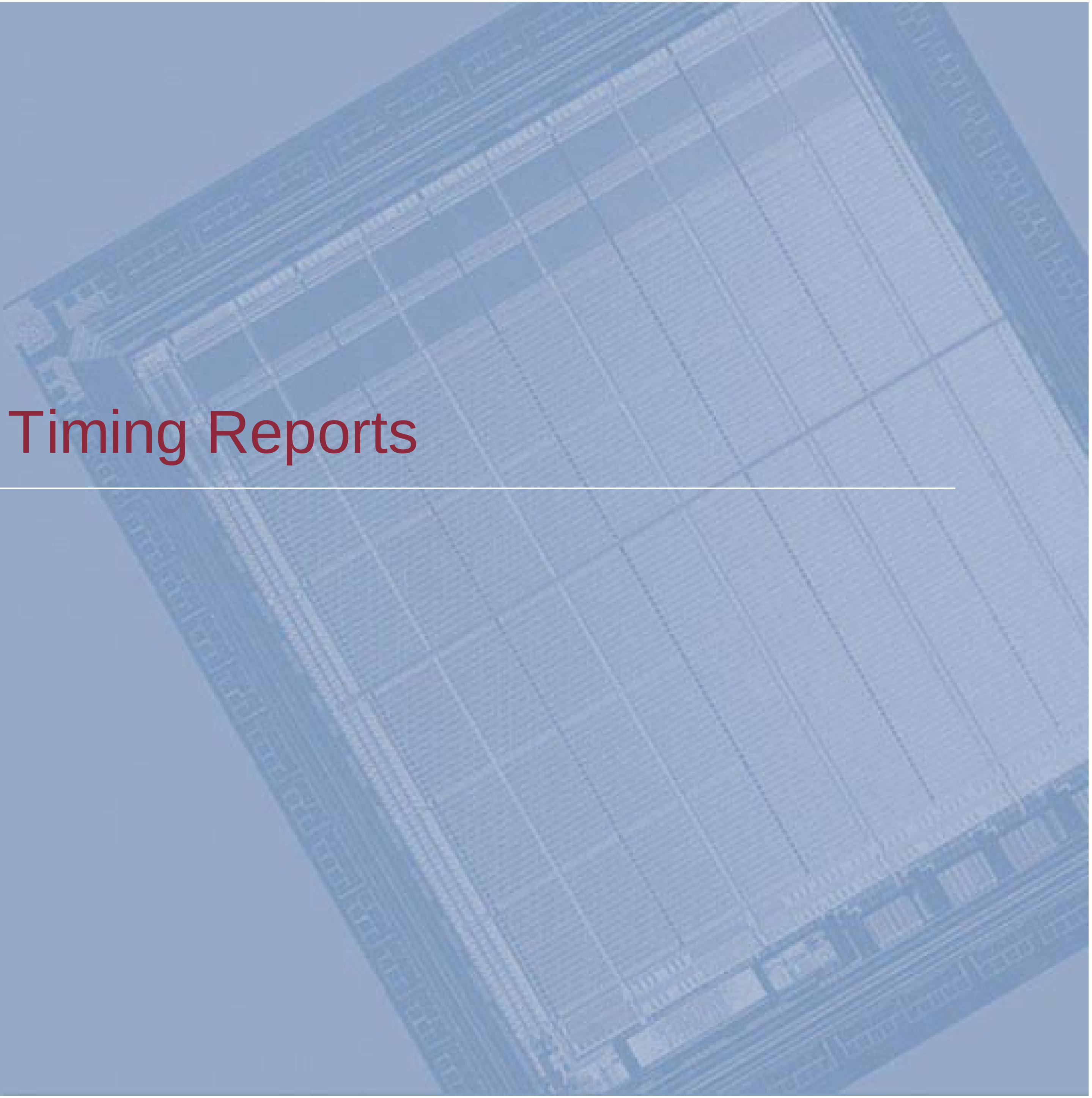


| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Setup (ns) | Minimum Period (ns) |
|---|---|---|---|---|---|---|---|---|
| 1 | | | 4.744 | 0.568 | 6.543 | 7.111 | 0.402 | 5.146 |
| 2 | | | 4.725 | 0.606 | 6.524 | 7.130 | 0.376 | 5.108 |
| 3 | | | 4.711 | 0.621 | 6.510 | 7.131 | 0.376 | 5.093 |

| | Net Name | Cell Name | Op | De |
|---|---|---|---|---|
| 1 | | | | |
| 2 | | | | |
| 3 | | | | |
| 4 | | | - | |

Select path and right click

Path Highlighted in ChipPlanner



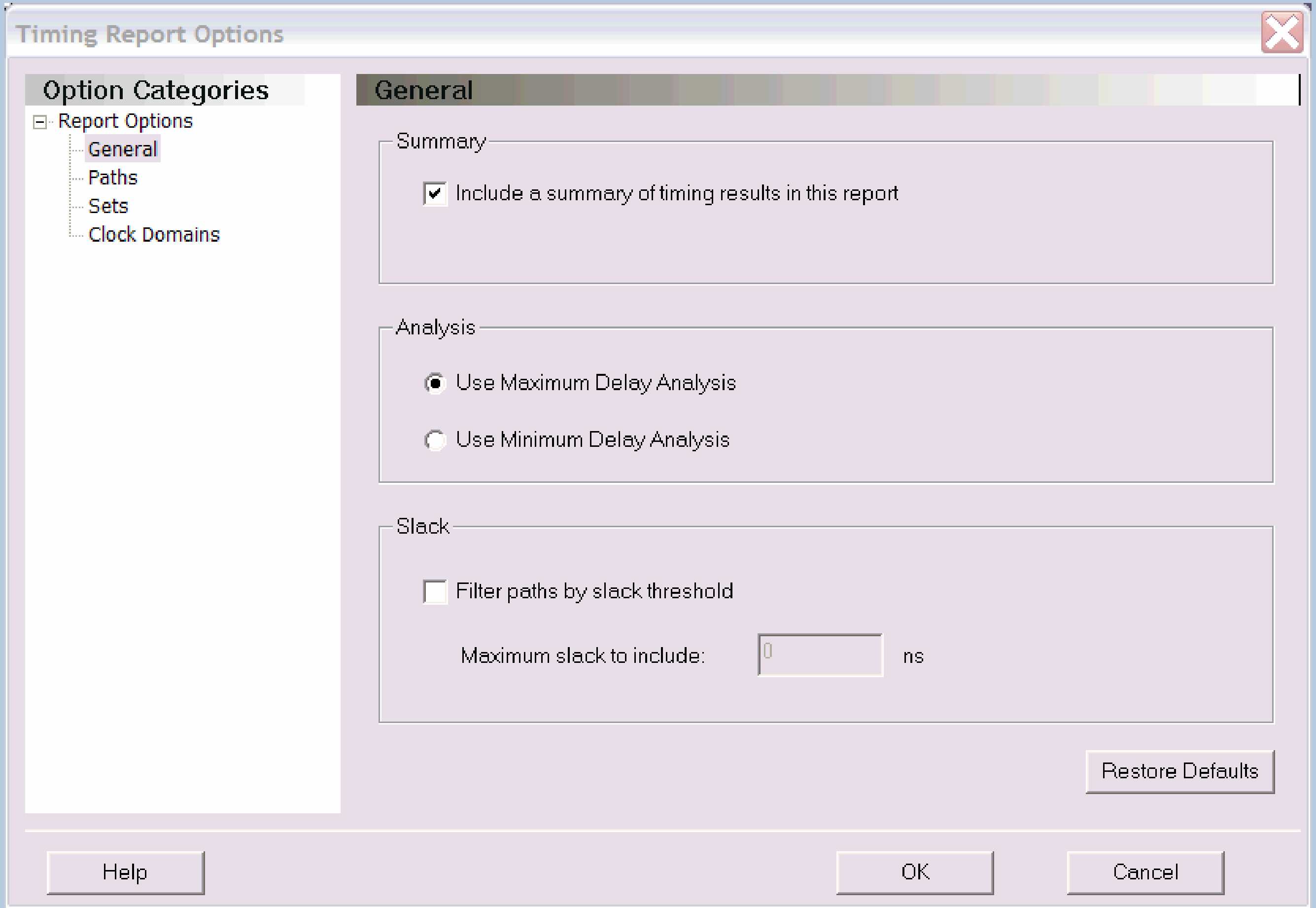
# Timing Reports

# SmartTime
## *Timing Reports*

- SmartTime Can Generate Two Types of Reports:
  - **Timing Report**
  - **Timing Violation Report**
- Timing Report Contains Timing Information of the Design in a Text Format
  - **Information Can Be Customized**
- Timing Violation Report Contains a Flat List of Paths With Timing Violations (No Breakdown by Clock Domain).

# SmartTime
## *Timing Report Options*

- Include Summary in Timing Report



Timing Report Options

Option Categories

- Report Options
  - General
  - Paths
  - Sets
  - Clock Domains

General

Summary

☑ Include a summary of timing results in this report

Analysis

● Use Maximum Delay Analysis

○ Use Minimum Delay Analysis

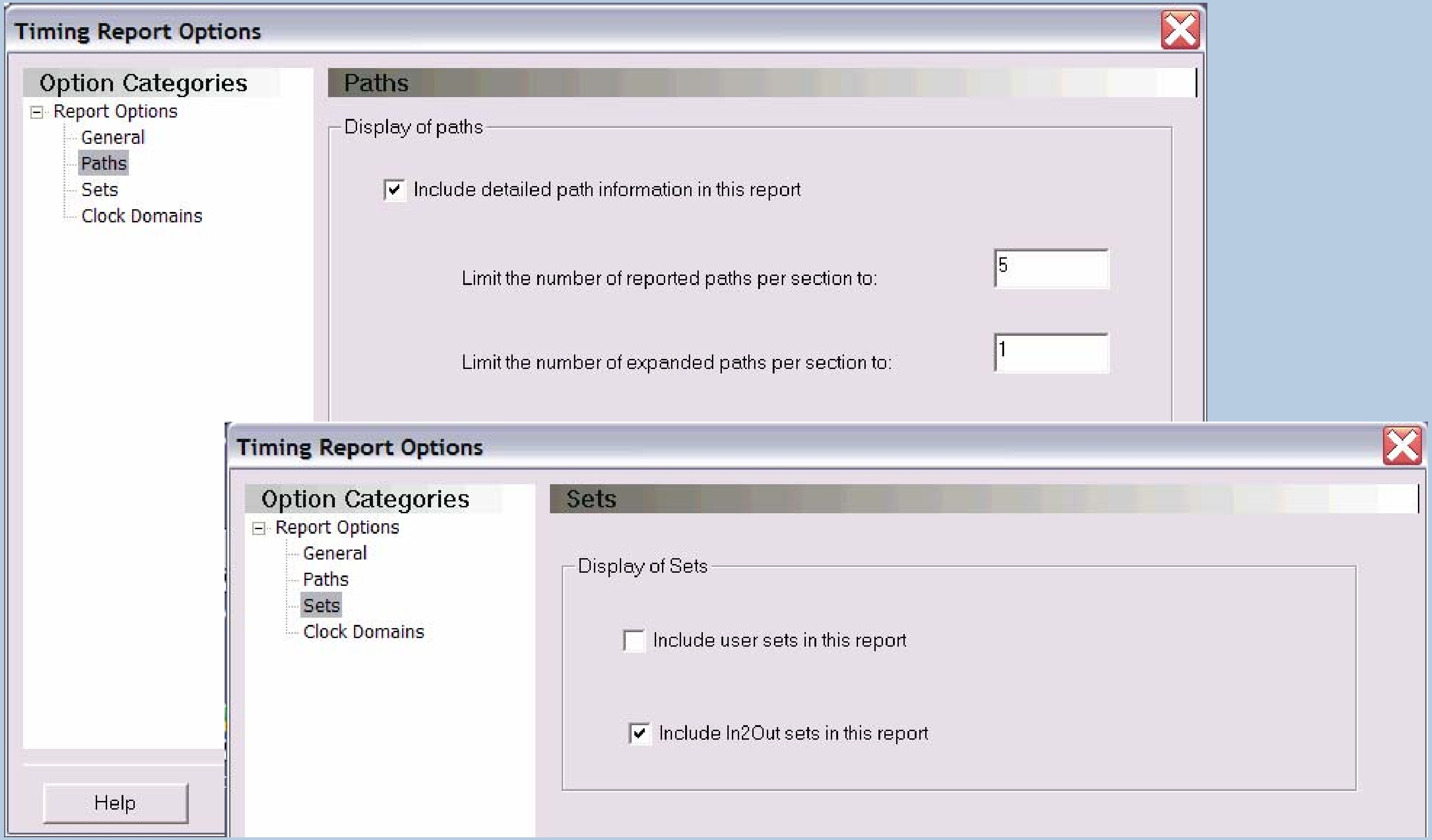
Slack

□ Filter paths by slack threshold

Maximum slack to include: 0 ns

# SmartTime
## *Timing Report Options*

- Paths & Sets Options
  - **Include User Defined Sets in Timing Report**



Timing Report Options

Option Categories
- Report Options
  - General
  - Paths
  - Sets
  - Clock Domains

Paths

Display of paths

☑ Include detailed path information in this report

Limit the number of reported paths per section to: 5

Limit the number of expanded paths per section to: 1

Timing Report Options

Option Categories
- Report Options
  - General
  - Paths
  - Sets
  - Clock Domains

Sets

Display of Sets

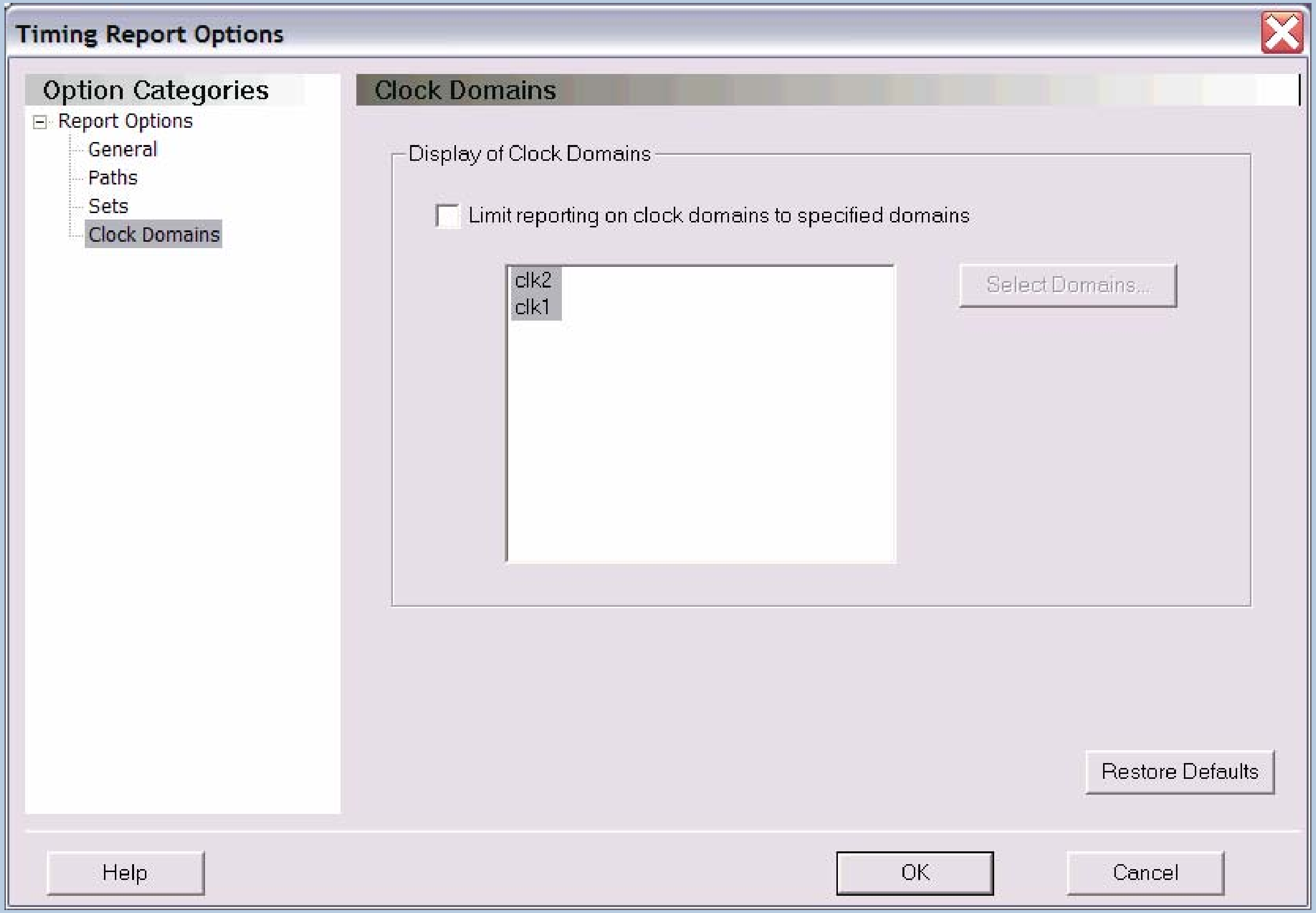
☐ Include user sets in this report

☑ Include In2Out sets in this report

# SmartTime
*Timing Report Options*

## Clock Domains

- **Specify Clock Domains to be Included in the Timing Report**



Timing Report Options

Clock Domains

Display of Clock Domains

□ Limit reporting on clock domains to specified domains

clk2
clk1

# SmartTime
## *Timing Report Structure*

- Header
  - **Design Information, Operating Conditions…**
- Summary
  - **Data-sheet (Freq, ext setup/hold, min/max clock-to-out…)**
- Clock Domain Details
  - **Path Sets (reg2reg, in2reg, reg2out, Custom…)**
    - **Path Details**
    - **Expanded Paths**
- Inter-clock Domain Details
- Pin-to-pin Path
  - **Path Sets (in2out, Custom…)**

# SmartTime
## *Summary Section in Timing Report*

- Clock Domain: p_spi_clk

| | |
|---|---|
| Period (ns): | 9.334 |
| Frequency (MHz): | 107.135 |
| External Setup(ns): | 2.103 |
| External Hold( ns): | 2.599 |
| Min Clock-To-Out (ns): | 5.302 |
| Max Clock-To-Out (ns): | 8.261 |

- Clock Domain: q_spi_clk

| | |
|---|---|
| Period (ns): | 9.334 |
| Frequency (MHz): | 107.135 |
| External Setup(ns): | 2.103 |
| External Hold( ns): | 2.599 |
| Min Clock-To-Out (ns): | 5.302 |
| Max Clock-To-Out (ns): | 8.261 |

- In-to-Out:

| | |
|---|---|
| Min Delay (ns): | 4.569 |
| Max Delay (ns): | 8.246 |

# SmartTime
## *Clock Details in Timing Report 1/2*

Clock Domain: p_spi_clk

### Path-Set Register-to-Register

**Path 1**

| | |
|---|---|
| ***From:*** | ***B_mbuf/r_adr[0]:CLK*** |
| ***To:*** | ***B_mbuf/clear[1]:D*** |
| ***Delay:*** | ***8.090*** |
| ***Slack:*** | ***-5.218*** |
| ***Arrival:*** | ***16.331*** |
| ***Departure:*** | ***11.113*** |
| ***Minimum period:*** | ***0.2359*** |
| ***Skew:*** | ***45.023*** |

**Path 2**

-------

**Path 3**

-------

**Expanded path 1**

-------

### Path-Set In-to-Register

**.....**

# SmartTime
## *Clock Details in Timing Report 2/2*

## Clock Domain: p_spi_clk

**Path-Set Register-to-Register**

- **Path 1**
- **Path 2**
- **Expanded path 1**

```
-----------------------------------------------------------
Total(ns)  Op   Delay(ns)  PinName (edge)
                                Type/name
0.000                      p_spi_clk
              +   1.912         Clock network
1.912                      B_mbuf/r_adr[0]:CLK (r)
              +   0.257         Cell: ADLIB:AO21TTF
2.169                      B_mbuf/clear_d_1[1]:Y (f)
              +   0.289         Net: B_mbuf/clear_d_1[1]_net_1
2.458                      B_mbuf/clear[1]:D (f)

2.458                      data arrival time
________________________________________________________________


4.000                      p_spi_clk
       +   1.879                Clock network
7.879                      B_mbuf/clear[1]:CLK (r)
       -   0.766                Library setup ADLIB:DFFC
7.113                      B_mbuf/clear[1]:D

7.113                      data required time
________________________________________________________________

7.113                      data required time
2.458                      data arrival time
4.655                      slack
```

**Path-Set In-to-Register**

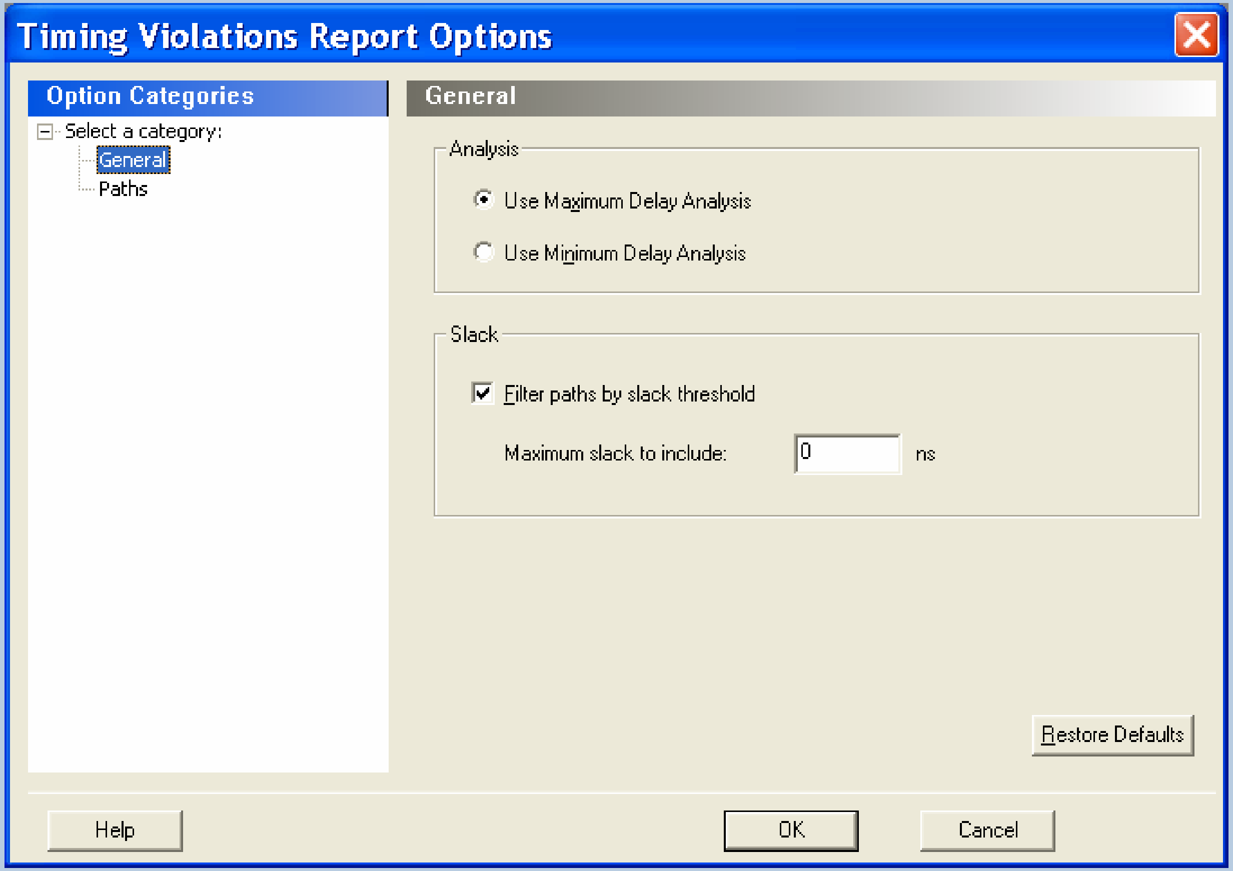
**.....**

ONECHIP is all you need

# SmartTime
## *Timing Violations Report Options*

## General Options

- **Specify Maximum or Minimum Delay Analysis**
- **Enter Slack Threshold**



Timing Violations Report Options

Analysis

● Use Maximum Delay Analysis

○ Use Minimum Delay Analysis

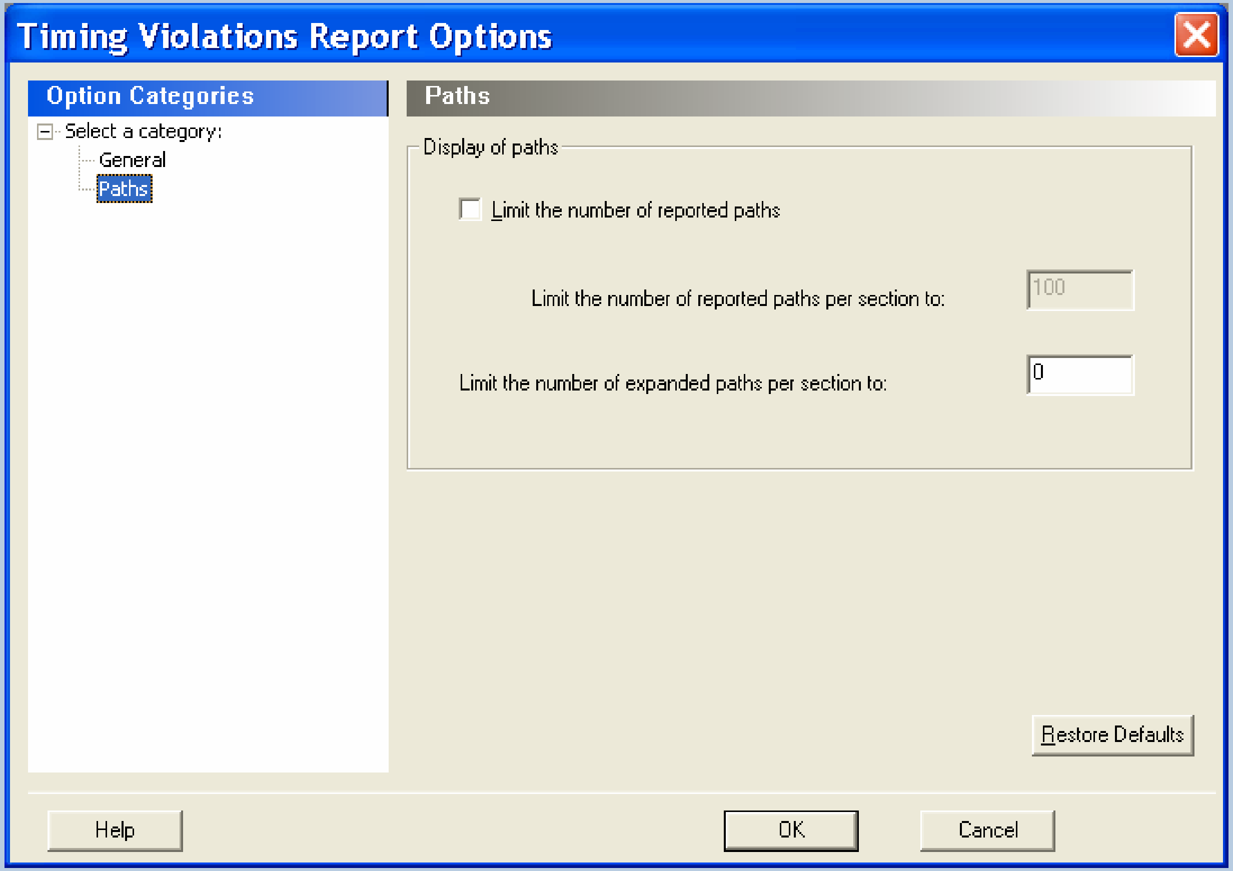
Slack

☑ Filter paths by slack threshold

Maximum slack to include: 0 ns

# SmartTime
## *Timing Violations Report Options*

- Path Options
  - **Limit Number of Reported Paths**



Timing Violations Report Options

Option Categories

Select a category:
- General
- Paths

Paths

Display of paths

□ Limit the number of reported paths

Limit the number of reported paths per section to: 100

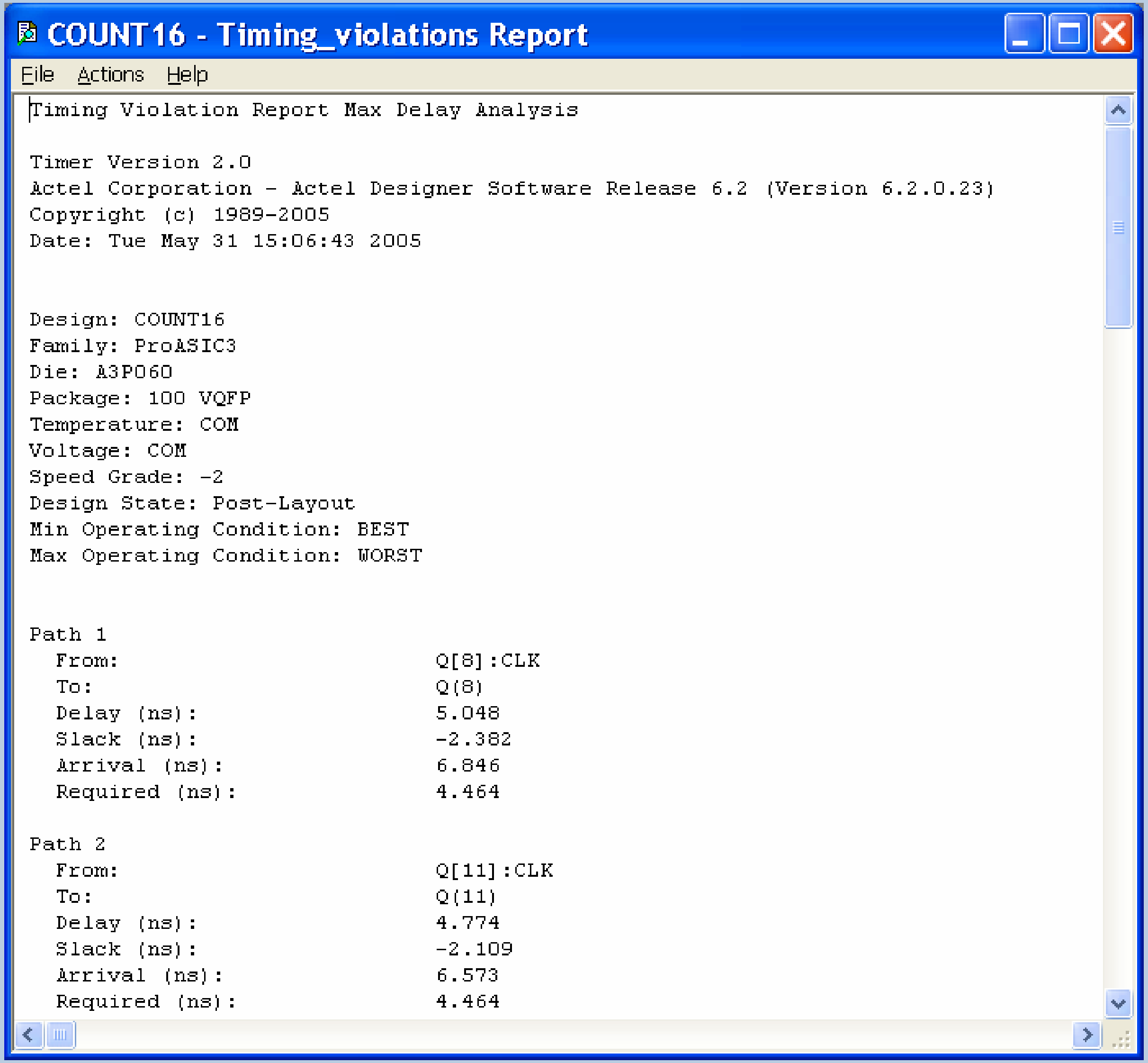
Limit the number of expanded paths per section to: 0

# SmartTime
## *Violation Report Structure*

- Header
  - **Design Information, Operating Conditions…**
- Paths
  - **List of Paths With Timing Violations**

# SmartTime

## *Violation Report*



```
Timing Violation Report Max Delay Analysis

Timer Version 2.0
Actel Corporation - Actel Designer Software Release 6.2 (Version 6.2.0.23)
Copyright (c) 1989-2005
Date: Tue May 31 15:06:43 2005


Design: COUNT16
Family: ProASIC3
Die: A3P060
Package: 100 VQFP
Temperature: COM
Voltage: COM
Speed Grade: -2
Design State: Post-Layout
Min Operating Condition: BEST
Max Operating Condition: WORST

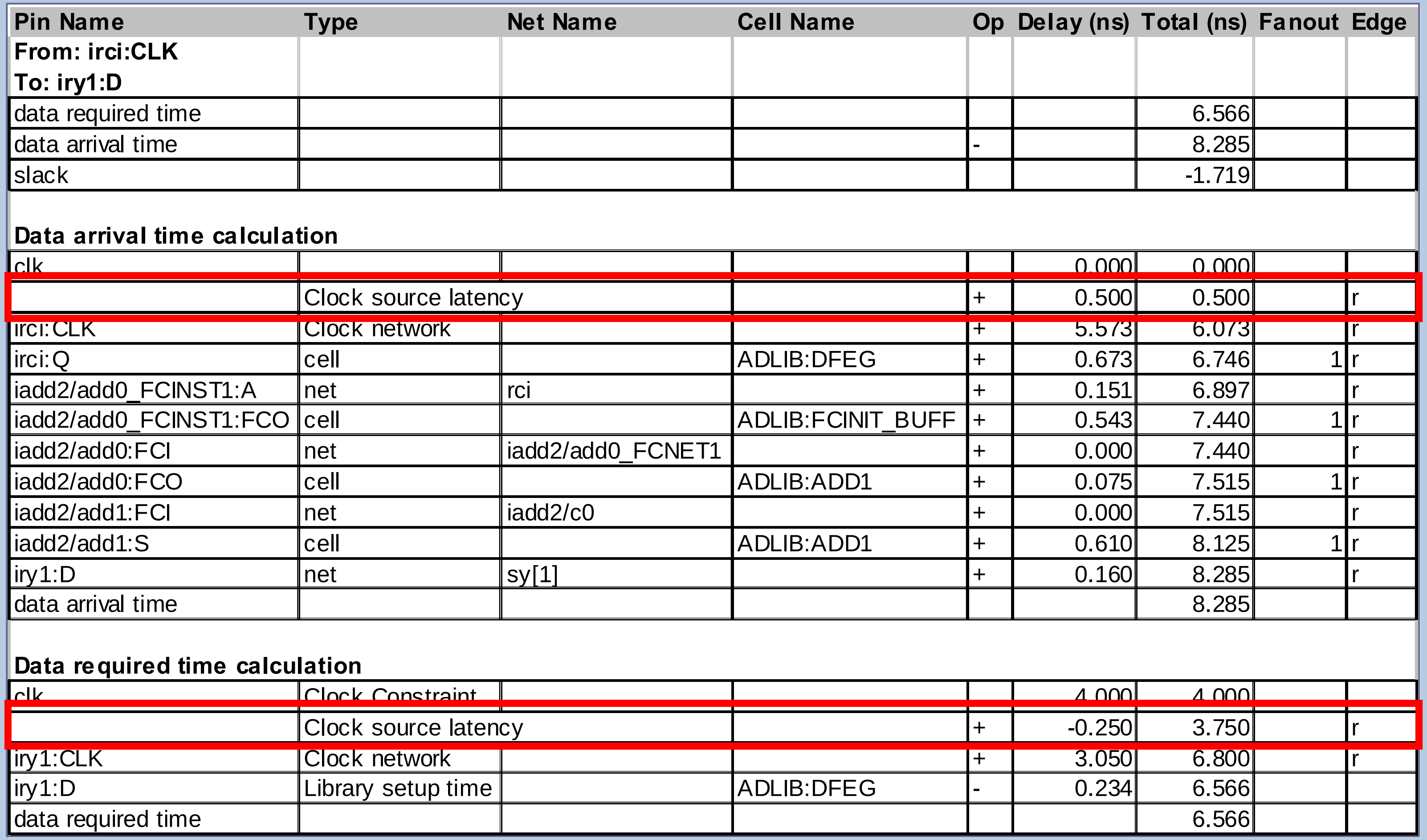

Path 1
  From:                         Q[8]:CLK
  To:                           Q(8)
  Delay (ns):                   5.048
  Slack (ns):                   -2.382
  Arrival (ns):                 6.846
  Required (ns):                4.464

Path 2
  From:                         Q[11]:CLK
  To:                           Q(11)
  Delay (ns):                   4.774
  Slack (ns):                   -2.109
  Arrival (ns):                 6.573
  Required (ns):                4.464
```

# SmartTime 7.2 New Features

- Clock Source Latency
- Asynchronous Signals
- Datasheet Report
- Ease-of-Use
  - **Analyzing the clock network**
  - **Path Set improvements**
  - **Automatic creation of Generated clocks**

# Clock Source Latency: Analysis



| Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|
| **From: irci:CLK**<br>**To: iry1:D** | | | | | | | | |
| data required time | | | | | | 6.566 | | |
| data arrival time | | | | - | | 8.285 | | |
| slack | | | | | | -1.719 | | |
| **Data arrival time calculation** | | | | | | | | |
| clk | | | | | 0.000 | 0.000 | | |
| | Clock source latency | | | + | 0.500 | 0.500 | | r |
| irci:CLK | Clock network | | | + | 5.573 | 6.073 | | r |
| irci:Q | cell | | ADLIB:DFEG | + | 0.673 | 6.746 | 1 | r |
| iadd2/add0_FCINST1:A | net | rci | | + | 0.151 | 6.897 | | r |
| iadd2/add0_FCINST1:FCO | cell | | ADLIB:FCINIT_BUFF | + | 0.543 | 7.440 | 1 | r |
| iadd2/add0:FCI | net | iadd2/add0_FCNET1 | | + | 0.000 | 7.440 | | r |
| iadd2/add0:FCO | cell | | ADLIB:ADD1 | + | 0.075 | 7.515 | 1 | r |
| iadd2/add1:FCI | net | iadd2/c0 | | + | 0.000 | 7.515 | | r |
| iadd2/add1:S | cell | | ADLIB:ADD1 | + | 0.610 | 8.125 | 1 | r |
| iry1:D | net | sy[1] | | + | 0.160 | 8.285 | | r |
| data arrival time | | | | | | 8.285 | | |
| **Data required time calculation** | | | | | | | | |
| clk | Clock Constraint | | | | 4.000 | 4.000 | | |
| | Clock source latency | | | + | -0.250 | 3.750 | | r |
| iry1:CLK | Clock network | | | + | 3.050 | 6.800 | | r |
| iry1:D | Library setup time | | ADLIB:DFEG | - | 0.234 | 6.566 | | |
| data required time | | | | | | 6.566 | | |

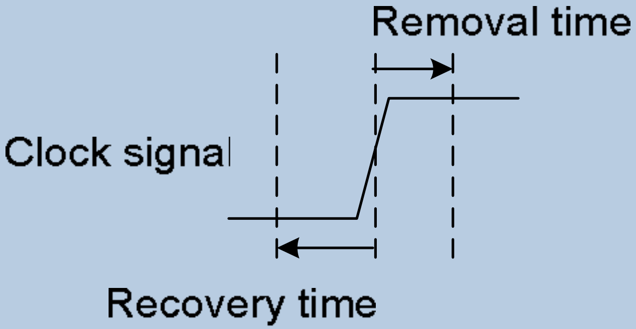
**Late Launch**

**Early Capture**

# Removal/Recovery Checks

## Definition

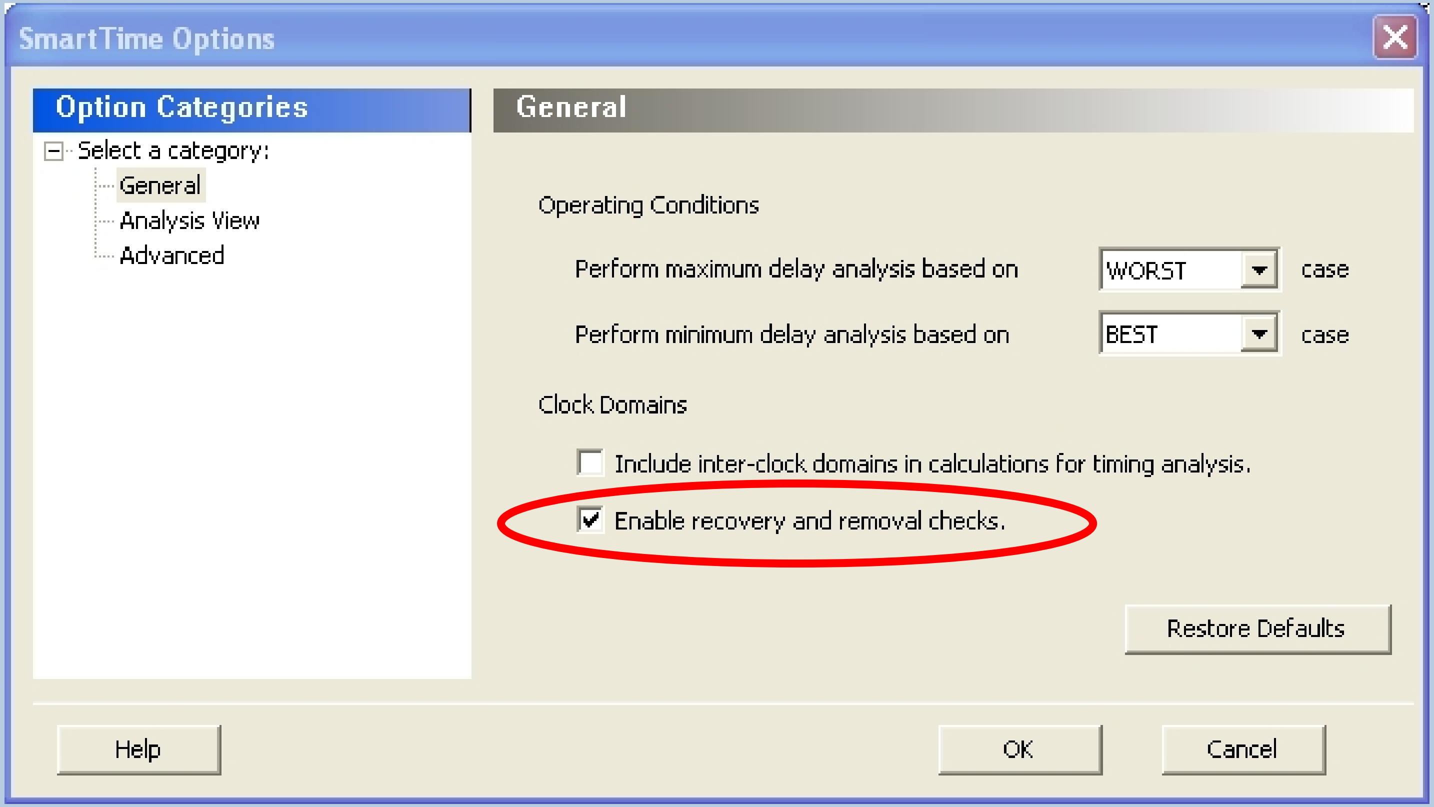
- An asynchronous signal should not be de-activated around the active clock edge



- Recovery needs to be checked in Max delay analysis
- Removal needs to be checked in Min delay analysis

# Removal/Recovery Checks

- Activation: SmartTime Options dialog



SmartTime Options

Option Categories

Select a category:
- General
- Analysis View
- Advanced

General

Operating Conditions

Perform maximum delay analysis based on WORST case

Perform minimum delay analysis based on BEST case

Clock Domains

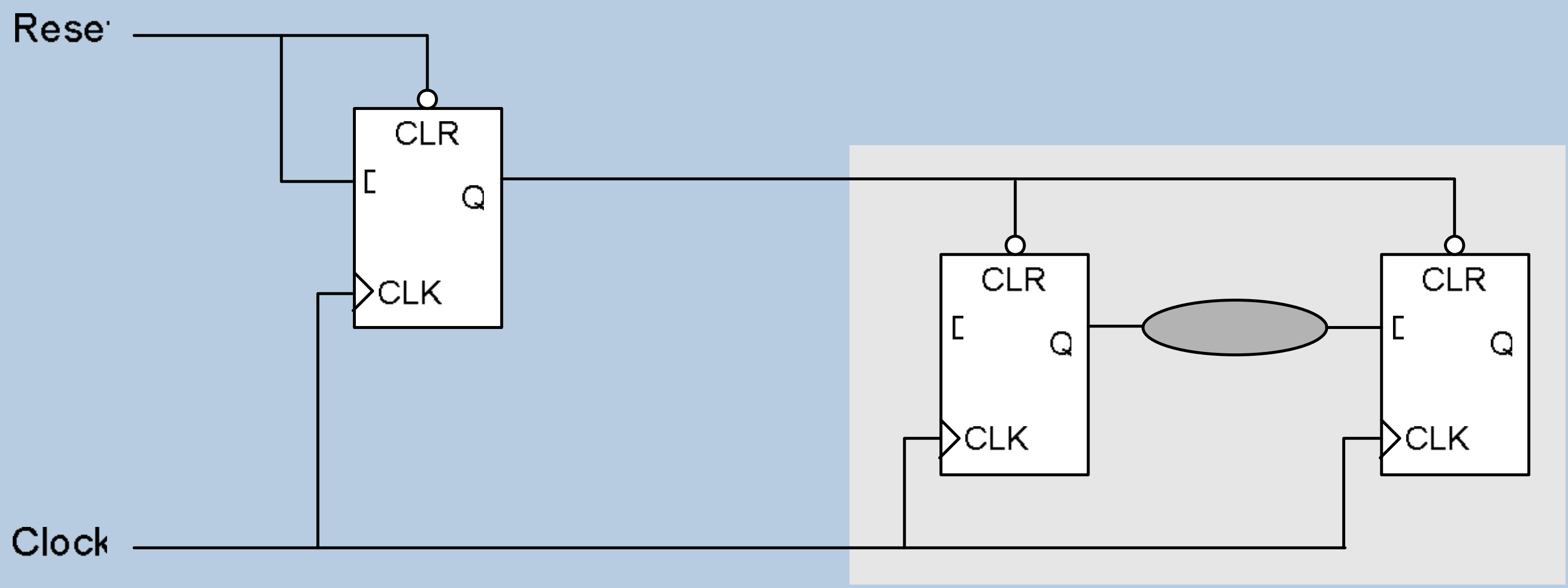
□ Include inter-clock domains in calculations for timing analysis.

☑ Enable recovery and removal checks.

- By default:
  - **No check is done on asynchronous signals**
  - **Signals don't propagate through asynchronous pin of registers**

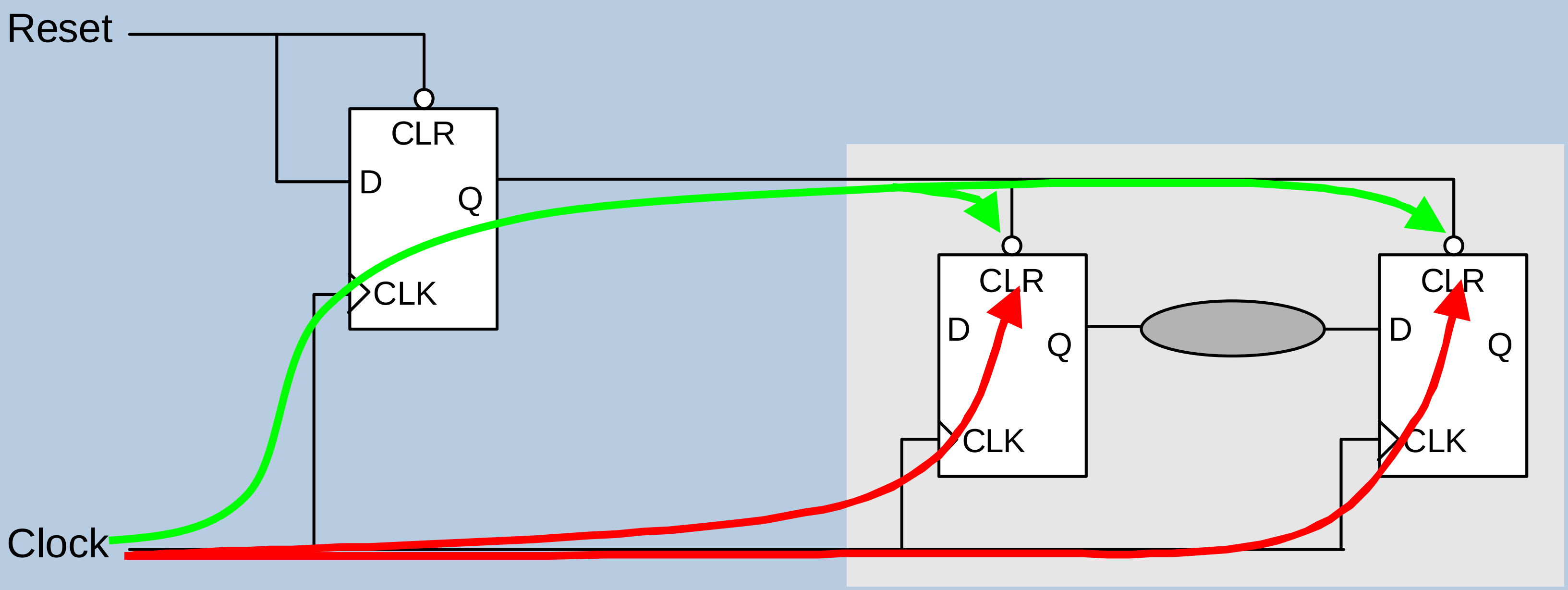
# Removal/Recovery Checks

- Example: Active low reset with synchronous de-activation



# Removal/Recovery Checks

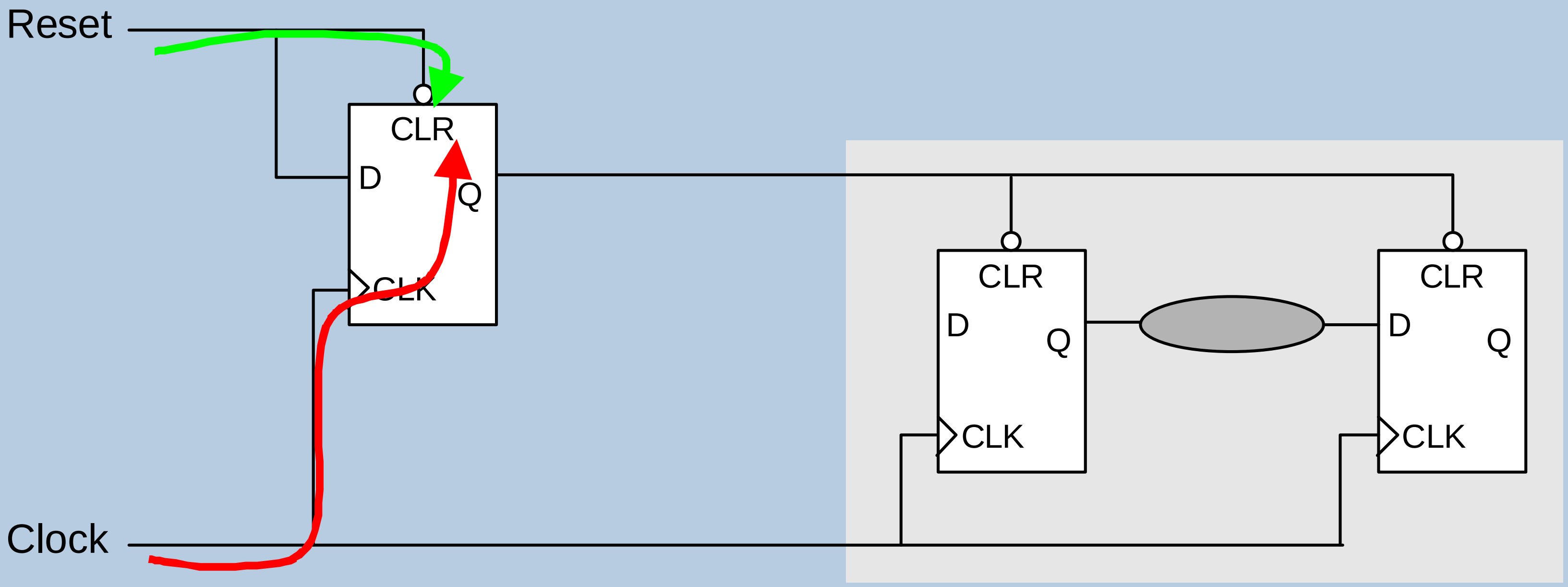
- Recovery/Removal Check



- Minimum period is limited by the propagation between the reset register and the other registers.

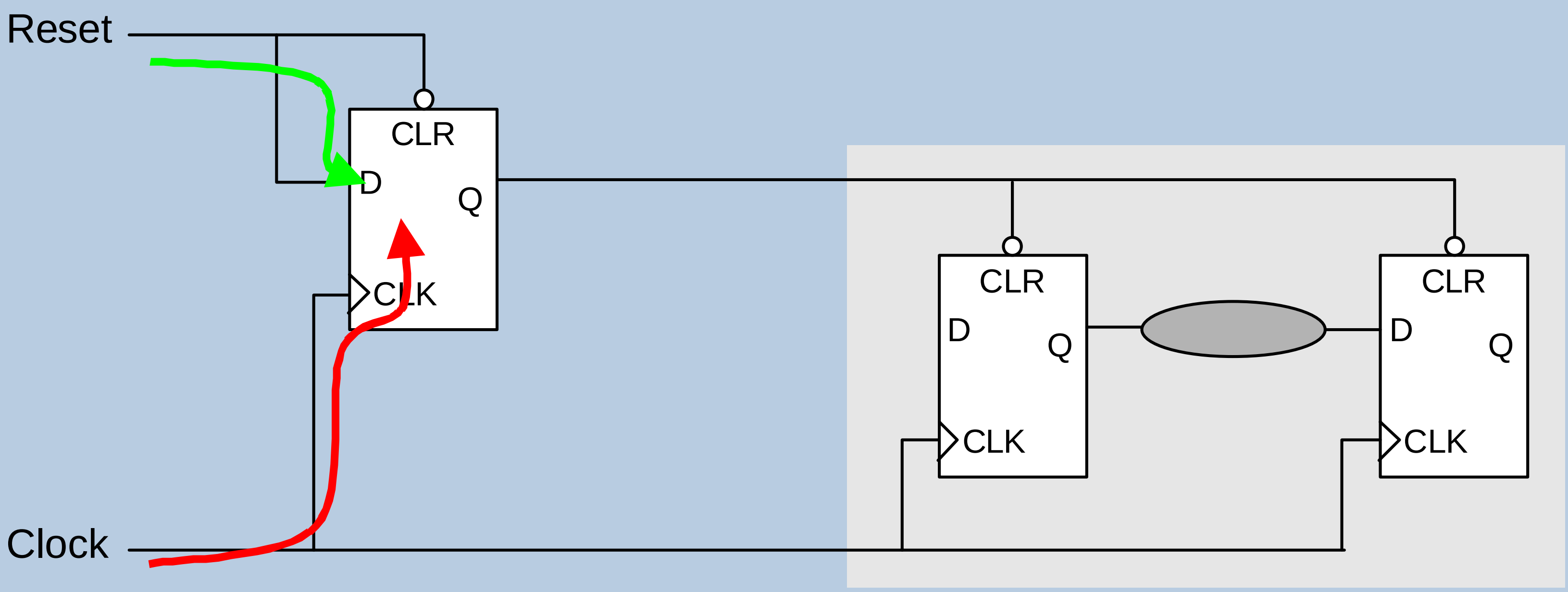
# Removal/Recovery Checks

- External Recovery/Removal

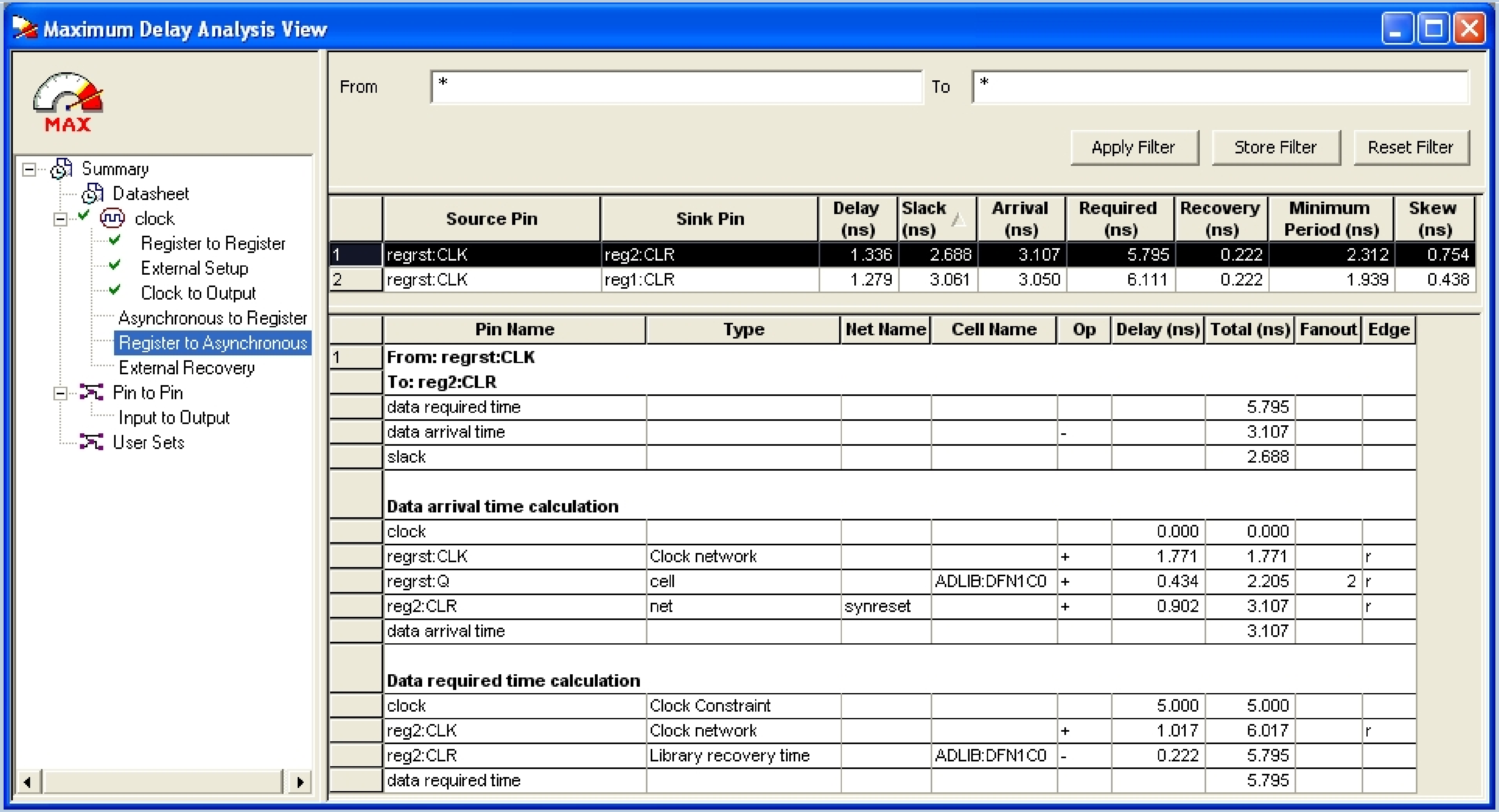


# Removal/Recovery Checks

- External Setup/Hold



# Removal/Recovery Checks: Analysis



Maximum Delay Analysis View

- Summary
  - Datasheet
  - ✓ clock
    - ✓ Register to Register
    - ✓ External Setup
    - ✓ Clock to Output
    - Asynchronous to Register
    - Register to Asynchronous
    - External Recovery
  - Pin to Pin
    - Input to Output
  - User Sets

From: *

To: *

Apply Filter | Store Filter | Reset Filter

| | Source Pin | Sink Pin | Delay (ns) | Slack (ns) | Arrival (ns) | Required (ns) | Recovery (ns) | Minimum Period (ns) | Skew (ns) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | regrst:CLK | reg2:CLR | 1.336 | 2.688 | 3.107 | 5.795 | 0.222 | 2.312 | 0.754 |
| 2 | regrst:CLK | reg1:CLR | 1.279 | 3.061 | 3.050 | 6.111 | 0.222 | 1.939 | 0.438 |

| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **From: regrst:CLK** | | | | | | | | |
| | **To: reg2:CLR** | | | | | | | | |
| | data required time | | | | | | 5.795 | | |
| | data arrival time | | | | - | | 3.107 | | |
| | slack | | | | | | 2.688 | | |
| | **Data arrival time calculation** | | | | | | | | |
| | clock | | | | | 0.000 | 0.000 | | |
| | regrst:CLK | Clock network | | | + | 1.771 | 1.771 | | r |
| | regrst:Q | cell | | ADLIB:DFN1C0 | + | 0.434 | 2.205 | 2 | r |
| | reg2:CLR | net | synreset | | + | 0.902 | 3.107 | | r |
| | data arrival time | | | | | | 3.107 | | |
| | **Data required time calculation** | | | | | | | | |
| | clock | Clock Constraint | | | | 5.000 | 5.000 | | |
| | reg2:CLK | Clock network | | | + | 1.017 | 6.017 | | r |
| | reg2:CLR | Library recovery time | | ADLIB:DFN1C0 | - | 0.222 | 5.795 | | |
| | data required time | | | | | | 5.795 | | |

# Datasheet Report

- Content
  - Pin Description
    - Pin location on the package
    - Port name
    - Type (input, output, inout, clock)
    - I/O Technology used
  - DC Timing Characteristics
    - Electrical parameters of each I/O technology (slew, output load, voltages,)
  - AC Timing Characteristics
    - External Timing Requirements
- New analysis view in the SmartTime Analyzer
- New report
  - Text format or CSV (Comma Separated Value)

# Datasheet: AC Timing Characteristics

- Maximum clock frequency for all external clocks
- External Setup/Recovery/Hold/Removal for each input ports with respect to external clocks
- Clock-to-out for output ports
- Input-to-Output for combinational paths

ONE CHIP is all you need

# Datasheet: Example

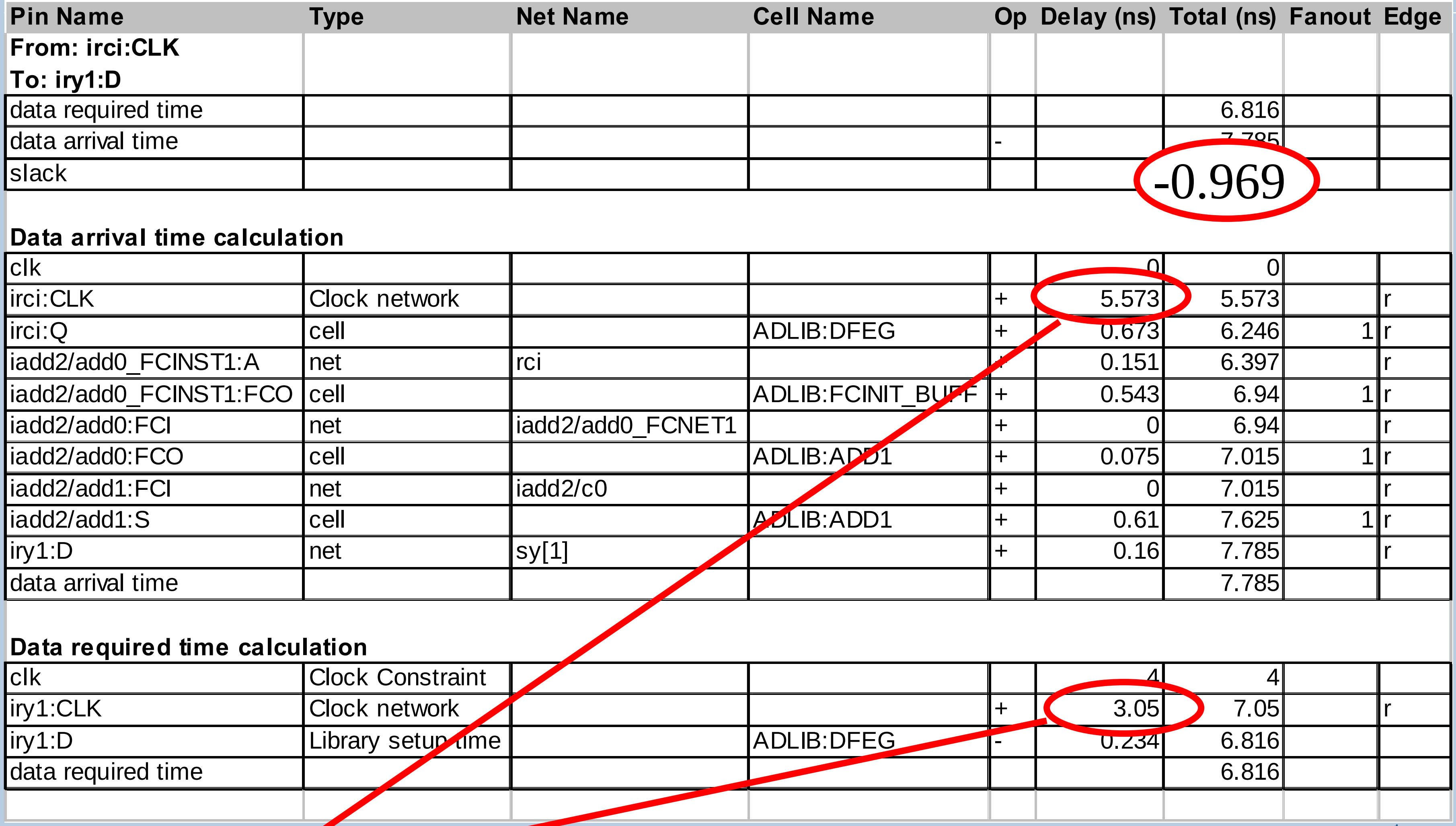
```
Pin Description
+-------+----------+--------+-----------+
| Name  | Location | Type   | Techno    |
+-------+----------+--------+-----------+
| a[0]  | J14      | Input  | LVCMOS15  |
| b[0]  | H15      | Input  | LVCMOS25  |
| reset | K1       | Input  | SSTL2I    |
| ci    | B8       | Input  | LVTTL (1) |
| clk   | R7       | Clock  | GTLP25    |
| y[0]  | C9       | Output | LVTTL (2) |
| co    | B7       | Output | LVTTL (3) |
| en    | L2       | Input  | PCI       |
+-------+----------+--------+-----------+

DC Electrical Characteristics
+-----------+------+----------+-------+-----------+------+--------+------+--------+
| Name      | Vcci | Resistor | Input | Hot       | Vccr | Output | Slew | Output |
|           | (V)  | Pull     | Delay | Swappable | (V)  | Drive  |      | Load   |
|           |      |          |       |           |      | (mA)   |      |        |
+-----------+------+----------+-------+-----------+------+--------+------+--------+
| GTLP25    | 2.5  |          | no    | yes       | 1    |        |      |        |
| LVCMOS15  | 1.5  | Up       | no    | yes       |      |        |      |        |
| LVCMOS25  | 2.5  | None     | no    | yes       |      |        |      |        |
| LVTTL (1) | 3.3  | None     | no    | yes       |      |        |      |        |
| LVTTL (2) | 3.3  | None     |       | yes       |      | 24     | Low  | 35     |
| LVTTL (3) | 3.3  | None     |       | yes       |      | 12     | High | 40     |
| PCI       | 3.3  |          | no    | no        |      |        |      |        |
| SSTL2I    | 2.5  |          | no    | yes       | 1.25 |        |      |        |
+-----------+------+----------+-------+-----------+------+--------+------+--------+
```

# Datasheet: Example

```
AC Electrical Characteristics
+-------------------+------------+--------+------------+--------+---------+------+
| Description       |            |        |            | Min    | Max     | Unit |
+-------------------+------------+--------+------------+--------+---------+------+
| Clock frequency   | clk        |        |            |        | 189.143 | MHz  |
| Clock period      | clk        |        |            | 5.287  |         | ns   |
| Setup time        | a[0]       | before | clk (rise) | -0.946 |         | ns   |
| Setup time        | b[0]       | before | clk (rise) | -2.642 |         | ns   |
| Setup time        | ci         | before | clk (rise) | -3.100 |         | ns   |
| Setup time        | reset      | before | clk (rise) | -0.096 |         | ns   |
| Hold time         | a[0]       | after  | clk (rise) | -1.278 |         | ns   |
| Hold time         | b[0]       | after  | clk (rise) | -2.062 |         | ns   |
| Hold time         | ci         | after  | clk (rise) | -2.241 |         | ns   |
| Hold time         | reset      | after  | clk (rise) | -0.429 |         | ns   |
| Recovery time     | reset      | before | clk (rise) | -0.266 |         | ns   |
| Removal time      | reset      | after  | clk (rise) | -0.429 |         | ns   |
| Propagation delay | clk (rise) | to     | co         | 3.545  | 7.420   | ns   |
| Propagation delay | clk (rise) | to     | y[0]       | 6.720  | 14.309  | ns   |
+-------------------+------------+--------+------------+--------+---------+------+
```

# Clock Network Details



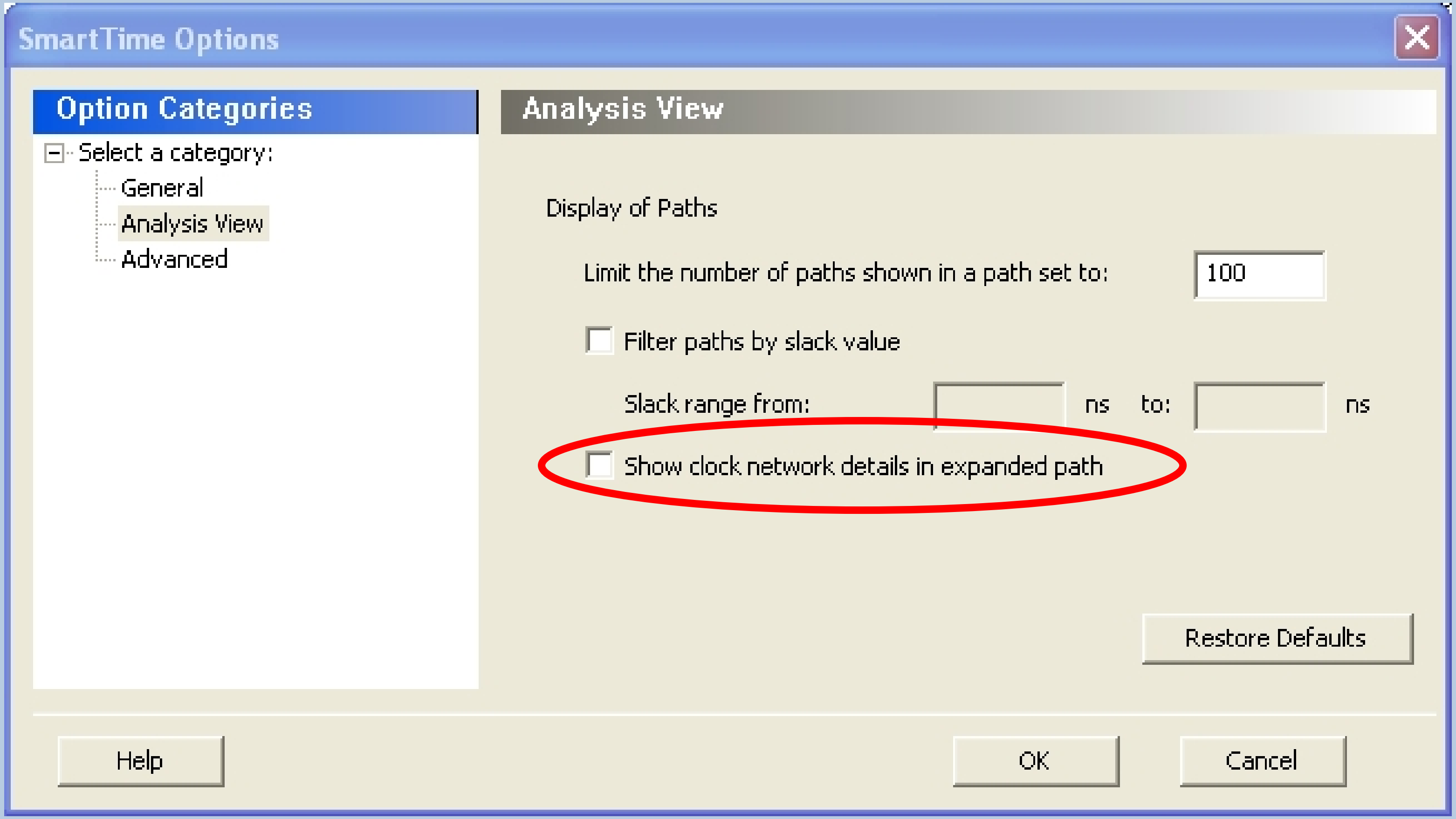
| Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|
| **From: irci:CLK**<br>**To: iry1:D** | | | | | | | | |
| data required time | | | | | | 6.816 | | |
| data arrival time | | | | - | | 7.785 | | |
| slack | | | | | | -0.969 | | |
| **Data arrival time calculation** | | | | | | | | |
| clk | | | | | 0 | 0 | | |
| irci:CLK | Clock network | | | + | 5.573 | 5.573 | | r |
| irci:Q | cell | | ADLIB:DFEG | + | 0.673 | 6.246 | 1 | r |
| iadd2/add0_FCINST1:A | net | rci | | + | 0.151 | 6.397 | | r |
| iadd2/add0_FCINST1:FCO | cell | | ADLIB:FCINIT_BUFF | + | 0.543 | 6.94 | 1 | r |
| iadd2/add0:FCI | net | iadd2/add0_FCNET1 | | + | 0 | 6.94 | | r |
| iadd2/add0:FCO | cell | | ADLIB:ADD1 | + | 0.075 | 7.015 | 1 | r |
| iadd2/add1:FCI | net | iadd2/c0 | | + | 0 | 7.015 | | r |
| iadd2/add1:S | cell | | ADLIB:ADD1 | + | 0.61 | 7.625 | 1 | r |
| iry1:D | net | sy[1] | | + | 0.16 | 7.785 | | r |
| data arrival time | | | | | | 7.785 | | |
| **Data required time calculation** | | | | | | | | |
| clk | Clock Constraint | | | | 4 | 4 | | |
| iry1:CLK | Clock network | | | + | 3.05 | 7.05 | | r |
| iry1:D | Library setup time | | ADLIB:DFEG | - | 0.234 | 6.816 | | |
| data required time | | | | | | 6.816 | | |

$$\text{Skew} = \boxed{5.573} - \boxed{3.05} = 2.523\ \text{ns}$$

ONE CHIP is all you need

# Clock Network Details

- Menu: Tools > Options



SmartTime Options

Option Categories

Select a category:
- General
- Analysis View
- Advanced

Analysis View

Display of Paths

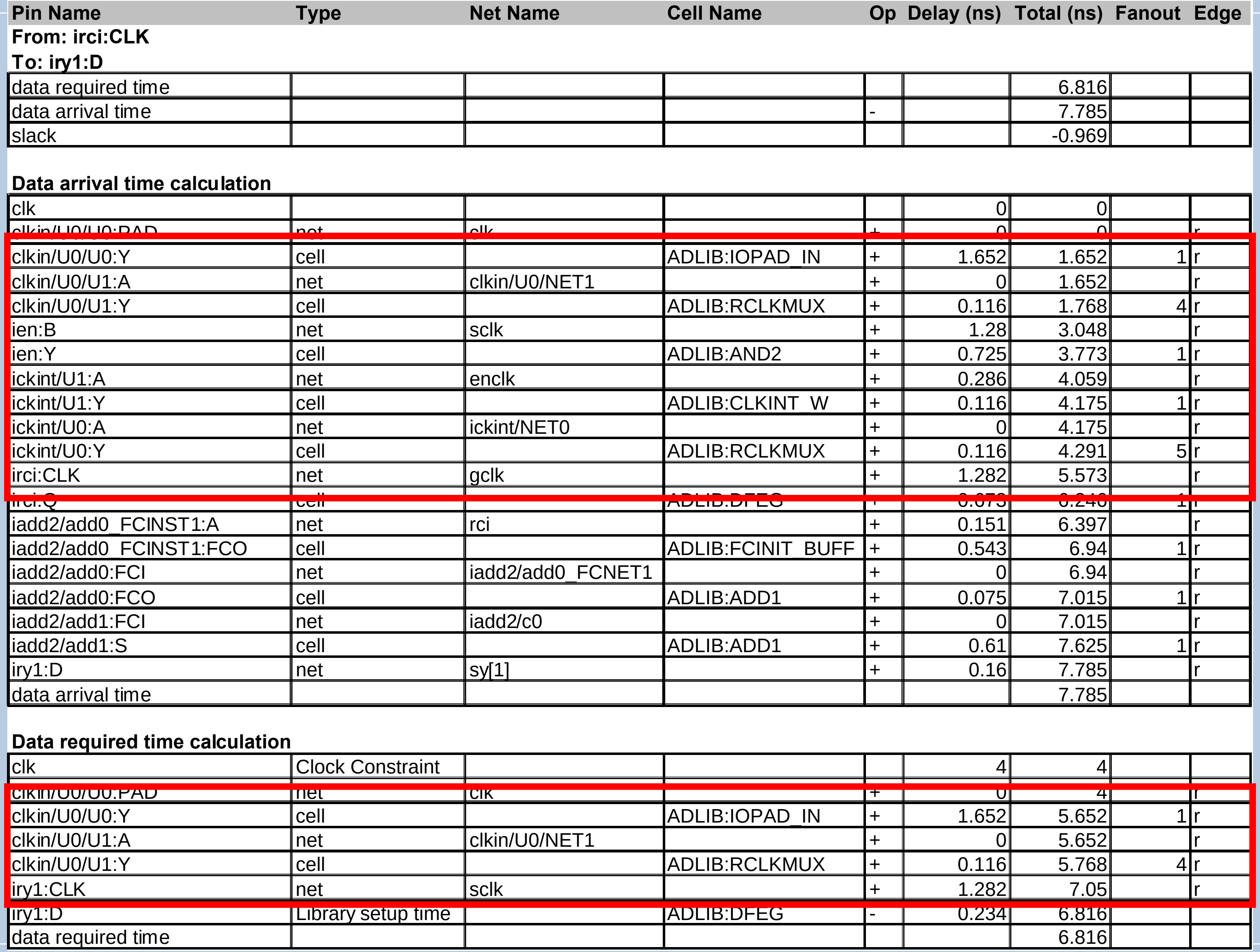
Limit the number of paths shown in a path set to: 100

□ Filter paths by slack value

Slack range from: ns to: ns

□ Show clock network details in expanded path

# Clock Network Details



| Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|
| **From: irci:CLK** | | | | | | | | |
| **To: iry1:D** | | | | | | | | |
| data required time | | | | | | 6.816 | | |
| data arrival time | | | | - | | 7.785 | | |
| slack | | | | | | -0.969 | | |

**Data arrival time calculation**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| clk | | | | | 0 | 0 | | |
| clkin/U0/U0:PAD | net | clk | | + | 0 | 0 | | r |
| clkin/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 1.652 | 1.652 | 1 | r |
| clkin/U0/U1:A | net | clkin/U0/NET1 | | + | 0 | 1.652 | | r |
| clkin/U0/U1:Y | cell | | ADLIB:RCLKMUX | + | 0.116 | 1.768 | 4 | r |
| ien:B | net | sclk | | + | 1.28 | 3.048 | | r |
| ien:Y | cell | | ADLIB:AND2 | + | 0.725 | 3.773 | 1 | r |
| ickint/U1:A | net | enclk | | + | 0.286 | 4.059 | | r |
| ickint/U1:Y | cell | | ADLIB:CLKINT_W | + | 0.116 | 4.175 | 1 | r |
| ickint/U0:A | net | ickint/NET0 | | + | 0 | 4.175 | | r |
| ickint/U0:Y | cell | | ADLIB:RCLKMUX | + | 0.116 | 4.291 | 5 | r |
| irci:CLK | net | gclk | | + | 1.282 | 5.573 | | r |
| irci:Q | cell | | ADLIB:DFEG | + | 0.673 | 6.246 | 1 | r |
| iadd2/add0_FCINST1:A | net | rci | | + | 0.151 | 6.397 | | r |
| iadd2/add0_FCINST1:FCO | cell | | ADLIB:FCINIT_BUFF | + | 0.543 | 6.94 | 1 | r |
| iadd2/add0:FCI | net | iadd2/add0_FCNET1 | | + | 0 | 6.94 | | r |
| iadd2/add0:FCO | cell | | ADLIB:ADD1 | + | 0.075 | 7.015 | 1 | r |
| iadd2/add1:FCI | net | iadd2/c0 | | + | 0 | 7.015 | | r |
| iadd2/add1:S | cell | | ADLIB:ADD1 | + | 0.61 | 7.625 | 1 | r |
| iry1:D | net | sy[1] | | + | 0.16 | 7.785 | | r |
| data arrival time | | | | | | 7.785 | | |

**Data required time calculation**

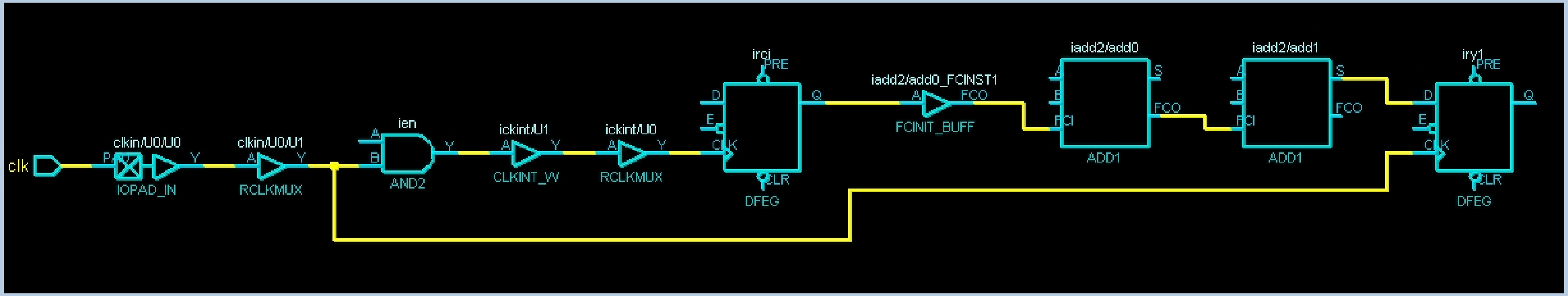
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| clk | Clock Constraint | | | | 4 | 4 | | |
| clkin/U0/U0:PAD | net | clk | | + | 0 | 4 | | r |
| clkin/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 1.652 | 5.652 | 1 | r |
| clkin/U0/U1:A | net | clkin/U0/NET1 | | + | 0 | 5.652 | | r |
| clkin/U0/U1:Y | cell | | ADLIB:RCLKMUX | + | 0.116 | 5.768 | 4 | r |
| iry1:CLK | net | sclk | | + | 1.282 | 7.05 | | r |
| iry1:D | Library setup time | | ADLIB:DFEG | - | 0.234 | 6.816 | | |
| data required time | | | | | | 6.816 | | |

**Source Clock Network**

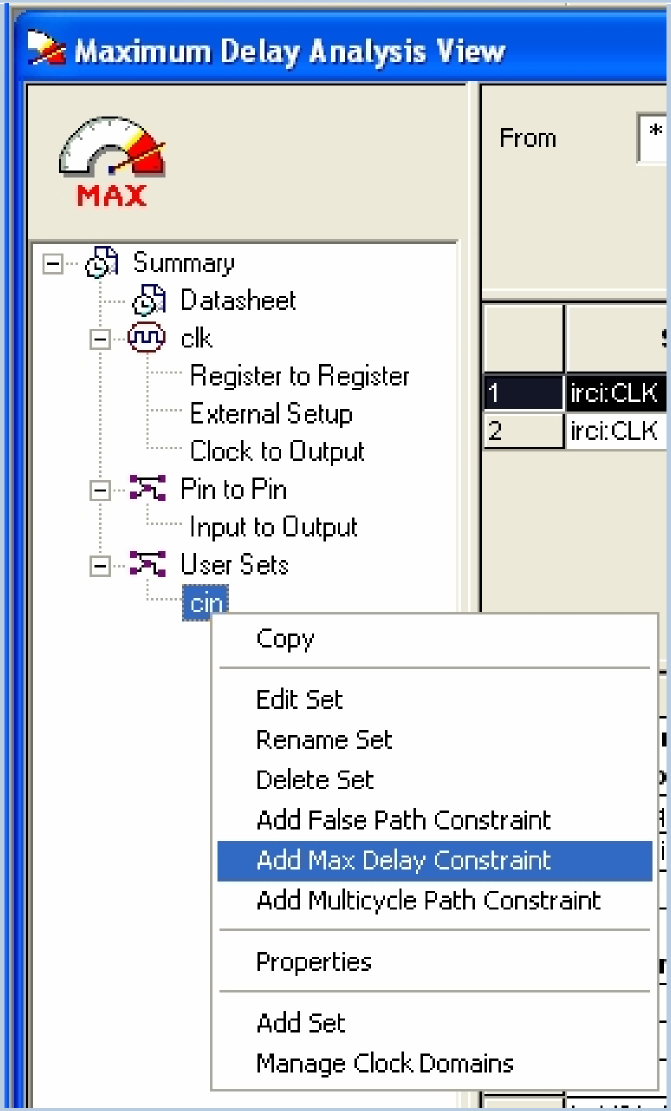
**Sink Clock Network**

# Clock Network Details

- Schematic



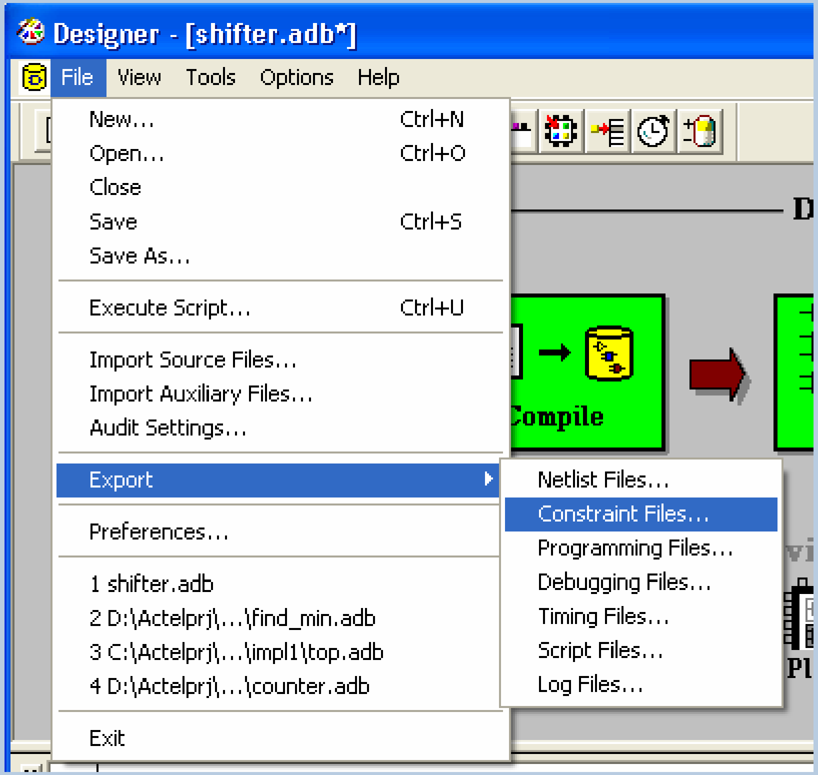
# Path Set Management

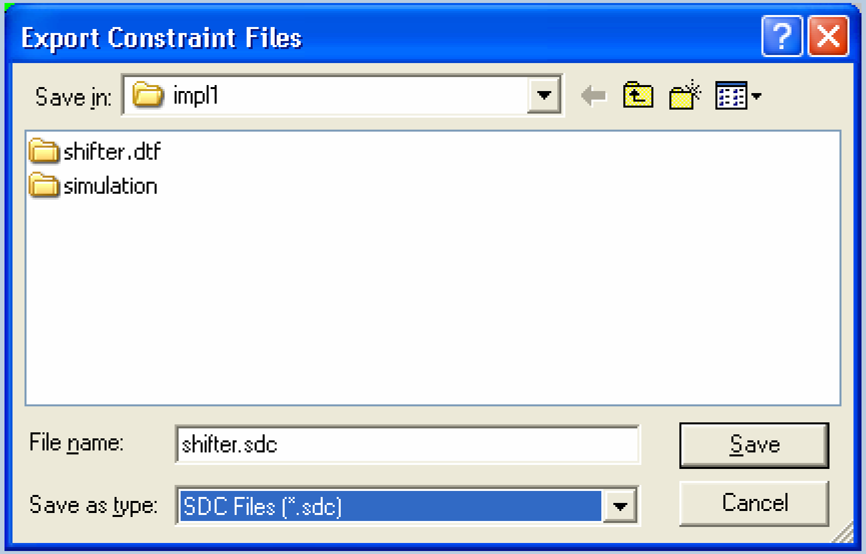


- Specify an exception for an entire set
- Modify existing sets
- Create/Edit/Delete sets using Tcl

# Exporting SDC Timing Constraints

- Constraints Entered in SmartTime GUI Can Be Exported from Designer





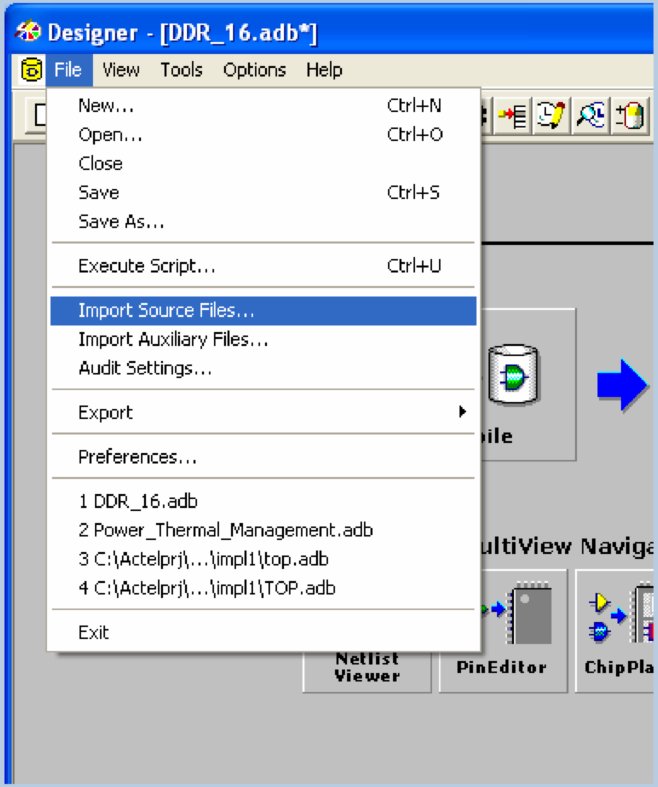
Save in: impl1

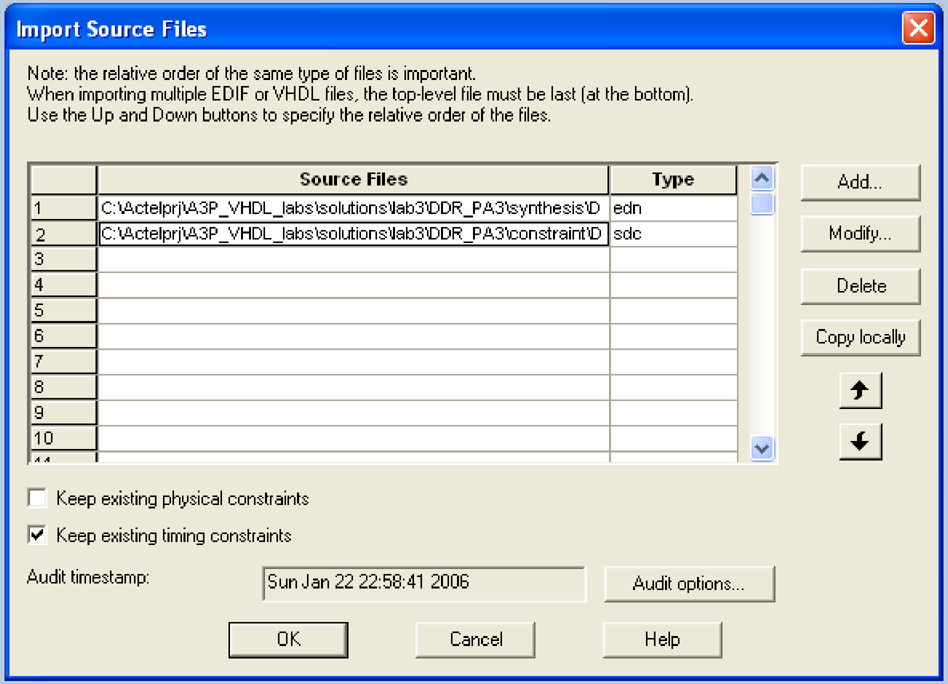
File name: shifter.sdc

Save as type: SDC Files (*.sdc)

# Importing SDC Timing Constraints

- SDC Timing Constraints Can Be Imported into Designer as Source File or Auxiliary File
  - **Source Files are Audited**





Note: the relative order of the same type of files is important.
When importing multiple EDIF or VHDL files, the top-level file must be last (at the bottom).
Use the Up and Down buttons to specify the relative order of the files.

| | Source Files | Type |
|---|---|---|
| 1 | C:\Actelprj\A3P_VHDL_labs\solutions\lab3\DDR_PA3\synthesis\D | edn |
| 2 | C:\Actelprj\A3P_VHDL_labs\solutions\lab3\DDR_PA3\constraint\D | sdc |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 | | |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |

☐ Keep existing physical constraints

☑ Keep existing timing constraints

Audit timestamp: Sun Jan 22 22:58:41 2006

# Constraint Recommendations

- Set Realistic Constraints

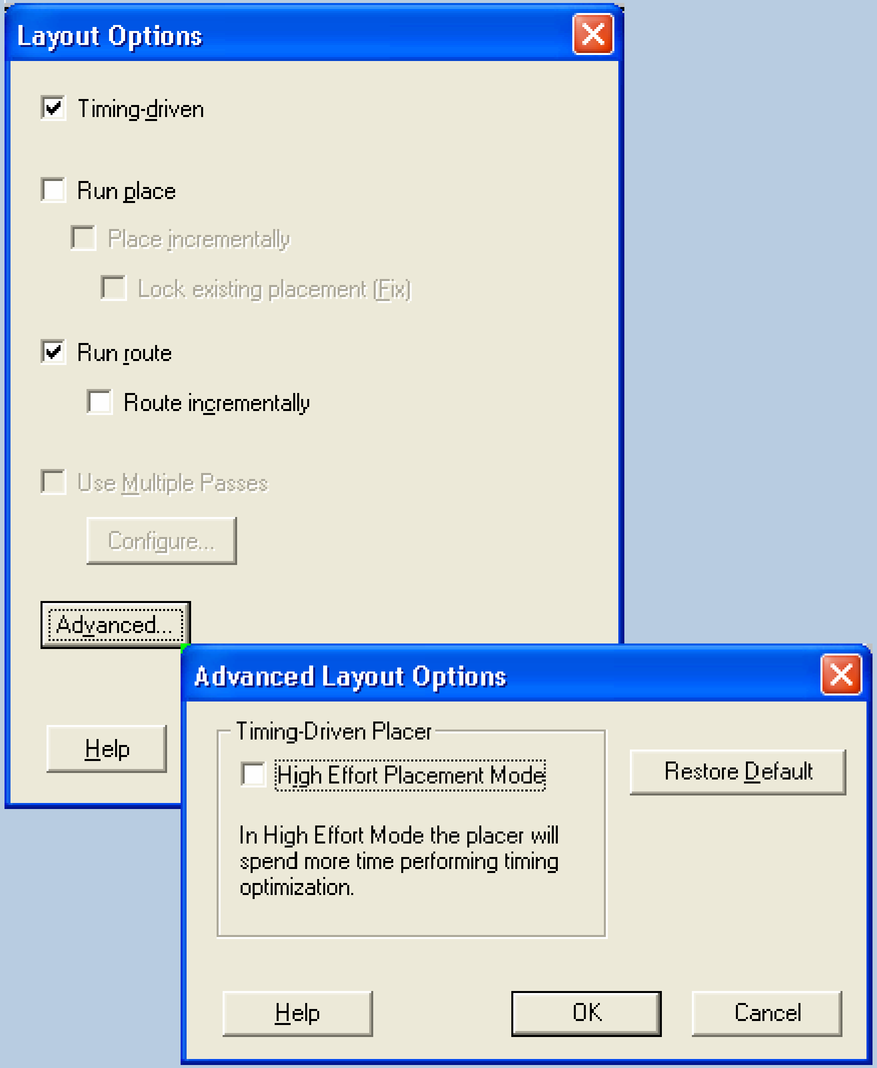
- Set Sufficient Constraints

- Don't Over constrain
  - **Improperly-Constrained Design Can Lead to Long Run Times, Multiple Iterations and/or Sub-optimal Results**
  - `max_delay` **Is Not** **Equivalent to Clock Constraint or Clock Period**

# Layout

- Assign Physical Locations to Unassigned I/Os
- Place Logic Modules
- Assign Routing Tracks to Nets
- Calculate Detailed Delays for All Paths

# Layout Options
## *ProASIC3\E*



**Layout Options**

- ☑ Timing-driven
- □ Run place
  - □ Place incrementally
    - □ Lock existing placement (Fix)
- ☑ Run route
  - □ Route incrementally
- □ Use Multiple Passes

**Advanced Layout Options**

Timing-Driven Placer

- □ High Effort Placement Mode

In High Effort Mode the placer will spend more time performing timing optimization.

- Layout Mode
  - **Timing-Driven: Constraints Defined in SmartTime**
    - **De-selecting Causes Standard Layout to be Used**
- Place and Route Tools
  - **Can Be Turned On or Off**
- Incremental Placement *and* Routing
- Multi Pass Layout Option
- Advanced Layout Options
  - **High Effort Placer**
- Known Limitations
  - **Router Cannot Run in Incremental Mode if there Has Been Change in Global Assignments**
    - **Users Must Manually Uncheck Incremental Routing Option and Re-run Layout**

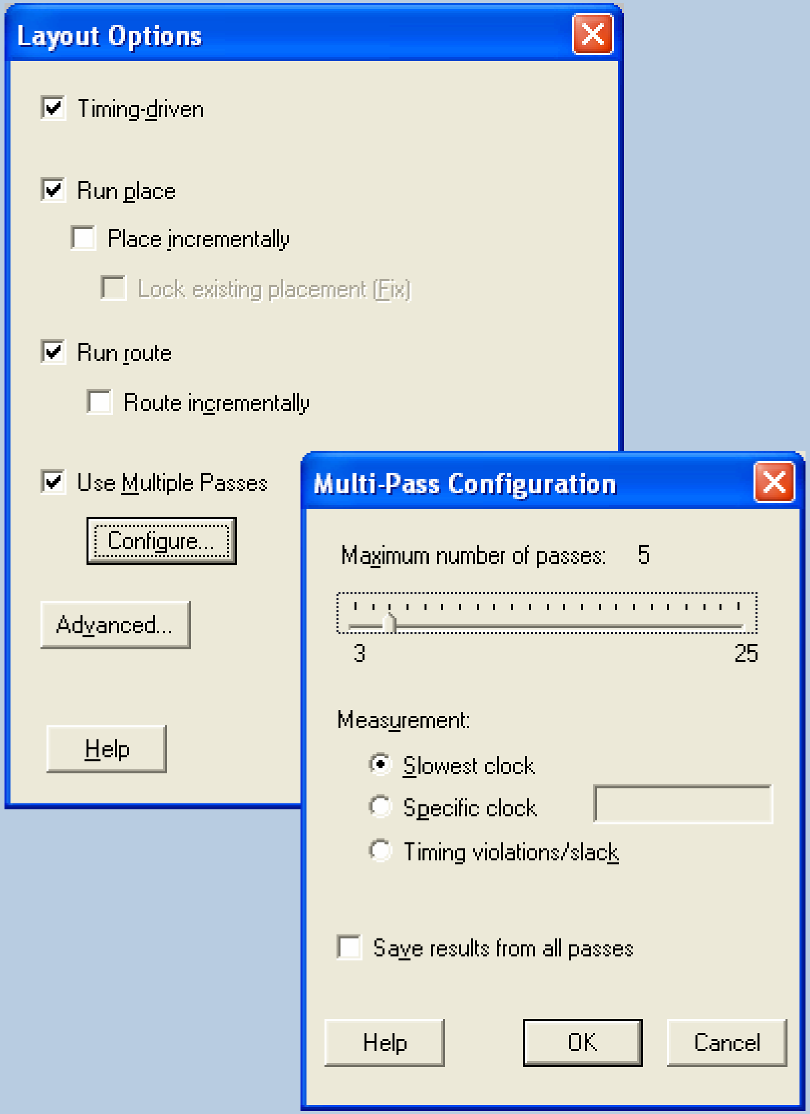
# Designer High Effort Placer
## *ProASIC3\E*

- "High Effort" timing-driven placer mode
  - Performs greater optimization of the placement at the expense of extra runtime
  - The objective is to further increase performance
- Placer is guided by highly detailed feedback from continuous timing evaluations
  - Based on new high speed timing analysis that operates using incremental changes in the placement algorithms
- Improvement over Designer 6.2
  - Additional 3% average QOR increase (total 10% QOR increase)
  - Reduced Runtime penalty (average is 2x vs. 3x – 4x)
- Initiated via Advanced Layout Options and Tcl

# ProASIC3\E Local Clock Assignment

- Finds and creates legal clock assignments for clock nets not already assigned by the user
- Runs automatically as part of layout
- Performs Auto-assignment of nets given certain criteria
  - **Runs when > 6 globals (or > 2 PLLs are detected)**
    - **Globals come from user netlist or PDC constraints**
      - ***CCC macro instantiation***
      - ***Global promotion through PDC constraints***
    - **If > 6 global nets, LCA will assign the global nets to**
      - ***Chip wide globals or***
      - ***Quadrant regions***
    - **The choice of chip wide globals or a quadrant region will depend on**
      - ***Fanout of the nets***
      - ***Resources and user constraints***
      - ***Shared loads***

# Layout Options
## *ProASIC<u>PLUS</u>*



Layout Options

☑ Timing-driven

☑ Run place

□ Place incrementally

□ Lock existing placement (Fix)

☑ Run route

□ Route incrementally

☑ Use Multiple Passes

Multi-Pass Configuration

Maximum number of passes: 5

Measurement:

● Slowest clock

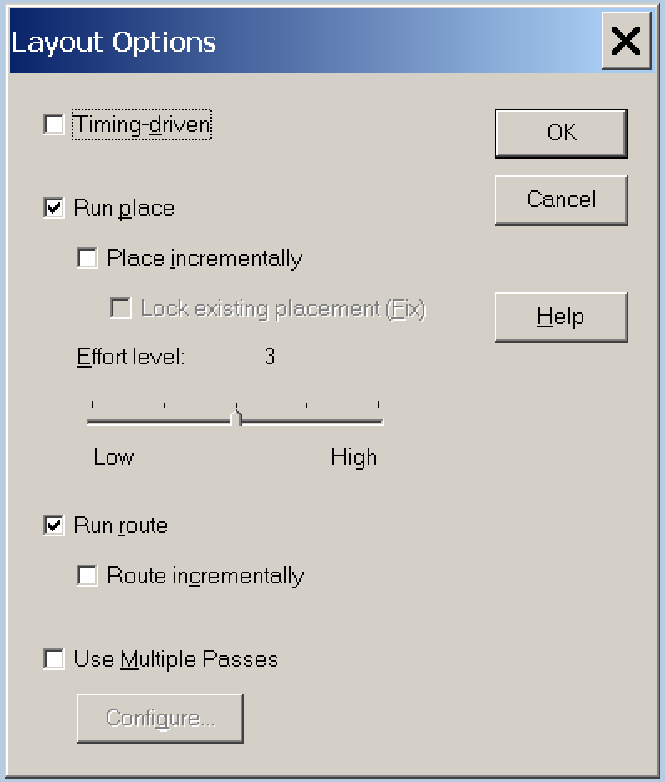
○ Specific clock

○ Timing violations/slack

□ Save results from all passes

- Layout Mode
  - **Timing-Driven: Constraints Defined in SmartTime**
    - **De-selecting Causes Standard Layout to be Used**
- Place and Route Tools
  - **Can Be Turned On or Off**
- Incremental Placement *and* Routing
  - **Lock Existing Placement: Treats All Unchanged Macros as Fixed Placements**
- Multiple Passes
  - **P&R Runs Multiple Times**
    - **Specify:**
      - ***Number of Iterations***
      - ***What to Optimize (Specific Clock, Timing Violations, etc.)***
      - ***Which Results to Save (Best or All)***

# Layout Options
*Axcelerator*



Layout Options

□ Timing-driven

☑ Run place

□ Place incrementally

□ Lock existing placement (Fix)

Effort level: 3

☑ Run route

□ Route incrementally

□ Use Multiple Passes

## Layout Mode

- Timing-Driven: Constraints Defined in SmartTime
  - De-selecting Causes Standard Layout to Be Used

## Place and Route Tools

- Can Be Turned On or Off

## Incremental Placement *and* Routing

- Lock Existing Placement:  Treats All Unchanged Macros as Fixed Placements

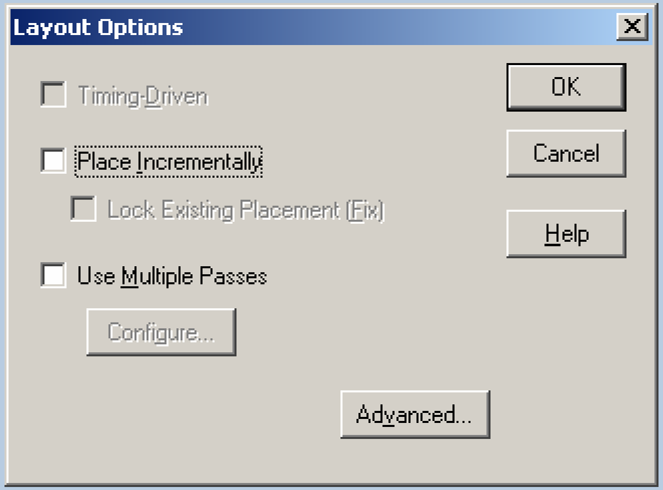
## Placement Effort Level

- Provides Degree of Control over Timing-Driven Placement Engine
- Range is from “Low” to “High”

## Multiple Passes

- P&R Runs Multiple Times

# Layout Modes
*SX Architecture*



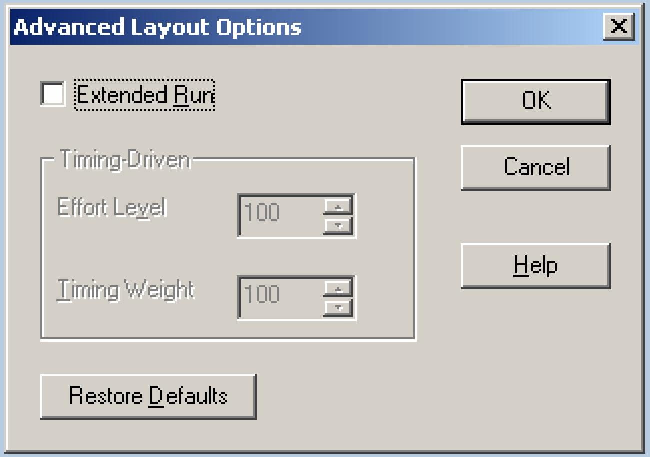
Layout Options

☐ Timing-Driven

☐ Place Incrementally

☐ Lock Existing Placement (Fix)

☐ Use Multiple Passes



Advanced Layout Options

☐ Extended Run

Timing-Driven

Effort Level: 100

Timing Weight: 100

## Layout Mode

- Timing-Driven: Constraints Defined in SmartTime (SX-A) or Timer (SX)
  - De-selecting Timing-Driven Layout Selects Standard Layout

## Incremental Placement

- Lock Existing Placement: Treats All Unchanged Macros as Fixed Placements
  - De-selecting Allows Placer to Relocate Unchanged Macros if Necessary

## Multiple Passes

- P&R Runs Multiple Times

## Advanced Options Allow Additional Control of Timing-driven Placement Engine

- SX, SXA and eX Families

# Advanced Layout Options
*SX Architecture*

## Extended Run

- Directs Layout to Use Larger Number of Iterations during Optimization to Improve Layout Quality
  - Causes Layout to Run up to 5 Times Longer

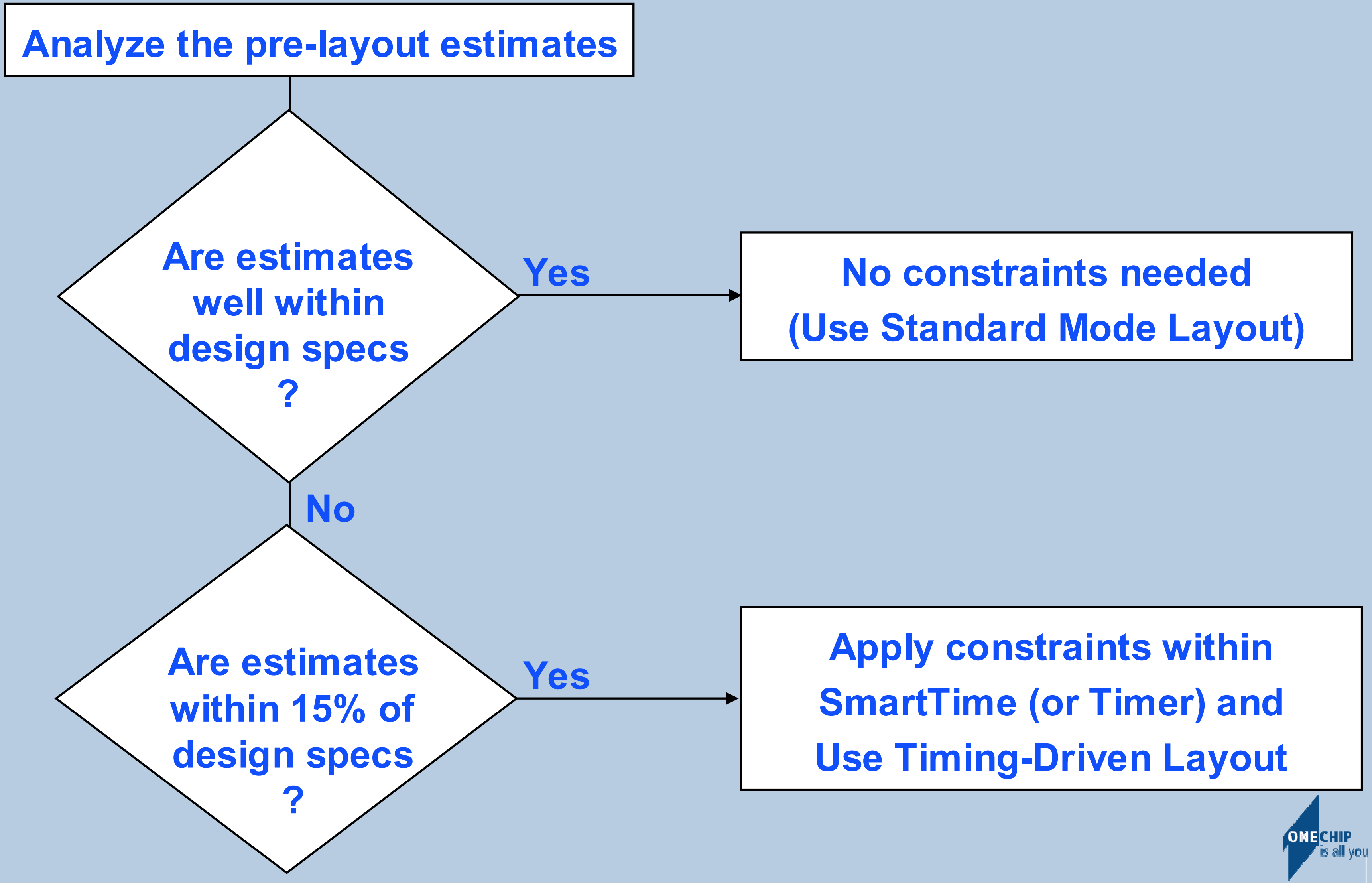
## Effort Level

- Specifies Duration of Timing-driven Phase of Optimization during Layout as Percentage of Default Duration
  - Default Value is 100
  - Selectable Range from 25 to 500
- Reducing Effort Level also Reduces Run Time of Timing-driven Place and Route (TDPR).
  - With Effort Level of 25, TDPR Is Almost Four Times Faster than Default of 100
    - *However, with Fewer Iterations Performance May Suffer*
  - Routability May or May Not Be Affected

# Advanced Layout Options (cont.)
## *SX Architecture*

- Timing Weight
  - Setting this Option Changes Weight of Timing Objective Function
    - Recommended Range: 10 - 150 (Default is 100)
    - Bias TDPR in Favor of either Routability or Performance
  - Weight Is Specified as Percentage of Default Weight
    - Value of 100 Has No Effect
    - Value Less than 100 – More Emphasis on Routability and Less on Performance
      - *Appropriate for Design that Fails to Route with TDPR*
    - Value Higher than 100 – More Emphasis on Performance
      - *BUT … Very High Value of Timing Weight Might Degrade Performance!*

# Which Layout Mode to Use?



Analyze the pre-layout estimates

Are estimates well within design specs ?

Yes

No constraints needed (Use Standard Mode Layout)

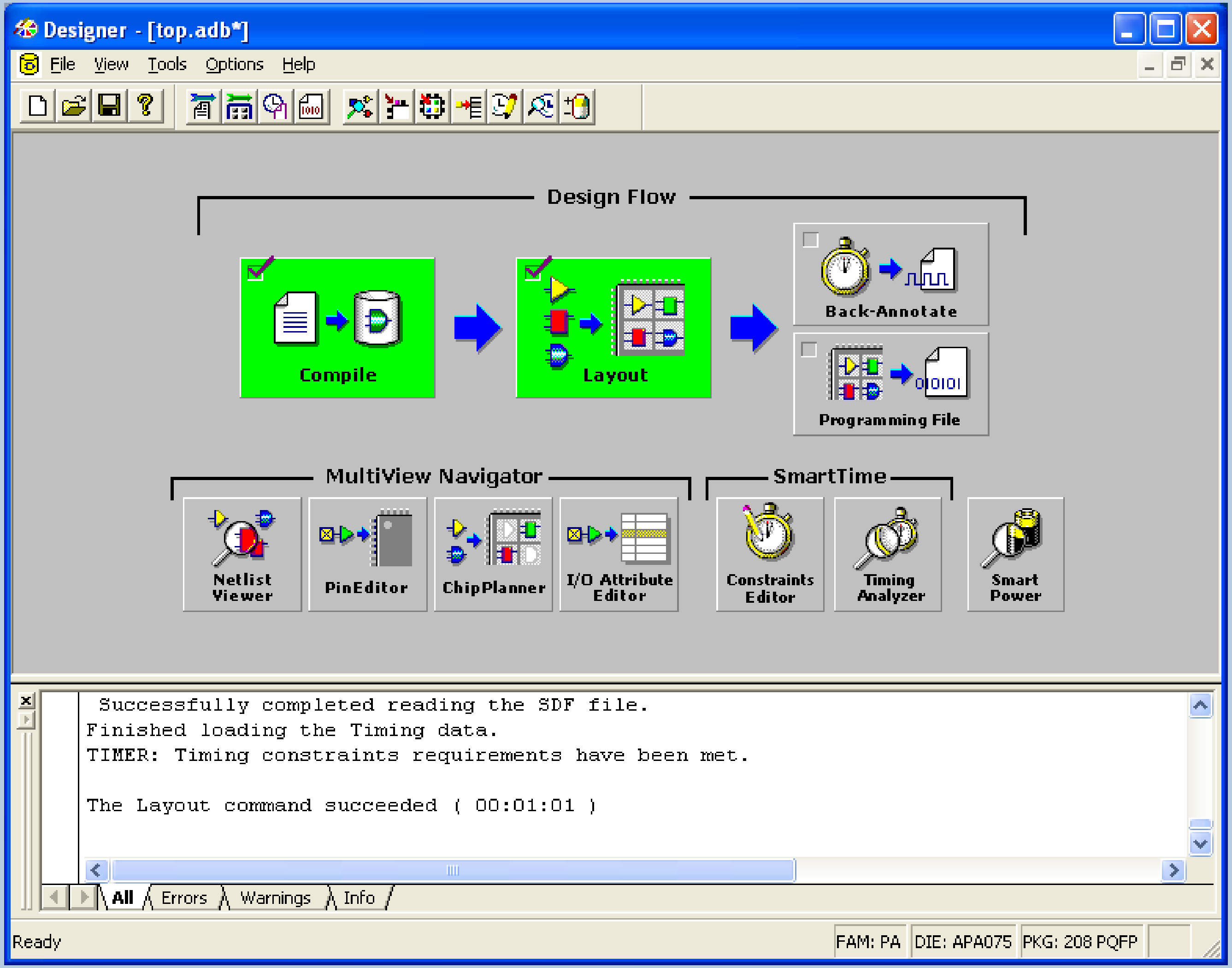
No

Are estimates within 15% of design specs ?

Yes

Apply constraints within SmartTime (or Timer) and Use Timing-Driven Layout

# Completed Layout

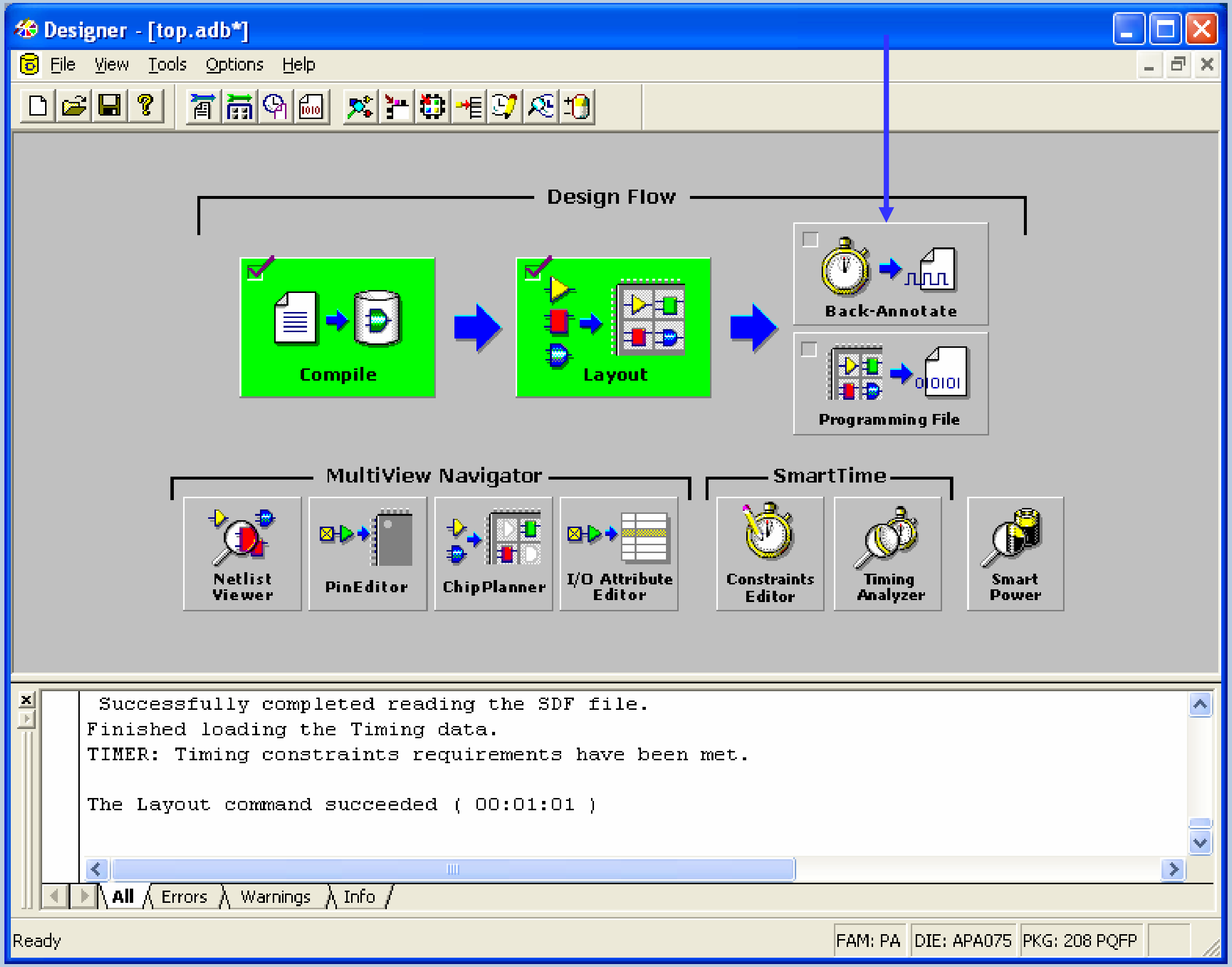


```
 Successfully completed reading the SDF file.
Finished loading the Timing data.
TIMER: Timing constraints requirements have been met.

The Layout command succeeded ( 00:01:01 )
```

# Exporting SDF File

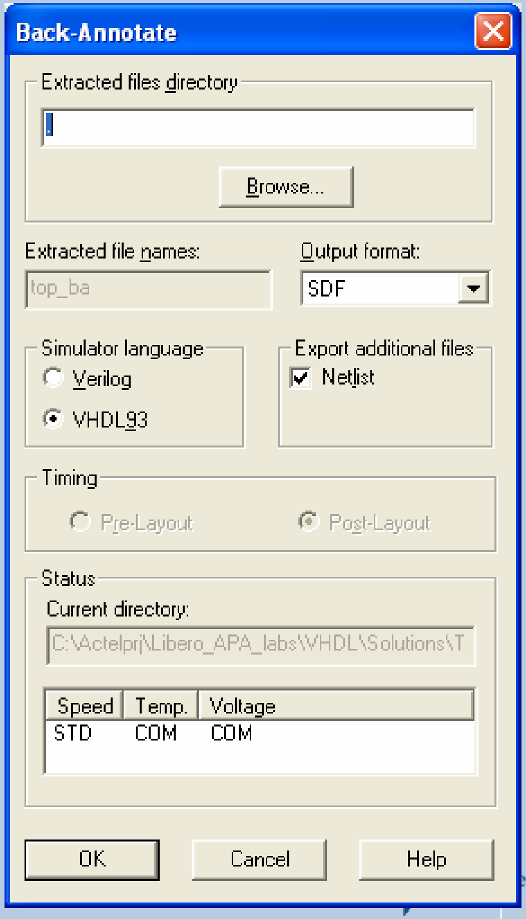
Extract Timing delays
for post-layout simulation



```
 Successfully completed reading the SDF file.
Finished loading the Timing data.
TIMER: Timing constraints requirements have been met.

The Layout command succeeded ( 00:01:01 )
```

Ready | FAM: PA | DIE: APA075 | PKG: 208 PQFP



Extracted files directory:

Extracted file names: top_ba

Output format: SDF

Simulator language: ○ Verilog ● VHDL93

Export additional files: ☑ Netlist

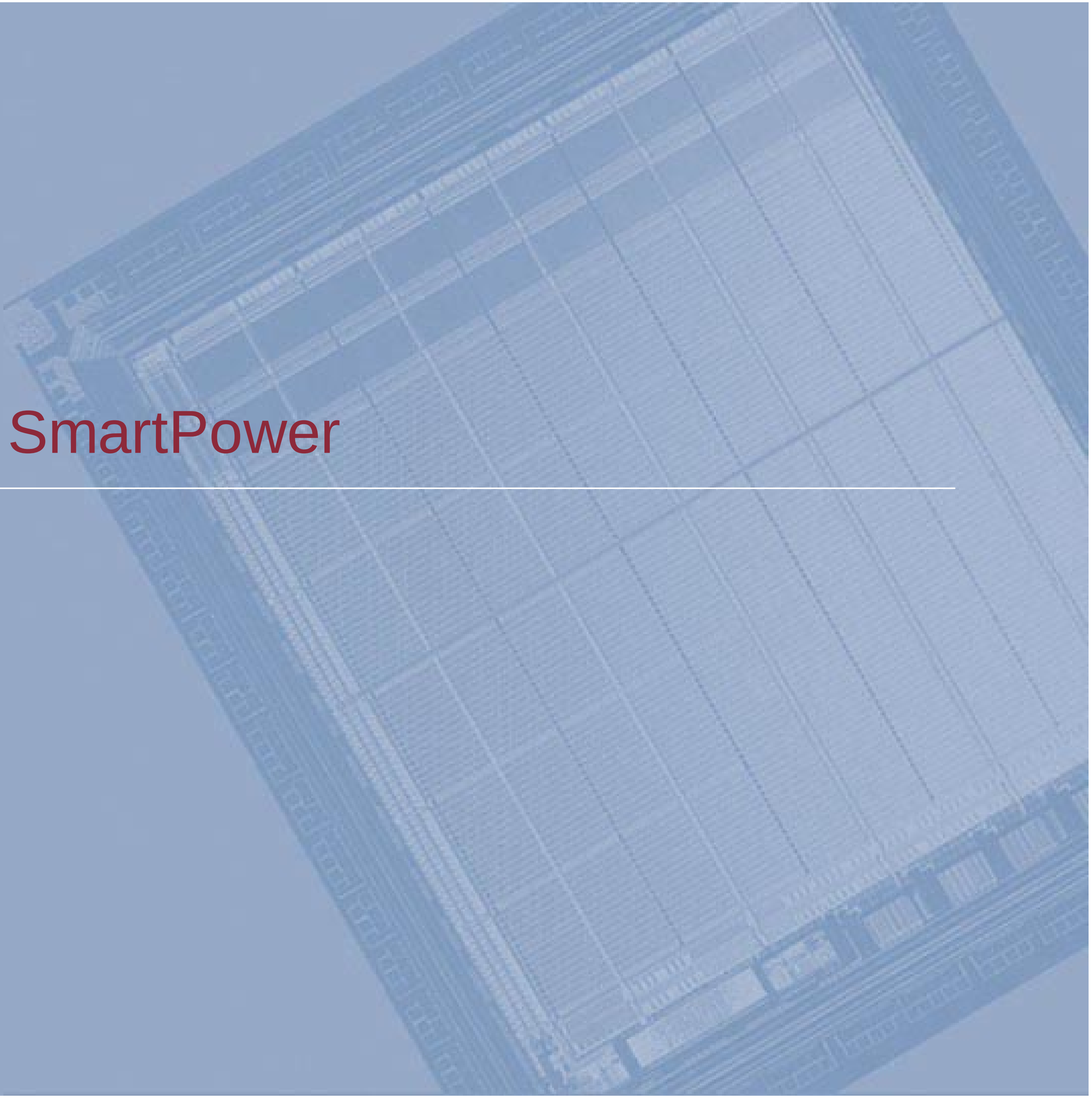
Timing: ○ Pre-Layout ● Post-Layout

Status

Current directory: C:\Actelprj\Libero_APA_labs\VHDL\Solutions\T

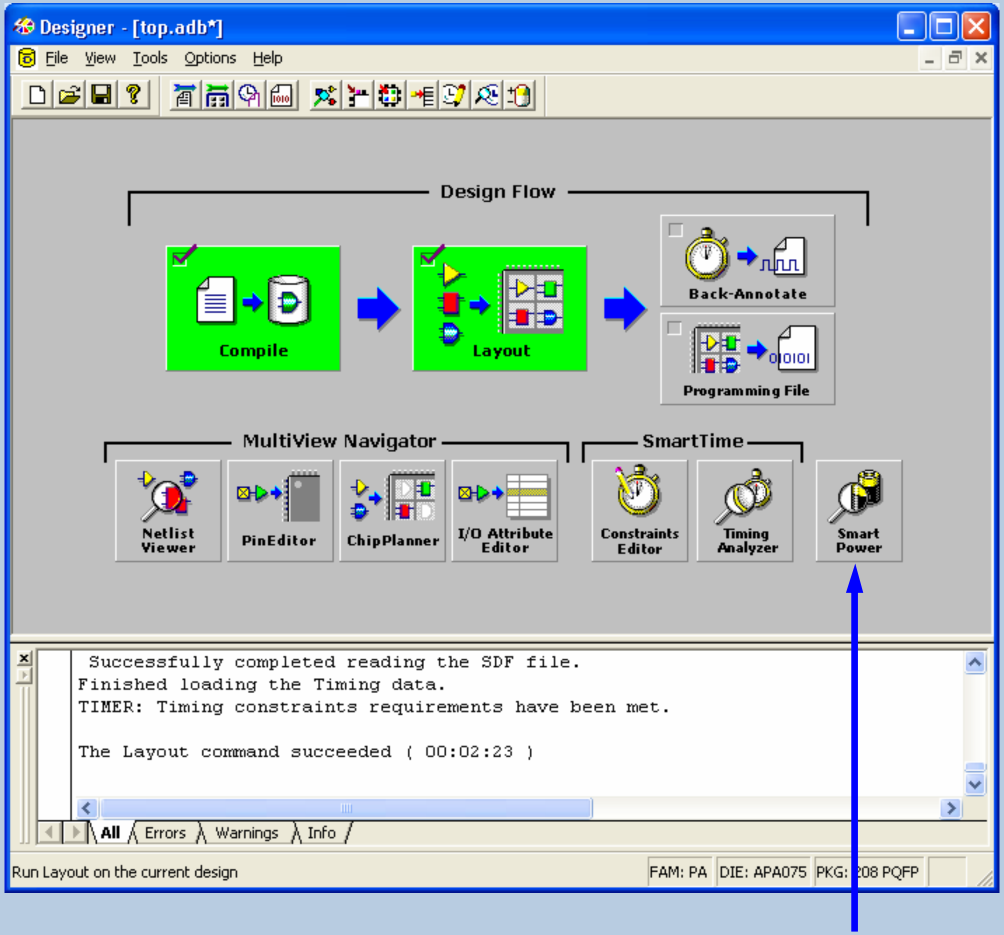
| Speed | Temp. | Voltage |
|---|---|---|
| STD | COM | COM |

# SmartPower



# SmartPower

- SmartPower Supports Fusion, ProASIC3/E, ProASIC$^{PLUS}$, ProASIC and Axcelerator
  - **SmartPower Icon Not Visible for other Families**
- SmartPower Report Contains Clock Domains, Set of Pins, and Annotated Pins
- Detailed Information Available in Designer Documentation
  - **SmartPower.pdf**



```
 Successfully completed reading the SDF file.
Finished loading the Timing data.
TIMER: Timing constraints requirements have been met.

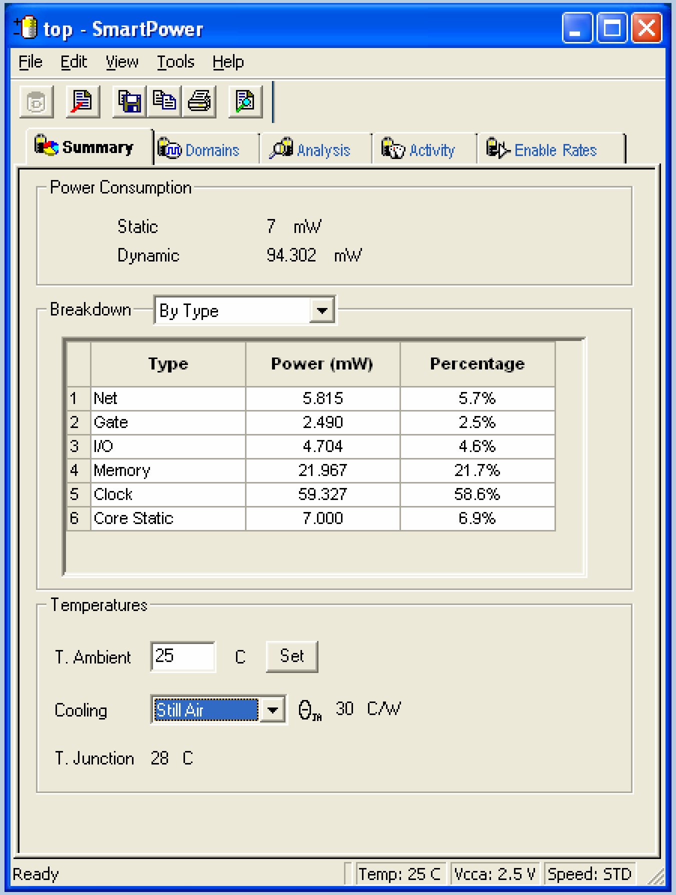
The Layout command succeeded ( 00:02:23 )
```

Run Layout on the current design | FAM: PA | DIE: APA075 | PKG: 208 PQFP

SmartPower icon

# SmartPower GUI

- 5 Display Tabs
  - Summary
    - Total Static and Dynamic Power of Design
    - Average Switching Activity of Clock Pins and Data Pins of Selected Clock Domain
    - Impact of Power Consumption on Junction Temperature for Given Cooling Scenario
  - Domains
    - Shows List of Existing Clock Domains with their Corresponding Frequencies
  - Analysis
    - Provides Detailed Hierarchical Reports of Dynamic Power Consumption
  - Activity
    - Allows Entry of Switching Activity Information for Clock and Data Inputs in Design
  - Enable Rates
    - Specify Enable Rates for each Tri-state and Bi-Directional I/O



Power Consumption

Static 7 mW

Dynamic 94.302 mW

Breakdown: By Type

| | Type | Power (mW) | Percentage |
|---|---|---|---|
| 1 | Net | 5.815 | 5.7% |
| 2 | Gate | 2.490 | 2.5% |
| 3 | I/O | 4.704 | 4.6% |
| 4 | Memory | 21.967 | 21.7% |
| 5 | Clock | 59.327 | 58.6% |
| 6 | Core Static | 7.000 | 6.9% |

Temperatures

T. Ambient: 25 C Set

Cooling: Still Air $\theta_{JA}$ 30 C/W

T. Junction 28 C

Ready | Temp: 25 C | Vcca: 2.5 V | Speed: STD

# SmartPower Summary Tab

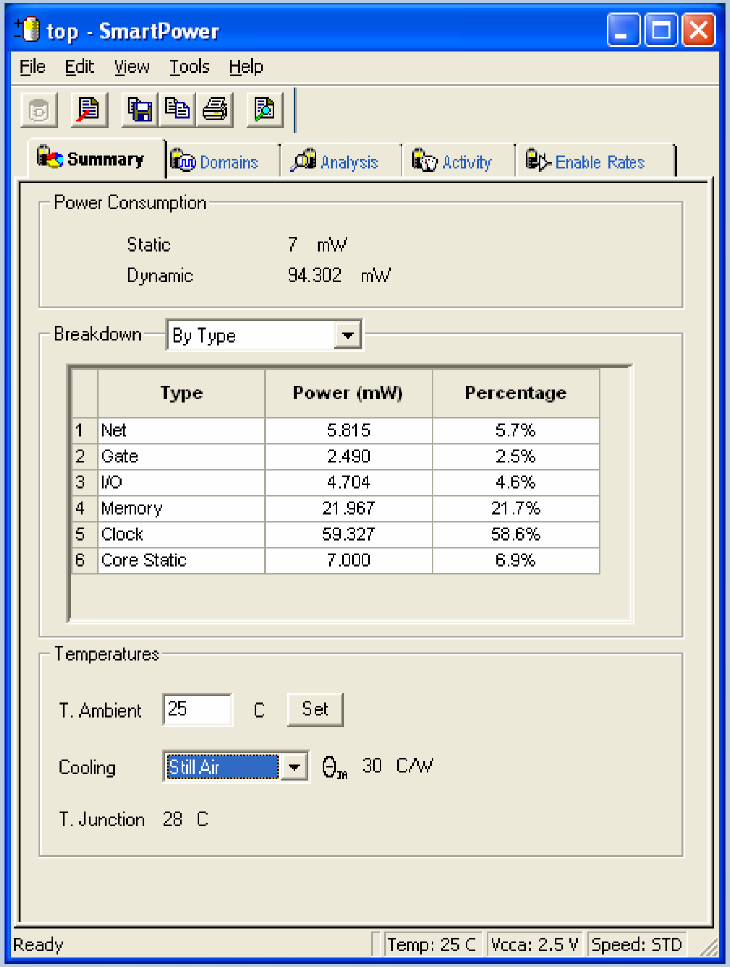
- Displays:
  - Static and Dynamic Power
  - Junction Temperature

Design Level Power Summary

Ambient Temp

Cooling Type

Calculated Junction Temp



Power Consumption

Static 7 mW

Dynamic 94.302 mW

Breakdown: By Type

|   | Type | Power (mW) | Percentage |
|---|---|---|---|
| 1 | Net | 5.815 | 5.7% |
| 2 | Gate | 2.490 | 2.5% |
| 3 | I/O | 4.704 | 4.6% |
| 4 | Memory | 21.967 | 21.7% |
| 5 | Clock | 59.327 | 58.6% |
| 6 | Core Static | 7.000 | 6.9% |

Temperatures

T. Ambient 25 C Set

Cooling Still Air $\theta_{JA}$ 30 C/W

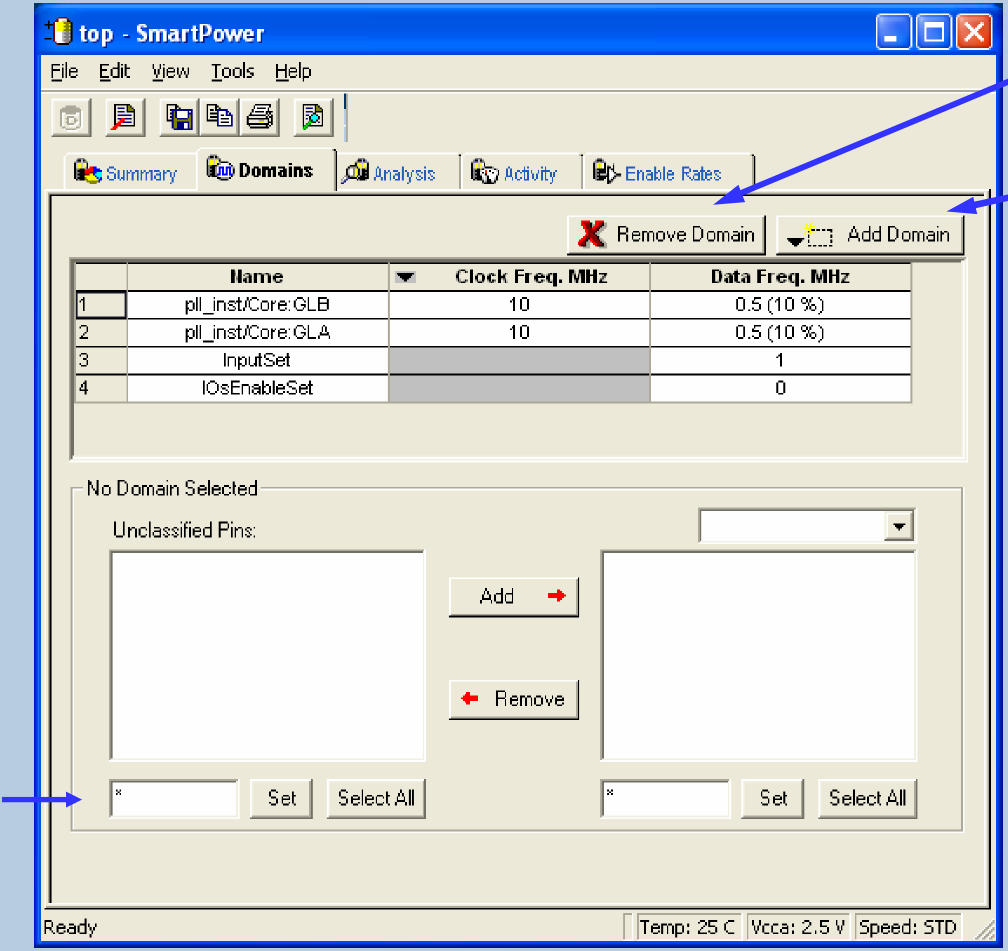
T. Junction 28 C

Ready | Temp: 25 C | Vcca: 2.5 V | Speed: STD

ONE CHIP is all you need

# SmartPower Domains Tab

- Shows Clock Domains with their Corresponding Frequencies



|  | Name | Clock Freq. MHz | Data Freq. MHz |
|---|---|---|---|
| 1 | pll_inst/Core:GLB | 10 | 0.5 (10 %) |
| 2 | pll_inst/Core:GLA | 10 | 0.5 (10 %) |
| 3 | InputSet |  | 1 |
| 4 | IOsEnableSet |  | 0 |

No Domain Selected

Unclassified Pins:

*

*

Ready

Temp: 25 C

Vcca: 2.5 V

Speed: STD

Delete selected domain

Create New Domain

Domain management window – add domains or select an existing domain

Pin management window - add pin to the current domain

Filter Boxes

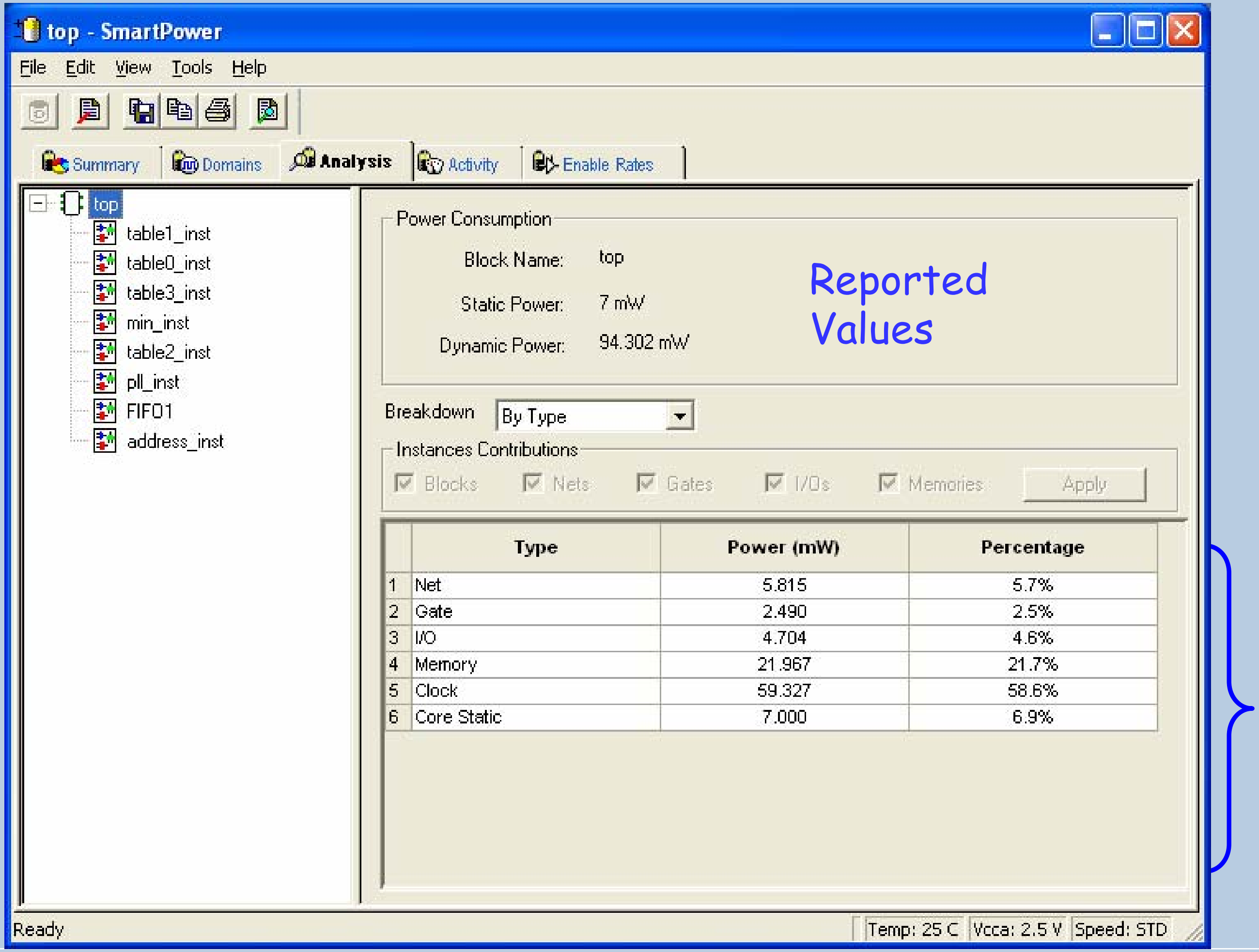
# SmartPower Notes

- Design must be in post-layout state to launch SmartPower
  - **Designer will run layout if SmartPower is launched in pre-layout state**
- When SmartPower is launched the first time, all clock domains are assigned a frequency of 10 MHz and all data frequencies are set to 1 MHz.
- Specify true clock and data rates to accurately estimate power consumption.

ONECHIP is all you need

# SmartPower
*Analysis Tab*

- Provides Detailed Hierarchical Reports of Dynamic Power Consumption



Power Consumption

Block Name: top

Static Power: 7 mW

Dynamic Power: 94.302 mW

Breakdown: By Type

Instances Contributions

☑ Blocks ☑ Nets ☑ Gates ☑ I/Os ☑ Memories Apply

| | Type | Power (mW) | Percentage |
|---|---|---|---|
| 1 | Net | 5.815 | 5.7% |
| 2 | Gate | 2.490 | 2.5% |
| 3 | I/O | 4.704 | 4.6% |
| 4 | Memory | 21.967 | 21.7% |
| 5 | Clock | 59.327 | 58.6% |
| 6 | Core Static | 7.000 | 6.9% |

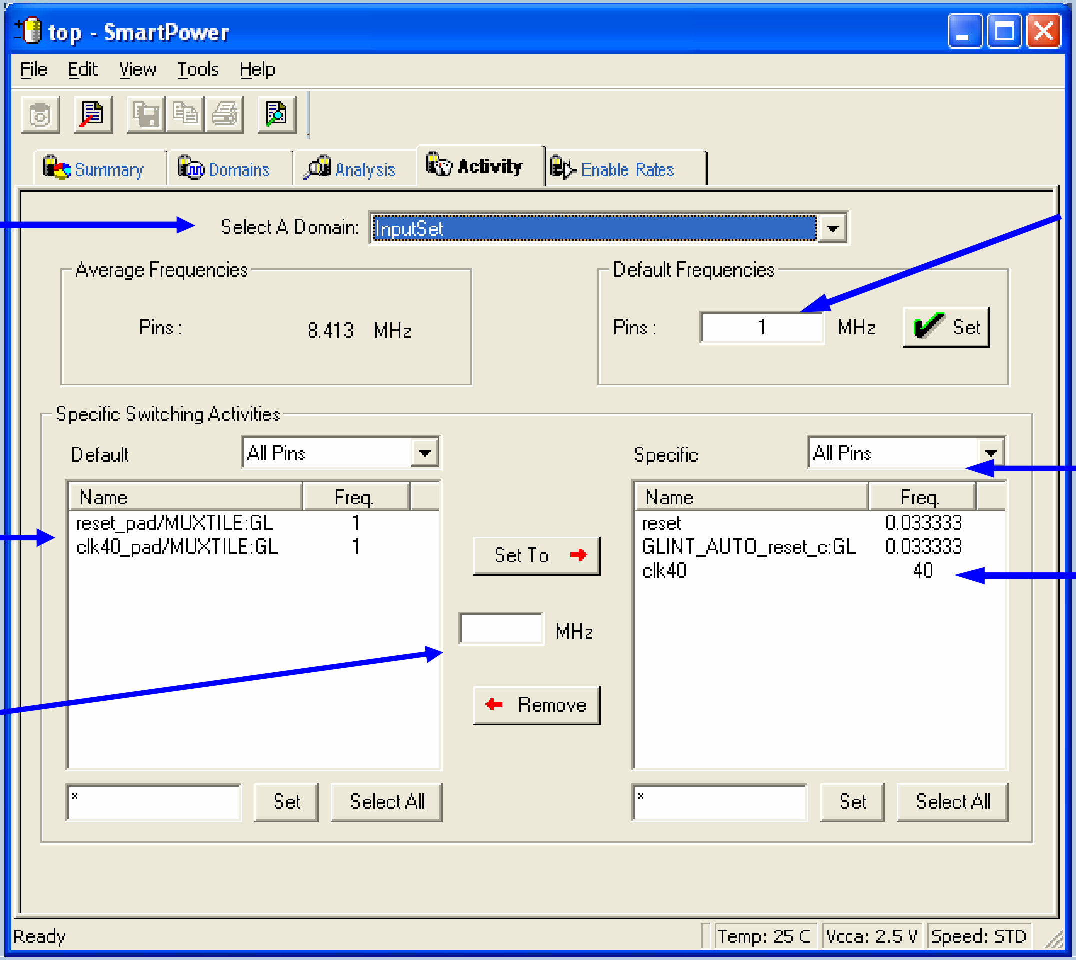
Hierarchy Instances Window

Reported Values

Report Window

# SmartPower Activity Tab

- Allows Entry of Switching Activity Information on Interconnects of Design



Select A Domain: InputSet

Average Frequencies

Pins : 8.413 MHz

Default Frequencies

Pins : 1 MHz ✓ Set

Specific Switching Activities

Default: All Pins

| Name | Freq. |
|---|---|
| reset_pad/MUXTILE:GL | 1 |
| clk40_pad/MUXTILE:GL | 1 |

Specific: All Pins

| Name | Freq. |
|---|---|
| reset | 0.033333 |
| GLINT_AUTO_reset_c:GL | 0.033333 |
| clk40 | 40 |

Ready | Temp: 25 C | Vcca: 2.5 V | Speed: STD

Selected Clock Domain

Global Frequency

Non-Annotated Pins

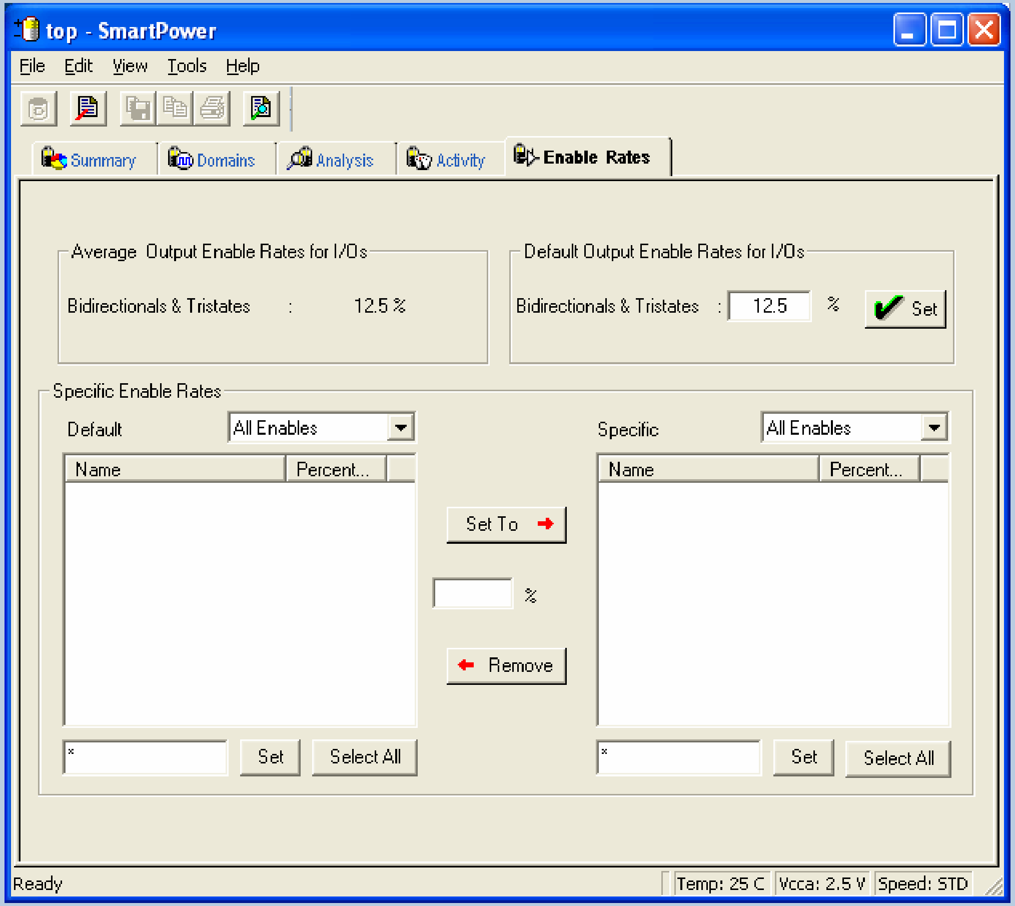
Pin Type

Annotated Pins

Specified Frequency

# SmartPower Enable Rates Tab

- Specify the Output Enable Rate of each tri-state and bidirectional I/O
  - **The enable rate is the percent of time that the I/O is driving**



top - SmartPower

Average Output Enable Rates for I/Os

Bidirectionals & Tristates : 12.5 %

Default Output Enable Rates for I/Os

Bidirectionals & Tristates : 12.5 %

Specific Enable Rates

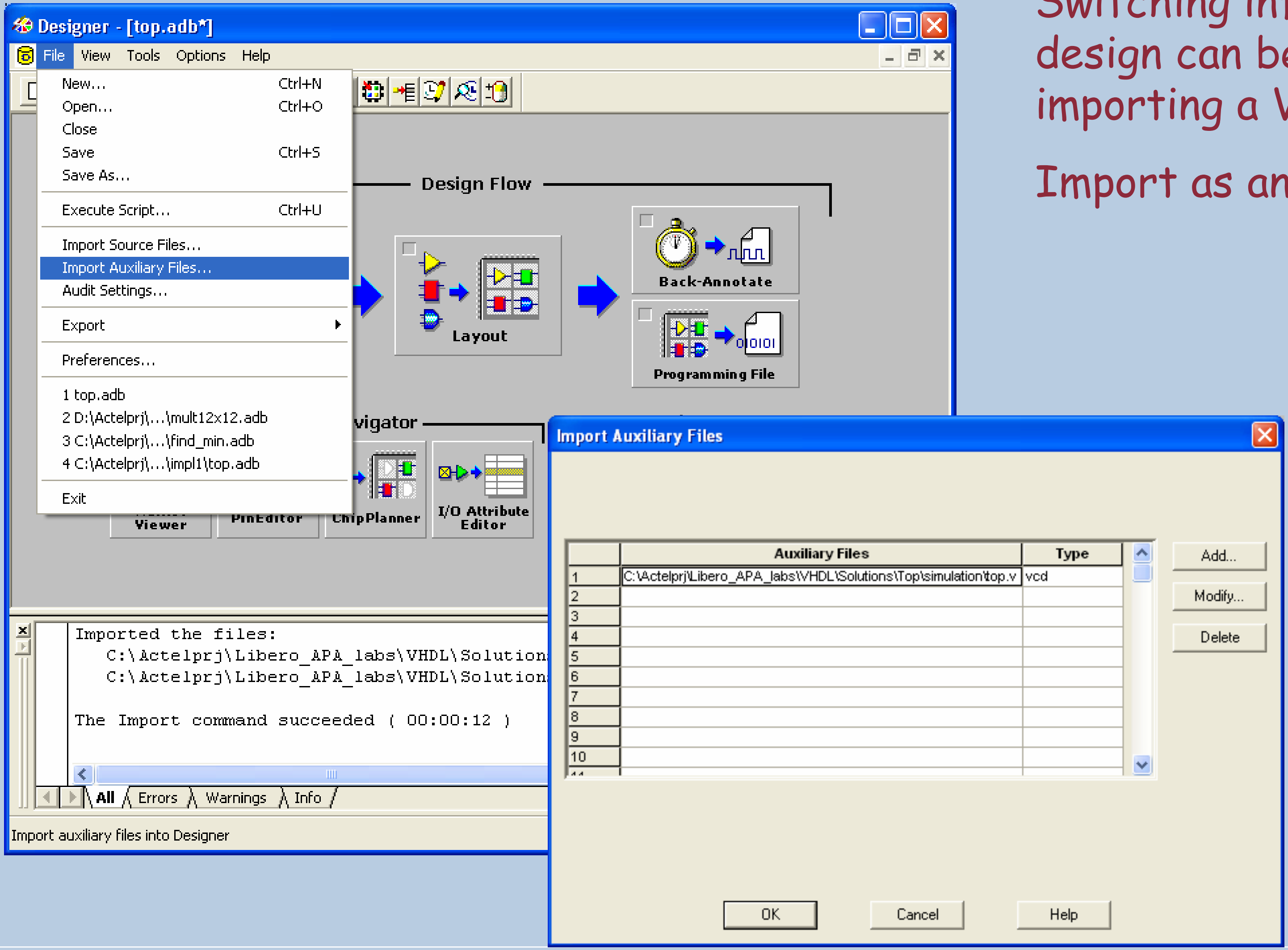
Default: All Enables

Specific: All Enables

Ready | Temp: 25 C | Vcca: 2.5 V | Speed: STD

# SmartPower

## *Importing a VCD File*



```
Imported the files:
   C:\Actelprj\Libero_APA_labs\VHDL\Solution
   C:\Actelprj\Libero_APA_labs\VHDL\Solution

The Import command succeeded ( 00:00:12 )
```

Import auxiliary files into Designer

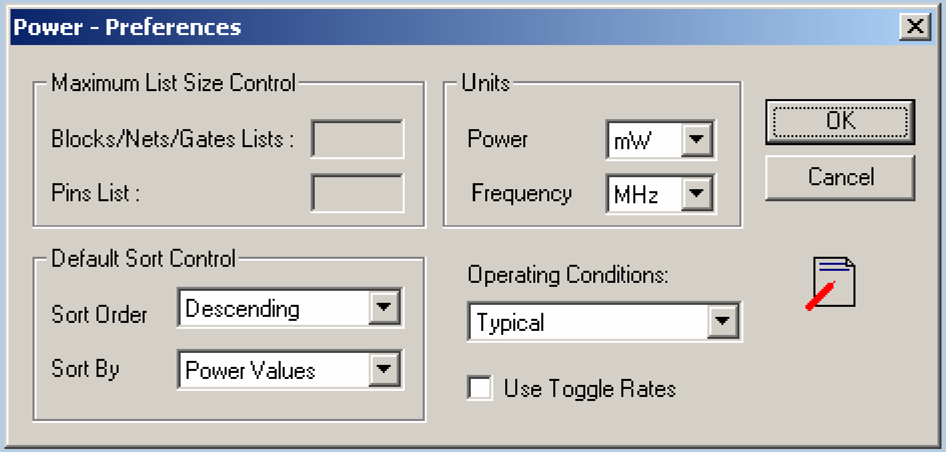
|  | Auxiliary Files | Type |
|---|---|---|
| 1 | C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\simulation\top.v | vcd |
| 2 |  |  |
| 3 |  |  |
| 4 |  |  |
| 5 |  |  |
| 6 |  |  |
| 7 |  |  |
| 8 |  |  |
| 9 |  |  |
| 10 |  |  |

Switching information for the design can be entered by importing a VCD or SAIF file

Import as an Auxiliary file

# SmartPower Preferences

- Max List Size Allows Limiting Instances or Pins Listed
- Units, Operating Conditions, and List Sort Controls Are Self-explanatory
- Block Expansion Control Allows Reported Values to Be Filtered by Minimum Power, Minimum Power Ratio, or Maximum Hierarchical Depth



Power - Preferences

Maximum List Size Control

Blocks/Nets/Gates Lists :

Pins List :

Units

Power: mW

Frequency: MHz

Default Sort Control

Sort Order: Descending

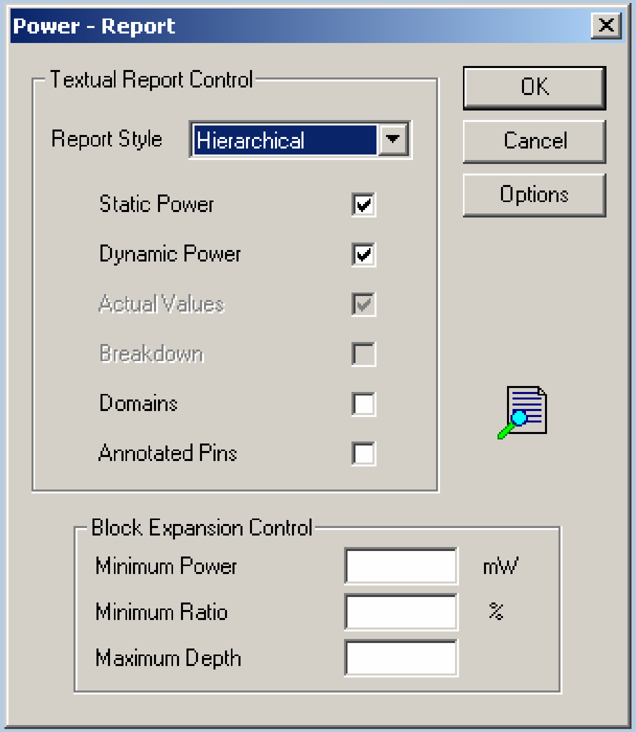
Sort By: Power Values

Operating Conditions: Typical

□ Use Toggle Rates

# SmartPower Power Report

- Text Format
- Select Hierarchical, Flat or Breakdown as Report Style
- Select Static and/or Dynamic Power for Reporting
- Options Menu Invokes Preferences Menu



Textual Report Control

Report Style: Hierarchical

☑ Static Power

☑ Dynamic Power

☑ Actual Values

□ Breakdown

□ Domains

□ Annotated Pins

Block Expansion Control

Minimum Power: mW

Minimum Ratio: %

Maximum Depth:

# SmartPower 7.2
## *New Features*

## Power Breakdown

- Breakdown by type in Summary (I/Os, gates, nets, clocks, memories…)
- Breakdown by power rail in Summary (VCCA, VCCI 3.3, VCCI 2.5….)
- Breakdown by type also available for any level of Hierarchy in the Analysis Tab

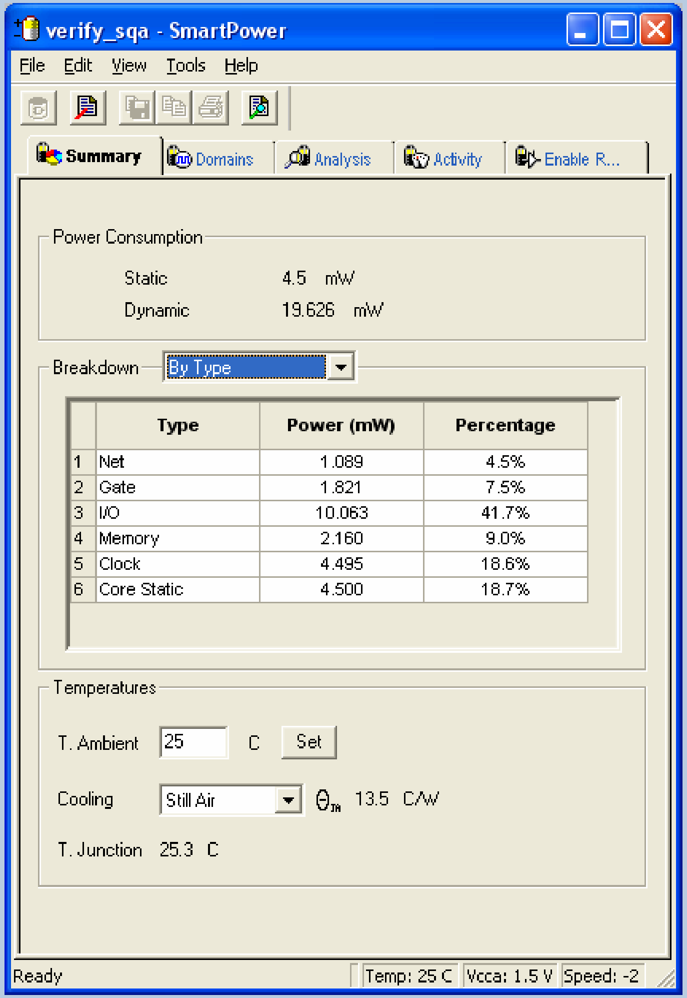
## Advanced Dynamic I/O power analysis

- The Power of all I/Os is reported in Summary/Breakdown
- To make it easier, we display I/O attributes (Load, Standard, Drive Strength…)
- You can set output enable rates for each bidirectional and tri-state (new Enable-rates Tab)

## Additional Ease-of-Use Features

# SmartPower 7.2

## Power Breakdown



Power Consumption

Static 4.5 mW

Dynamic 19.626 mW

Breakdown: By Type

| | Type | Power (mW) | Percentage |
|---|---|---|---|
| 1 | Net | 1.089 | 4.5% |
| 2 | Gate | 1.821 | 7.5% |
| 3 | I/O | 10.063 | 41.7% |
| 4 | Memory | 2.160 | 9.0% |
| 5 | Clock | 4.495 | 18.6% |
| 6 | Core Static | 4.500 | 18.7% |

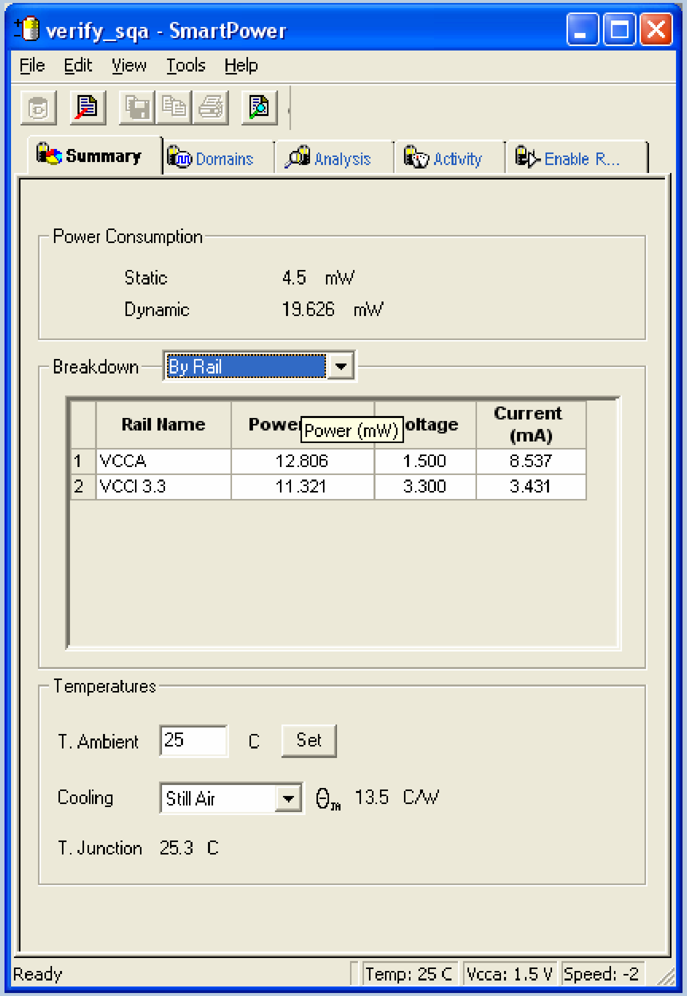
Temperatures

T. Ambient 25 C

Cooling: Still Air $\Theta_{JA}$ 13.5 C/W

T. Junction 25.3 C

Temp: 25 C | Vcca: 1.5 V | Speed: -2



Power Consumption

Static 4.5 mW

Dynamic 19.626 mW

Breakdown: By Rail

| | Rail Name | Powe | oltage | Current (mA) |
|---|---|---|---|---|
| 1 | VCCA | 12.806 | 1.500 | 8.537 |
| 2 | VCCI 3.3 | 11.321 | 3.300 | 3.431 |

Temperatures

T. Ambient 25 C

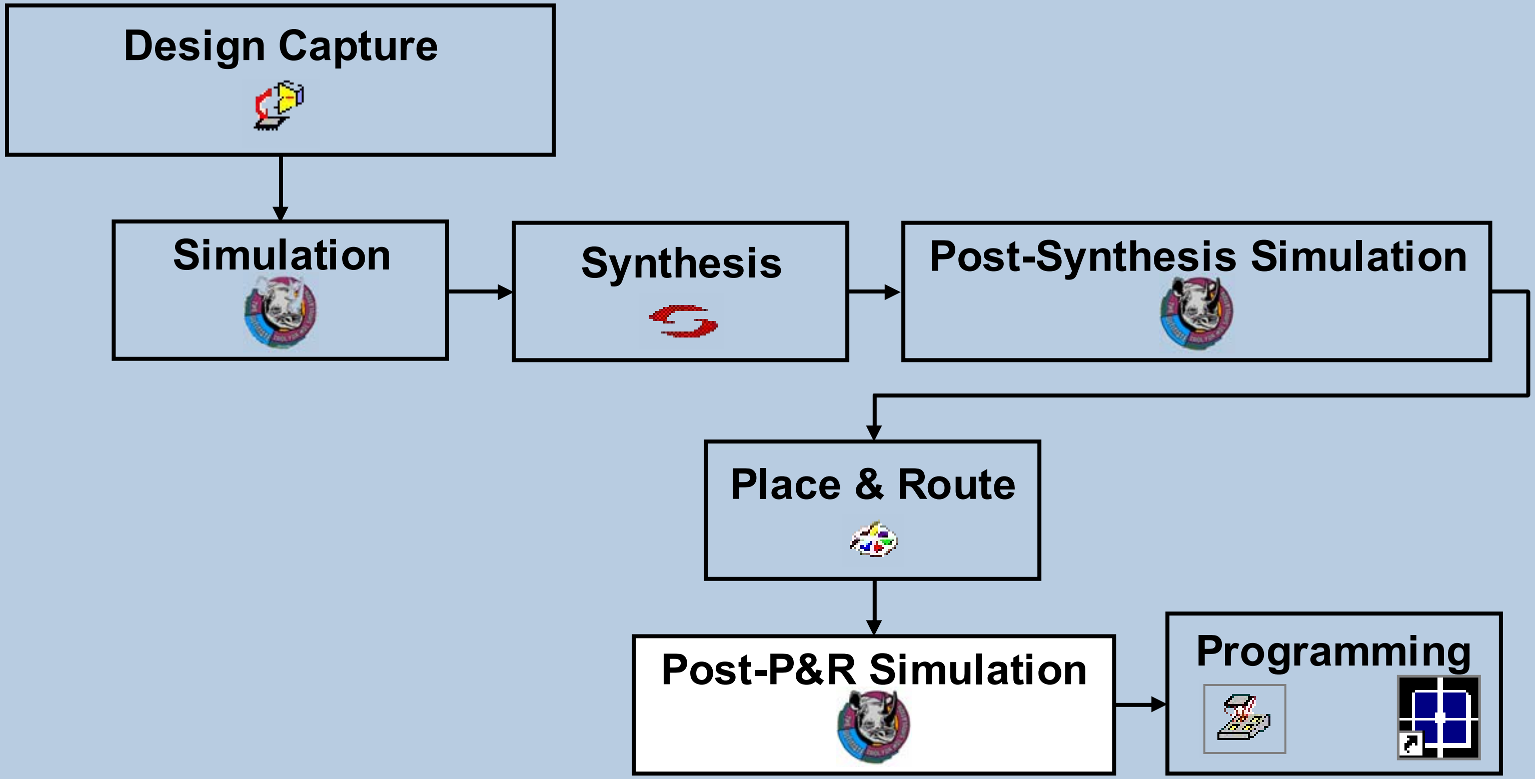
Cooling: Still Air $\Theta_{JA}$ 13.5 C/W

T. Junction 25.3 C

Temp: 25 C | Vcca: 1.5 V | Speed: -2

ONECHIP is all you need

# Post-Layout Simulation



Design Capture

Simulation

Synthesis

Post-Synthesis Simulation

Place & Route

Post-P&R Simulation

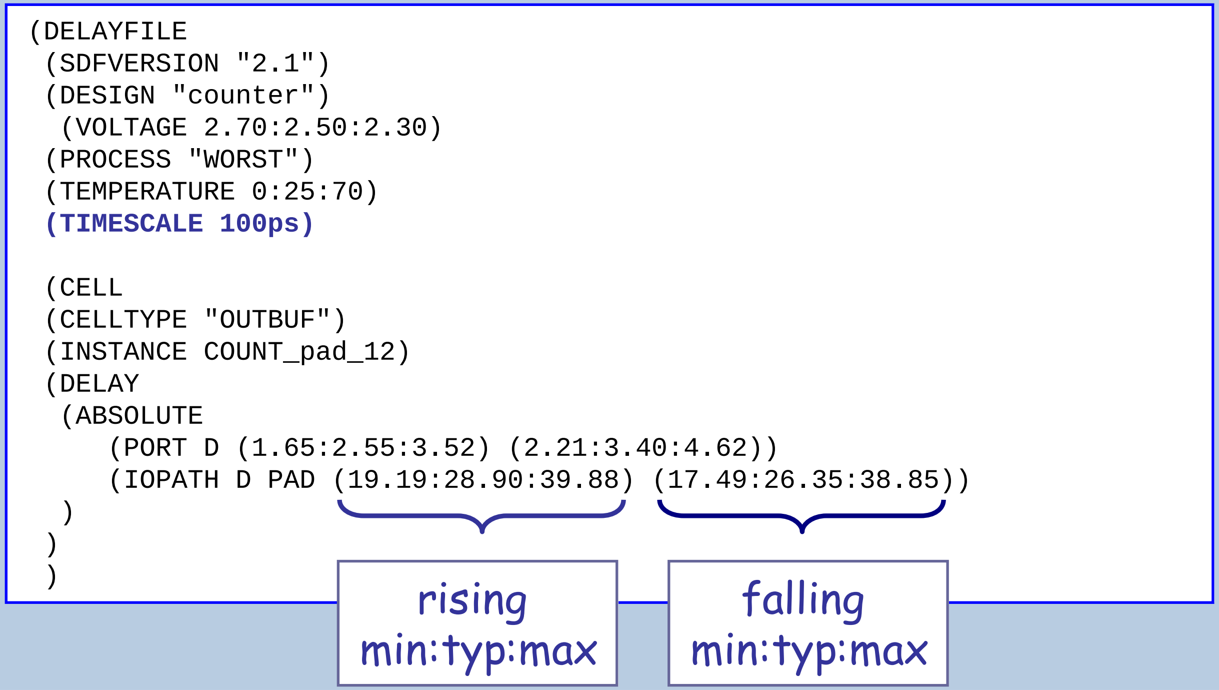
Programming

# Post-Layout Simulation

## Steps

- Route design
- Export .sdf file (Back-annotate)
- Run Post-layout Simulation

## SDF File Contains Delays for Min, Typ and Max



```
(DELAYFILE
 (SDFVERSION "2.1")
 (DESIGN "counter")
  (VOLTAGE 2.70:2.50:2.30)
 (PROCESS "WORST")
 (TEMPERATURE 0:25:70)
 (TIMESCALE 100ps)

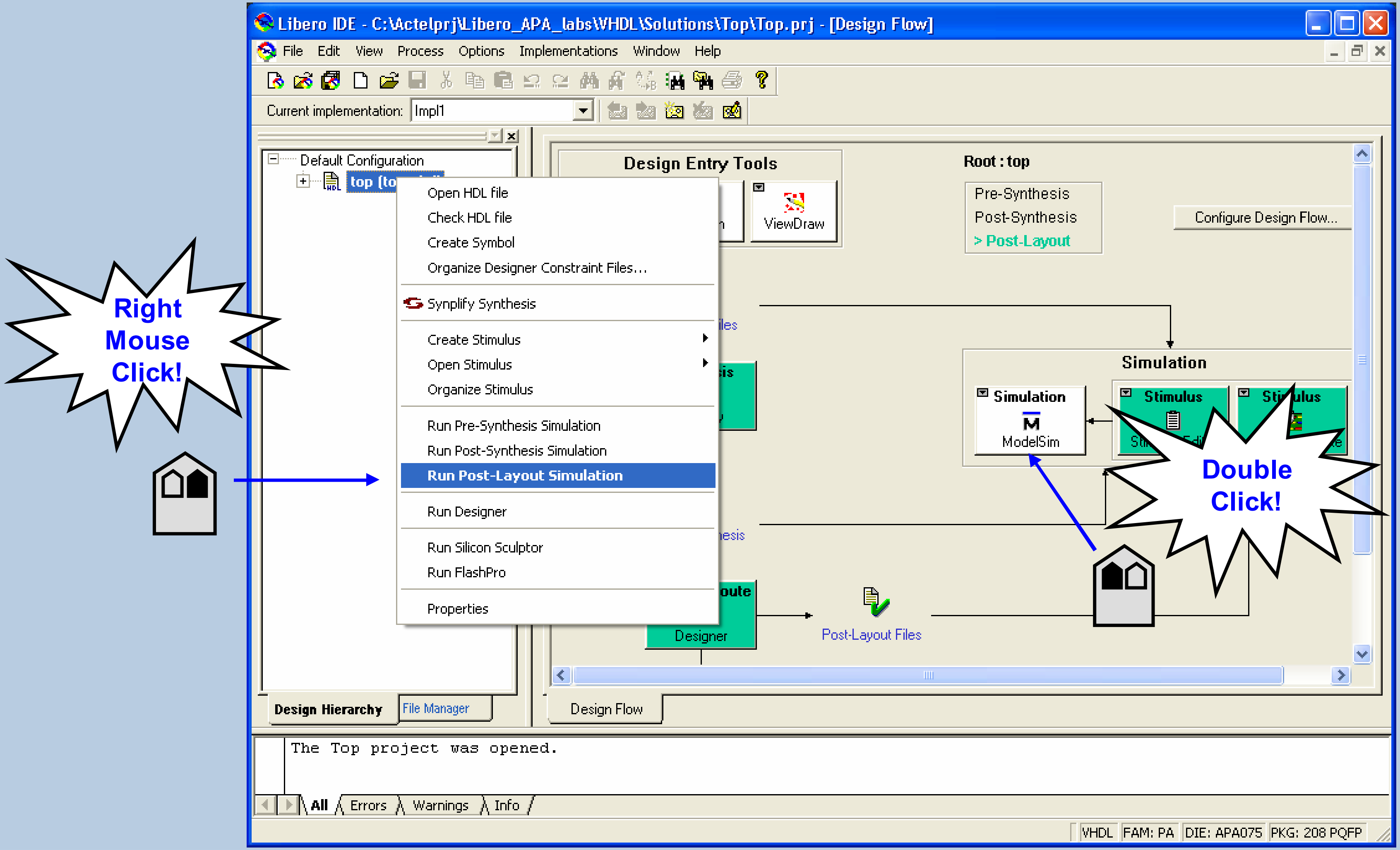
 (CELL
 (CELLTYPE "OUTBUF")
 (INSTANCE COUNT_pad_12)
 (DELAY
  (ABSOLUTE
     (PORT D (1.65:2.55:3.52) (2.21:3.40:4.62))
     (IOPATH D PAD (19.19:28.90:39.88) (17.49:26.35:38.85))
  )
 )
 )
```

rising
min:typ:max

falling
min:typ:max

# Post-Layout Simulation

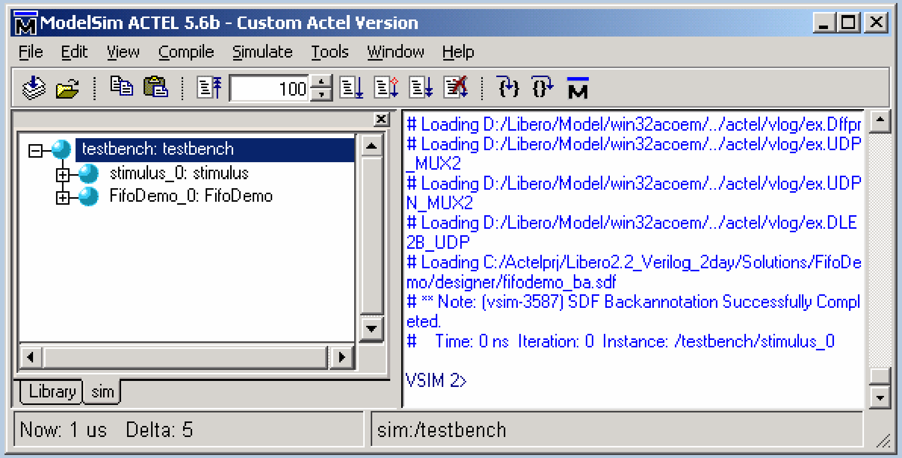
- Click on “Simulation” in Design Flow Window or…



```
The Top project was opened.
```

# Post-Layout Simulation

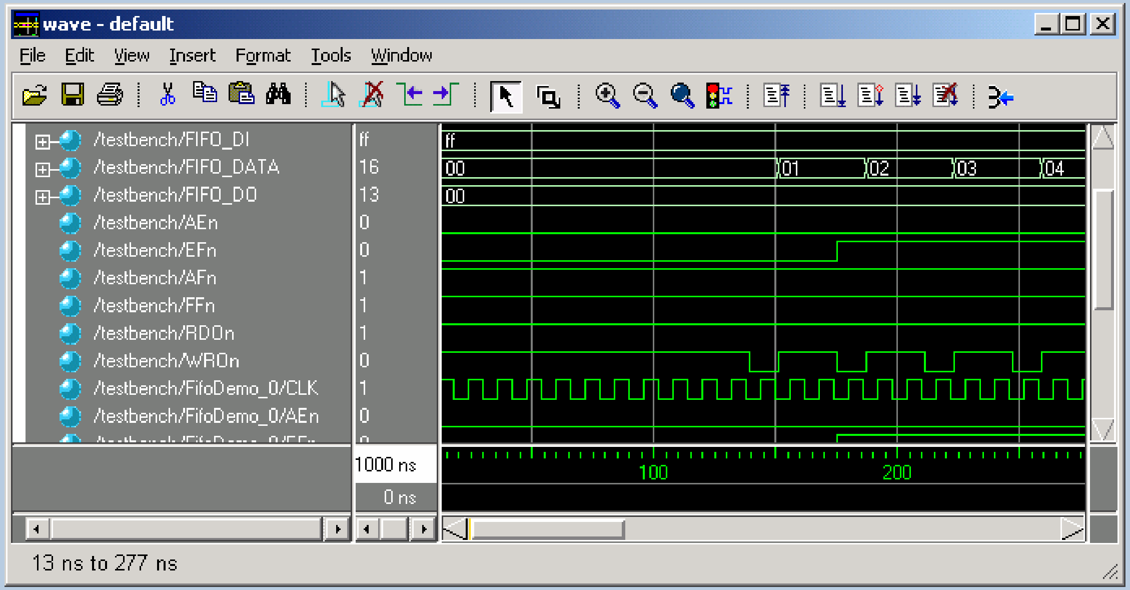
- Structural Netlist and .sdf File Used for Simulation
  - **Simulator runs for 1 uS as Default**
  - **Max Operating Conditions Default**


ModelSim ACTEL 5.6b - Custom Actel Version
File Edit View Compile Simulate Tools Window Help
100
testbench: testbench
stimulus_0: stimulus
FifoDemo_0: FifoDemo
Library
sim

```
# Loading D:/Libero/Model/win32acoem/../actel/vlog/ex.Dffpr
# Loading D:/Libero/Model/win32acoem/../actel/vlog/ex.UDP
_MUX2
# Loading D:/Libero/Model/win32acoem/../actel/vlog/ex.UDP
N_MUX2
# Loading D:/Libero/Model/win32acoem/../actel/vlog/ex.DLE
2B_UDP
# Loading C:/Actelprj/Libero2.2_Verilog_2day/Solutions/FifoDe
mo/designer/fifodemo_ba.sdf
# ** Note: (vsim-3587) SDF Backannotation Successfully Compl
eted.
#    Time: 0 ns  Iteration: 0  Instance: /testbench/stimulus_0

VSIM 2>
```

Now: 1 us    Delta: 5    sim:/testbench



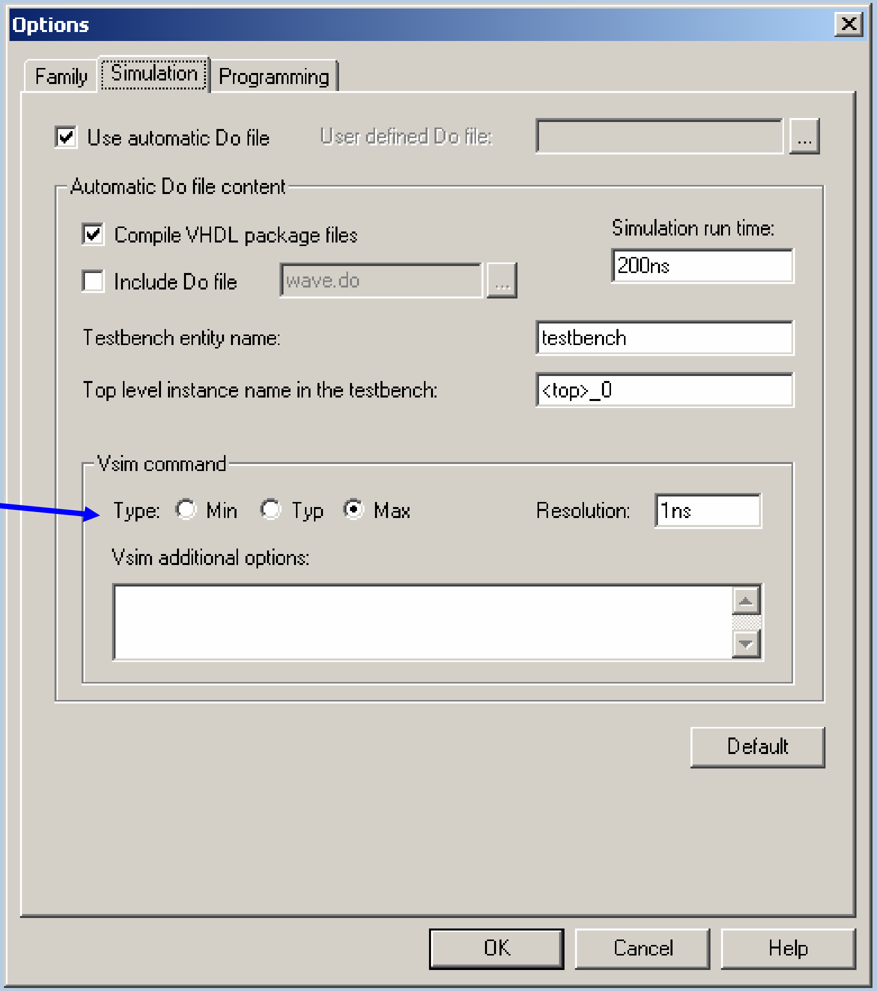
```
/testbench/FIFO_DI              ff
/testbench/FIFO_DATA            16
/testbench/FIFO_DO              13
/testbench/AEn                  0
/testbench/EFn                  0
/testbench/AFn                  1
/testbench/FFn                  1
/testbench/RDOn                 1
/testbench/WROn                 0
/testbench/FifoDemo_0/CLK       1
/testbench/FifoDemo_0/AEn       0
                                1000 ns
                                0 ns
```

13 ns to 277 ns

ONECHIP is all you need

# Post-Layout Simulation
*Selecting Operating Conditions*

- Post-layout Operating Conditions Can Be Specified within Libero
  - **Tools > Options from Libero Main Window**
  - **Select Simulation Tab in Options Window**
  - **Choose Min/Typ/Max**



☑ Use automatic Do file  User defined Do file: [ ]

Automatic Do file content

☑ Compile VHDL package files

□ Include Do file  wave.do

Simulation run time: 200ns

Testbench entity name: testbench

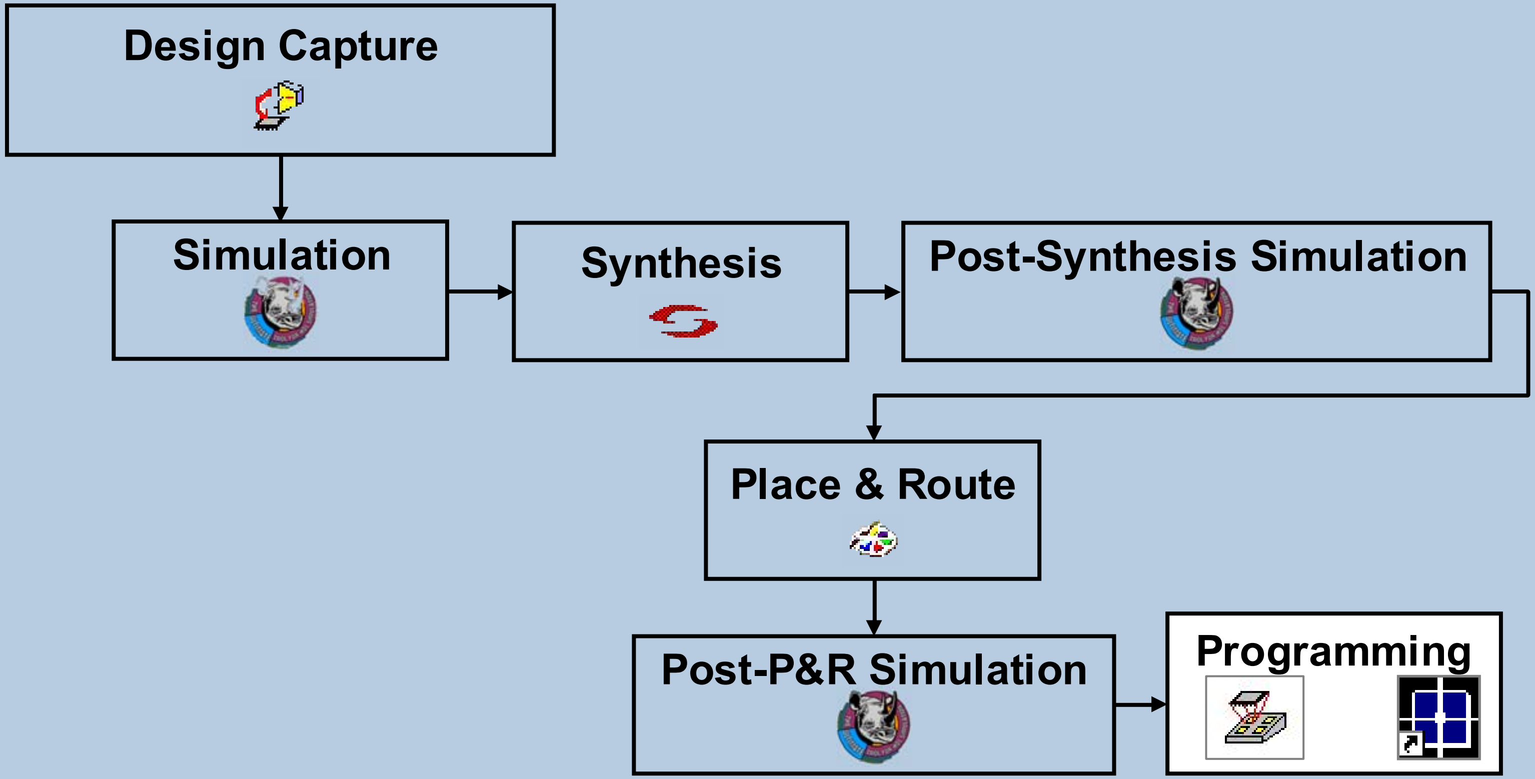
Top level instance name in the testbench: <top>_0

Vsim command

Type: ○ Min ○ Typ ● Max  Resolution: 1ns

Vsim additional options:

# Programming & Debugging



Design Capture

Simulation

Synthesis

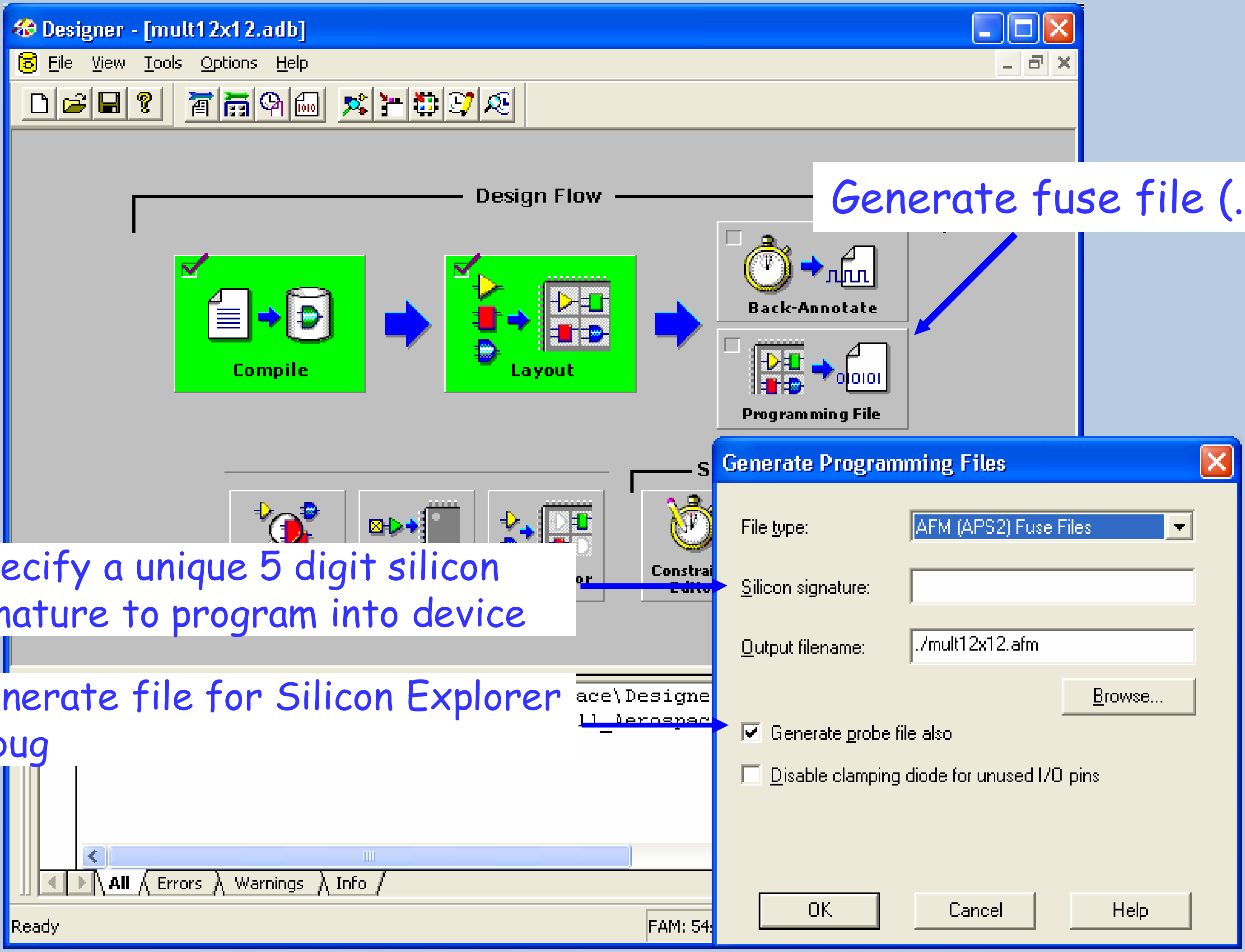
Post-Synthesis Simulation

Place & Route

Post-P&R Simulation

Programming

# Generating Programming File
*Antifuse*



Generate Programming Files

File type: AFM (APS2) Fuse Files

Silicon signature:

Output filename: ./mult12x12.afm

Browse...

☑ Generate probe file also

☐ Disable clamping diode for unused I/O pins

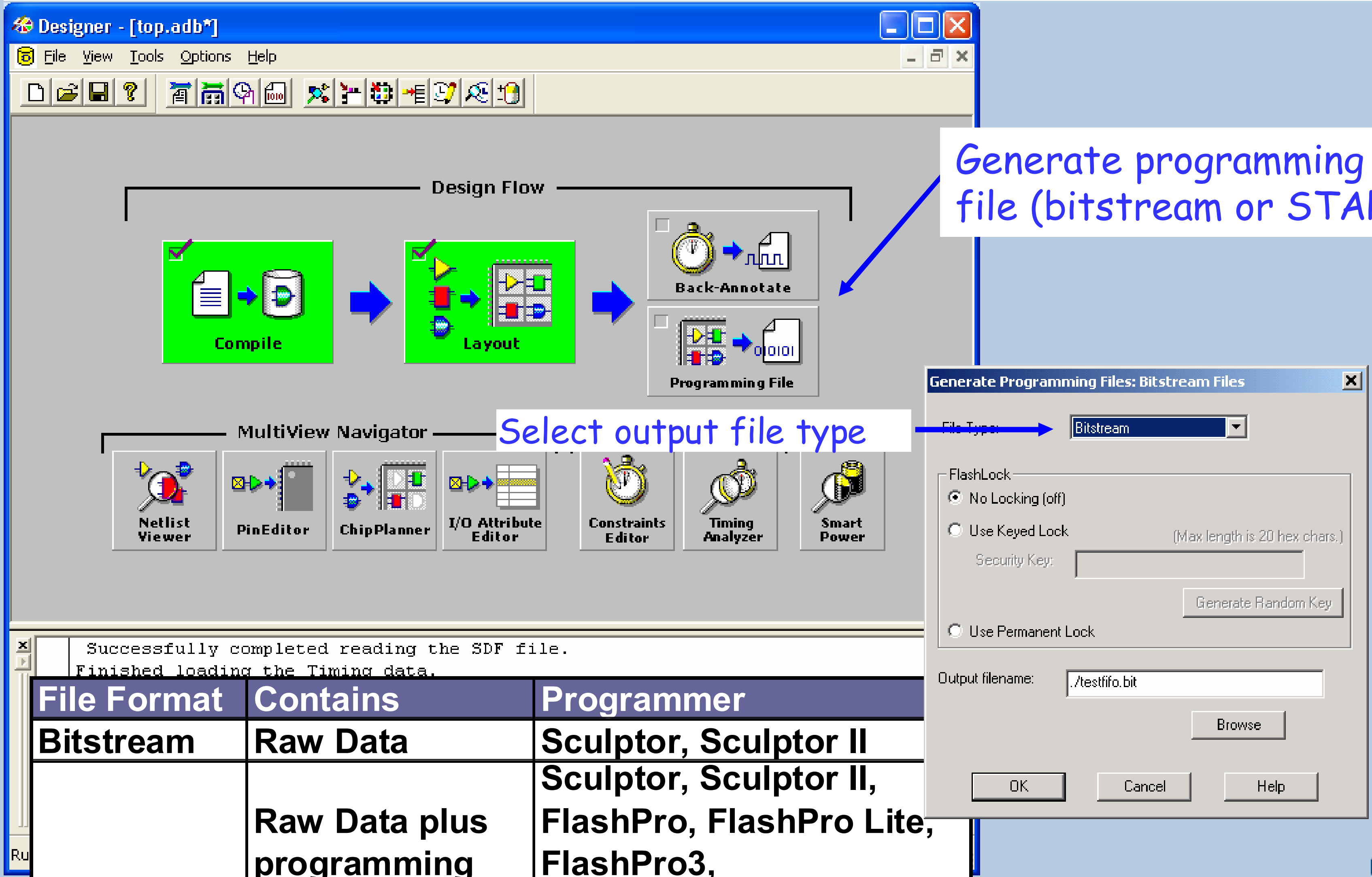
OK Cancel Help

Generate fuse file (.afm)

Specify a unique 5 digit silicon signature to program into device

Generate file for Silicon Explorer debug

# Generating Programming File
*Flash*



```
Successfully completed reading the SDF file.
Finished loading the Timing data.
```

Generate programming file (bitstream or STAPL)

Select output file type

File Type: Bitstream

FlashLock
- ● No Locking (off)
- ○ Use Keyed Lock (Max length is 20 hex chars.)
  Security Key:
- ○ Use Permanent Lock

Output filename: ./testfifo.bit

| File Format | Contains | Programmer |
|---|---|---|
| Bitstream | Raw Data | Sculptor, Sculptor II |
| STAPL | Raw Data plus programming information | Sculptor, Sculptor II, FlashPro, FlashPro Lite, FlashPro3, In-system programming |

ONECHIP is all you need

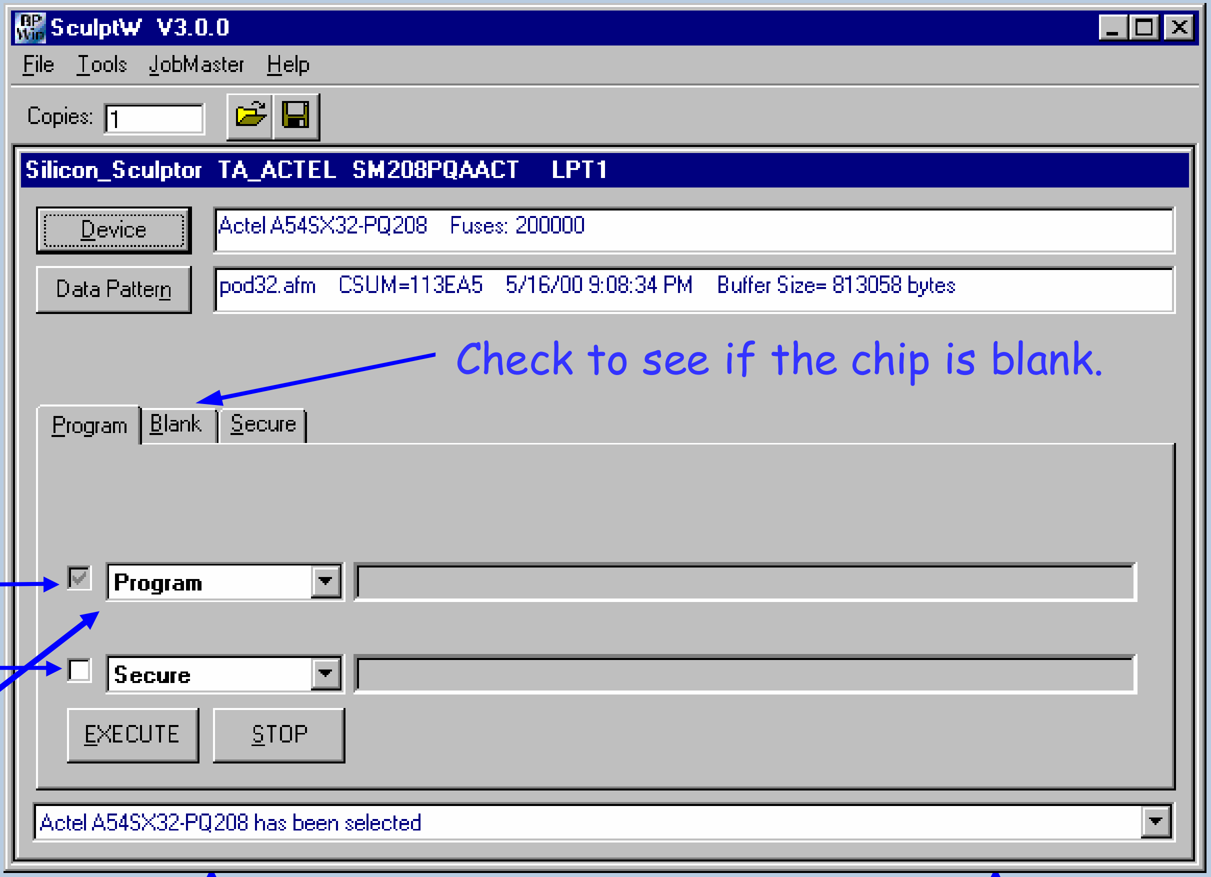
# Sculptor II Overview

- PC-based Parallel-port, Single Device Programmer
- Designed to Allow Concurrent Programming of Multiple Units from Same PC
- Replaces Silicon Sculptor I as Actel's Programmer of Choice
- Silicon Sculptor II Benefits:
  - **Programs All Actel Packages**
    - **Antifuse and Flash Programming Support**
  - **Universal Actel Socket Adapters**
  - **Works with Silicon Sculptor I Adapter Modules**
  - **Uses Same Software as Silicon Sculptor I**
  - **Provides Extensive Self-test Capability**

# Sculptor II Software

- Available from Actel Website
  - http://www.actel.com/custsup/updates/silisculpt/
- Requirements (Windows Version)
  - Microsoft Windows 95/98, Win NT or Win 2000
- Requirements (DOS Version)
  - 286 with 4MB RAM, Approx. 6MB Hard Drive Space
  - DOS-driven Program - Memory Managers Not Required
  - DOS Shell from Windows 95/98 - OK
  - Does Not Work with Windows NT

# Silicon Sculptor II Windows Interface



Actel A54SX32-PQ208 Fuses: 200000

pod32.afm CSUM=113EA5 5/16/00 9:08:34 PM Buffer Size= 813058 bytes

☑ Program

□ Secure

Actel A54SX32-PQ208 has been selected

1. Select > Device
2. Buffer > Load

Check to see if the chip is blank.

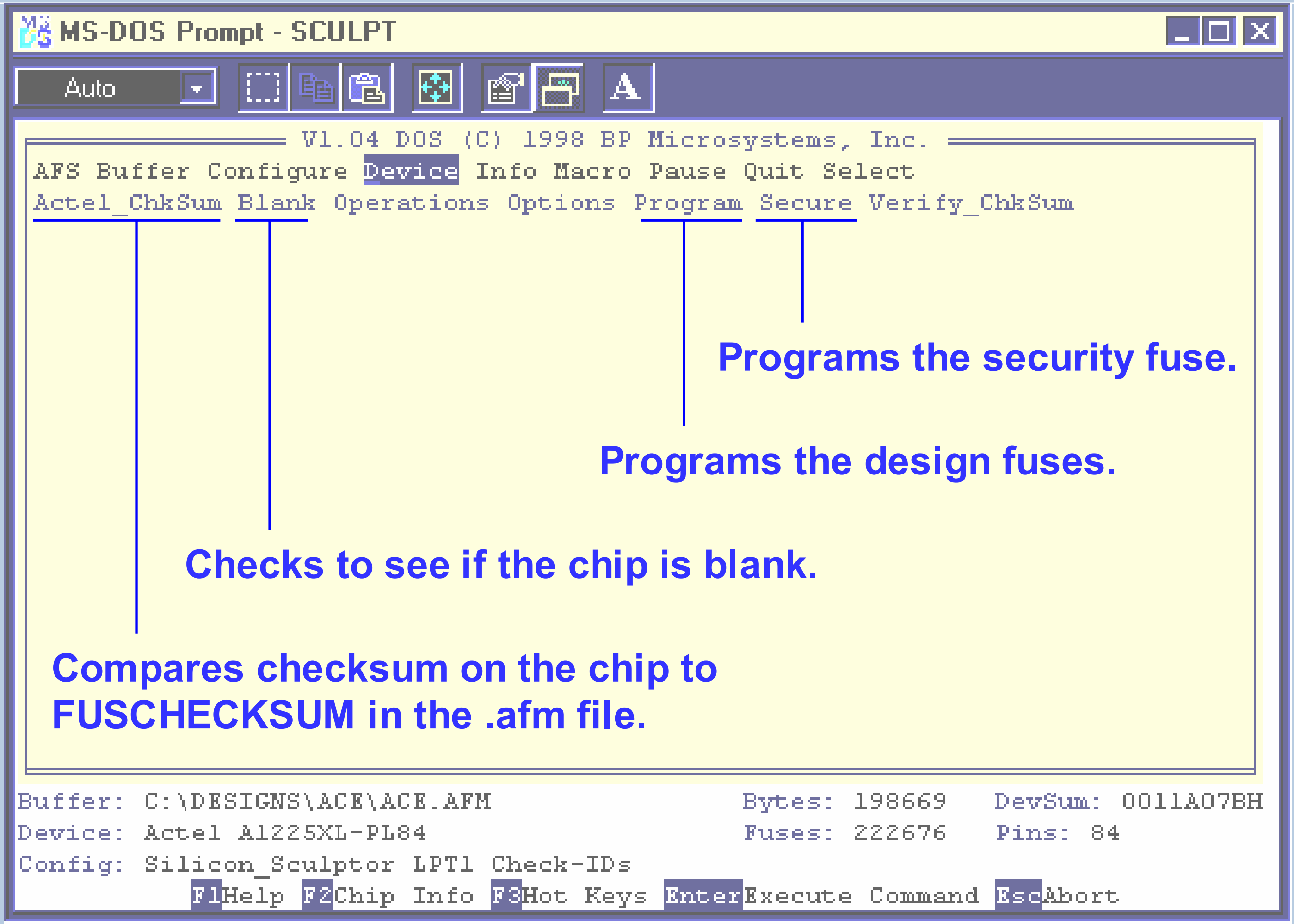
Programs the design fuses.

Programs the security fuse.

Checksum Command (under the pull down menu) compares checksum on the chip to FUSCHECKSUM in the .afm file.

Status Area

# Silicon Sculptor II DOS Interface



```
V1.04 DOS (C) 1998 BP Microsystems, Inc.
AFS Buffer Configure Device Info Macro Pause Quit Select
Actel_ChkSum Blank Operations Options Program Secure Verify_ChkSum
```

Programs the security fuse.

Programs the design fuses.

Checks to see if the chip is blank.

Compares checksum on the chip to FUSCHECKSUM in the .afm file.

```
Buffer:  C:\DESIGNS\ACE\ACE.AFM              Bytes:  198669    DevSum:  0011A07BH
Device:  Actel A1225XL-PL84                  Fuses:  222676    Pins:  84
Config:  Silicon_Sculptor LPT1 Check-IDs
              F1Help  F2Chip Info  F3Hot Keys  EnterExecute Command  EscAbort
```

2. Buffer > Load

1. Select > Device

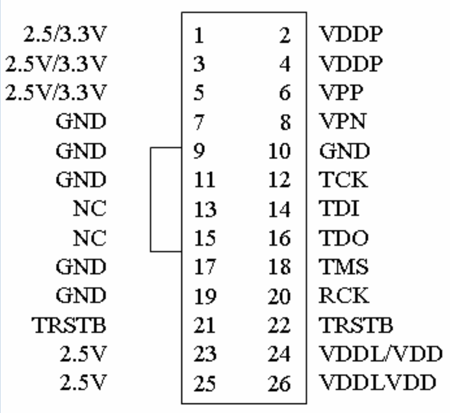
Status Area

# Flash Programming

- Flash FPGA Devices Can Be Programmed Multiple Ways
  - **Off-board Programming with Silicon Sculptor II**
  - **In-System Programming (ISP) using JTAG Interface with:**
    - **Silicon Sculptor II (ProASIC, ProASIC$^{\underline{PLUS}}$, ProASIC3\E, Fusion)**
    - **Flash Pro (ProASIC or ProASIC$^{\underline{PLUS}}$)**
    - **Flash Pro Lite (ProASIC$^{\underline{PLUS}}$)**
    - **Flash Pro 3 (ProASIC3\E, Fusion)**
  - **Programming via Microprocessor Interface**
    - **(ProASIC$^{\underline{PLUS}}$, ProASIC3\E, Fusion)**

# FlashPro Programmer
## *ProASIC, ProASIC$^{\underline{PLUS}}$*

- Small Form Factor - 24 in$^3$
- Low Cost
- Hardware Features
  - Small 26-pin Header
    - *Samtec FTSH-113-01-L-D-K*
  - 20” Ribbon Cable
  - ECP Parallel Port
- Software Features
  - Win 95/98/NT/00 O/S
  - STAPL Support
  - Daisy Chain Capability
  - Log File Generation
  - Self-test Option



| | | | |
|---|---|---|---|
| 2.5/3.3V | 1 | 2 | VDDP |
| 2.5V/3.3V | 3 | 4 | VDDP |
| 2.5V/3.3V | 5 | 6 | VPP |
| GND | 7 | 8 | VPN |
| GND | 9 | 10 | GND |
| GND | 11 | 12 | TCK |
| NC | 13 | 14 | TDI |
| NC | 15 | 16 | TDO |
| GND | 17 | 18 | TMS |
| GND | 19 | 20 | RCK |
| TRSTB | 21 | 22 | TRSTB |
| 2.5V | 23 | 24 | VDDL/VDD |
| 2.5V | 25 | 26 | VDDLVDD |

# FlashPro Lite Programmer
## *ProASIC$^{\underline{PLUS}}$*

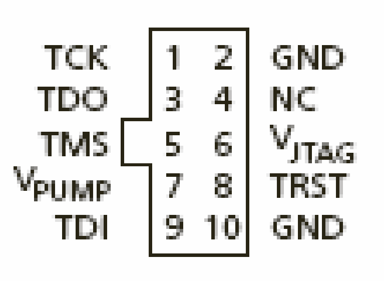
- Low Cost
- Ultra-small Form Factor
- Hardware Features
  - Draws Power from Target Board
  - Connects to Parallel Port
  - Supports In-system Programming
    - Samtec 26-pin Header
- Software Features
  - Supports Windows 98, NT, 2000, and XP Operating Systems
  - STAPL Support
  - Free Software Updates

ONE CHIP is all you need

# FlashPro 3
## *ProASIC3\E and Fusion*

- USB 2.0 High-speed Interface
  - **10-pin JTAG ISP**
  - **Altera-compatible Interface**

- Programs ProASIC3 Devices in Less than 2 Minute
- Powered by USB Connection
  - **Parallel Programming Requires Powered USB Hub**
- Variable TCK (up to 24 MHz)
  - **Recommend <= 20MHz for PA3/E**
- Optional Transition Board provides Adapter Cables for 26- and 10-pin SAMTEC

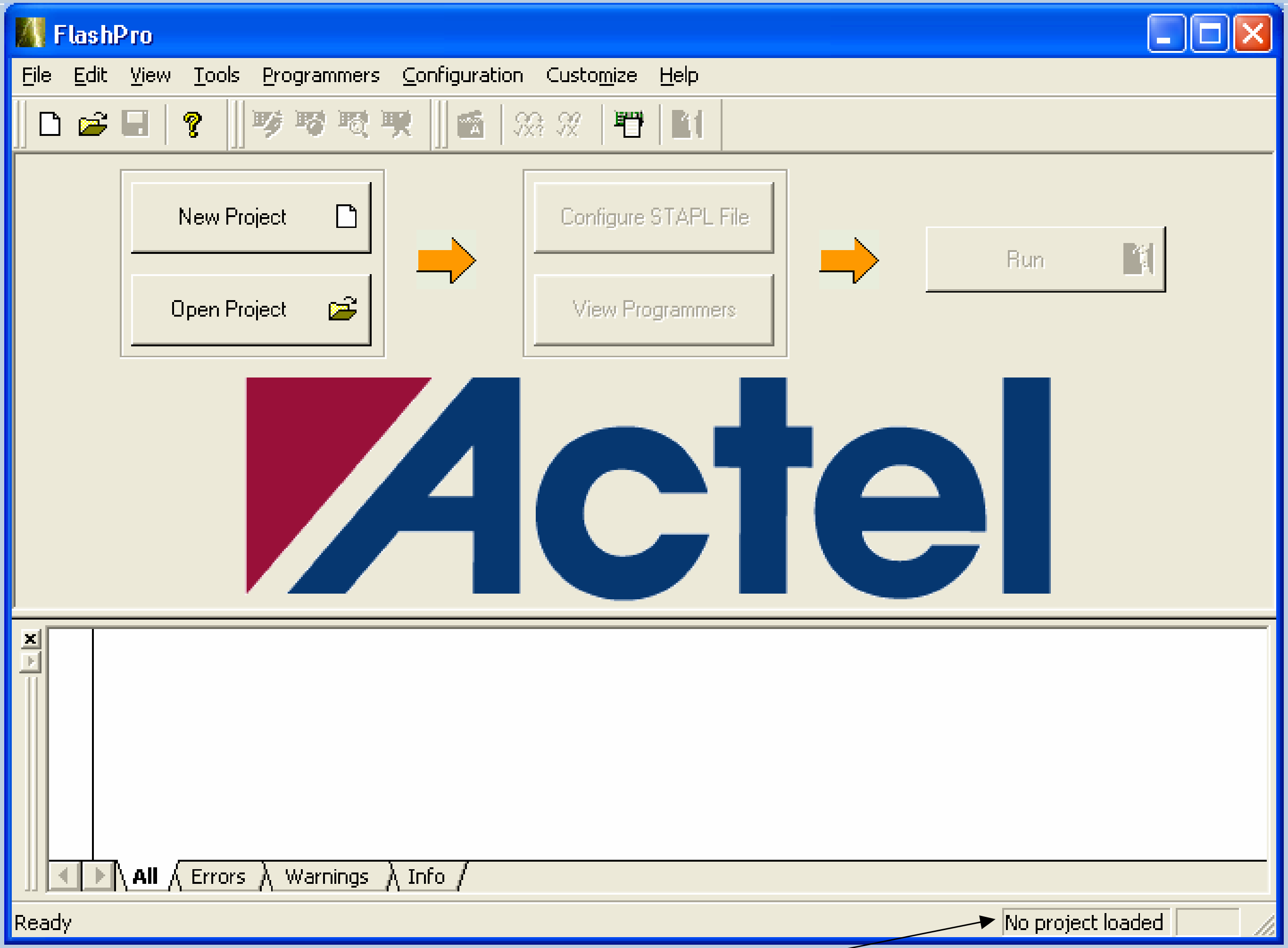


| | | | |
|---|---|---|---|
| TCK | 1 | 2 | GND |
| TDO | 3 | 4 | NC |
| TMS | 5 | 6 | $V_{JTAG}$ |
| $V_{PUMP}$ | 7 | 8 | TRST |
| TDI | 9 | 10 | GND |

# Programmer Summary

| Programmer | Device Support | Availability |
|---|---|---|
| Silicon Scupltor II | All antifuse FPGAs<br>ProASIC and ProASIC$^{PLUS}$<br>ProASIC3\E | Available |
| FlashPro | ProASIC and ProASIC$^{PLUS}$ | Available |
| FlashPro Lite | ProASIC$^{PLUS}$ | Available |
| FlashPro 3 | ProASIC3\E and Fusion | Available |

# FlashPro 4.2 User Interface



Menu Bar

Tool Bar

Flow Window

Log Window

Status Bar

# Programming with FlashPro 4.2

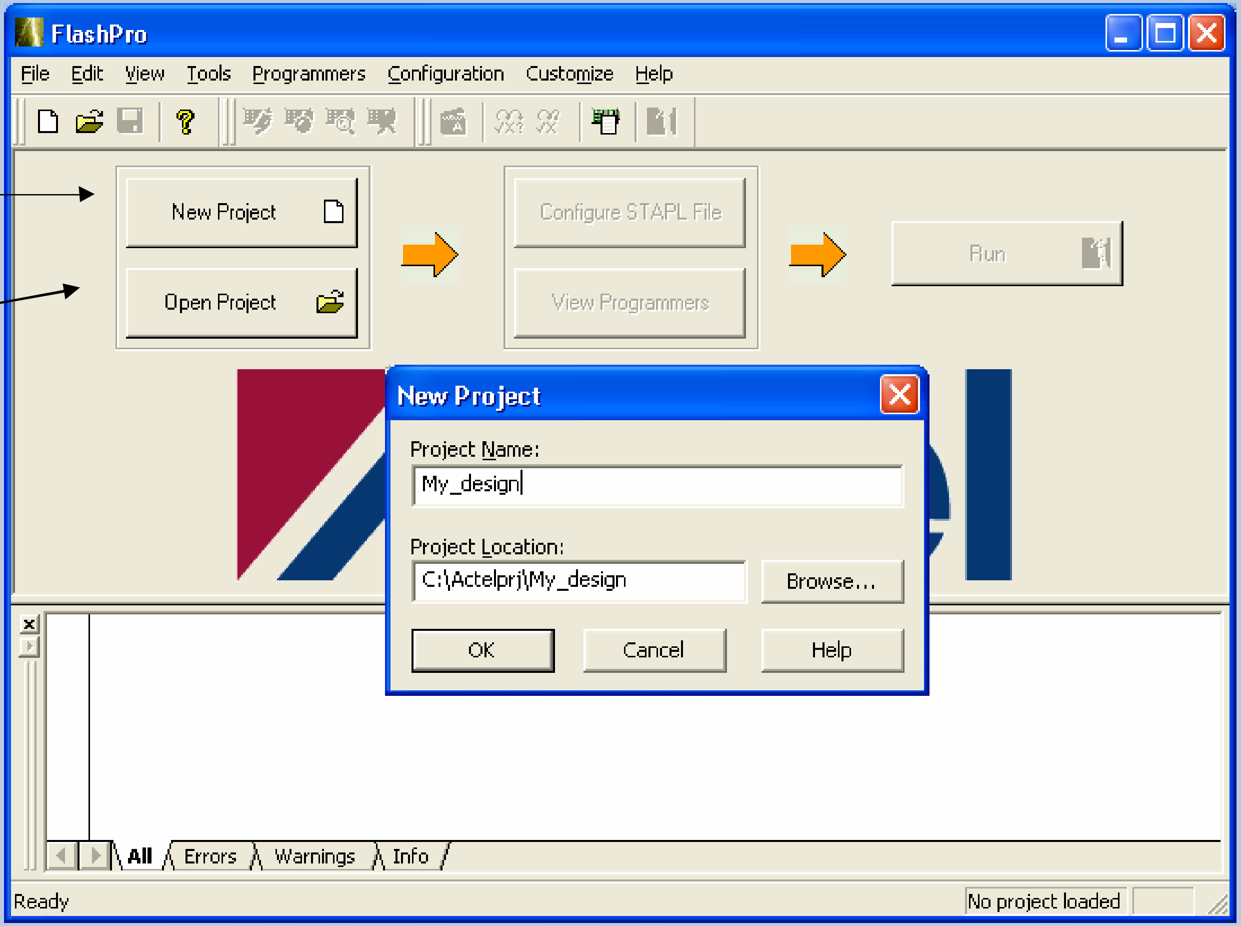
- Launch FlashPro
- Load STAPL File
- Select Action
- Execute Action

# FlashPro 4.2
## *Create / Open Project*

- Select New or Open in FlashPro 4.2 GUI to Create a Project or Open and Existing Project

Create New Project

Open Existing Project



New Project

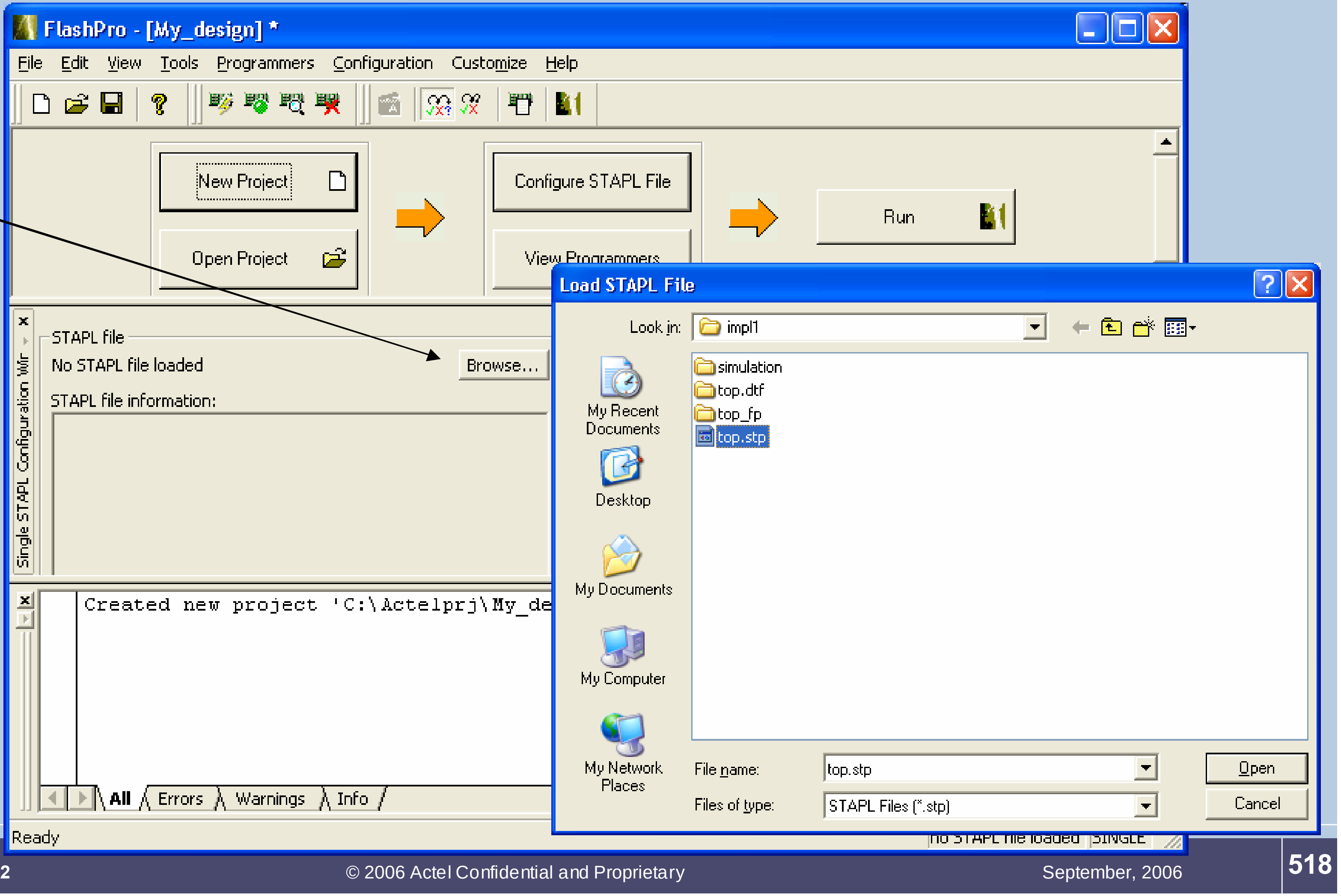
Project Name: My_design

Project Location: C:\Actelprj\My_design

# FlashPro 4.2
## *Load STAPL File*

- Select Configure STAPL File to Load Programming File
  - **Single STAPL File Configuration Window is Displayed**

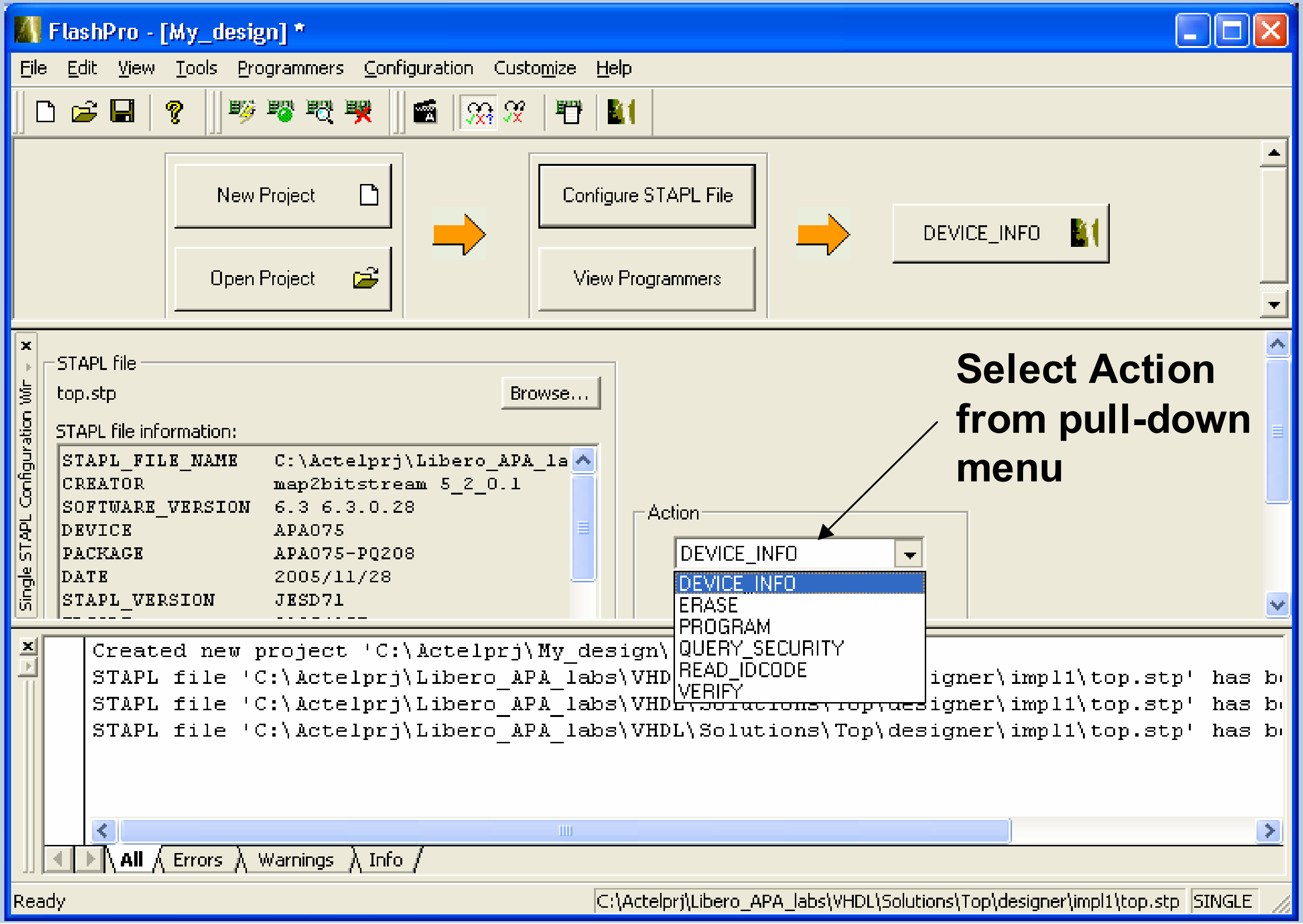
**Browse to STAPL file**



```
Created new project 'C:\Actelprj\My_de
```

# FlashPro 4.2
## *Select Action*

- Select Action to Perform from Pull-down Menu in Single STAPL Configuration Window



STAPL file top.stp

STAPL file information:

```
STAPL_FILE_NAME    C:\Actelprj\Libero_APA_la
CREATOR            map2bitstream 5_2_0.1
SOFTWARE_VERSION   6.3 6.3.0.28
DEVICE             APA075
PACKAGE            APA075-PQ208
DATE               2005/11/28
STAPL_VERSION      JESD71
```

Action: DEVICE_INFO

```
Created new project 'C:\Actelprj\My_design\
STAPL file 'C:\Actelprj\Libero_APA_labs\VHD                          igner\impl1\top.stp' has b
STAPL file 'C:\Actelprj\Libero_APA_labs\VHD                          igner\impl1\top.stp' has b
STAPL file 'C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\designer\impl1\top.stp' has b
```

C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\designer\impl1\top.stp

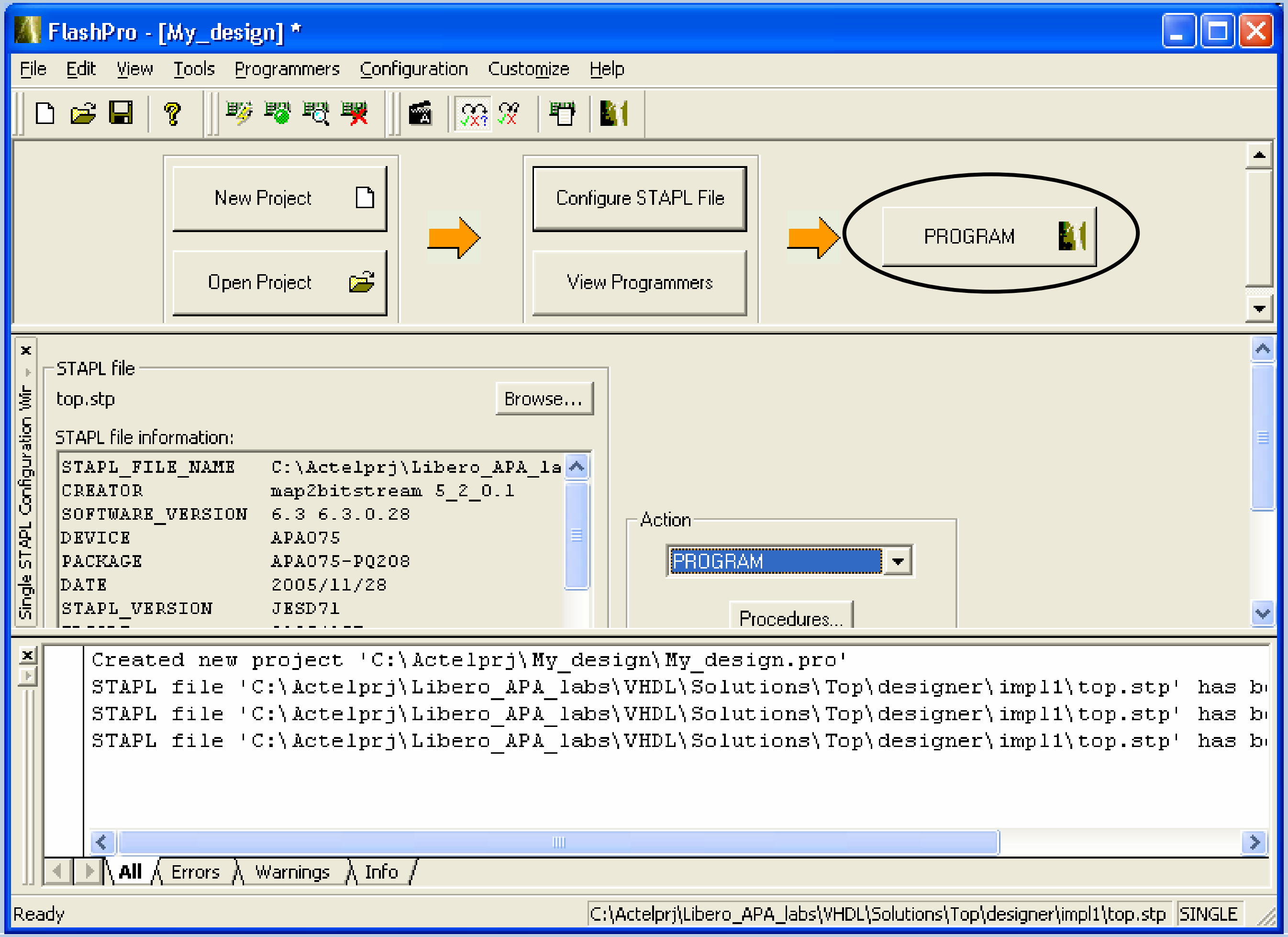
**STAPL file details**

**Select Action from pull-down menu**

# FlashPro 4.2
*Execute Action*

## ■ Click Button in Flow Window to Execute Action

- **Button Matches Selected Action**



STAPL file: top.stp

STAPL file information:

```
STAPL_FILE_NAME    C:\Actelprj\Libero_APA_la
CREATOR            map2bitstream 5_2_0.1
SOFTWARE_VERSION   6.3 6.3.0.28
DEVICE             APA075
PACKAGE            APA075-PQ208
DATE               2005/11/28
STAPL_VERSION      JESD71
```

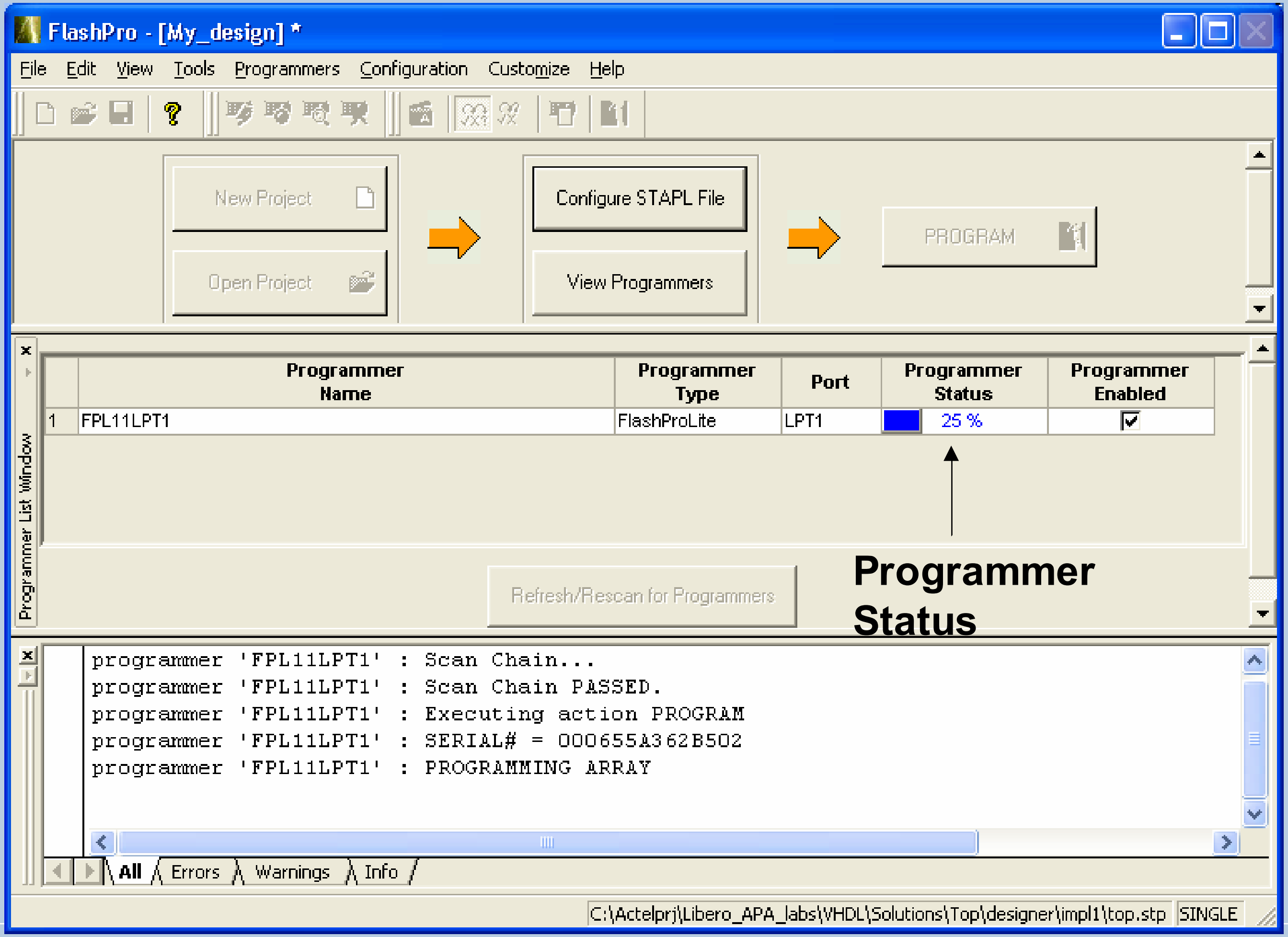
Action: PROGRAM

```
Created new project 'C:\Actelprj\My_design\My_design.pro'
STAPL file 'C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\designer\impl1\top.stp' has b
STAPL file 'C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\designer\impl1\top.stp' has b
STAPL file 'C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\designer\impl1\top.stp' has b
```

C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\designer\impl1\top.stp

# FlashPro 4.2
## *Programmer Status*

- Programmer Status is Displayed in Programming List Window


FlashPro - [My_design] *
File Edit View Tools Programmers Configuration Customize Help
New Project
Open Project
Configure STAPL File
View Programmers
PROGRAM
Programmer List Window
Refresh/Rescan for Programmers
All Errors Warnings Info
C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\designer\impl1\top.stp SINGLE

|  | Programmer Name | Programmer Type | Port | Programmer Status | Programmer Enabled |
|---|---|---|---|---|---|
| 1 | FPL11LPT1 | FlashProLite | LPT1 | 25 % | ☑ |

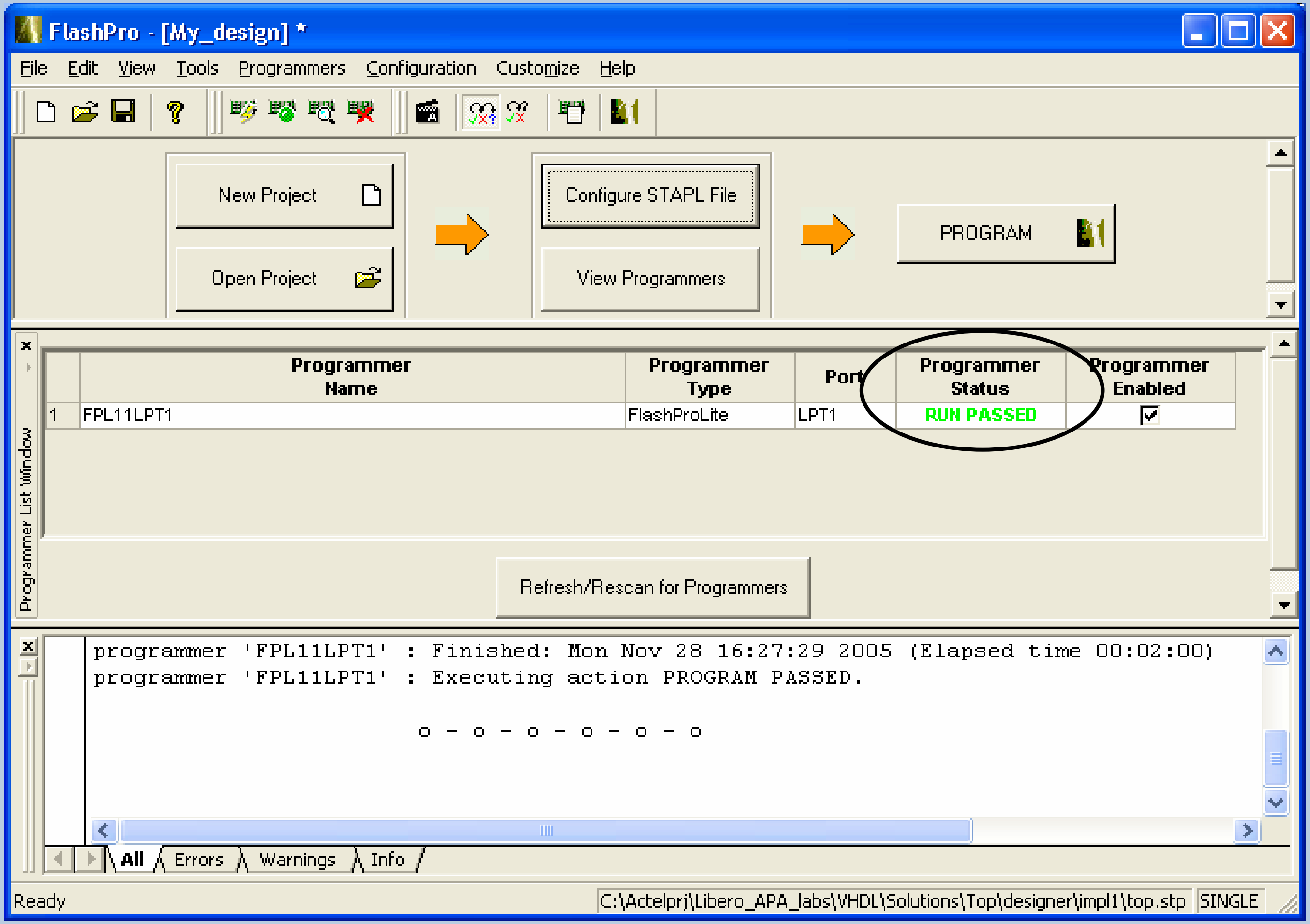
```
programmer 'FPL11LPT1' : Scan Chain...
programmer 'FPL11LPT1' : Scan Chain PASSED.
programmer 'FPL11LPT1' : Executing action PROGRAM
programmer 'FPL11LPT1' : SERIAL# = 000655A362B502
programmer 'FPL11LPT1' : PROGRAMMING ARRAY
```

**Programming List Window**

**Programmer Status**

# FlashPro 4.2
## *Programming Complete*

- Successful Programming is Indicated in the Programmer Status Column



| | Programmer Name | Programmer Type | Port | Programmer Status | Programmer Enabled |
|---|---|---|---|---|---|
| 1 | FPL11LPT1 | FlashProLite | LPT1 | RUN PASSED | ☑ |

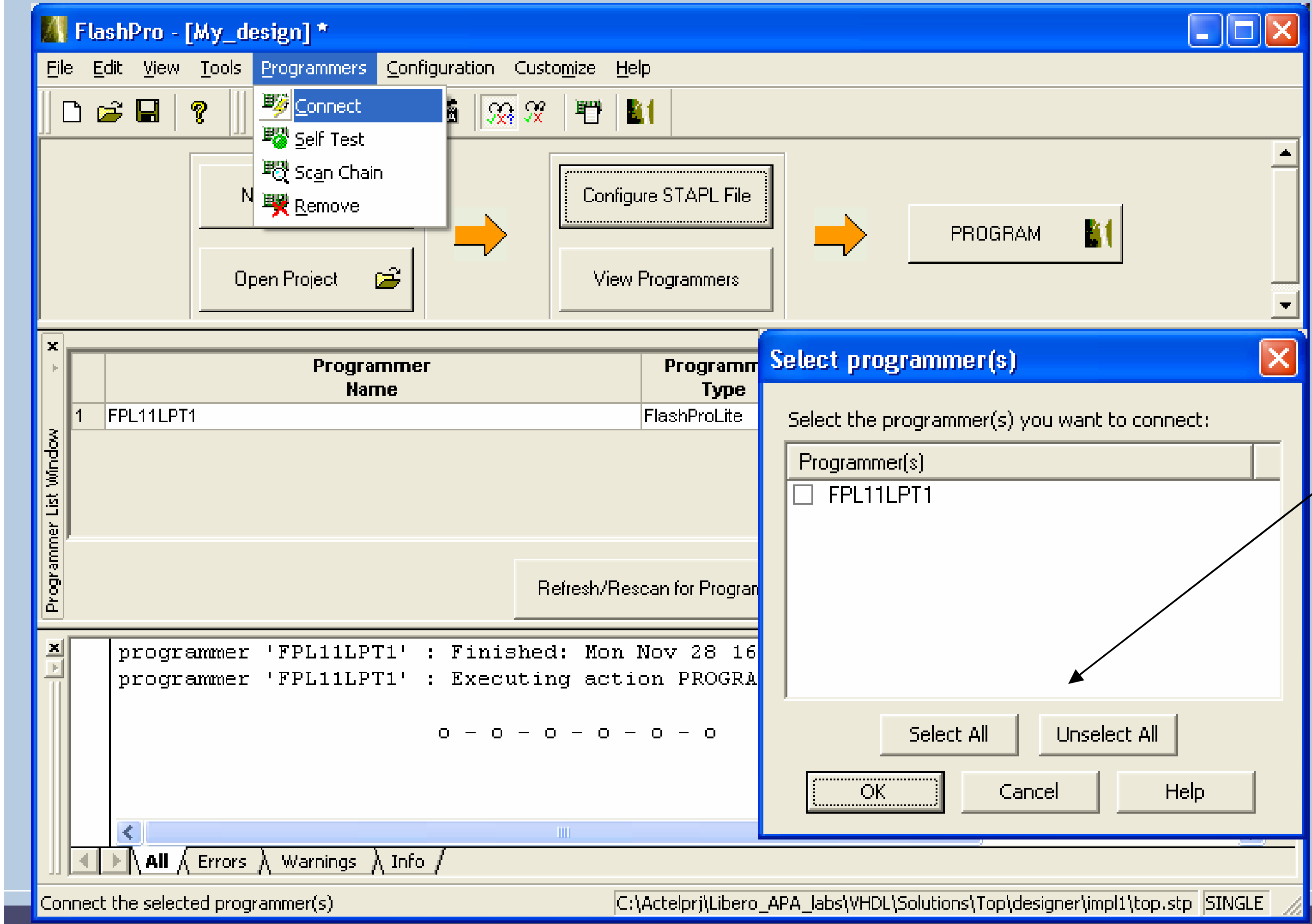
```
programmer 'FPL11LPT1' : Finished: Mon Nov 28 16:27:29 2005 (Elapsed time 00:02:00)
programmer 'FPL11LPT1' : Executing action PROGRAM PASSED.

                         o - o - o - o - o - o
```

Ready C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\designer\impl1\top.stp SINGLE

# FlashPro 4.2
## *Connecting Multiple Programmers*

- FlashPro 4.2 Supports Connecting Multiple Programmers To One Computer



| | Programmer Name | Programm Type |
|---|---|---|
| 1 | FPL11LPT1 | FlashProLite |

```
programmer 'FPL11LPT1' : Finished: Mon Nov 28 16
programmer 'FPL11LPT1' : Executing action PROGRA

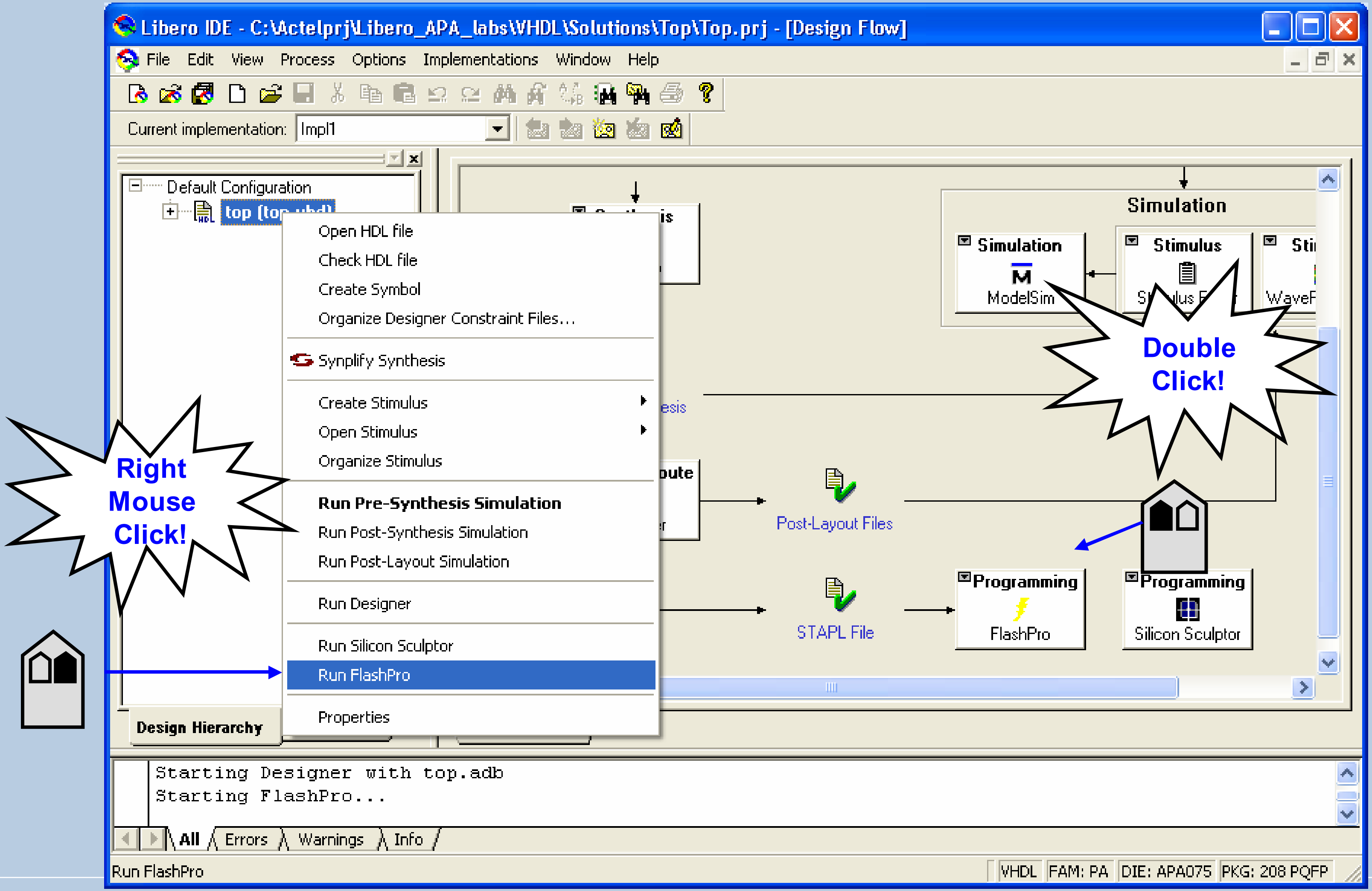
                         o - o - o - o - o - o
```

Connect the selected programmer(s) | C:\Actelprj\Libero_APA_labs\VHDL\Solutions\Top\designer\impl1\top.stp | SINGLE

**Select or un-select all programmers**

# Invoking Programming Software from Libero

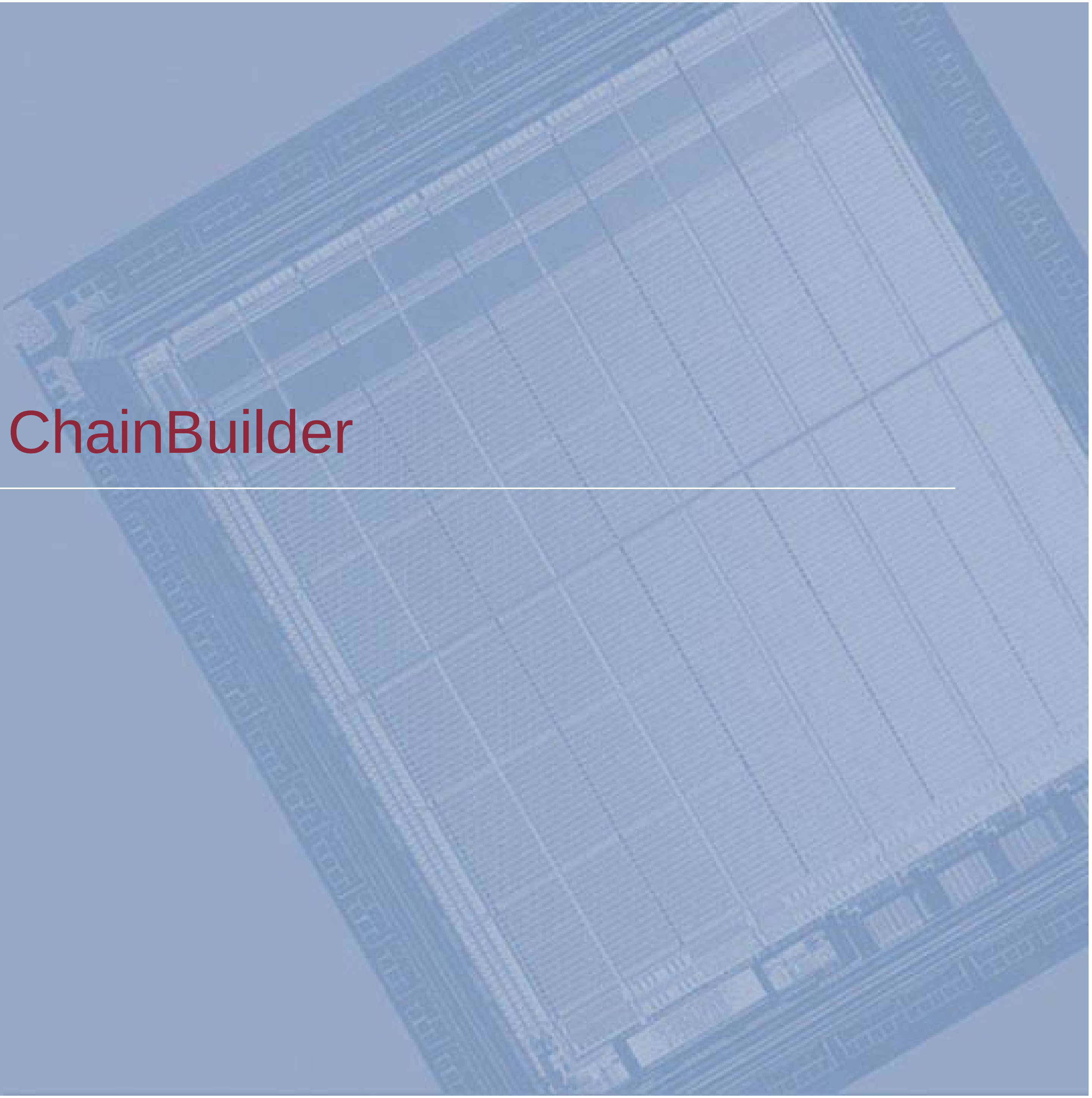
- Click on “Programming” in Design Flow Window or…



```
Starting Designer with top.adb
Starting FlashPro...
```

# ChainBuilder

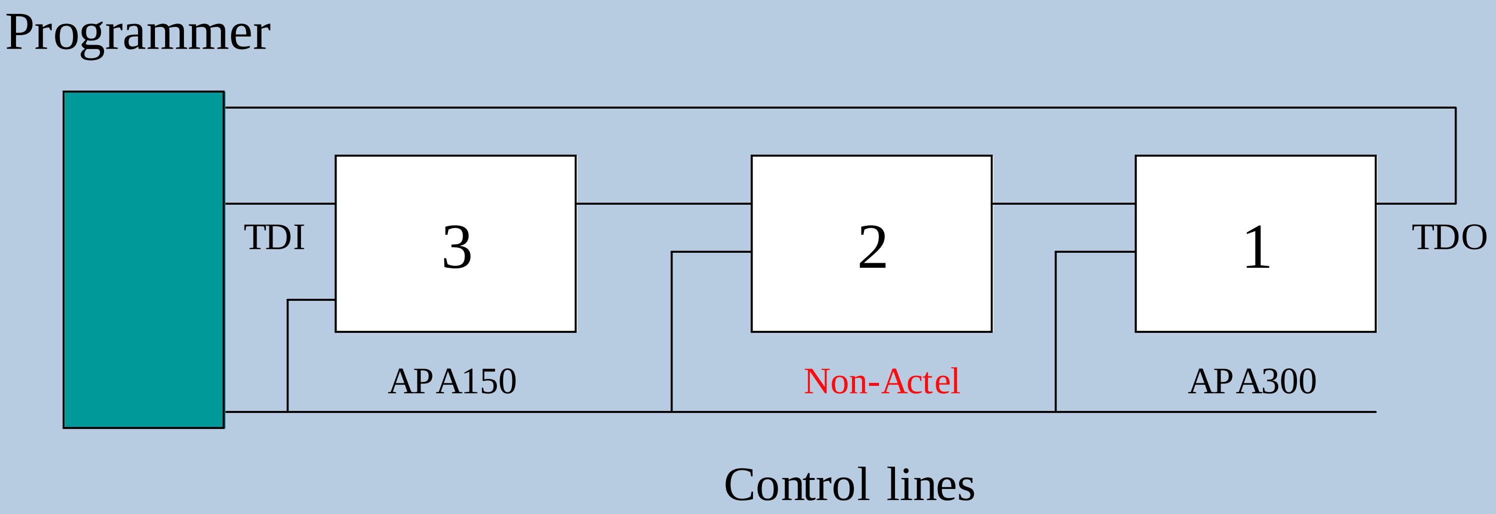
Actel



# ChainBuilder

*Overview*

ChainBuilder Allows ProASIC3\E and ProASIC$^{\underline{\text{PLUS}}}$ FPGAs to be Programmed in JTAG Chains Containing non-Actel Devices



# ChainBuilder
*Features*

## Main Features

- **GUI Assignment of STAPL Files to Individual Fusion, ProASIC3\E and ProASIC$^{\underline{PLUS}}$ Devices**
- **Builds Single STAPL File to Program Multiple Devices in Chain**
- **Project File for Portability**

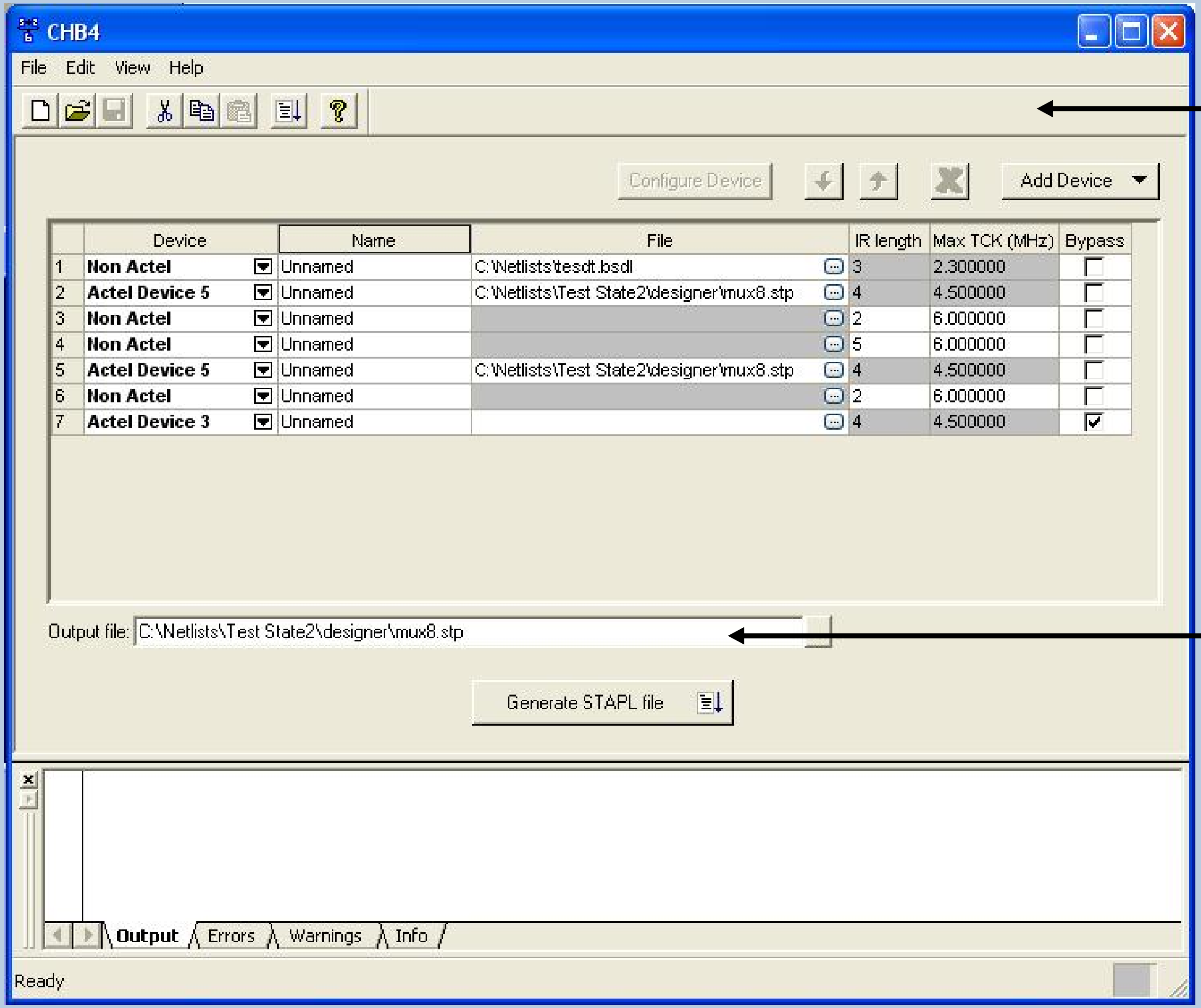
## Non-Actel Device Support

- **BSDL Support to Define non-Actel Devices**
- **IR (Instruction Register) Length Entry to Define non-Actel Devices**

## Serial Programming

- **Devices Programmed One at a Time**
- **Two Devices = Twice the Programming Time**

# ChainBuilder
## *Main Window*



| | Device | Name | File | IR length | Max TCK (MHz) | Bypass |
|---|---|---|---|---|---|---|
| 1 | Non Actel | Unnamed | C:\Netlists\tesdt.bsdl | 3 | 2.300000 | ☐ |
| 2 | Actel Device 5 | Unnamed | C:\Netlists\Test State2\designer\mux8.stp | 4 | 4.500000 | ☐ |
| 3 | Non Actel | Unnamed | | 2 | 6.000000 | ☐ |
| 4 | Non Actel | Unnamed | | 5 | 6.000000 | ☐ |
| 5 | Actel Device 5 | Unnamed | C:\Netlists\Test State2\designer\mux8.stp | 4 | 4.500000 | ☐ |
| 6 | Non Actel | Unnamed | | 2 | 6.000000 | ☐ |
| 7 | Actel Device 3 | Unnamed | | 4 | 4.500000 | ☑ |

Output file: C:\Netlists\Test State2\designer\mux8.stp

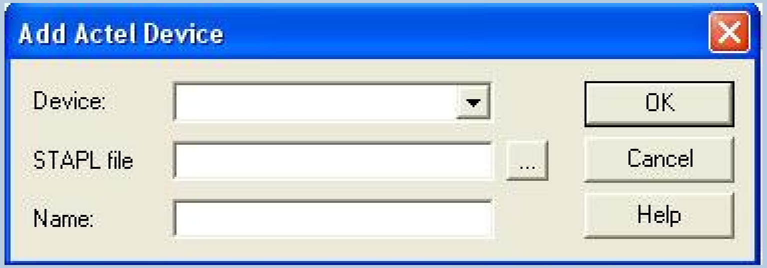
**Tool Bar**

Main Window:
- **Lists the devices in the chain**
- **Lists the associated STAPL file (for APA devices)**
- **Can bypass devices that are not going to be programmed**
  - ◆Non-APA devices are forced to bypass
- **Copy, export or print the list of devices in the chain**

**Output File**

Output Window:
- **Lists Warnings and Error Messages**
- **Warning means there is an error but the STAPL file can be generated**
- **Error implies STAPL file will not be generated**
- **Output window can be copied, exported or printed**

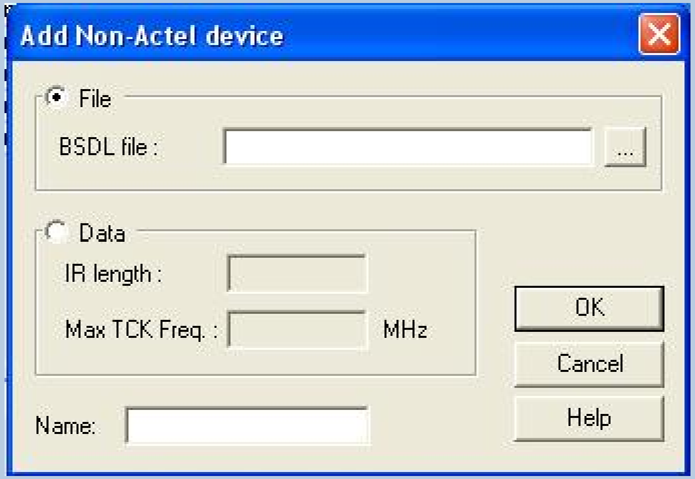
# ChainBuilder
## *Adding a Device*


Add Actel Device

Device:

STAPL file

Name:


Add Non-Actel device

● File

BSDL file :

○ Data

IR length :

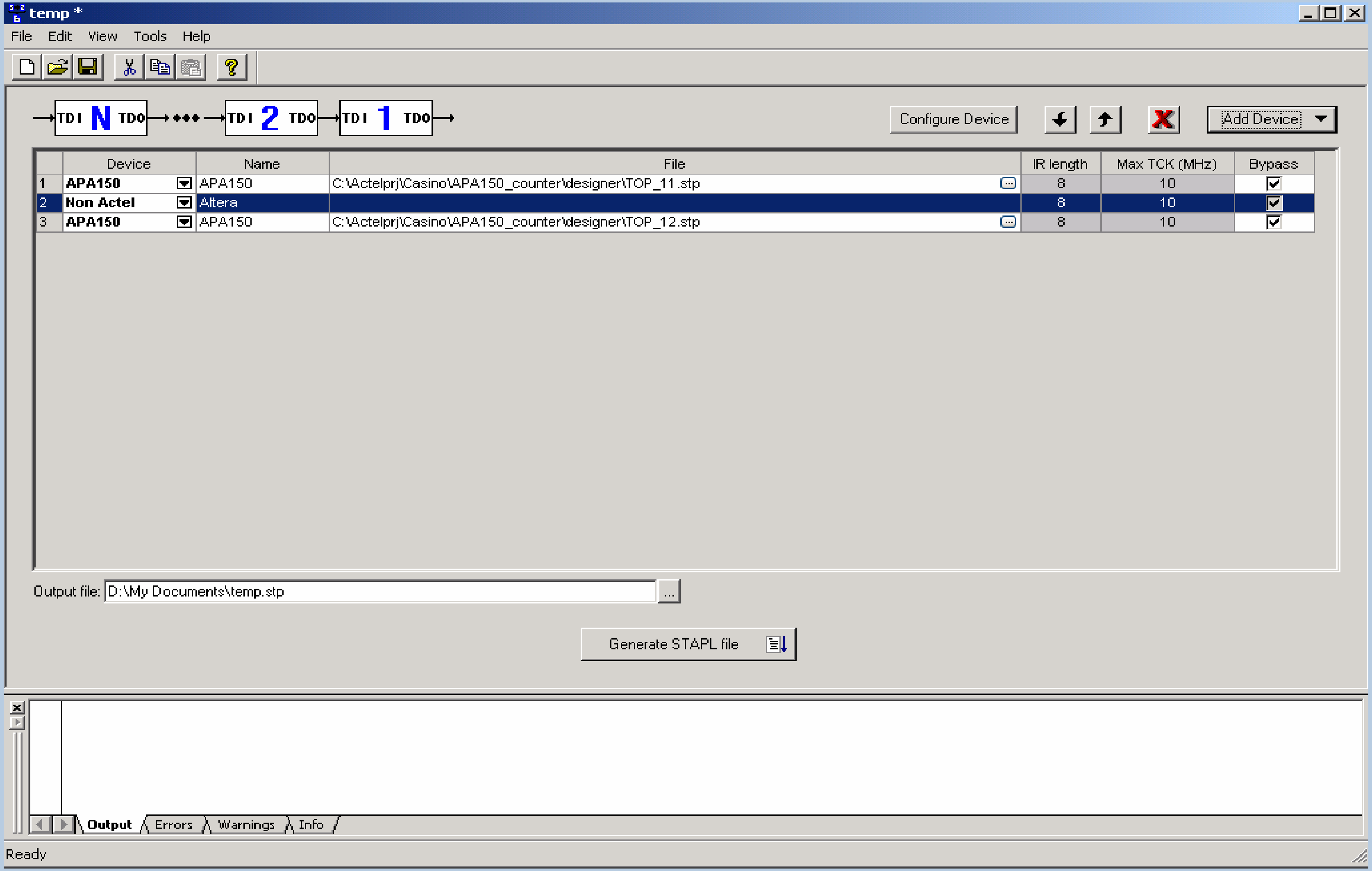
Max TCK Freq. : MHz

Name:

- Actel Device
  - Lists Actel Devices Available
  - User Can Specify Custom Name
  - User Can Select STAPL File
- Non-Actel Device
  - User Can Select BSDL File
    - Provides Max TCK Frequency and IR Length for Device
  - Users Can Enter Data Directly if They Do Not Have Access to BSDL File
  - User Can Enter Custom Name for Device

ONECHIP is all you need

# ChainBuilder
## *Adding a Device (cont.)*



temp *
File Edit View Tools Help
TDI N TDO ••• TDI 2 TDO TDI 1 TDO
Configure Device
Add Device
Output Errors Warnings Info
Ready

|   | Device | Name | File | IR length | Max TCK (MHz) | Bypass |
|---|---|---|---|---|---|---|
| 1 | APA150 | APA150 | C:\Actelprj\Casino\APA150_counter\designer\TOP_11.stp | 8 | 10 | ☑ |
| 2 | Non Actel | Altera |  | 8 | 10 | ☑ |
| 3 | APA150 | APA150 | C:\Actelprj\Casino\APA150_counter\designer\TOP_12.stp | 8 | 10 | ☑ |

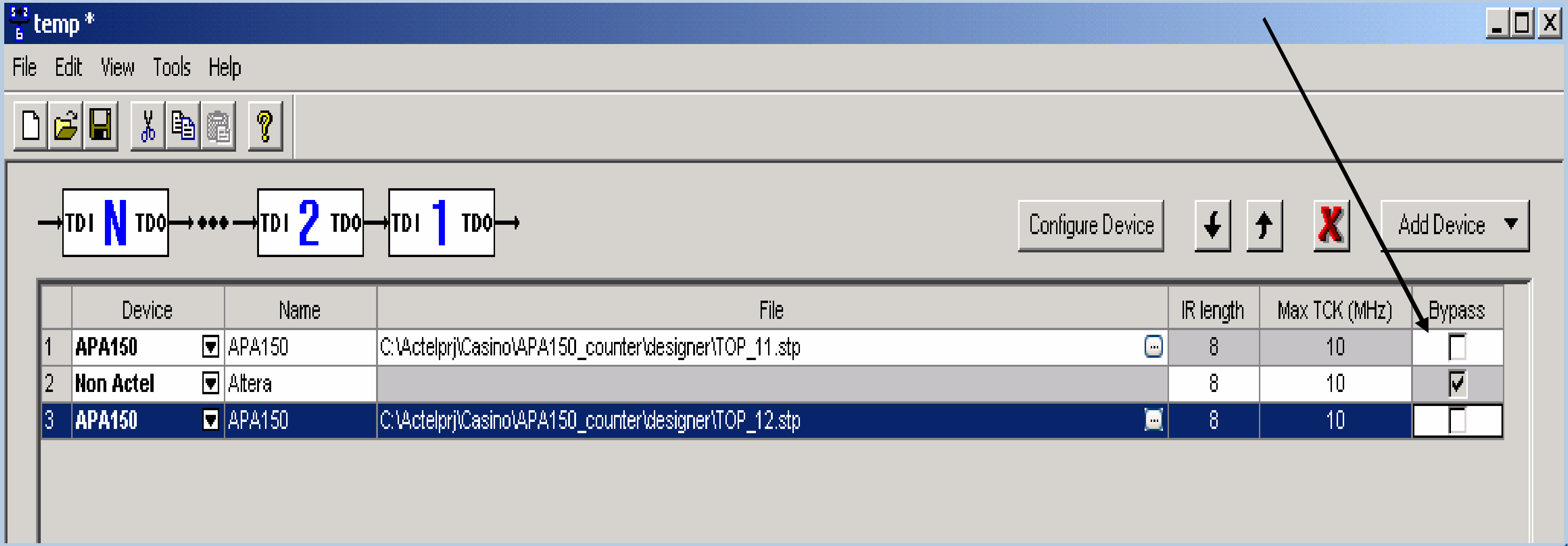
Output file: D:\My Documents\temp.stp

Generate STAPL file

# ChainBuilder
## *Bypass Feature*

- If Device is Checked in Bypass Column, Device Is Bypassed in Chain
  - **No Functions (such as Programming) Are Performed on it**

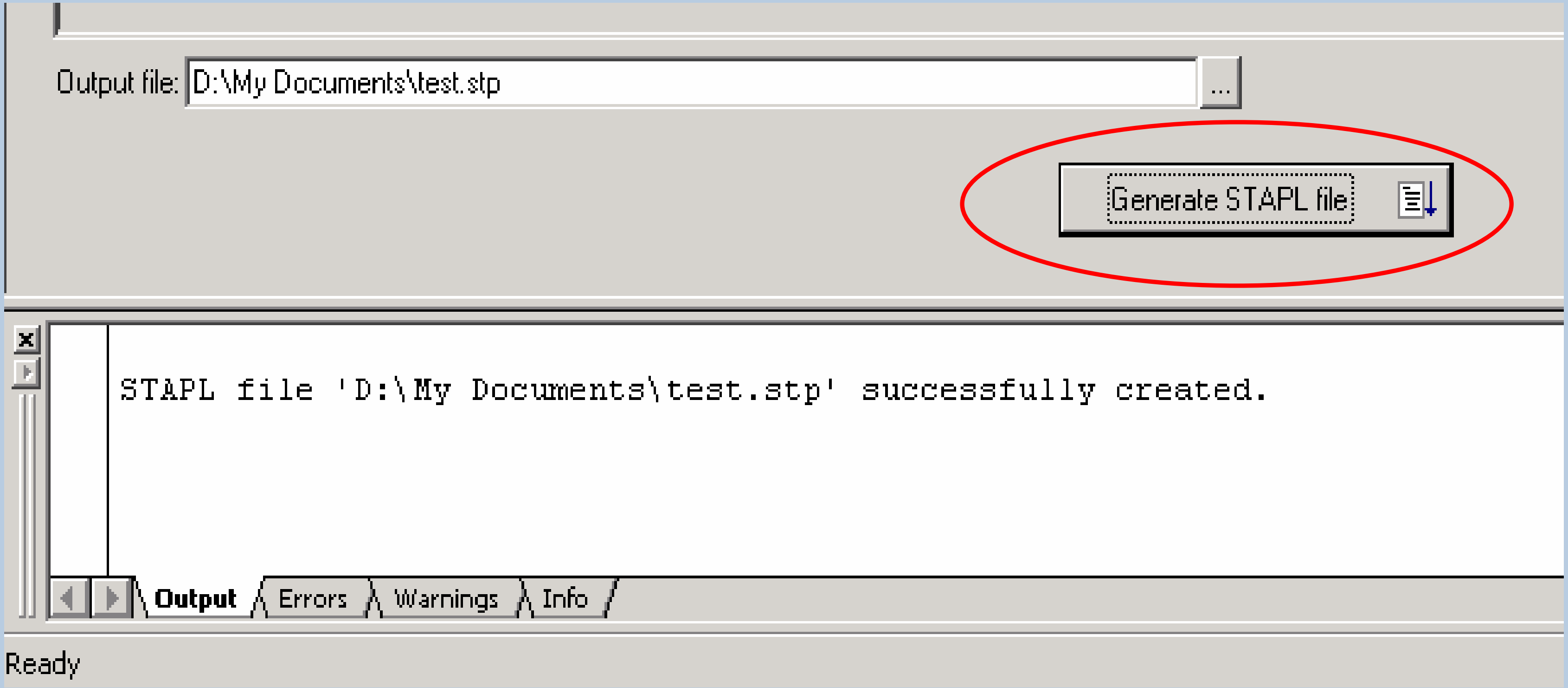
Bypass checkbox



|   | Device | Name | File | IR length | Max TCK (MHz) | Bypass |
|---|---|---|---|---|---|---|
| 1 | **APA150** | APA150 | C:\Actelprj\Casino\APA150_counter\designer\TOP_11.stp | 8 | 10 | □ |
| 2 | **Non Actel** | Altera |  | 8 | 10 | ☑ |
| 3 | **APA150** | APA150 | C:\Actelprj\Casino\APA150_counter\designer\TOP_12.stp | 8 | 10 | □ |

# ChainBuilder
## *Generate STAPL File*

- Click Generate STAPL File Button to Generate STAPL File for JTAG Chain

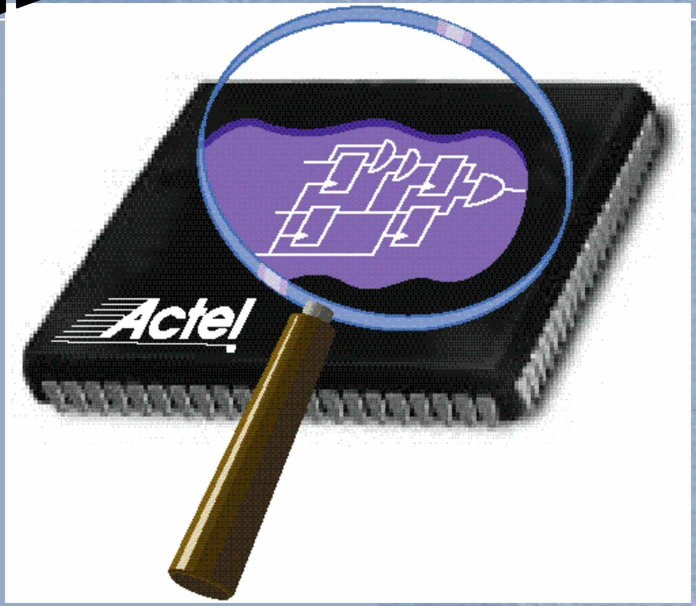


Output file: D:\My Documents\test.stp

```
STAPL file 'D:\My Documents\test.stp' successfully created.
```

# Silicon Explorer

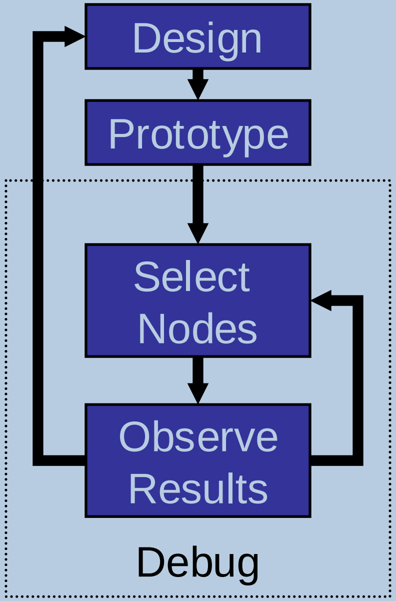
Actel

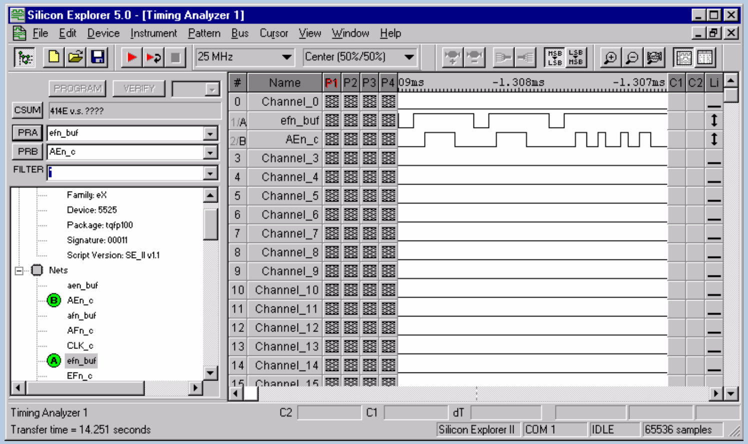


# Silicon Explorer

## Debug Designs in Real Time!

- **Select Internal FPGA Nodes on the Fly for Viewing while Device Runs at FULL Speed!**
- **Reduce Debug Time and Decrease your Time to Market!**




Silicon Explorer 5.0 - [Timing Analyzer 1]
File Edit Device Instrument Pattern Bus Cursor View Window Help
PROGRAM
VERIFY
09ms
-1.308ms
-1.307ms
C1 C2 Li
MSB LSB
LSB MSB

25 MHz

Center (50%/50%)

CSUM 414E v.s. ????

PRA efn_buf

PRB AEn_c

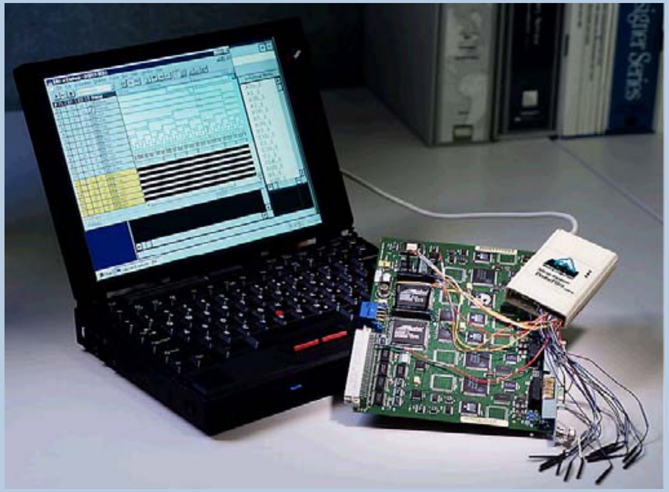
FILTER

- Family: eX
- Device: 5525
- Package: tqfp100
- Signature: 00011
- Script Version: SE_II v1.1
- Nets
  - aen_buf
  - B AEn_c
  - afn_buf
  - AFn_c
  - CLK_c
  - A efn_buf
  - EFn_c

| # | Name | P1 | P2 | P3 | P4 |
|---|---|---|---|---|---|
| 0 | Channel_0 | | | | |
| 1/A | efn_buf | | | | |
| 2/B | AEn_c | | | | |
| 3 | Channel_3 | | | | |
| 4 | Channel_4 | | | | |
| 5 | Channel_5 | | | | |
| 6 | Channel_6 | | | | |
| 7 | Channel_7 | | | | |
| 8 | Channel_8 | | | | |
| 9 | Channel_9 | | | | |
| 10 | Channel_10 | | | | |
| 11 | Channel_11 | | | | |
| 12 | Channel_12 | | | | |
| 13 | Channel_13 | | | | |
| 14 | Channel_14 | | | | |
| 15 | Channel_15 | | | | |

Timing Analyzer 1 C2 C1 dT

Transfer time = 14.251 seconds Silicon Explorer II COM 1 IDLE 65536 samples



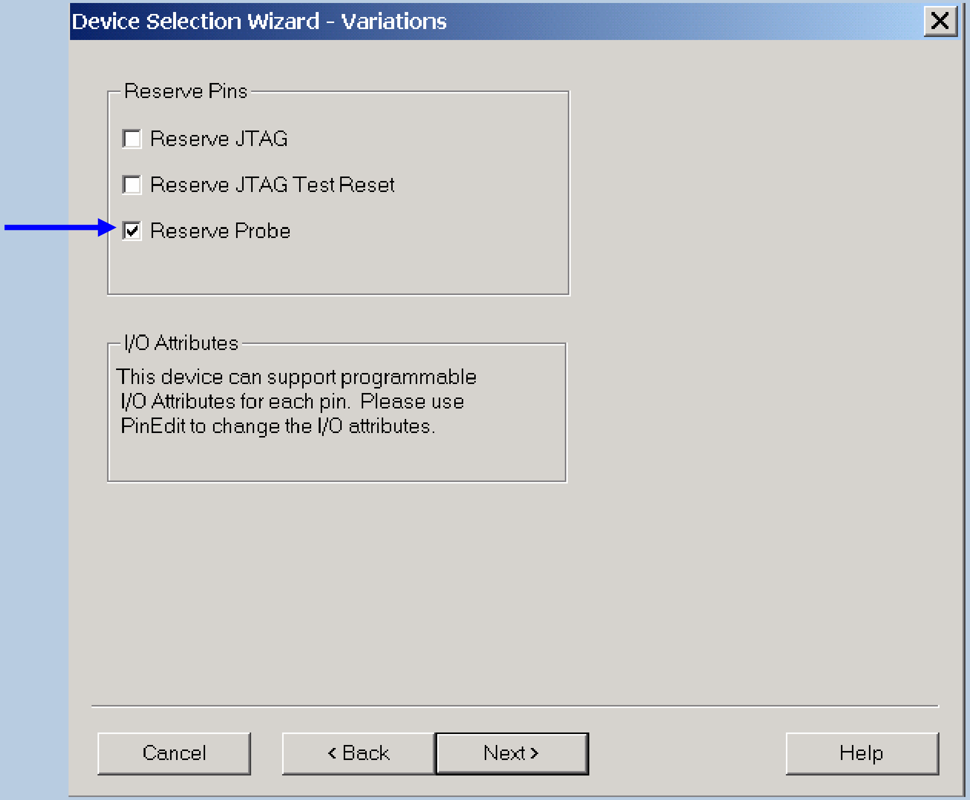
ONE CHIP is all you need

# Preparing for Debug

- If Possible, Avoid Using Probe Pins for Regular User I/O

Reserve Probe pins during compilation

- Make Probe Pins Accessible
  - **Jumper Leads, Dedicated Connector**



Device Selection Wizard - Variations

Reserve Pins

□ Reserve JTAG

□ Reserve JTAG Test Reset

☑ Reserve Probe

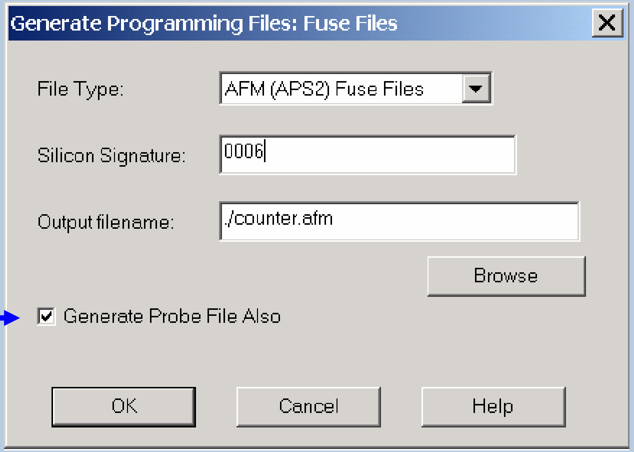
I/O Attributes

This device can support programmable I/O Attributes for each pin. Please use PinEdit to change the I/O attributes.

# Preparing for Debug (cont.)

- Silicon Explorer Used for Debugging
  - **Can Probe any Two INTERNAL Nodes in Real Time**
  - **Four Internal Nodes for Axcelerator**
- Also Functions as 18-channel Logic Analyzer
- Needs Only .prb File to Allow Debugging.
- Security Fuse Should NOT Be Programmed on Device

Generate Probe file →



Generate Programming Files: Fuse Files

File Type: AFM (APS2) Fuse Files

Silicon Signature: 0006

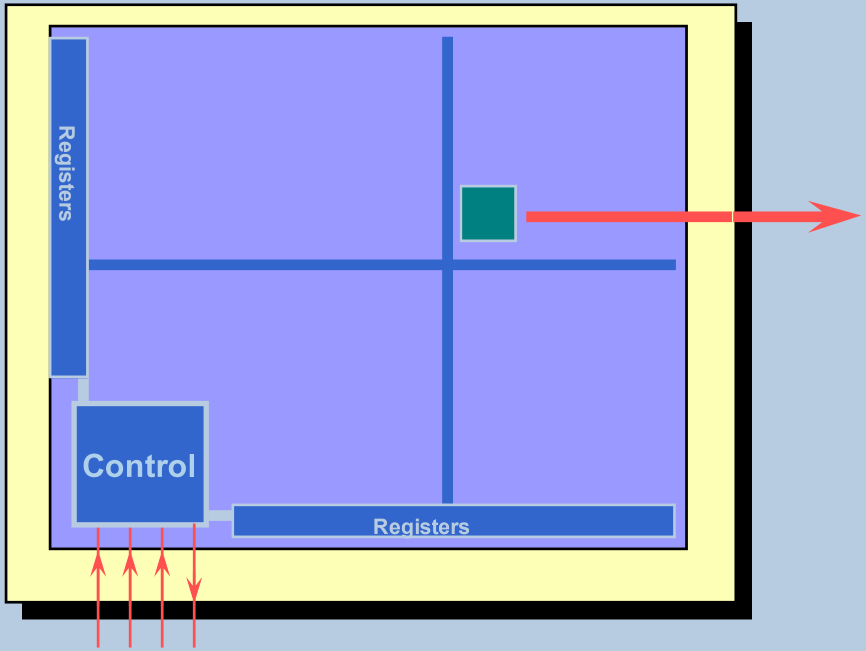
Output filename: ./counter.afm

☑ Generate Probe File Also

ONECHIP is all you need

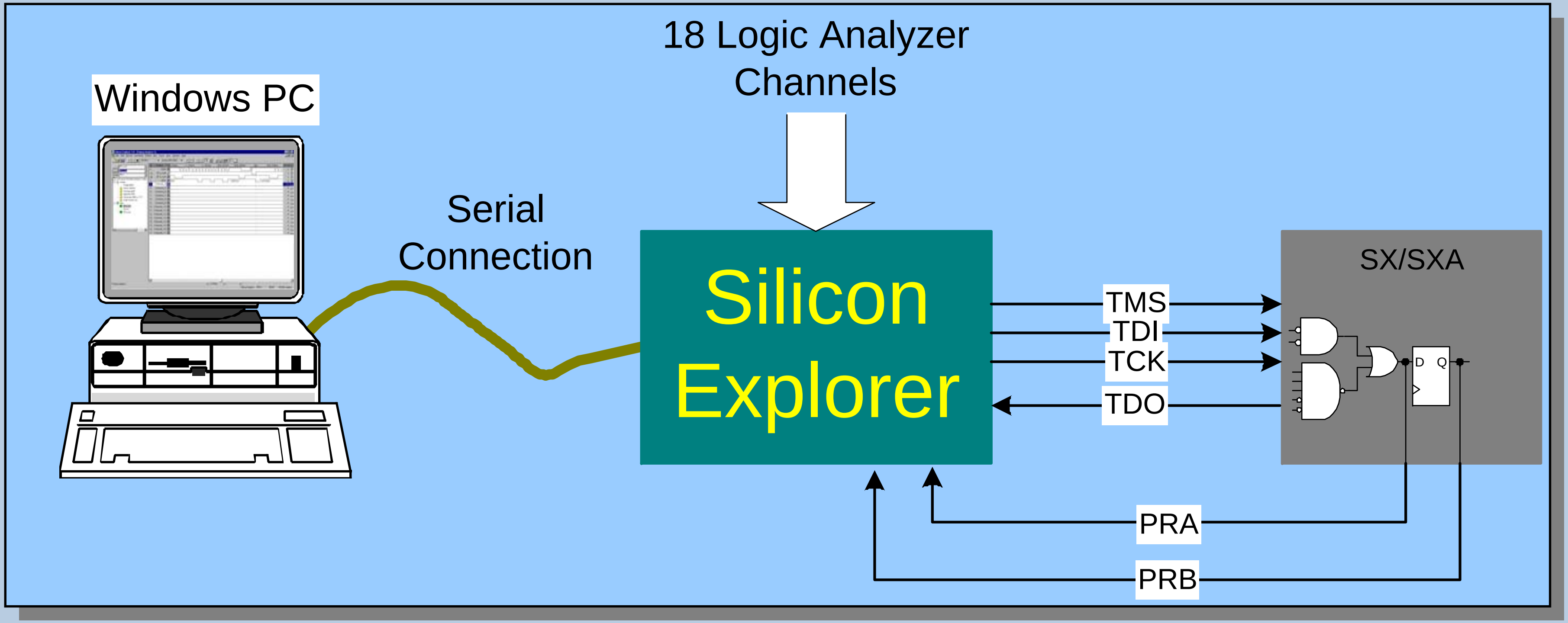
# Action Probe Circuitry

- Dynamic Internal Node Access
  - No Changes to Timing Relationships
  - No Changes to Fan-out or Node Loading
- Patented Architectural Feature
  - Antifuse Devices Only
  - Unique to Actel
- No Silicon Overhead
  - Uses Zero Logic Resources
  - Always there if Needed



# Silicon Explorer Setup

*SX/SX-A/eX*



# Silicon Explorer II

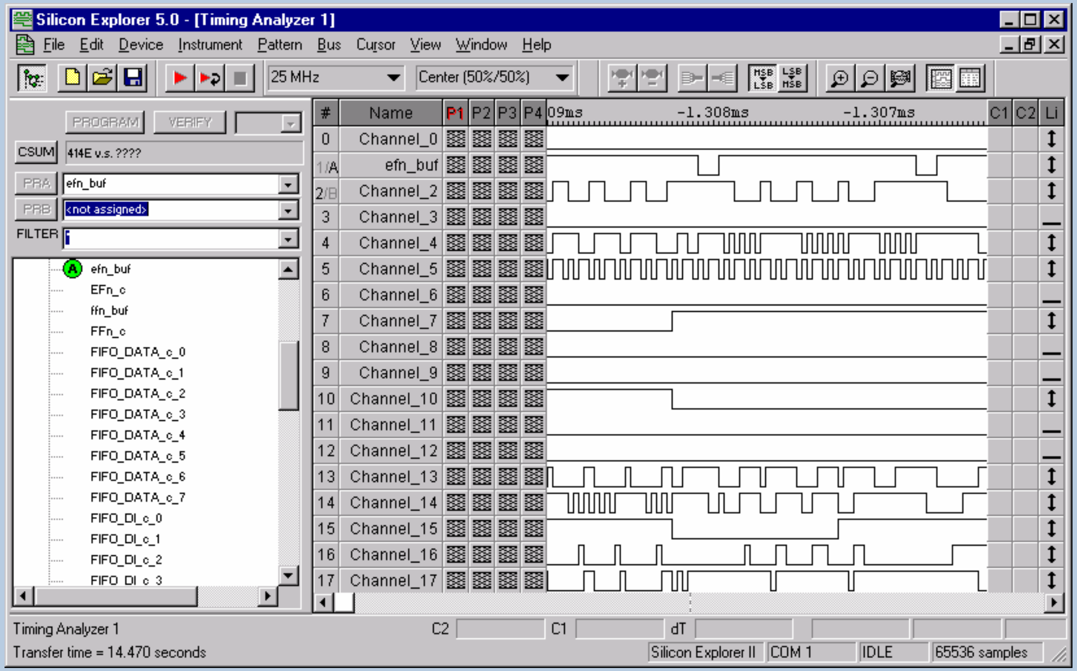
- Action Probe Control
- Serial Port Connection
  - No Plug-in Cards
- High-speed Signal Acquisition
- Sampling Rate
  - 100MHz Asynchronous
  - 66 MHz Synchronous
- Analyze PC-hosted Software
- Optional External Power Supply (Recommended for SX-A)
- Multilevel Triggering

# Silicon Explorer Software

## Full-featured 18 channel Logic Analyzer

- Flexible Signal Assignment
- Signal Grouping, Bussing
  - Decimal, Hex, Binary, Analog Radix Selection for Bussed Signals
- Edge and Level Trigger Selection
- 64K Samples per Channel

- Easy-to-learn, Easy-to-use Interface



25 MHz

Center (50%/50%)

CSUM 414E v.s. ????

PRA efn_buf

PRB <not assigned>

FILTER

efn_buf
EFn_c
ffn_buf
FFn_c
FIFO_DATA_c_0
FIFO_DATA_c_1
FIFO_DATA_c_2
FIFO_DATA_c_3
FIFO_DATA_c_4
FIFO_DATA_c_5
FIFO_DATA_c_6
FIFO_DATA_c_7
FIFO_DI_c_0
FIFO_DI_c_1
FIFO_DI_c_2
FIFO_DI_c_3

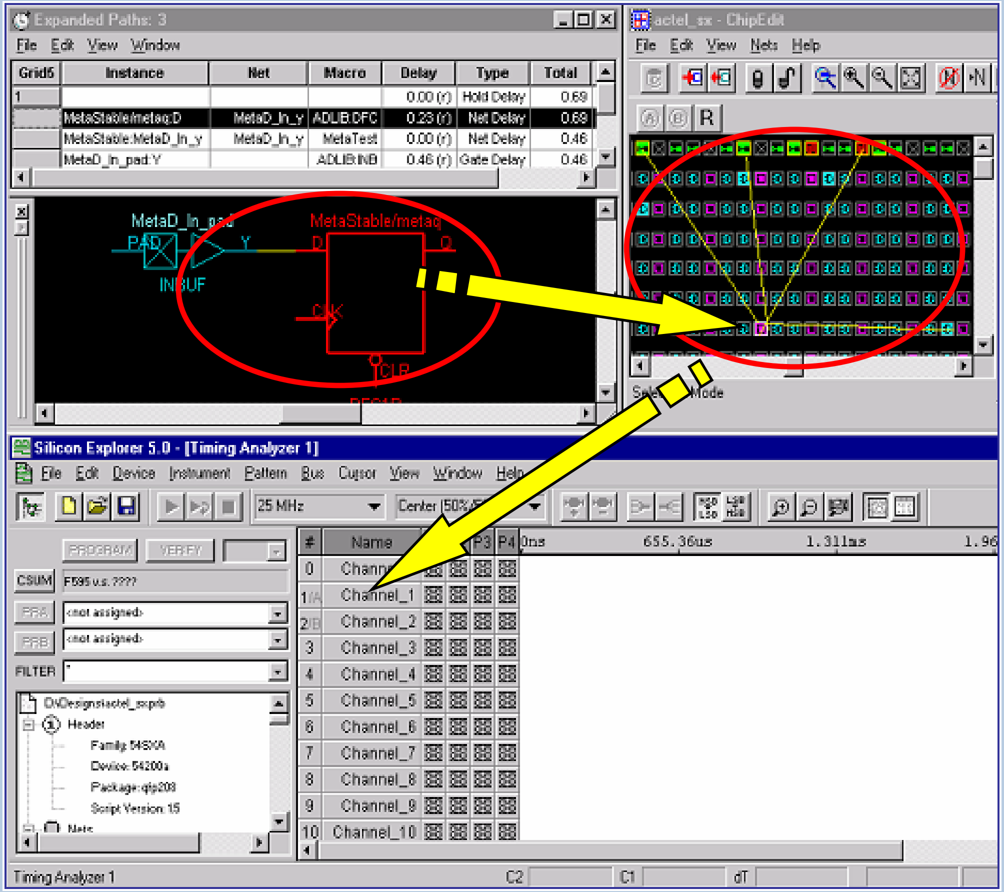
| # | Name |
|---|---|
| 0 | Channel_0 |
| 1/A | efn_buf |
| 2/B | Channel_2 |
| 3 | Channel_3 |
| 4 | Channel_4 |
| 5 | Channel_5 |
| 6 | Channel_6 |
| 7 | Channel_7 |
| 8 | Channel_8 |
| 9 | Channel_9 |
| 10 | Channel_10 |
| 11 | Channel_11 |
| 12 | Channel_12 |
| 13 | Channel_13 |
| 14 | Channel_14 |
| 15 | Channel_15 |
| 16 | Channel_16 |
| 17 | Channel_17 |

Timing Analyzer 1 C2 C1 dT

Transfer time = 14.470 seconds Silicon Explorer II COM 1 IDLE 65536 samples

# Designer Cross-Probing

- Designer Allows you to Verify and Optimize your Design
- Silicon Explorer II Helps you Perform In-system Debugging
- Cross-Probing Links All Design Views



| Grid5 | Instance | Net | Macro | Delay | Type | Total |
|---|---|---|---|---|---|---|
| 1 | | | | 0.00 (r) | Hold Delay | 0.69 |
| | MetaStable/metaq:D | MetaD_In_y | ADLIB:DFC | 0.23 (r) | Net Delay | 0.69 |
| | MetaStable:MetaD_In_y | MetaD_In_y | MetaTest | 0.00 (r) | Net Delay | 0.46 |
| | MetaD_In_pad:Y | | ADLIB:INB | 0.46 (r) | Gate Delay | 0.46 |

CSUM: F595 v.s. ????

PRA: <not assigned>

PRB: <not assigned>

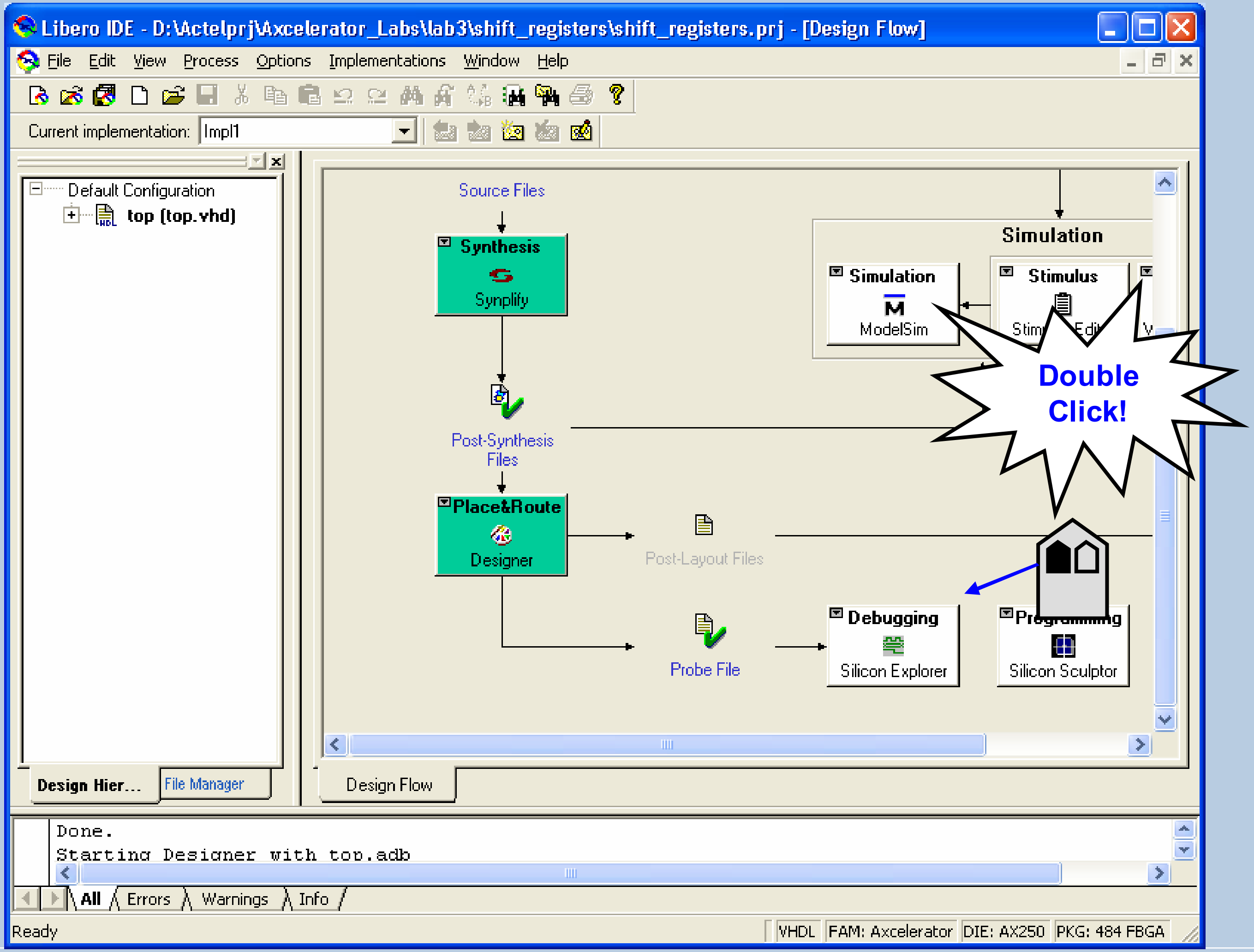
FILTER: *

D:\Designs\actel_sx.prb
Header
Family: 54SXA
Device: 54200a
Package: qfp208
Script Version: 15
Nets

| # | Name |
|---|---|
| 0 | Chann |
| 1/A | Channel_1 |
| 2/B | Channel_2 |
| 3 | Channel_3 |
| 4 | Channel_4 |
| 5 | Channel_5 |
| 6 | Channel_6 |
| 7 | Channel_7 |
| 8 | Channel_8 |
| 9 | Channel_9 |
| 10 | Channel_10 |

# Invoking Silicon Explorer

- Click on "Silicon Explorer" in Design Flow Window



```
Done.
Starting Designer with top.adb
```

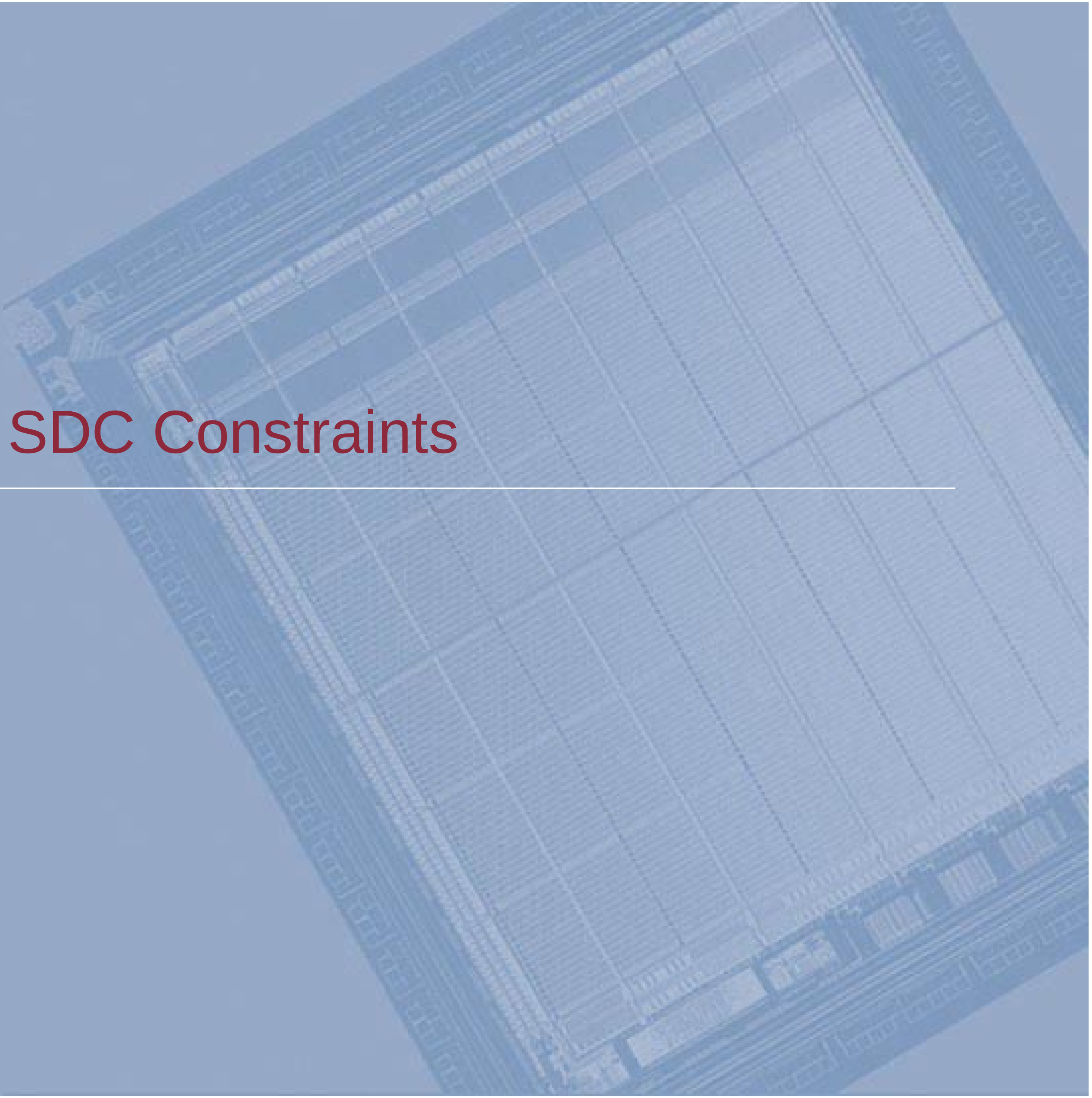
# Summary

- Libero FPGA Design Suite Includes:
  - Design Entry
    - ViewDraw, HDL Editor, SmartGen
  - Synthesis
    - Synplicity
  - Physical Synthesis
    - Magma PALACE
  - Verification
    - ModelSim, WaveFormer Lite
  - Designer (P&R, Timing Analysis and Constraints)
- Actel Continues to Improve Libero IDE
  - Increased Quality of Results
  - Ease of Use
  - Additional Features

# Back-up Slides

Actel

# SDC Constraints

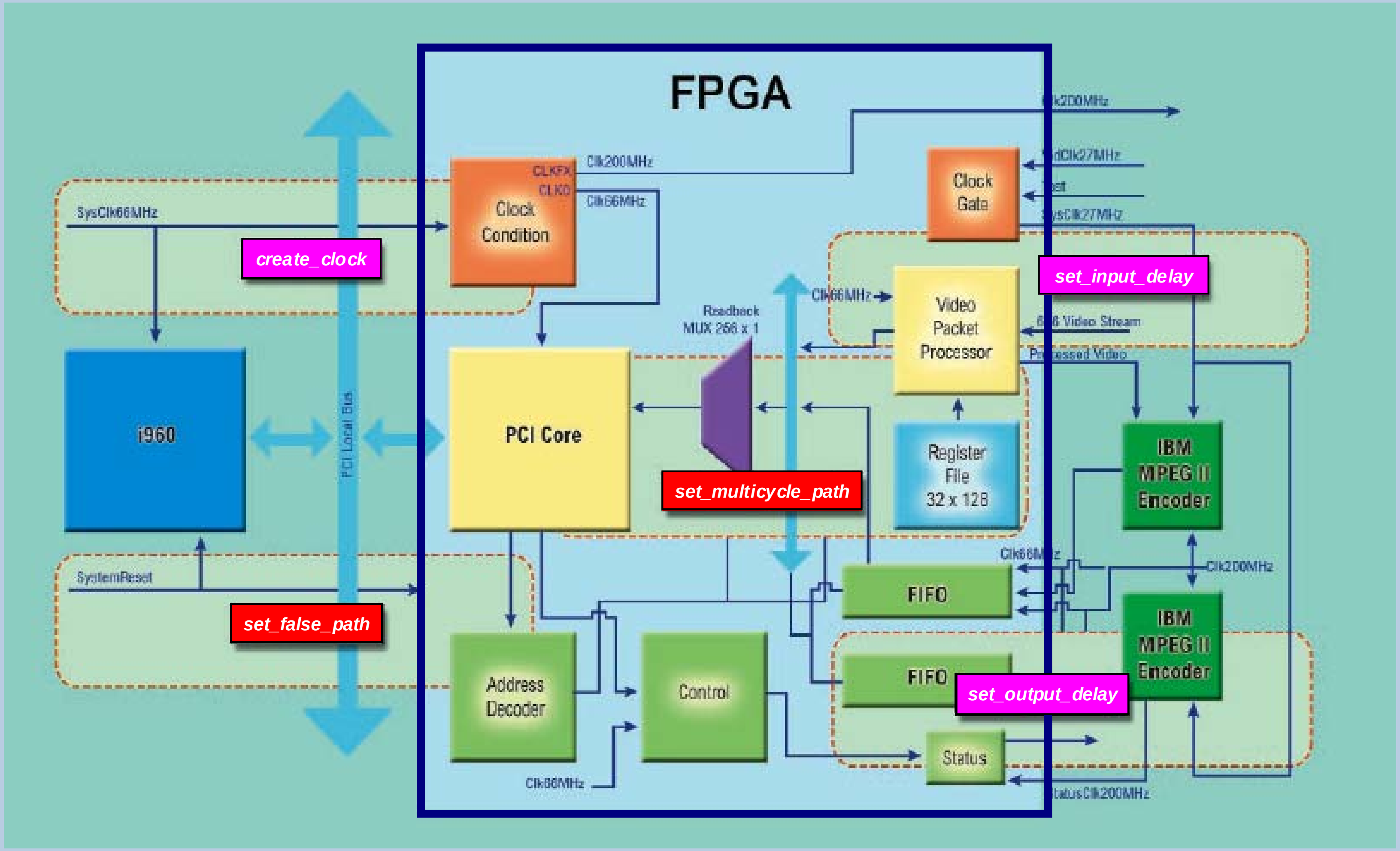


# SmartTime
## *Supported SDC Constraints*

- Synopsys Design Constraint (SDC) is the Accepted File Format for Timing Constraints
- SmartTime Supports the Following SDC Constraints:
  - `create_clock`
  - `set_input_delay`
  - `set_output_delay`
  - `set_false_path –from –through –to`
  - `set_ multicycle_path –from –through –to`

# Timing Constraints
## *Board-Level View*

- Constraining FPGA Designs with SDC

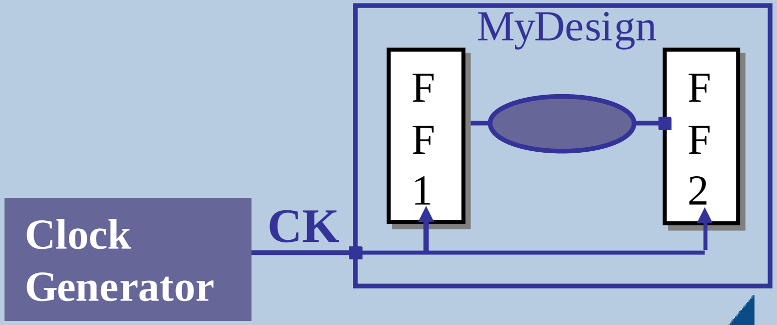


Source: Mentor Graphics Corporation ©, 2002

# Clock Constraints in SDC
## `create_clock`

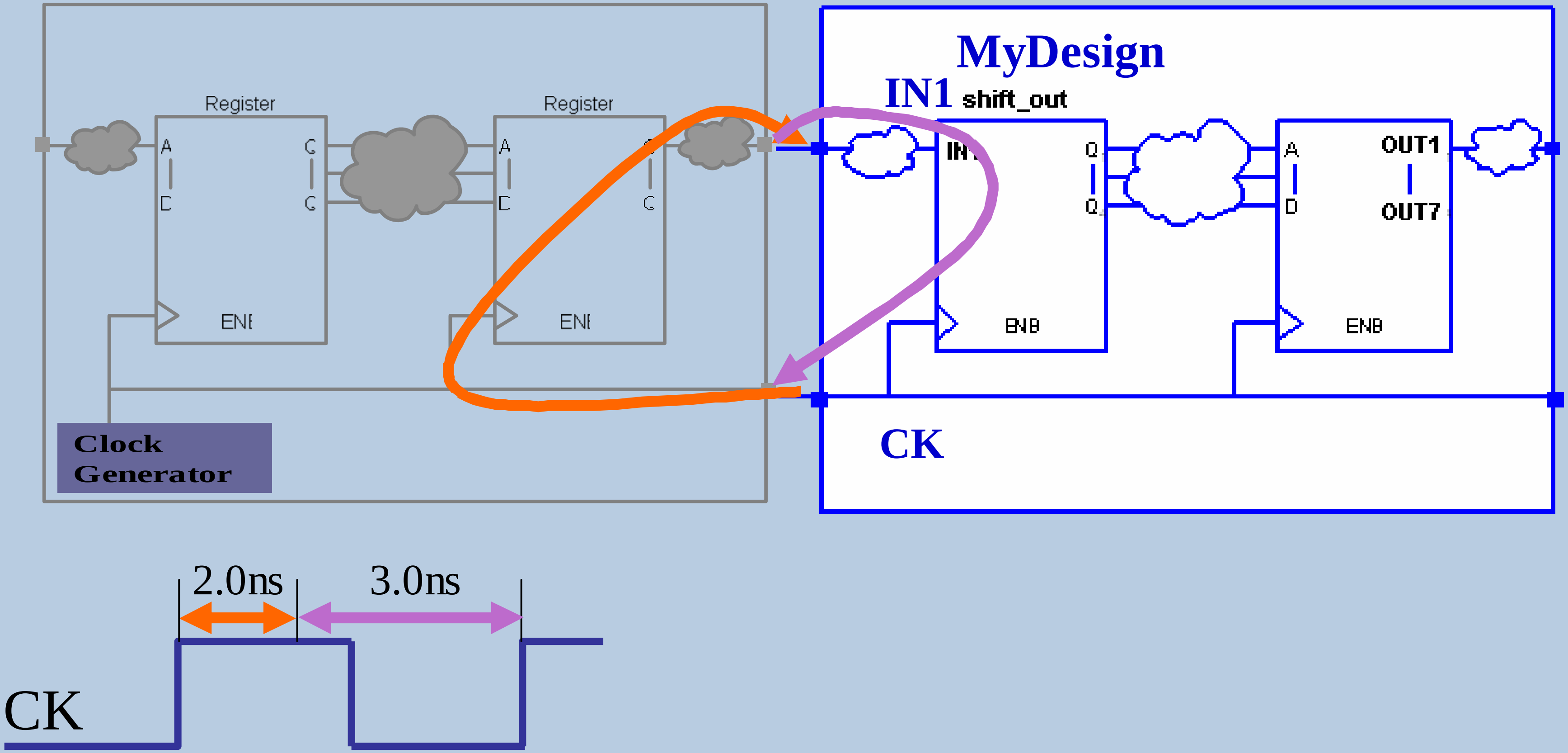
- Specifies Clock Domain Frequency
- Features
  - **Propagation Delays Are Computed to Each Flip-flop**
  - **Clock Skew Is Computed for Each Connected Pair of Flip-flops**
  - **Setup and Hold Checks Are Performed for Constrained Clock Domains**
- Syntax:
  - `create_clock -period period_value  [-waveform edge_list] source`

```
create_clock  -period 2.0 [get_ports {CK}]
```



# Input Delays in SDC
# `set_input_delay`

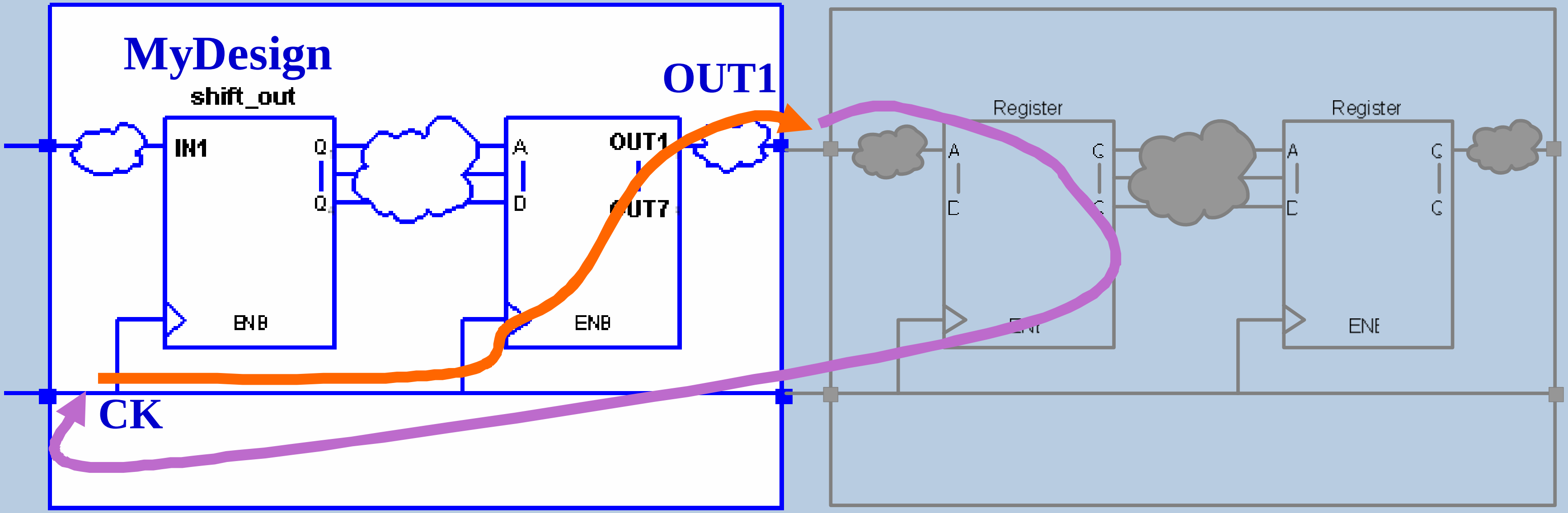
- Specifies Arrival Time at an Input Port Relative to a Clock Edge

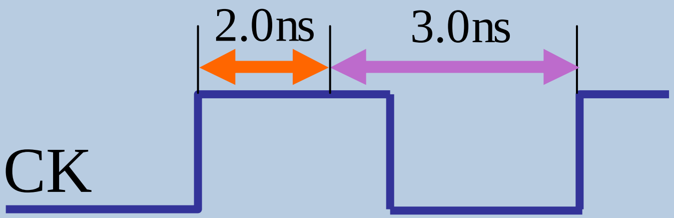


**SDC:** set_input_delay 2.00 -clock {CK}  {IN1}

# Output Delays in SDC
# `set_output_delay`

- Specifies the Amount of Time Before a Clock Edge for Which the Signal is Required.





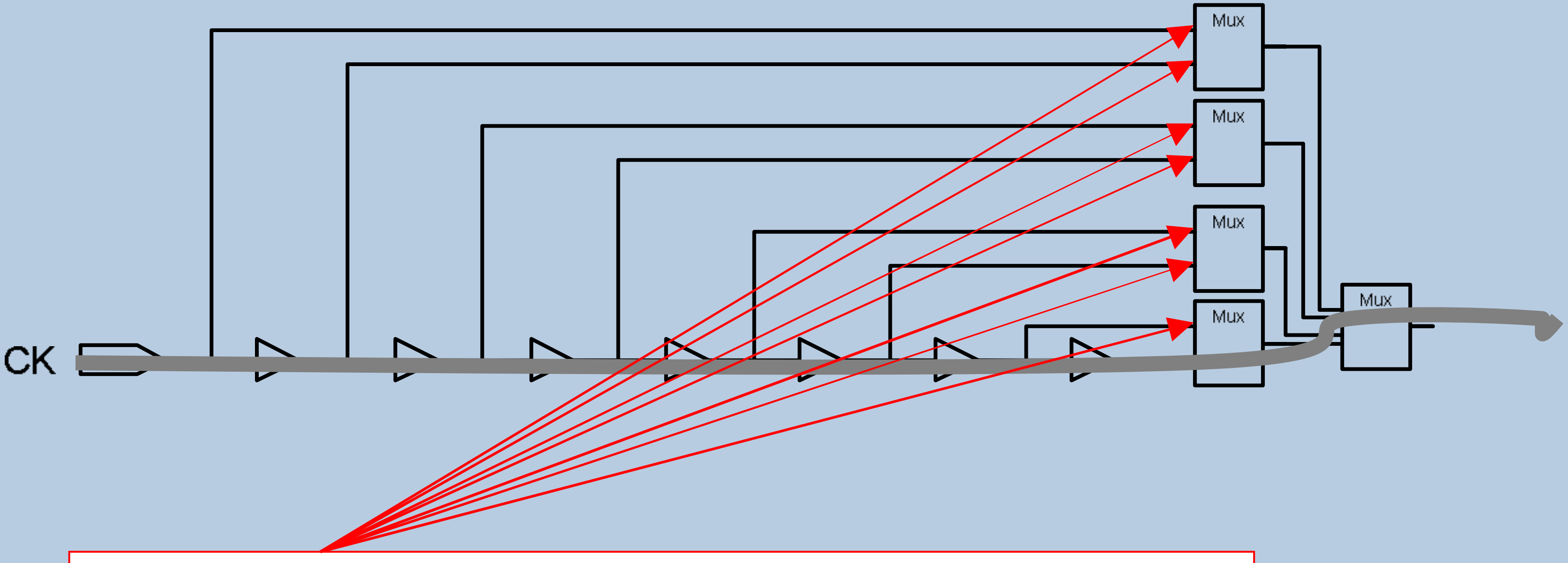
**Option "-min" for hold check**
**Option "-max" for setup check**

**SDC:** set_output_delay –max 3.00 -clock {CK} {OUT1}

# False Paths in SDC
# `set_false_path`

- Identifies Paths that are Considered False and Excluded from the Timing Analysis.
- Syntax

```
set_false_path [-from from_list] [-through through_list]
  [-to to_list]
```



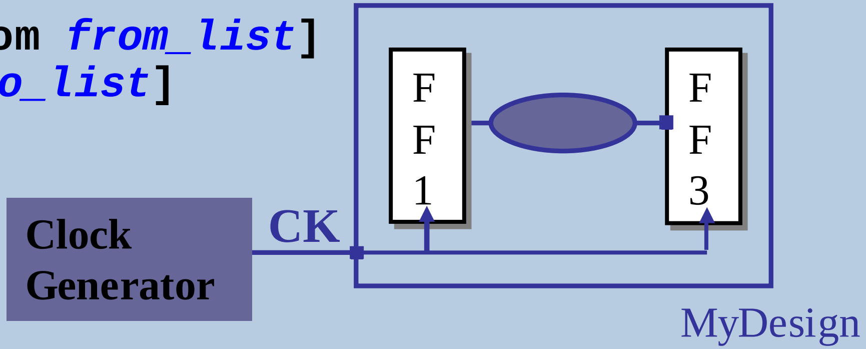
**SDC: set_false_path –through i1 i2 i3 i4 i5 i6 i7**

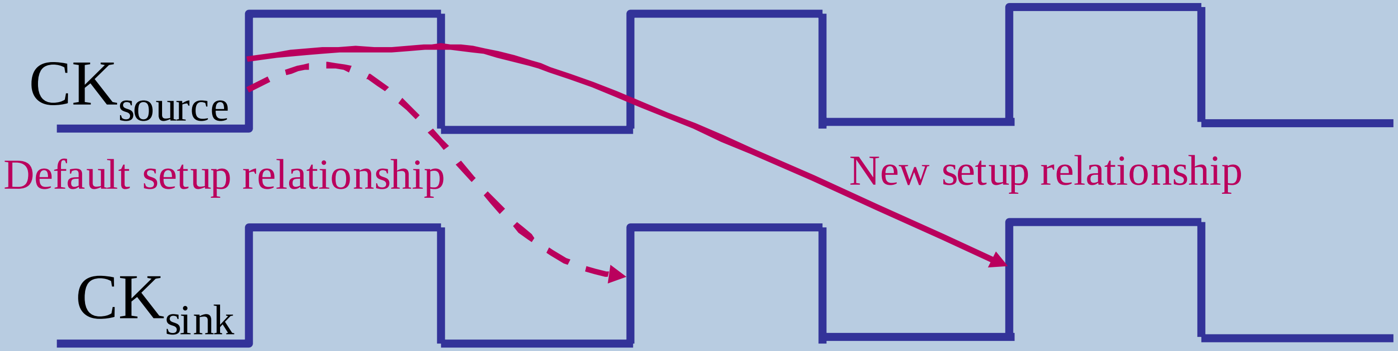
# Multicycle Paths in SDC
# `set_multicycle_path`

- Specifies Paths Where Allowable Data Path Delay Is More Than One Clock Cycle

- Syntax:

```
set_multicycle_path ncycles [-from from_list]
  [–through through_list] [-to to_list]
```





```
set_multicycle_path  2 -from [get_pins {FF1*}] -to {FF3:D}
```