The Abdus Salam
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ICTP-INFN Advanced Tranining Course on
FPGA and VHDL for Hardware Simulation and Synthesis
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Introduction

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These lecture notes are intended only for distribution to participants

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Introduction to VLSI ASIC Design and Technology

Paulo Moreira &
Jorgen Christiansen
CERN - Geneva, Switzerland

First half of this course is compressed set of transparencies from Paulo Moreira:
http://paulo.moreira.free.fr/

Overview

- Part 1: Basic CMOS technology (from Paulo Moreira)
  - CMOS Transistors
  - Parasitics
  - The CMOS inverter
  - Technology
  - Scaling
- Part 2: BASIC CMOS digital building blocks (from Paulo Moreira)
  - Gates: NAND, NOR, PASS
  - Sequential: Latch, Flip-Flop
  - Interconnects
  - Memory: ROM, RAM, PROM, FLASH , ,
  - A bit about Delay and phase locked loops (if time allows)
- Part 3: IC design methodology and Tools
  - Dealing with complexity
  - Low power
  - Design styles
  - Tools: Layout, simulation, HDL, P&R, synthesis
- Part 4: Packaging, Testing and good design practices
  - Package types
  - Cooling
  - I/O signals
  - How to test IC's
  - What not to do (if time allows)
- Part 5: Where is all this heading ?
  - Technology changes
  - Scaling of delays and implications on design tools
  - New technologies
- (Part 6): What is this "CERN thing"