The Abdus Salam
International Centre for Theoretical Physics

United Nations Educational, Scientific and Cultural Organization

IAEA International Atomic Energy Agency

First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific

16 June - 11 July 2008

Kuala Lumpur – Malaysia

The Abdus Salam International Centre for Theoretical Physics (ICTP), Italy, along with the International Islamic University Malaysia (IIUM) and the Tunku Abdul Rahman College, Kuala Lumpur, Malaysia will organize the above mentioned Workshop to be held at IIUM and TARC from 16 June to 11 July 2008.

SUMMARY AND PURPOSE

This Workshop is intended as an advanced training activity in Microelectronics, to introduce engineers, physicists and computer scientists to state-of-the-art design methodologies for Programmable Logic Devices. Emphasis will be placed on electronic system development with Field Programmable Gate Arrays (FPGA) using a Hardware Description Language, VHDL, as cost effective solution for research and training in microelectronics. With recent FPGA architectural evolutions and ever-increasing capacity, it is today possible and affordable to implement all elements of a digital design within an FPGA device. FPGAs are becoming very attractive for cost-effective system prototyping based on advantages such as very low non recurring engineering (NRE) fees, low cost design tools, flexible design cycle, virtually unlimited re-configurability, extreme versatility and performance, and the ability to easily implement and evaluate alternative design architectures. These financial and technological advantages are increasingly attracting the attention of experimental physicists, electronic engineers and computing scientists who see FPGAs as a cost-effective solution for implementing high performance designs in areas such as: Scientific Instrumentation, Telecommunications, Data Acquisition, Digital Signal Processing, Reconfigurable Computing, etc.
The purpose of this activity is to provide training in the latest FPGA design methodologies based on hardware description languages and logic synthesis. In order to promote research and human capacity development in design of microelectronic systems and devices it will also be offered a broad view of modern integrated circuits. This course offers a unique opportunity to get into the FPGA world from basic to complex topics through its intensive program, from step-by-step tutorials to design and implementation of fairly complex projects.

Some of the topics to be covered will include:

- **FPGA**: Technologies, Architectures, Design Methodology and Design Flow, Debugging Techniques
- **VHDL**: Modeling and Simulation, VHDL for Synthesis
- **Digital System Design**: combinational and sequential circuits. Digital Arithmetic
- **Digital Signal Processing**: Fourier Theory, Sampling Theory, Digital filters
- **Reuse methodology for System-on-a-Chip Designs**
- **Introduction to CMOS technology and VLSI design**
- **Hands-on Laboratory Exercises**: VHDL Modeling, Simulation and FPGA Design
- **Actel**: Mixed signal analog-digital FPGA design
- **Altera**: Formal verification techniques and hands on laboratory on systems design
- **Emerald System**: Overview of Microprocessor Architectures & Implementation of a Large Bus Size VLIW Microprocessor on FPGA
- **INTEL:** Validating the Intel Leading-Edge Architecture Microprocessor during Pre-Silicon

PARTICIPATION

Scientists, technologists, teachers and students from Asian Region that are members of the United Nations, UNESCO or IAEA may attend the Workshop. As the Workshop will be conducted in English, participants must have a good working knowledge of that language. A basic knowledge of digital electronics is also required.
As a rule, travel and subsistence expenses of the participants are borne by the home institution. However, limited funds are available for some participants from, and working in, developing countries, to be selected by the organizers. Such financial support is available only for those who attend the entire activity. Every effort should be made by candidates to secure support for their fare (or at least half fare) from their home country. **There is no registration fee to attend the Workshop**.

The **Application Form** obtainable from the ICTP WWW server:
http://agenda.ictp.it/smr.php?1977(**under: application_form**)

should be completed and returned before 21 January 2008:
by e-mail to:
smr1977@ictp.it
(please send file attachments as: either PDF (preferably), RTF zipped, or .doc)

Applicants from Malaysia: should send the application form as described above to: smr1977@ictp.it, cc: mamun.reaz@ieee.org, mamun.reaz@iiu.edu.my
(*recent photograph & signature of the candidate are compulsory*)

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Workshop Secretariat: Tel: +3904022409911 E-mail: smr1977@ictp.it Fax: +39040224600

November 2007

International Islamic University Malaysia

Tunku Abdul Rahman College

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Muhammad Alauddin Mohd Ali
UKM, Malaysia

Laboratory Sessions led by

Maria Liz Crespo
ICTP, Italy

DEADLINE
for requesting participation

21 January 2008