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First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Thursday 10 July 2008

SYNOPSIS Representative: Variation Aware Static Timing Analysis for sub-65nm ASIC Design (17:30-18:30)

time	title	presenter
17:30	SYNOPSIS Representative: Variation Aware Static Timing Analysis for sub-65nm ASIC Design	