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First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Wednesday 18 June 2008

Digital Design III (more complex elements: RAM, ROM, buses, pipeline concept, etc) (12:00-13:00)

time	title	presenter
12:00	Digital Design III (more complex elements: RAM, ROM, buses, pipeline concept, etc)	PIROUZ BAZARGAN-SABAT