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First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Thursday 19 June 2008

Laboratory Session. VHDL Behavioral Description and Simulation of Combinational Circuits. Contd. (16:30-19:00)

time	title	presenter
16:30	Laboratory Session. VHDL Behavioral Description and Simulation of Combinational Circuits. Contd.	MARIA LIZ CRESPO