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# First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

## Friday 20 June 2008

### (LiberoTM IDE) Timing Constraints and Analysis (11:00-12:00)

| time | title | presenter |
|---|---|---|
| 11:00 | (LiberoTM IDE) Timing Constraints and Analysis | NIZAR ABDALLAH |