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First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific

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Transistors.

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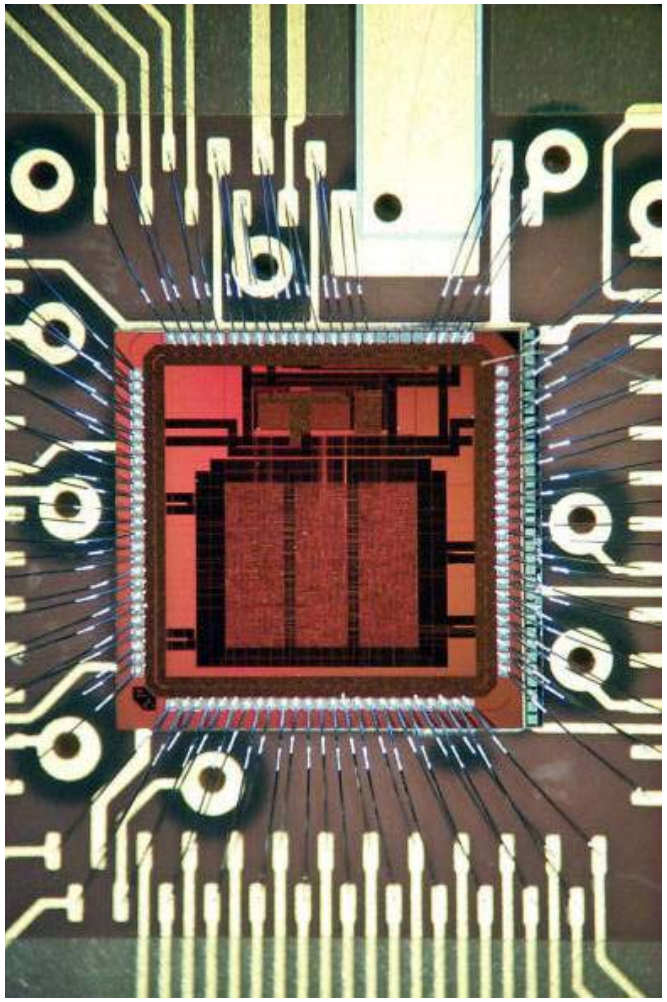
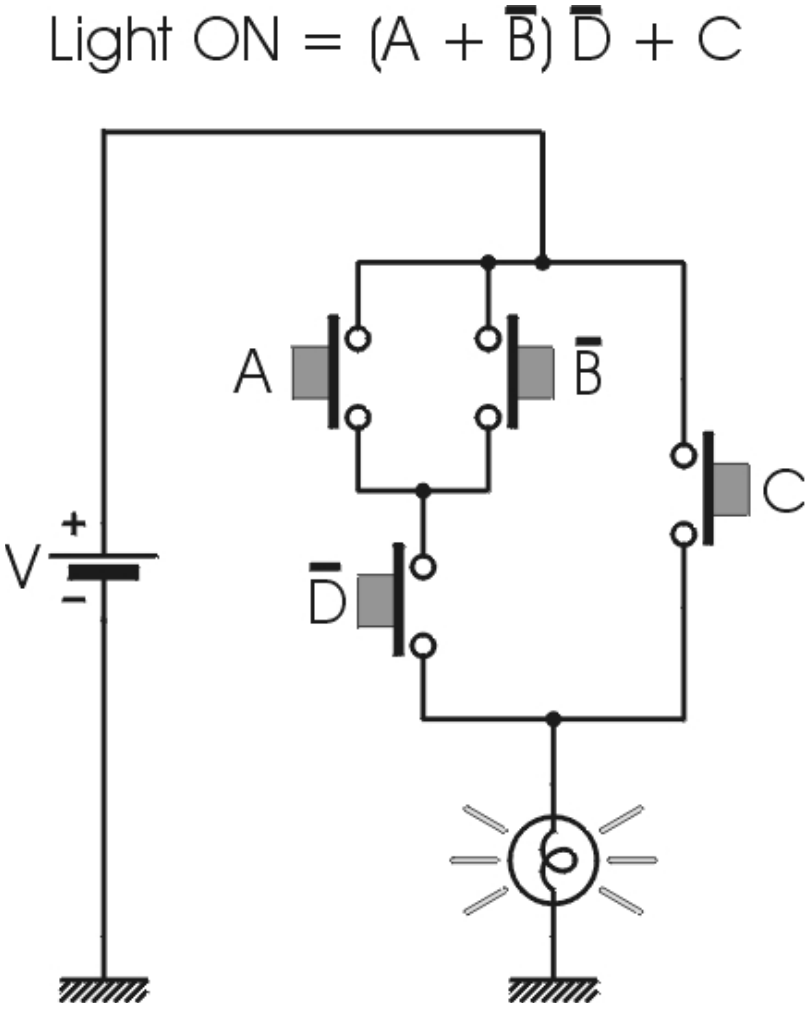
Outline

- Introduction
- Transistors
  - *DC behaviour*
  - *MOSFET capacitances*
  - *MOSFET model*
- The CMOS inverter
- Technology
- Scaling
- Gates
- Sequential circuits
- Storage elements
- Phase-Locked Loops
- Example

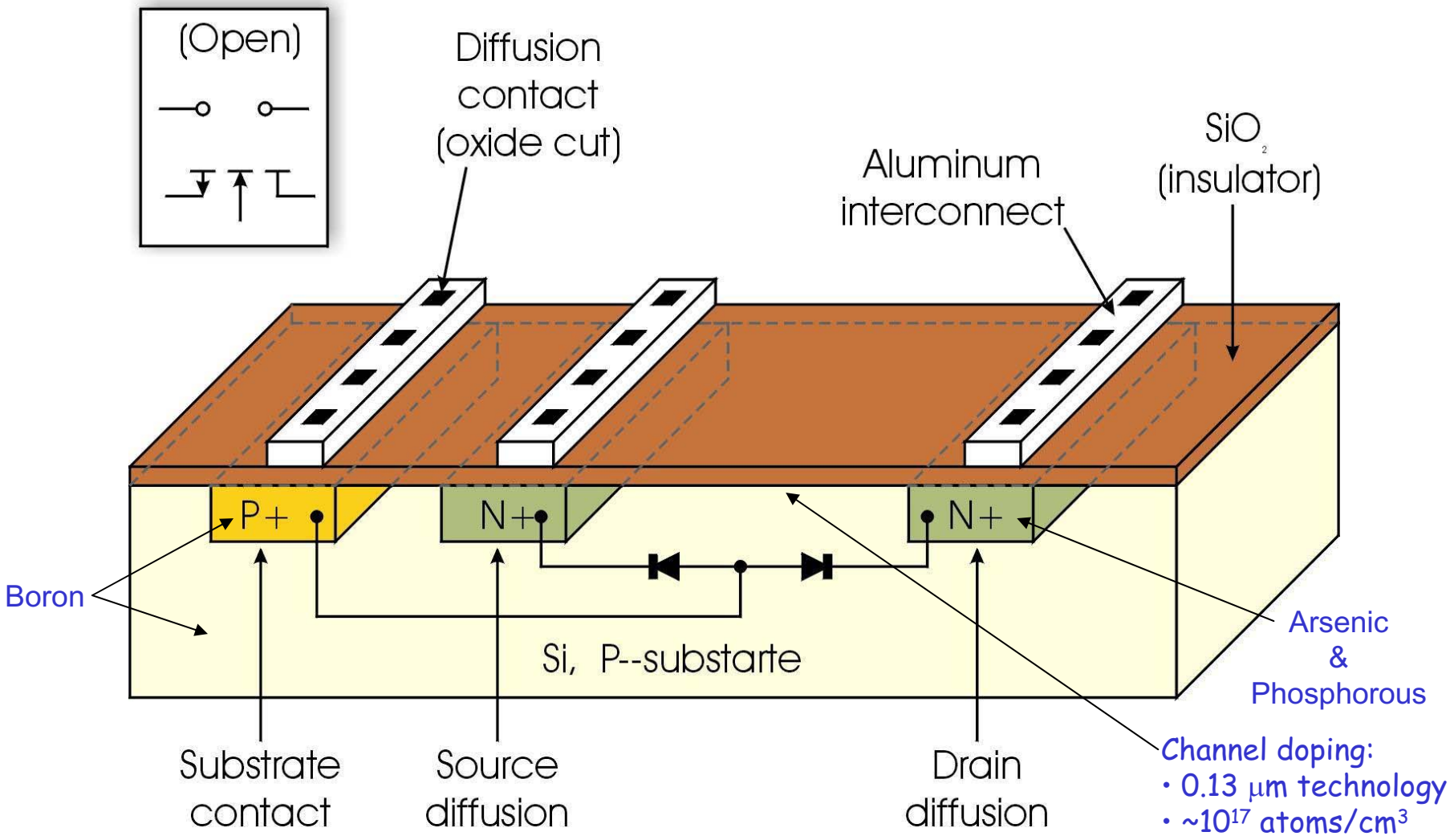


"Making Logic"

- Logic circuit "ingredients":
  - Power source
  - Switches
  - Inversion
  - Power gain
- Power always comes from some form of external EMF generator.
- NMOS and PMOS transistors:
  - Can perform the last three functions
  - They are the building blocks of CMOS technologies!

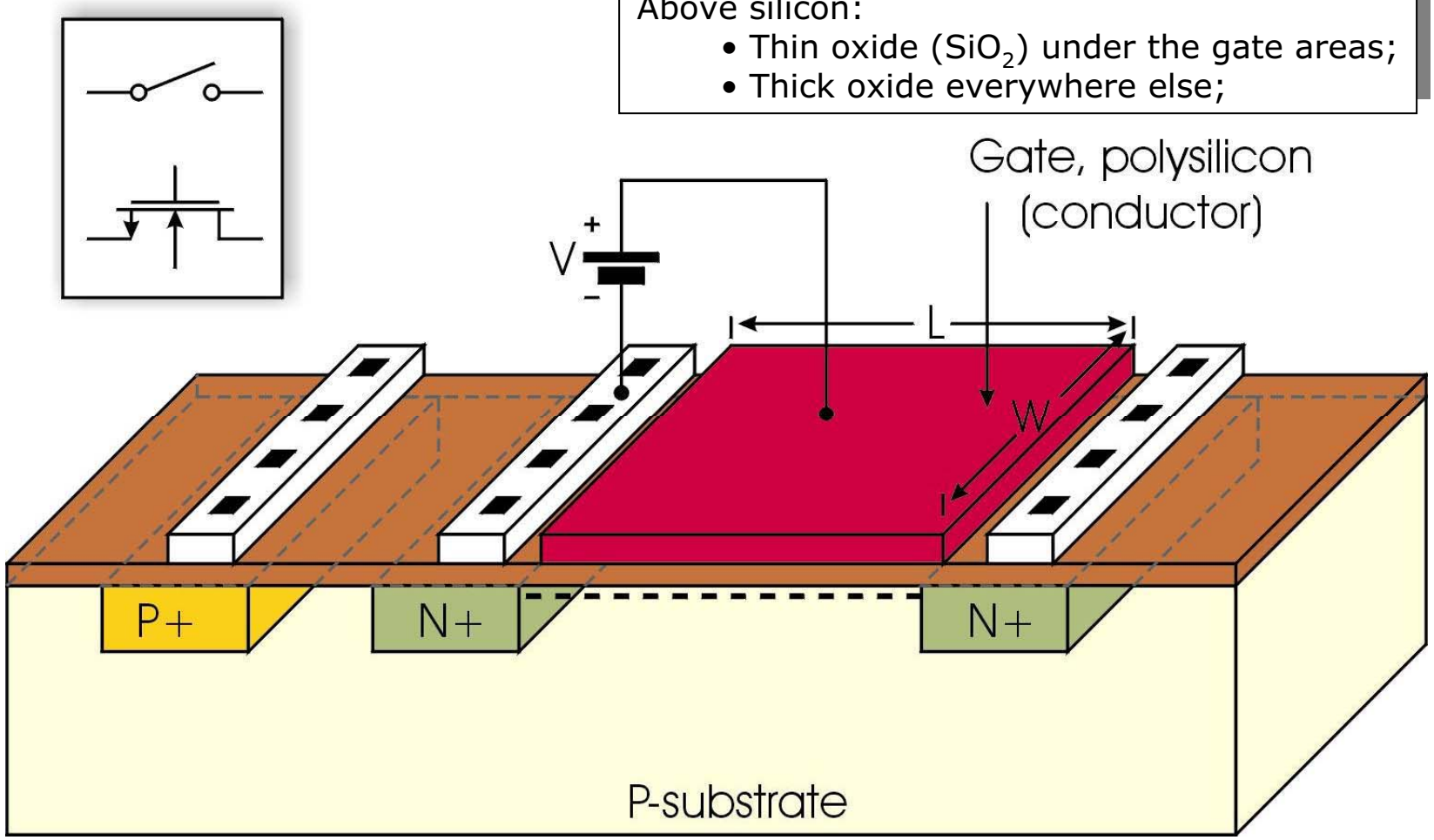


Silicon switches: the NMOS

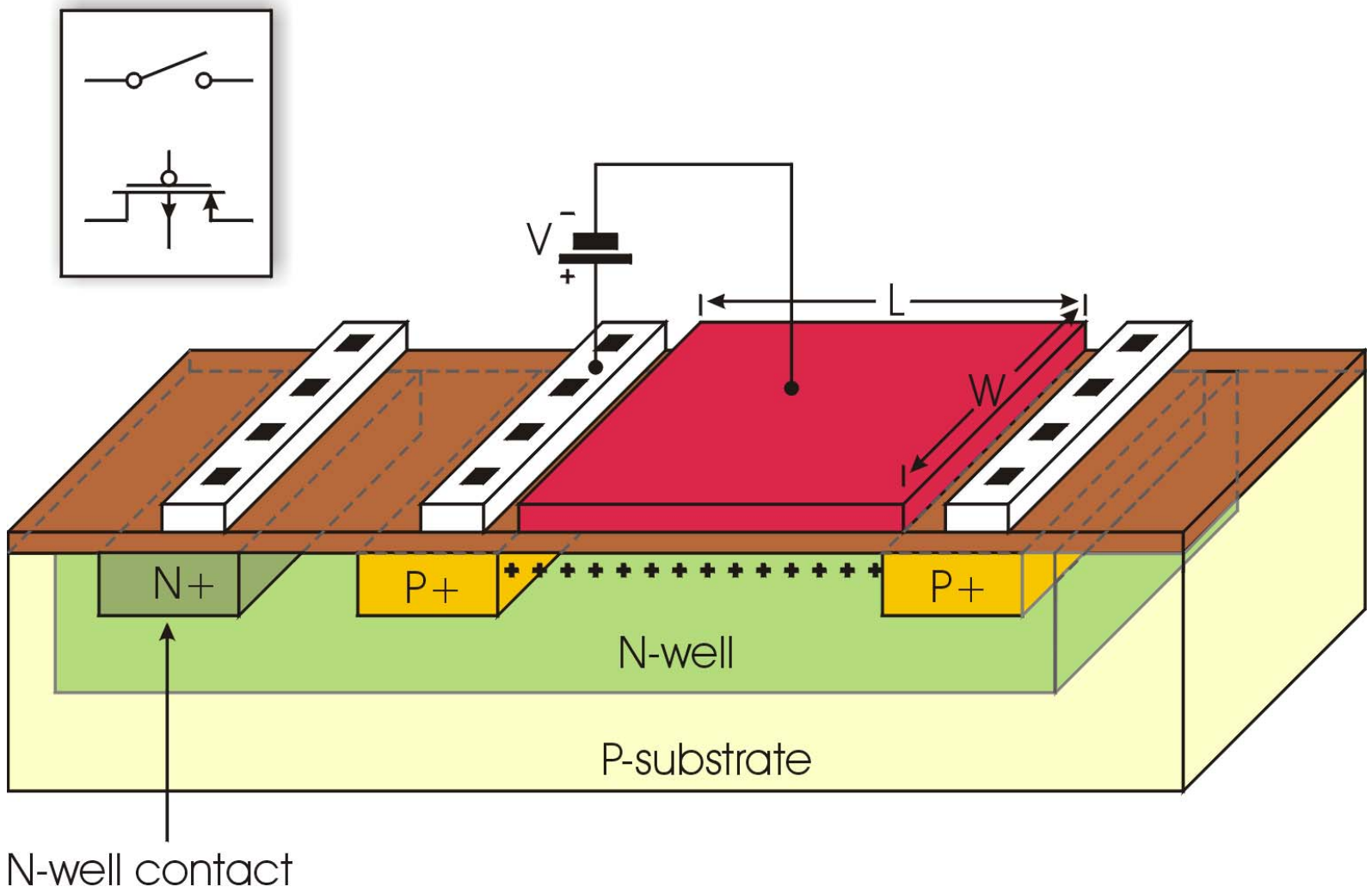


Silicon switches: the NMOS

Above silicon:
- Thin oxide (SiO_2) under the gate areas;
- Thick oxide everywhere else;



Silicon switches: the PMOS



MOSFET equations

- Cut-off region:

$$I_{ds} = 0 \quad \text{for} \quad V_{gs} - V_T < 0 \tag{1}$$

- Linear region:

$$I_{ds} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[\left(V_{gs} - V_T \right) \cdot V_{ds} - \frac{V_{ds}^2}{2} \right] \cdot \left(1 + \lambda \cdot V_{ds} \right) \text{ for } 0 < V_{ds} < V_{gs} - V_T \tag{2}$$

- Saturation:

$$I_{ds} = \frac{\mu \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(V_{gs} - V_T \right)^2 \cdot \left(1 + \lambda \cdot V_{ds} \right) \text{ for } V_{ds} > V_{gs} - V_T \tag{3}$$

- Oxide capacitance

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \left(\mathrm{F} / \mathrm{m}^2 \right)$$

- Process "transconductance"

$$\mu \cdot C_{ox} = \frac{\mu \cdot \varepsilon_{ox}}{t_{ox}} \quad \left(\mathrm{A} / \mathrm{V}^2 \right)$$

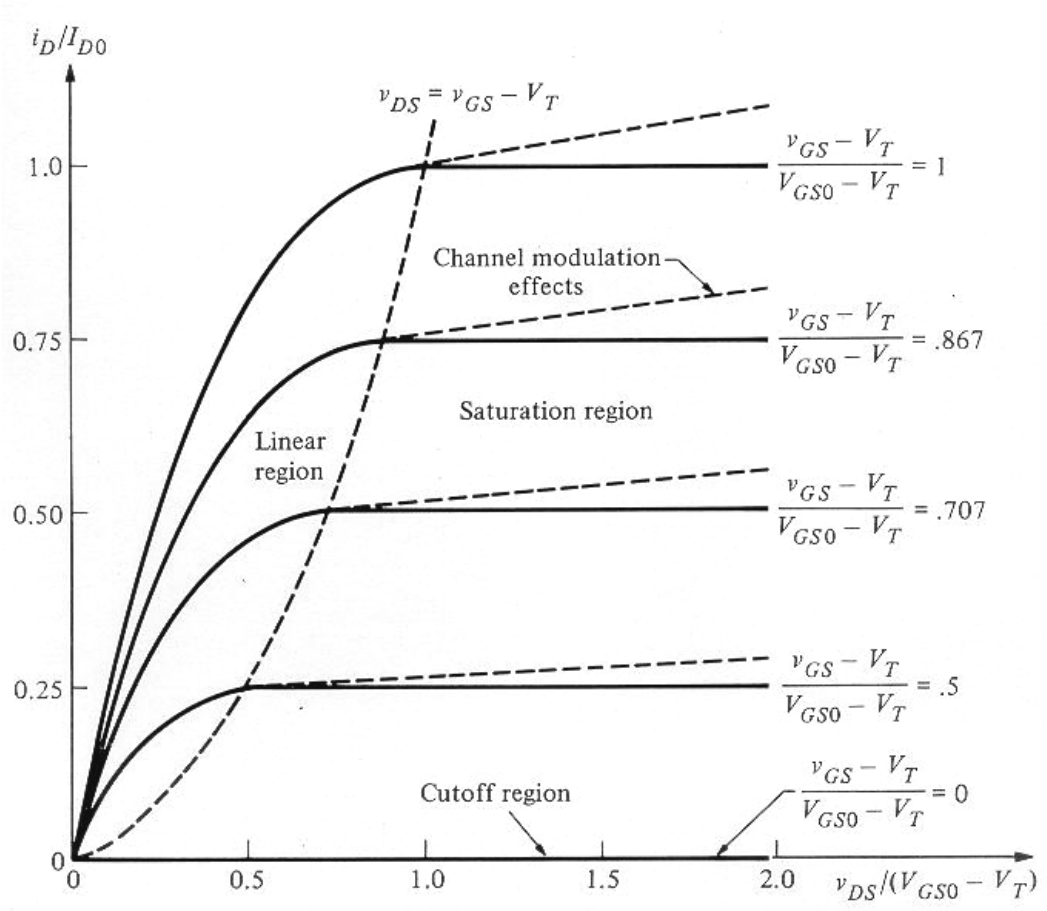
0.24μm process

t_{ox} = 5 nm (~10 atomic layers)

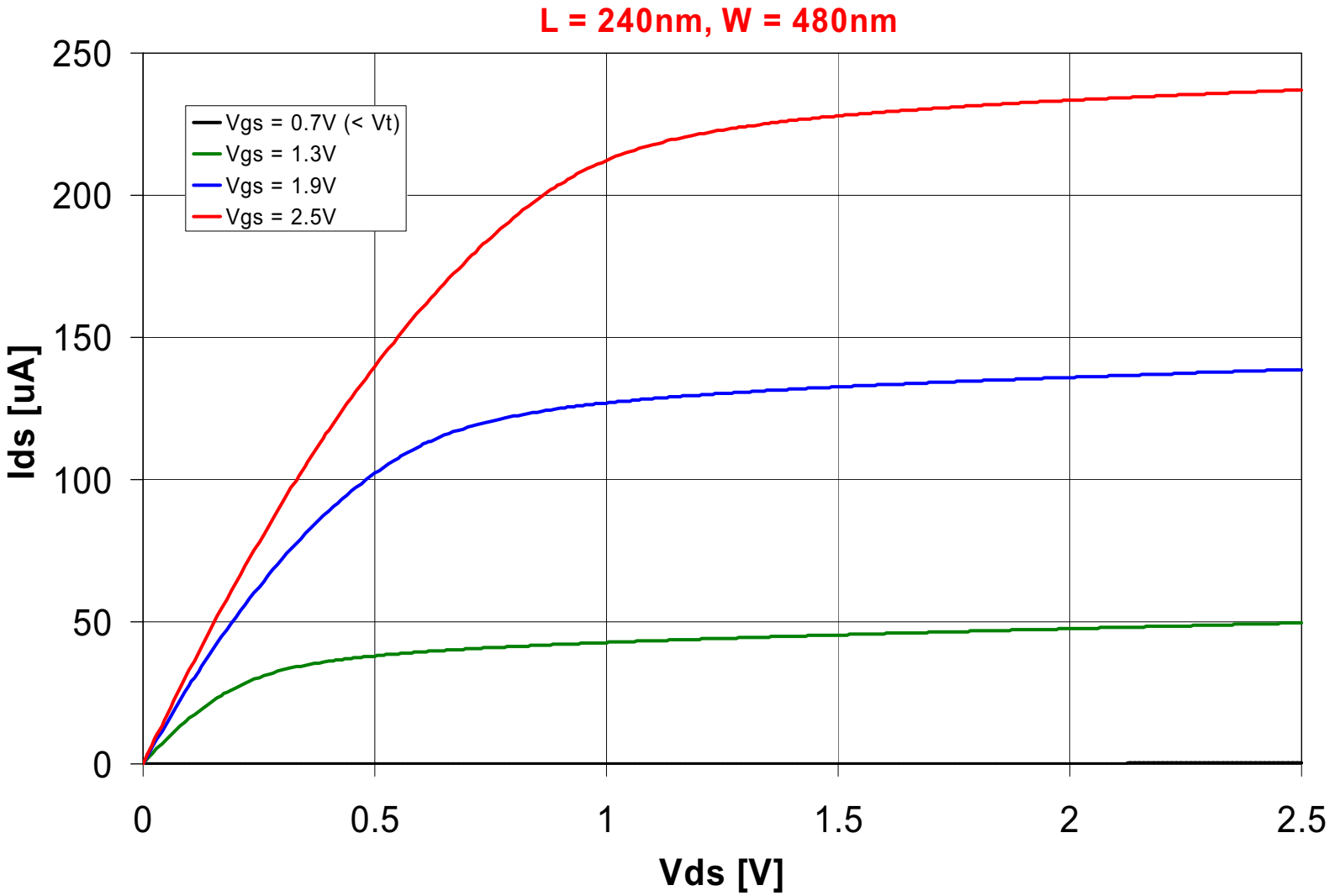
C_{ox} = 5.6 fF/μm^2

MOS output characteristics

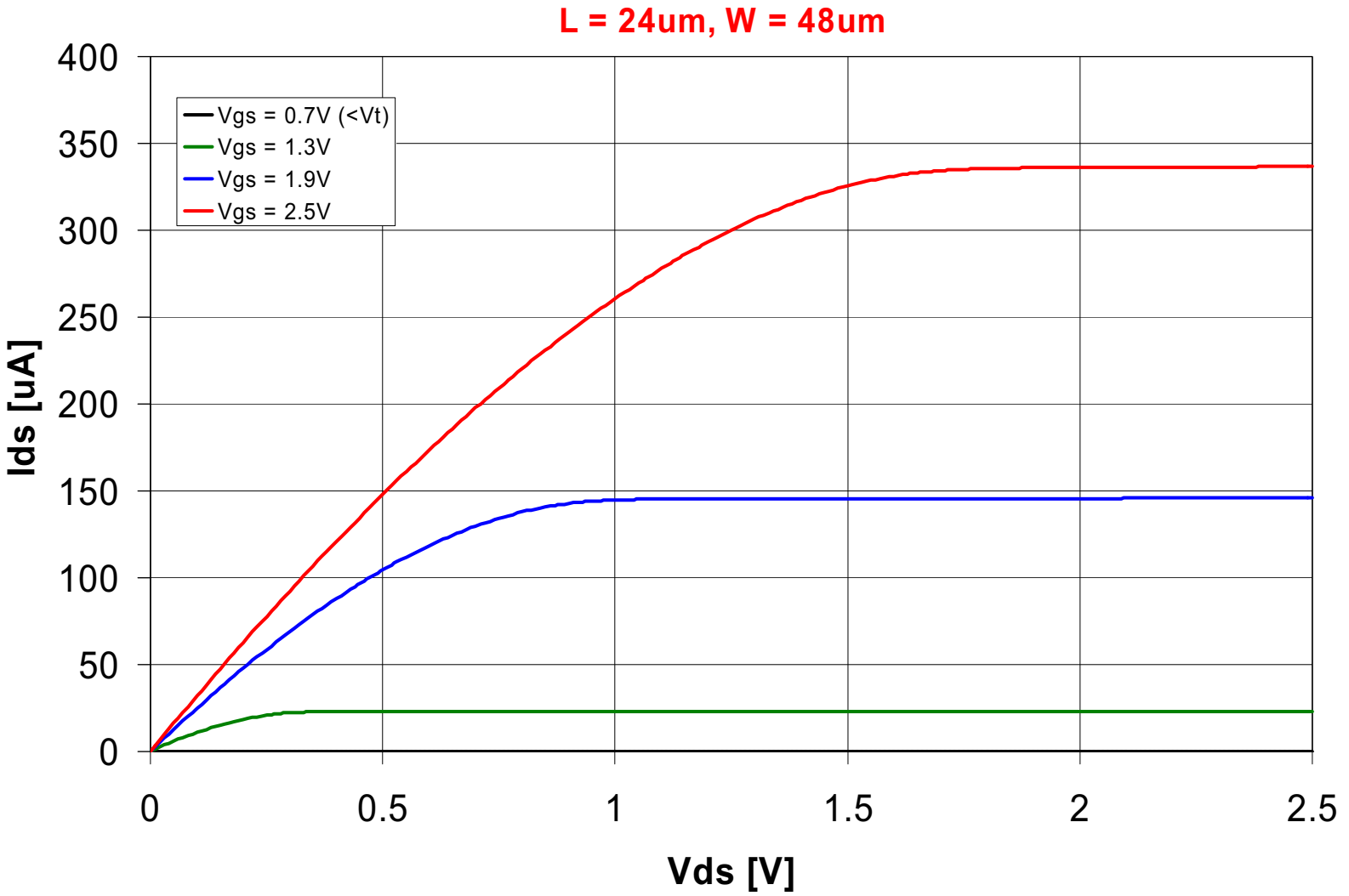
- **Linear region**:
  $V_{ds}<V_{gs}-V_T$
  - Voltage controlled resistor
- **Saturation region**:
  $V_{ds}>V_{gs}-V_T$
  - Voltage controlled current source
- Curves deviate from the ideal current source behavior due to:
  - Channel modulation effects



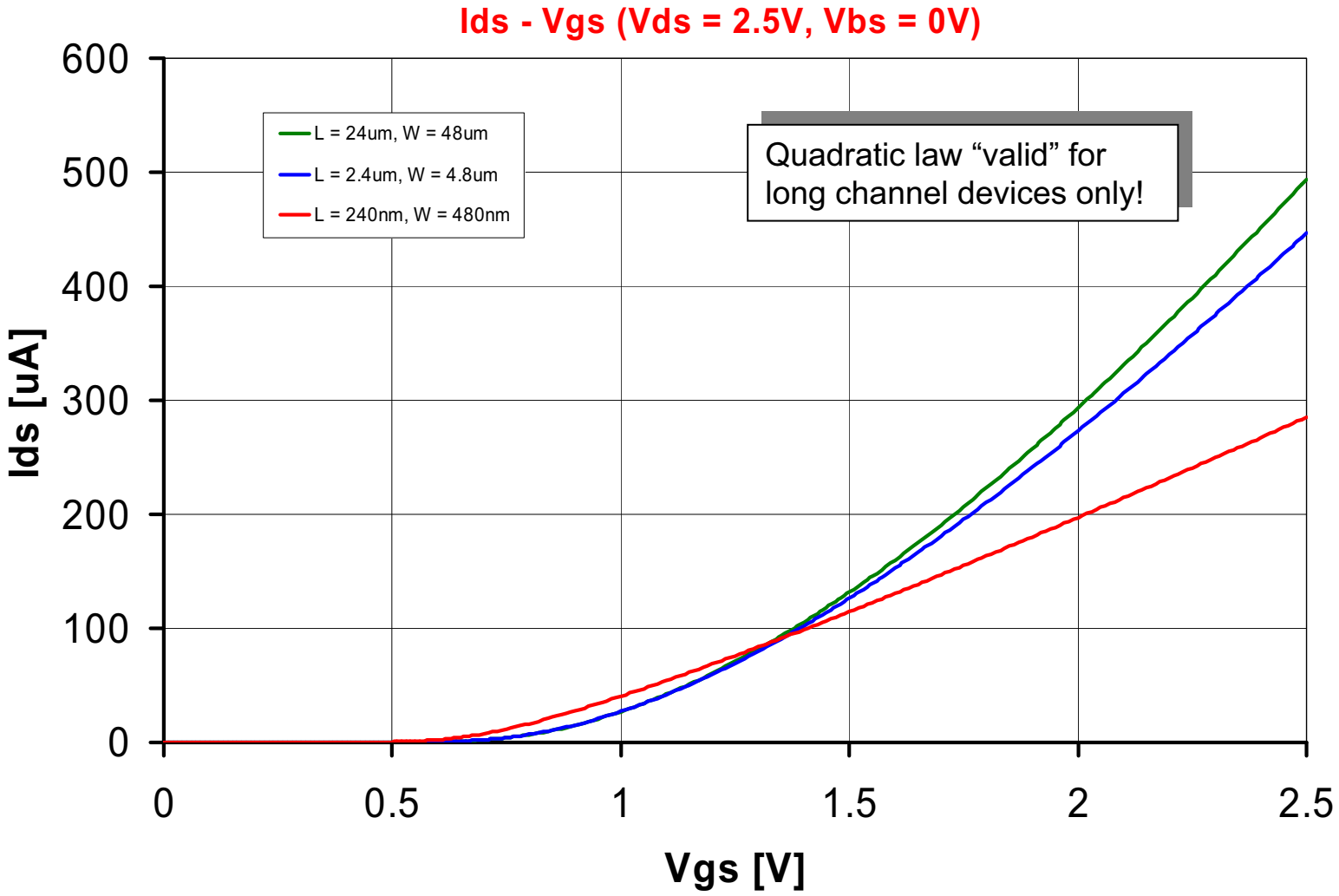
MOS output characteristics



MOS output characteristics

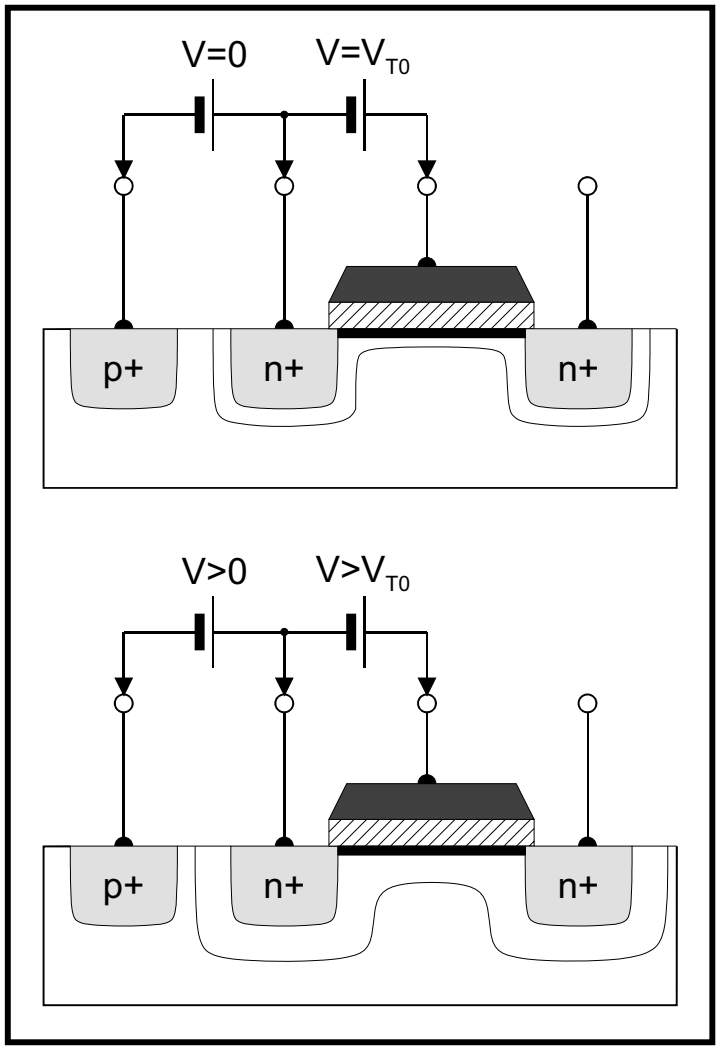


Is the quadratic law valid?

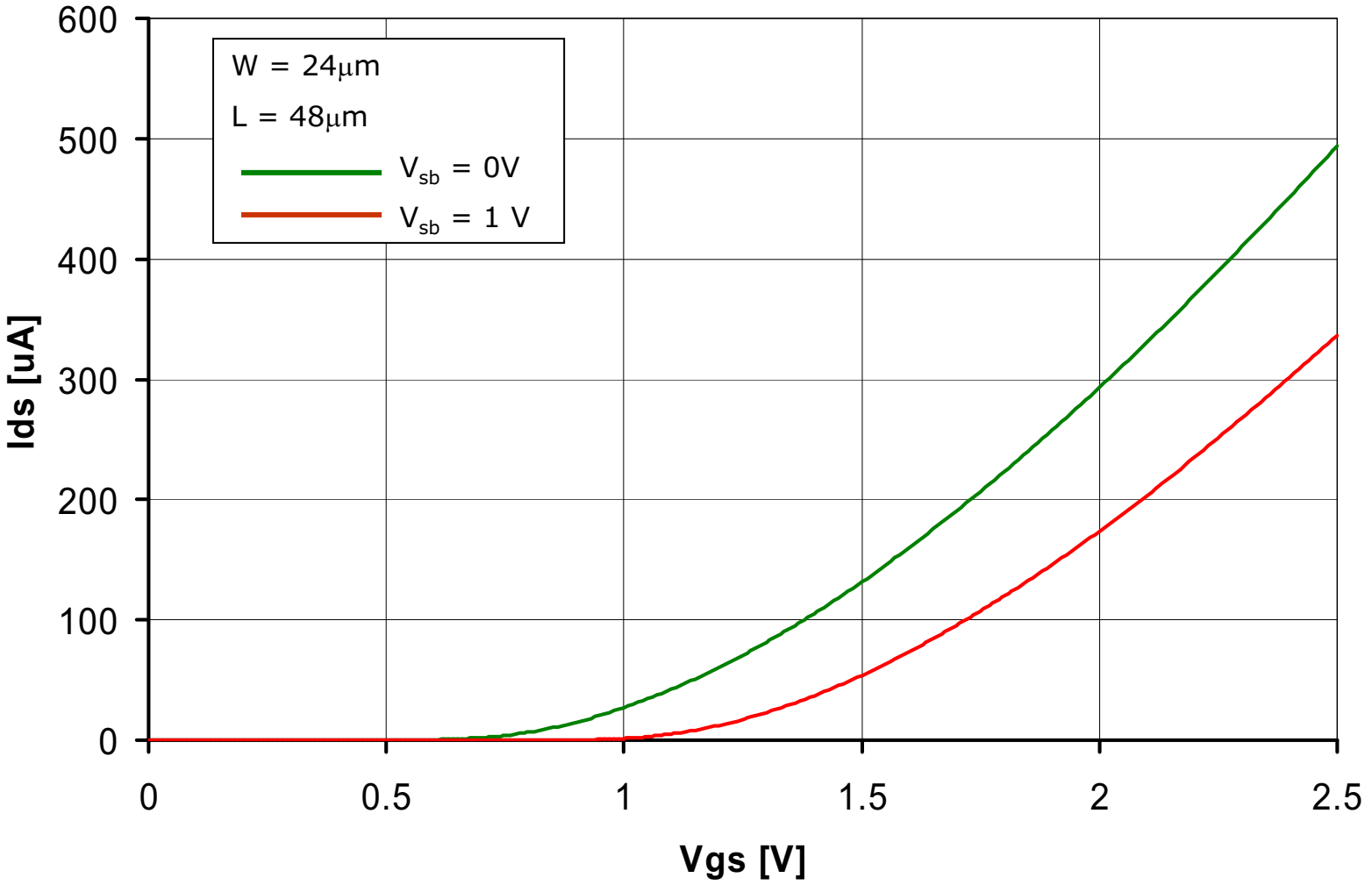


Bulk effect

- The threshold depends on:
  - Gate oxide thickness
  - Doping levels
  - Source-to-bulk voltage
- When the semiconductor surface inverts to n-type the channel is in "strong inversion"
- $V_{sb} = 0 \Rightarrow$ strong inversion for:
  - surface potential > $-2\phi_F$
- $V_{sb} > 0 \Rightarrow$ strong inversion for:
  - surface potential > $-2\phi_F + V_{sb}$



Bulk effect


W = 24μm
L = 48μm
V_{sb} = 0V
V_{sb} = 1 V
Ids [uA]
600
500
400
300
200
100
0
0
0.5
1
1.5
2
2.5
Vgs [V]

Weak inversion

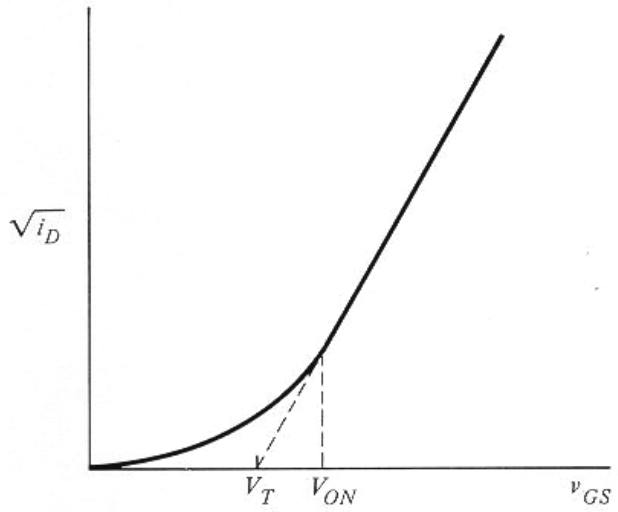
- Is I_d=0 when V_{gs}<V_T?
- For V_{gs}<V_T the drain current depends exponentially on V_{gs}
- In weak inversion and saturation (V_{ds} > ~150mV):

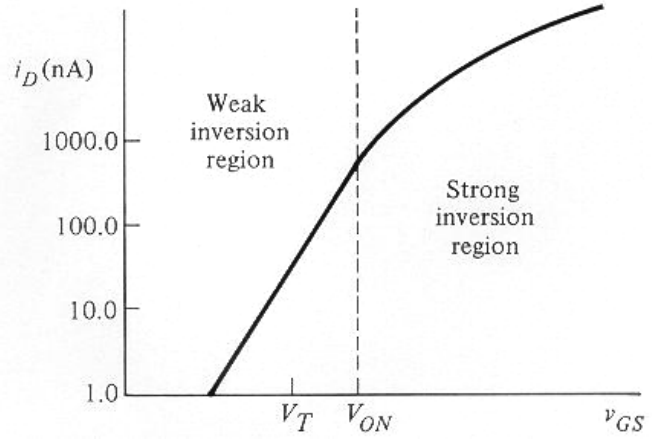
$$I_d \cong \frac{W}{L} \cdot I_{do} \cdot e^{\frac{q \cdot V_{gs}}{n \cdot k \cdot T}}$$

where

$$I_{do} = e^{-\frac{q \cdot V_T}{n \cdot k \cdot T}}$$

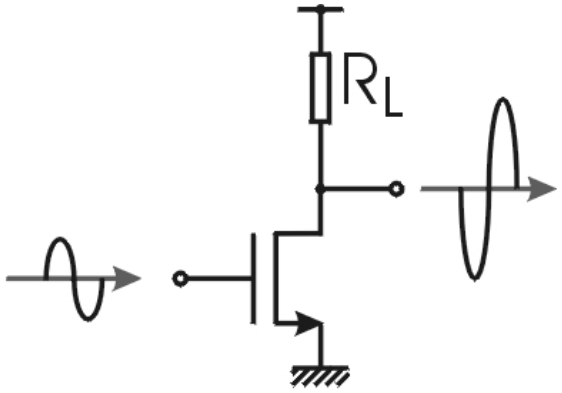
- Used in very low power designs
- Slow operation



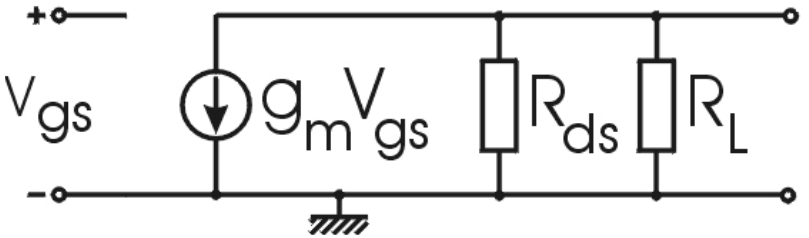


Gain & Inversion

- Gain:
  - Signal regeneration at every logic operation
  - "Static" flip-flops
  - "Static" RW memory cells
- Inversion:
  - Intrinsic to the common-source configuration
- The gain cell load can be:
  - Resistor
  - Current source
  - Another gain device (PMOS)



$$V_{out} = - g_m x (R_{ds} \| R_L) x V_{in}$$



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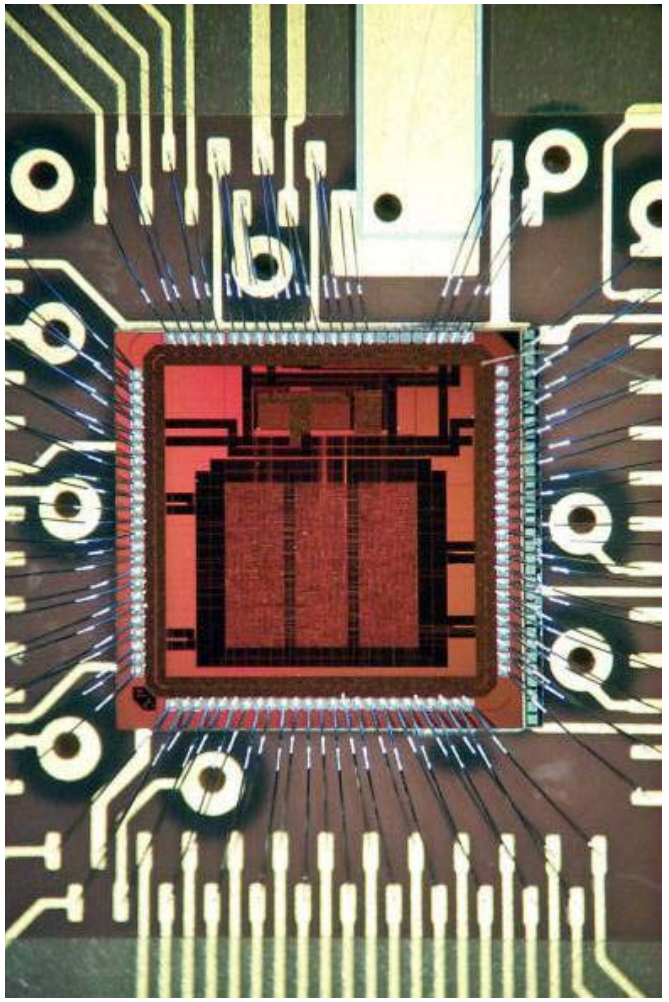
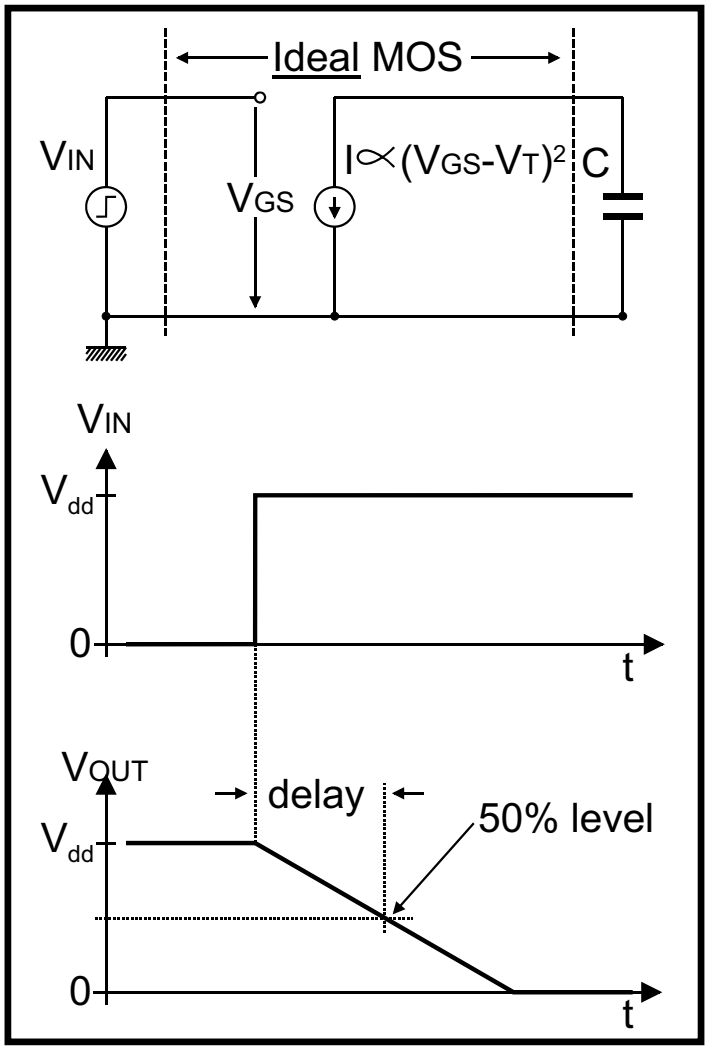


What causes delay?

- In MOS circuits capacitive loading is the main cause. (RC delay in the interconnects will be addressed latter)
- Capacitance loading is due to:
  - Device capacitance
  - Interconnect capacitance

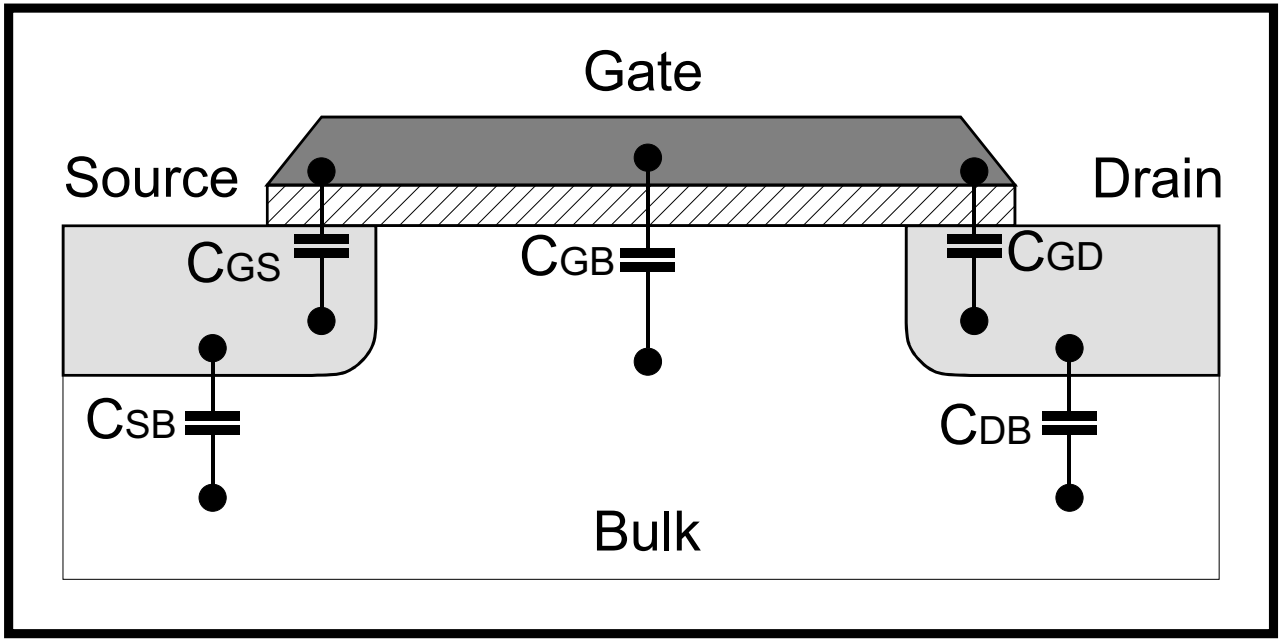
$$\Delta t = C \cdot \frac{\Delta V}{I} \approx \frac{C}{\mu \cdot C_{ox} \cdot V_{dd}} \cdot \frac{L}{W}$$

Assuming $V_T = 0$



MOSFET capacitances

- MOS capacitances have three origins:
  - The basic MOS structure
  - The channel charge
  - The pn-junctions depletion regions



MOS structure capacitances

- Source/drain diffusion extend below the gate oxide by:

  x_d - the lateral diffusion

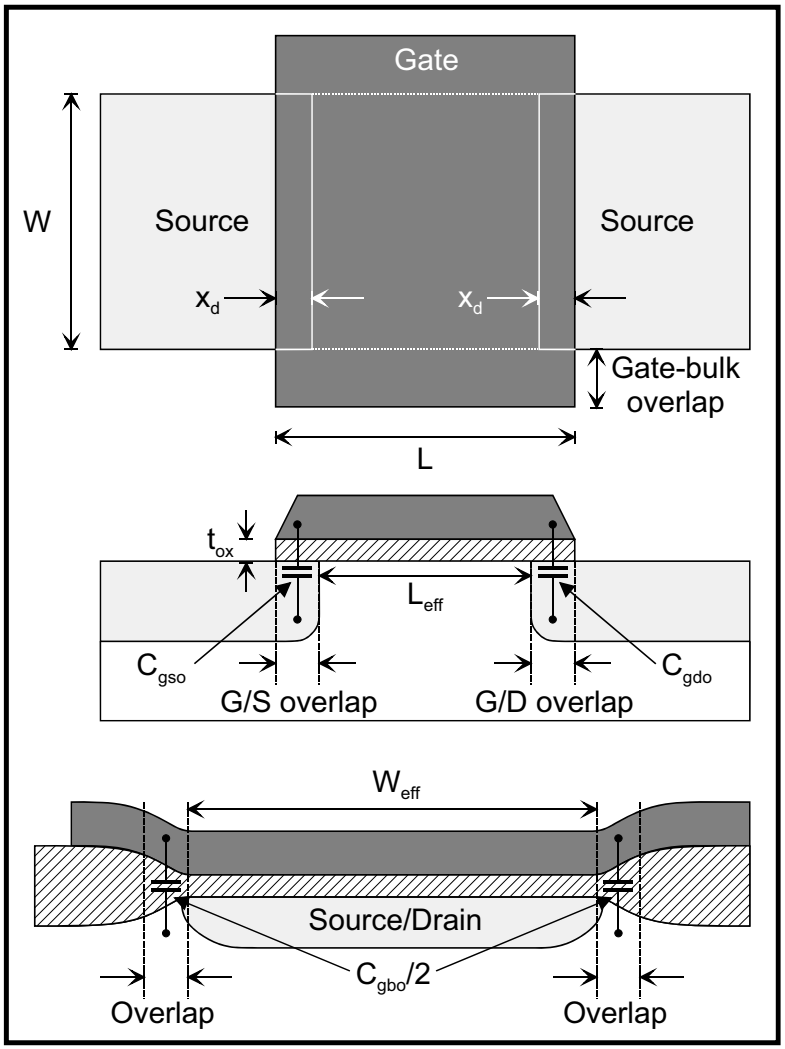
- This gives origin to the source/drain overlap capacitances:

$$C_{gso} = C_{gdo} = C_o \times W$$

$$C_o \ (\mathrm{F/m})$$

- Gate-bulk overlap capacitance:

$$C_{gbo} = C_o' \times L, \quad C_o' \ (\mathrm{F/m})$$



MOS structure capacitances

0.24 μm process

NMOS
L(drawn) = 0.24 μm
L(effective) = 0.18 μm
W(drawn) = 2 μm
C_o (s, d, b) = 0.36 fF/μm
C_{ox} = 5.6 fF/μm^2

$C_{gso} = C_{gdo}$ = 0.72 fF
C_{gbo} = 0.086 fF

C_g = 2.02 fF

Channel capacitance

- The channel capacitance is nonlinear
- Its value depends on the operation region
- Its formed of three components:

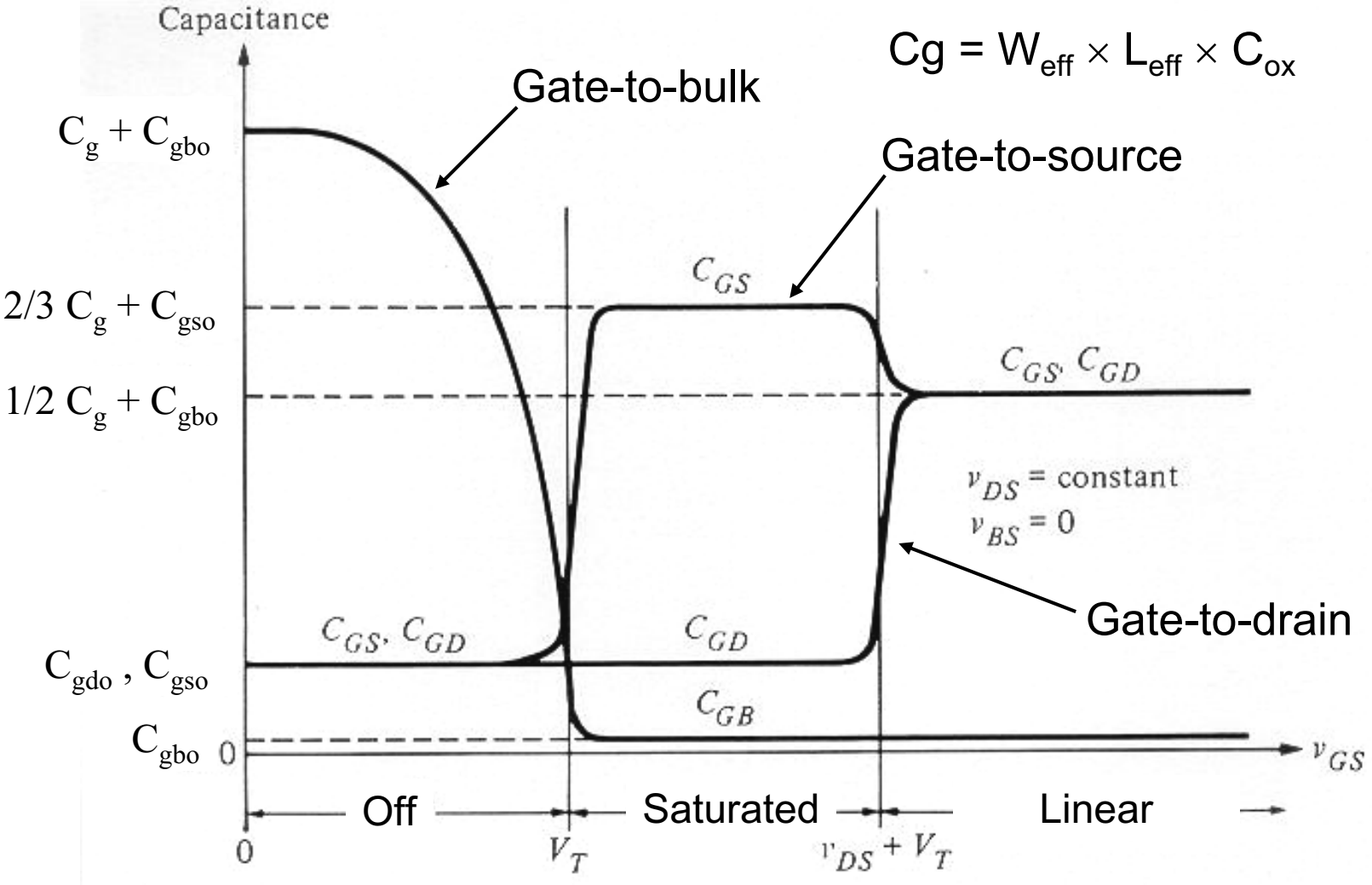
  C_{gb} - gate-to-bulk capacitance

  C_{gs} - gate-to-source capacitance

  C_{gd} - gate-to-drain capacitance

Operation region	**C_{gb}**	**C_{gs}**	**C_{gd}**
Cutoff	C_{ox} W L	0	0
Linear	0	(1/2) C_{ox} W L	(1/2) C_{ox} W L
Saturation	0	(2/3) C_{ox} W L	0

Channel capacitance



$$Cg = W_{eff} \times L_{eff} \times C_{ox}$$

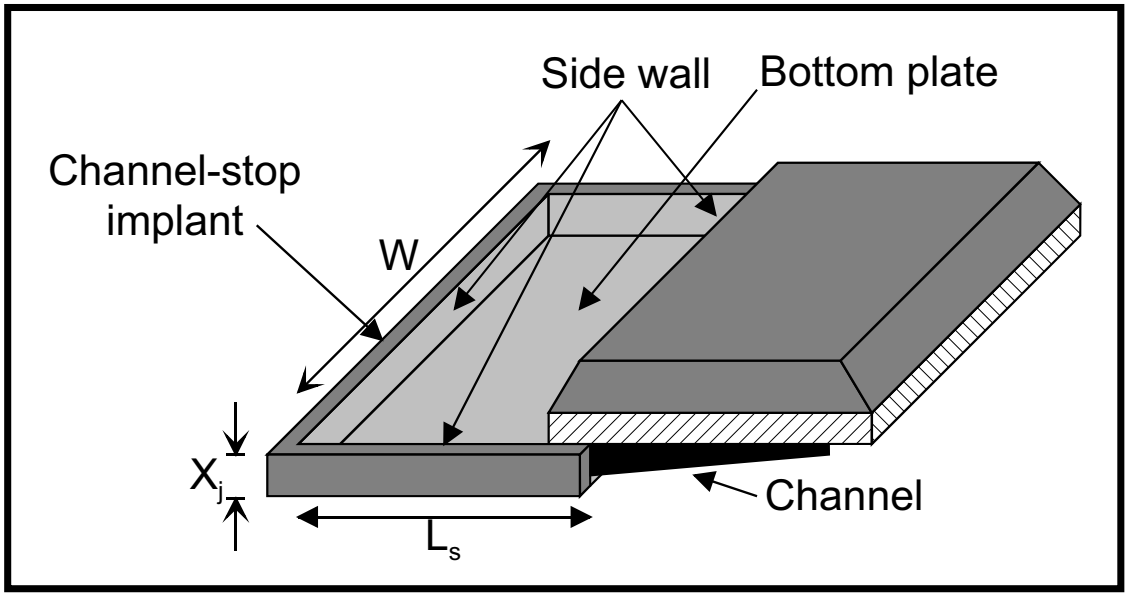
Junction capacitances

- C_{sb} and C_{db} are diffusion capacitances composed of:
  - Bottom-plate capacitance:

$$C_{bottom} = C_j \cdot W \cdot L_s$$

  - Side-wall capacitance:

$$C_{sw} = C_{jsw} \cdot (2 L_s + W)$$



Junction capacitances

0.24 μm process

NMOS
L(drawn) = 0.24 μm
L(effective) = 0.18 μm
W(drawn) = 2 μm
L_s = 0.8 μm
C_j (s, d) = 1.05 fF/μm^2
C_{jsw} = 0.09 fF/μm

C_{bottom} = 1.68 fF
C_{sw} = 0.32 fF

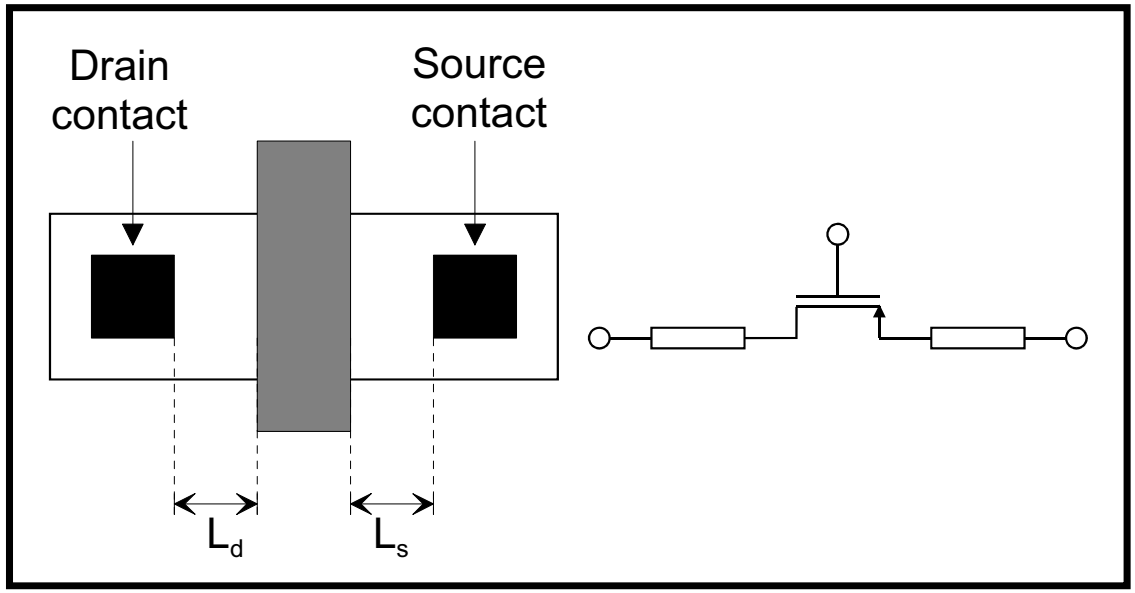
C_g = 2.02 fF

Source/drain resistance

- Scaled down devices ⇒ higher source/drain resistance:

$$R_{s,d} = \frac{L_{s,d}}{W} \cdot R_{sq} + R_c$$

- In sub-μ processes *silicidation* is used to reduce the source, drain and gate parasitic resistance



0.24 μm process

R (P+) = 4 Ω/sq
R (N-) = 4 Ω/sq

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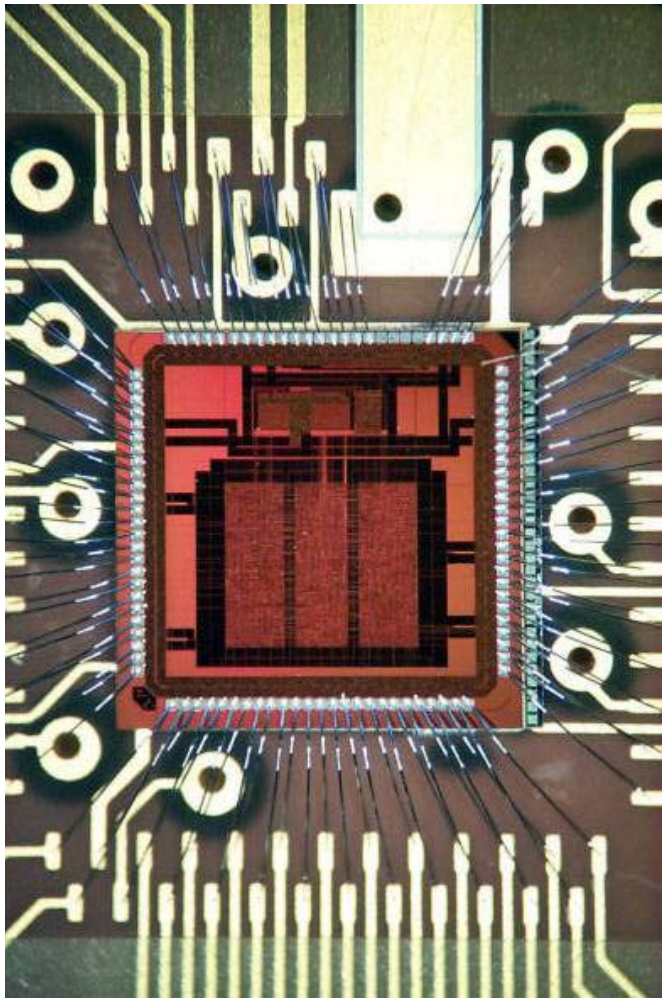
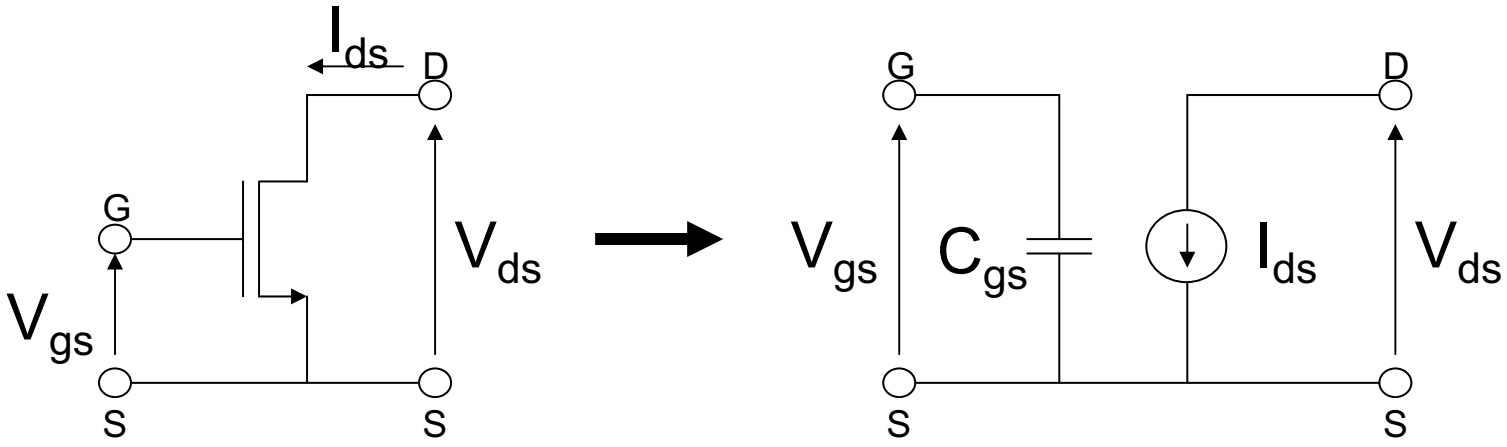


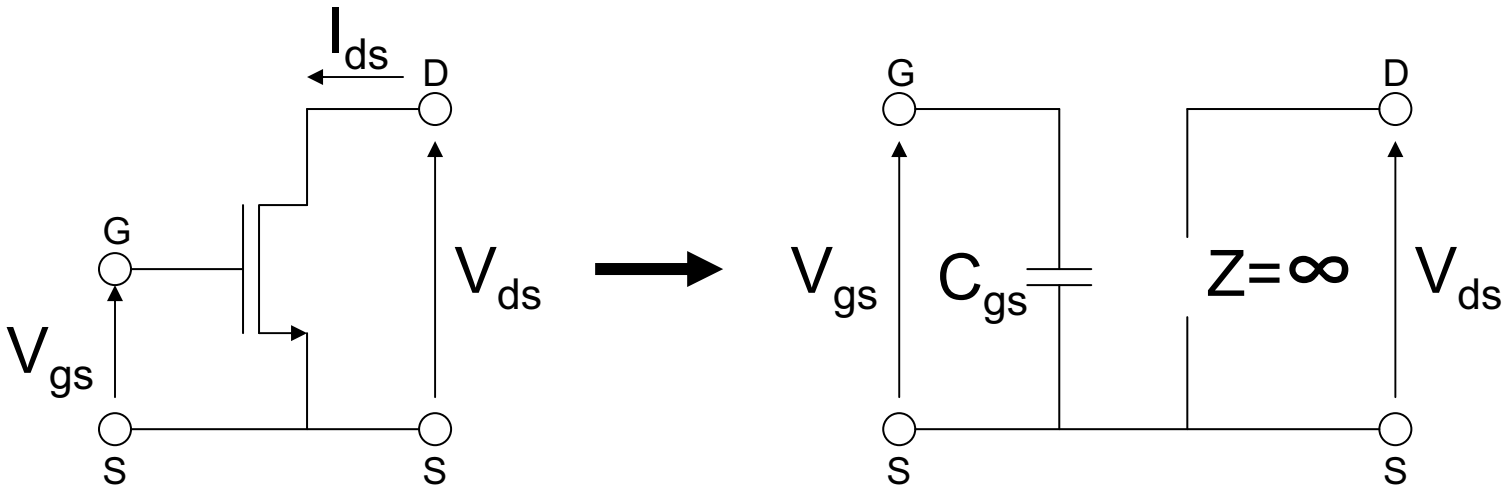
Ultra simplified MOSFET model

- Here it is an almost "simplistic" model of the MOSFET that will help you to easily follow the remaining material.
- The MOS transistor "is" a capacitor whose voltage controls the passage of current between two nodes called the ***source*** and the ***drain***.
- One of the electrodes of this capacitor is called the ***gate***, the other the ***source***.
- The "way" the current flows between the source and the drain depends on the gate-to-source voltage (V_{gs}) and on the drain-to-source voltage (V_{ds}).



Ultra simplified MOSFET model

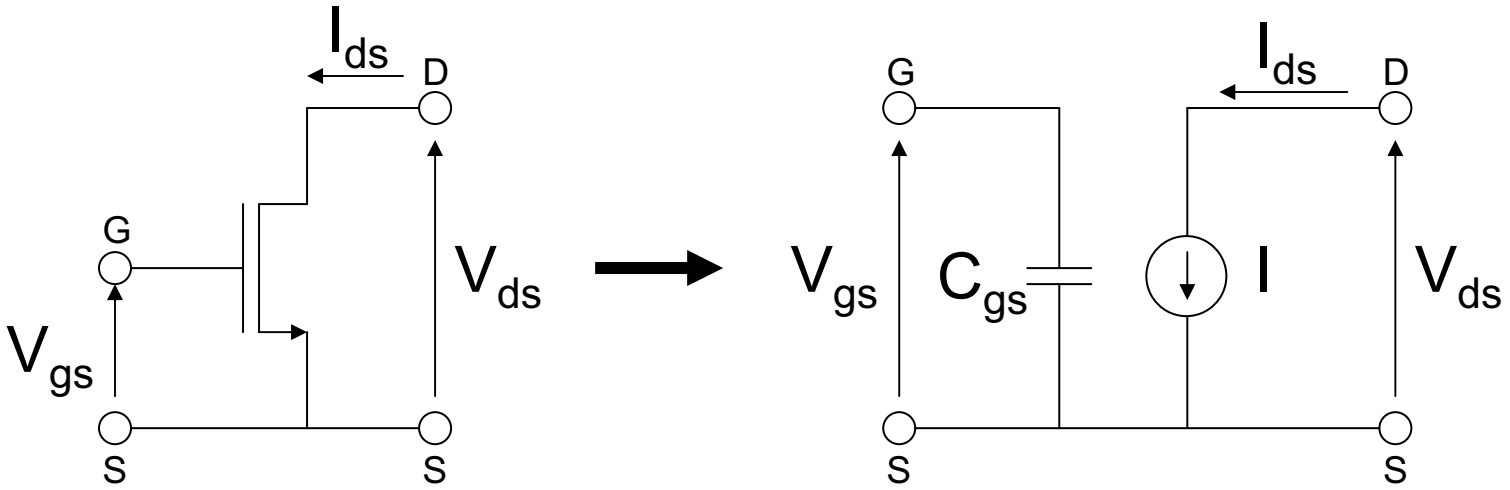
- If the gate-to-source voltage (V_{gs}) is less than a certain voltage, called the threshold voltage (V_{th}), no current flows in the drain circuit no matter what the drain-to-source voltage (V_{ds}) is!
- This is the actual definition of ***threshold voltage V_{th}.***
- That is, $I_{ds} = 0$ for $V_{gs} < V_{th}$
- This is the same as saying that the drain circuit is an infinite impedance (an open circuit)!



Ultra simplified MOSFET model

- If the gate-to-source voltage (V_{gs}) is bigger than the threshold voltage (V_{th}) ***and*** the drain-to-source voltage (V_{ds}) is bigger than $V_{gs} - V_{th}$ then the drain current only depends on the ***gate overdrive voltage*** ($V_{gs} - V_{th}$)
- That is, the drain circuit behaves as an "ideal" voltage controlled current source:

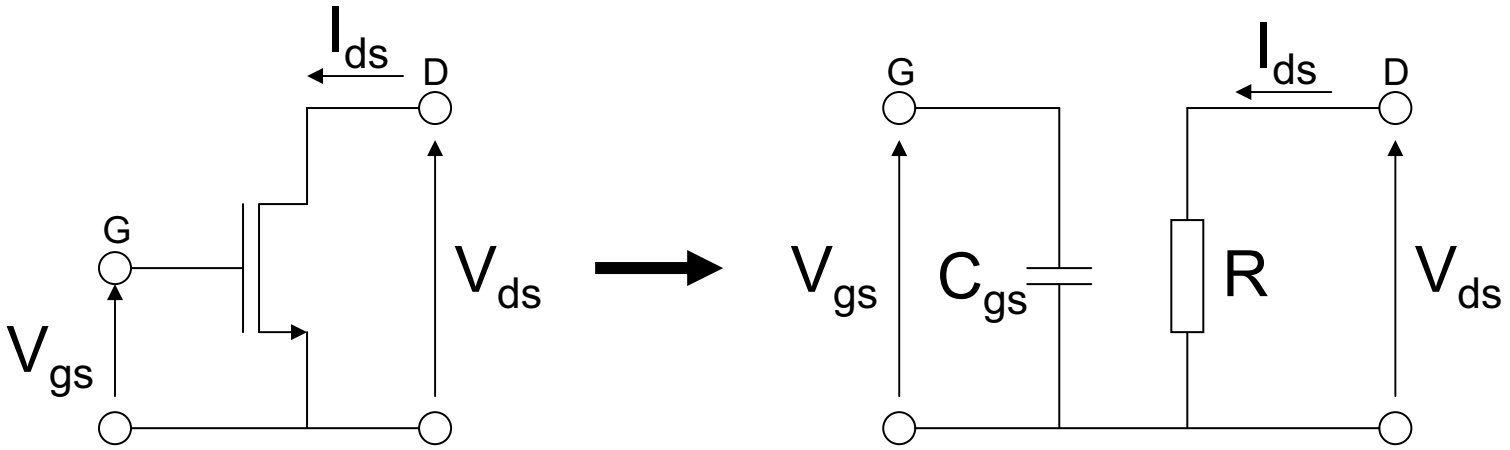
$$I_{ds} = \frac{\mu \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_T)^2$$



Ultra simplified MOSFET model

- If the gate-to-source voltage (V_{gs}) is bigger than the threshold voltage (V_{th}) ***and*** the drain-to-source voltage (V_{ds}) is smaller than $V_{gs} - V_{th}$ then the drain current depends both on the ***gate overdrive voltage*** ($V_{gs} - V_{th}$) and the ***drain-to-source voltage*** (V_{ds})
- That is, the drain circuit behaves as a voltage controlled resistor:

$$I_{ds} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{gs} - V_T\right) \cdot V_{ds}$$



Ultra simplified MOSFET model

- For PMOS transistors the same concepts are valid except that:
  - All voltages are negative (including V_{th})
  - Were we used bigger than you should use smaller than
  - The drain current actually flows out of the transistor instead of into the transistor.
- REMEMBER!
  - This is an almost 'simplistic' model of the device!
- However, it will allow us to understand qualitatively the behaviour of CMOS logic circuits!
  - Even some conclusions will be based on such a simple model.