The Abdus Salam
International Centre for Theoretical Physics

United Nations
Educational, Scientific and
Cultural Organization

IAEA
International Atomic Energy Agency

1977-6

First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific

16 June - 11 July, 2008

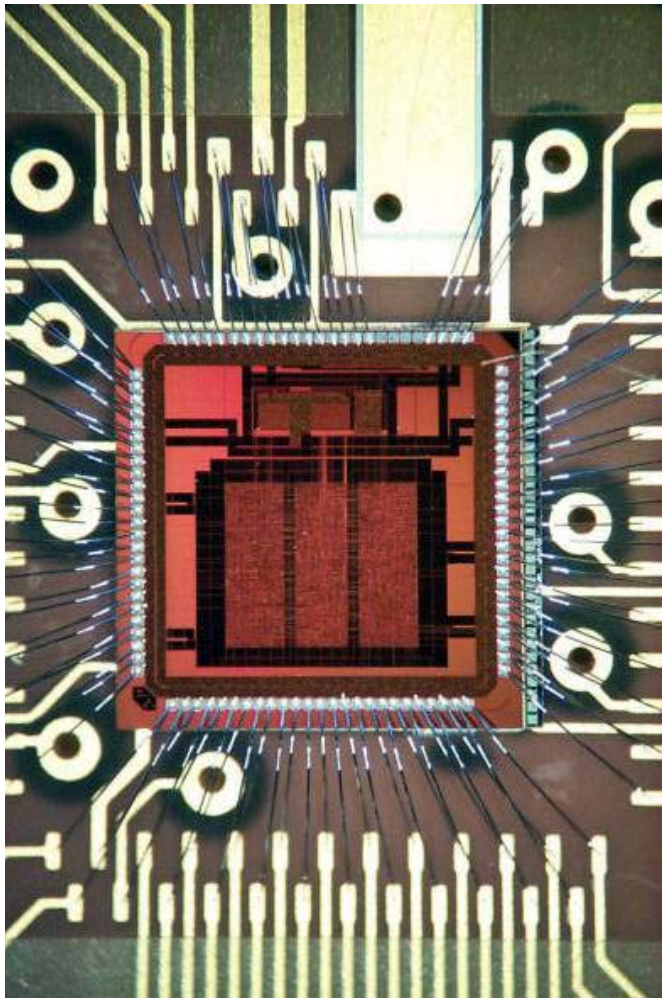
Gates.

Paulo Moreira

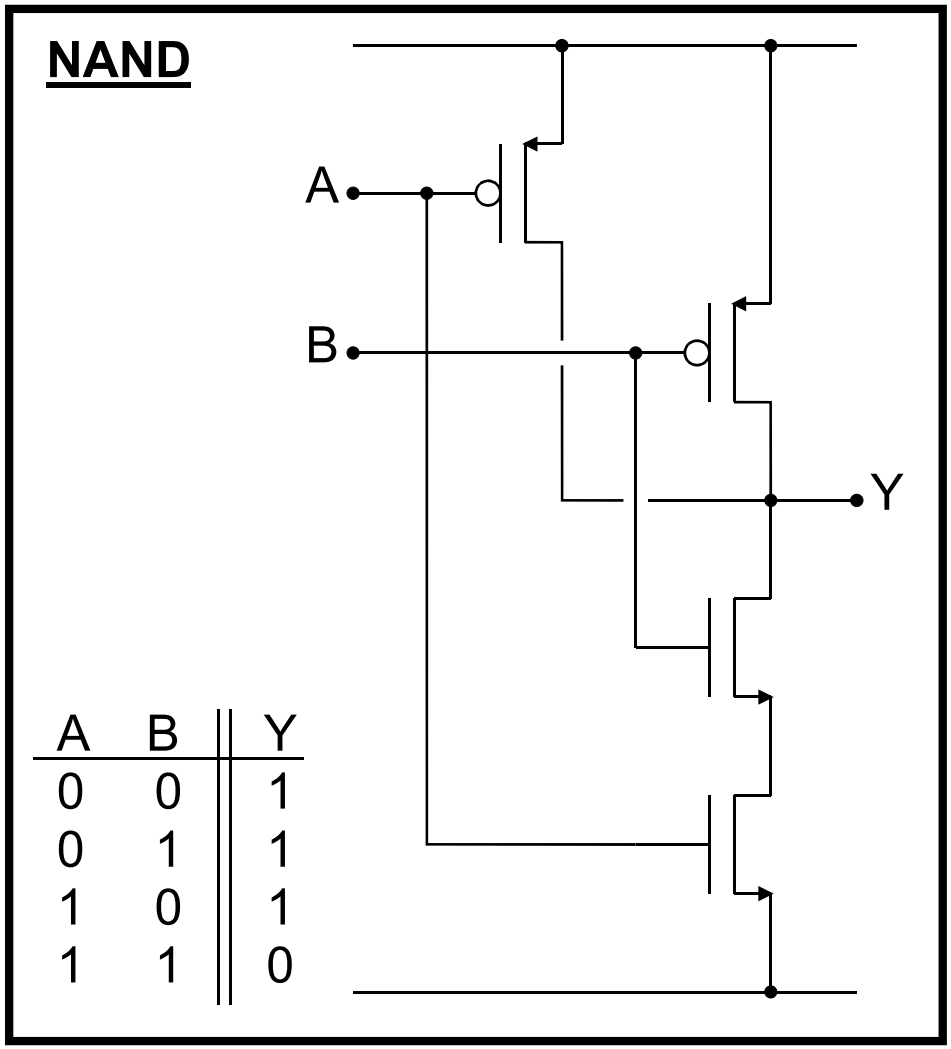
PH ESE ME Division
C E R N
CH-1211 Geneva 23
SWITZERLAND

Outline

- Introduction
- Transistors
- The CMOS inverter
- Technology
- Scaling
- Gates
  - The NAND gate
  - "Reading" CMOS gates
  - Designing CMOS gates
- Sequential circuits
- Storage elements
- Phase-Locked Loops
- Example



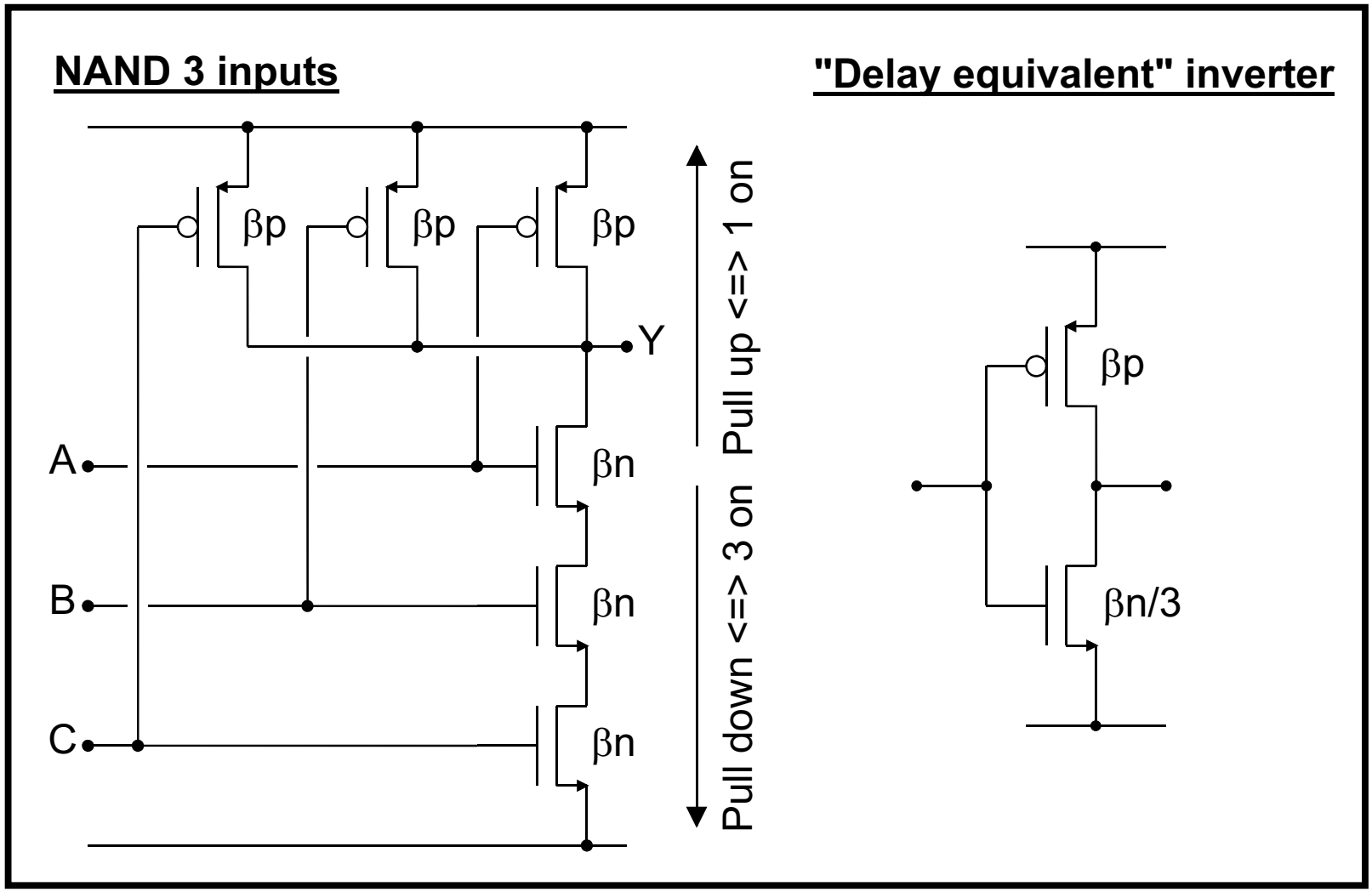
NAND 2-inputs



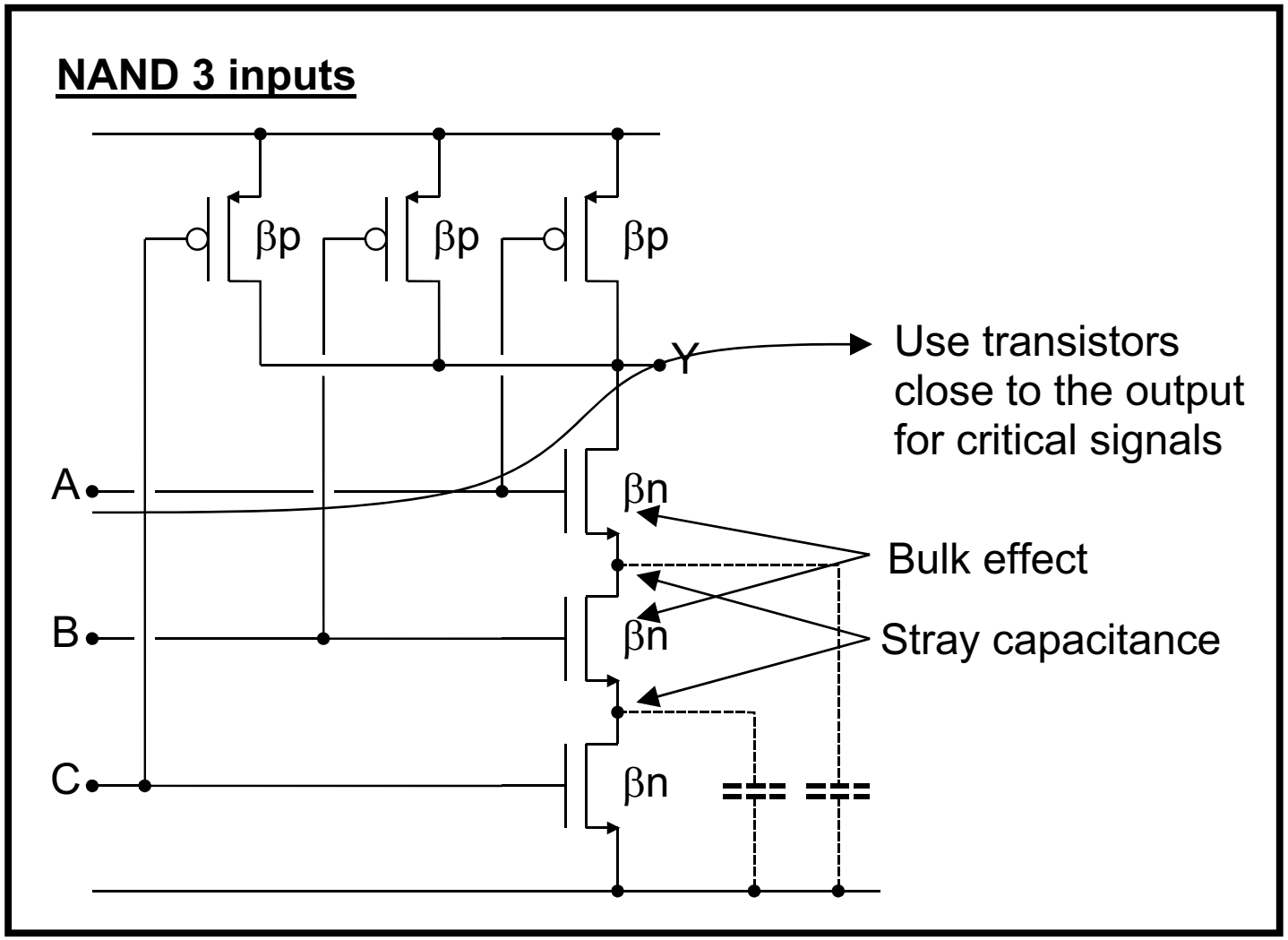
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

"Gates are inverters in disguise!"

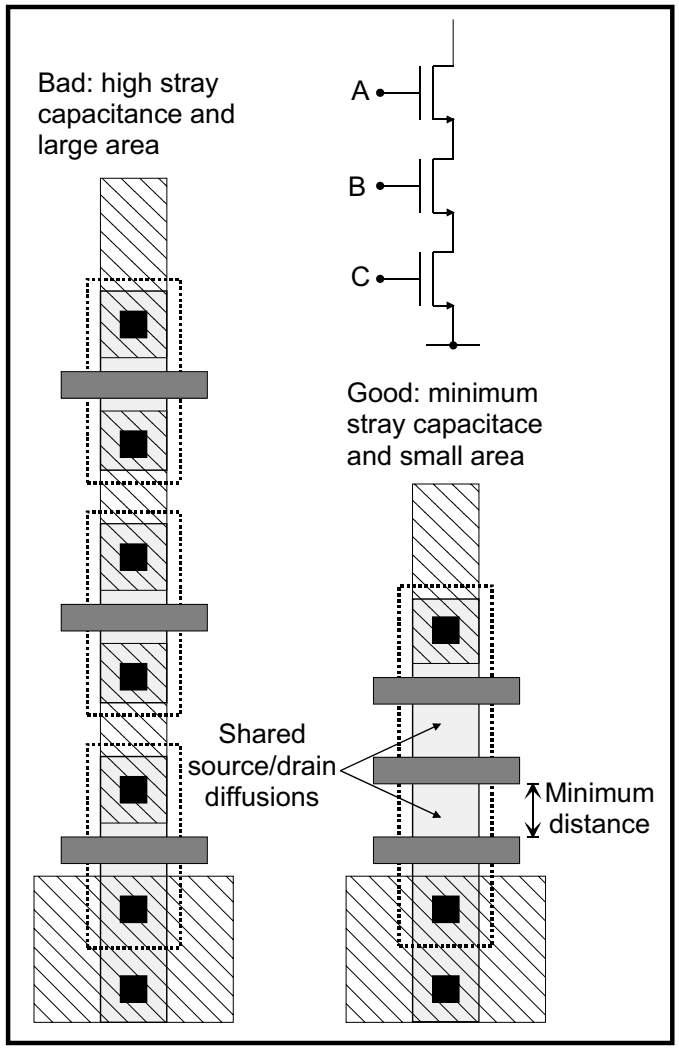
NAND 3-inputs



NAND 3-inputs



NAND 3-inputs



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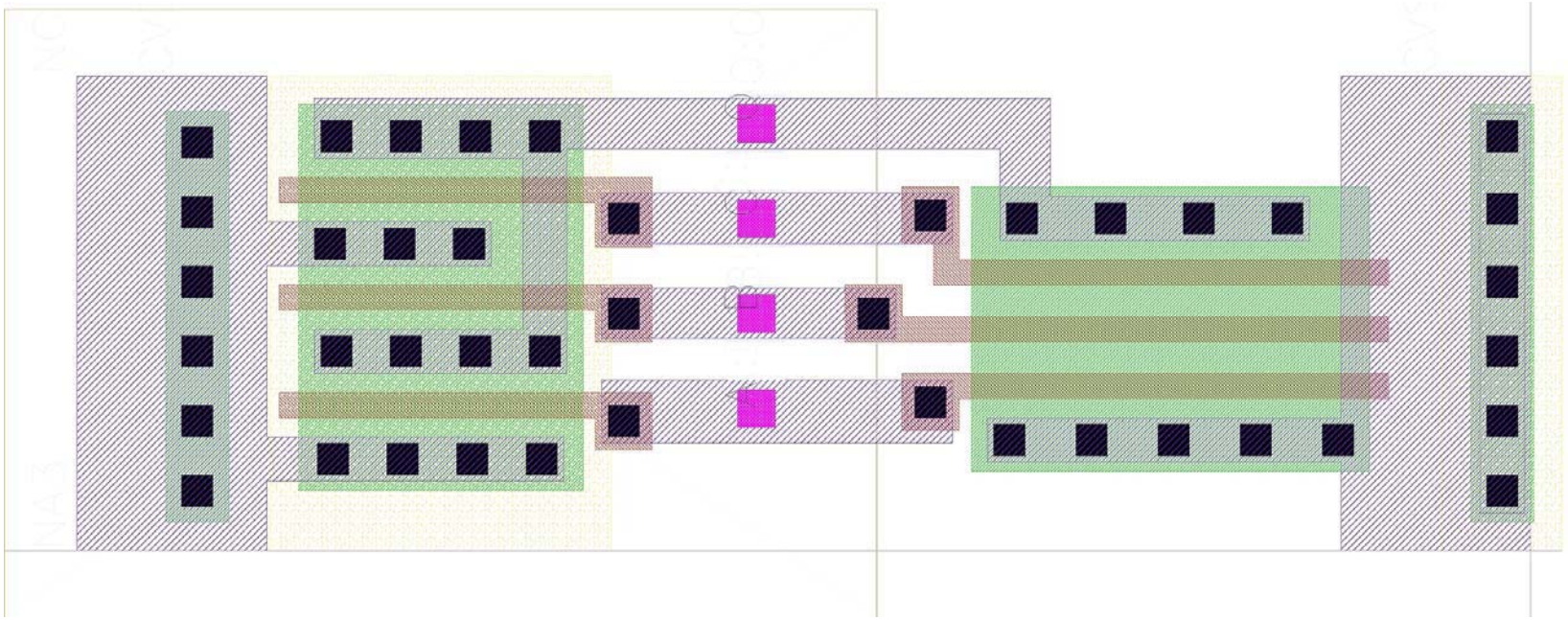
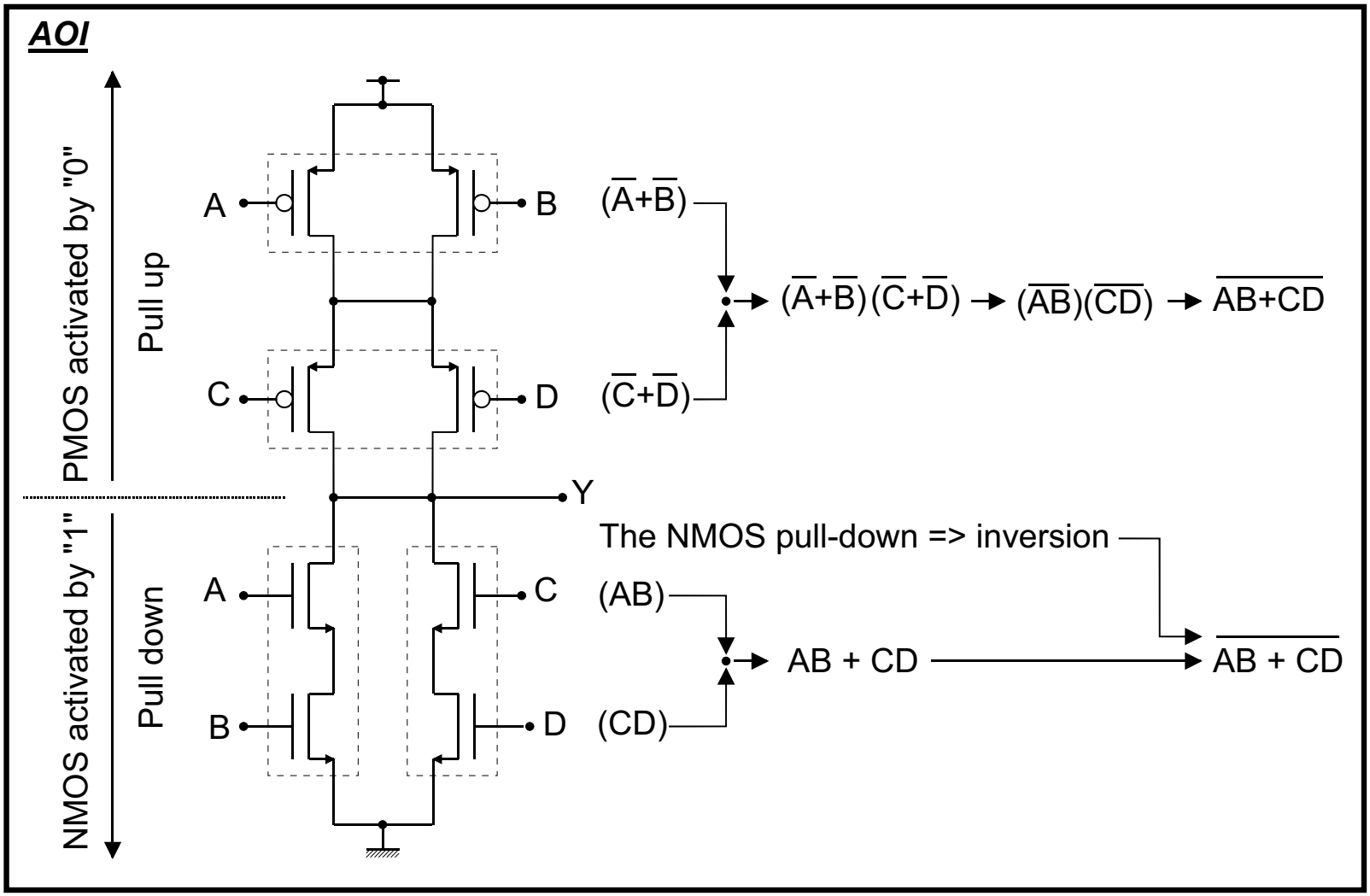
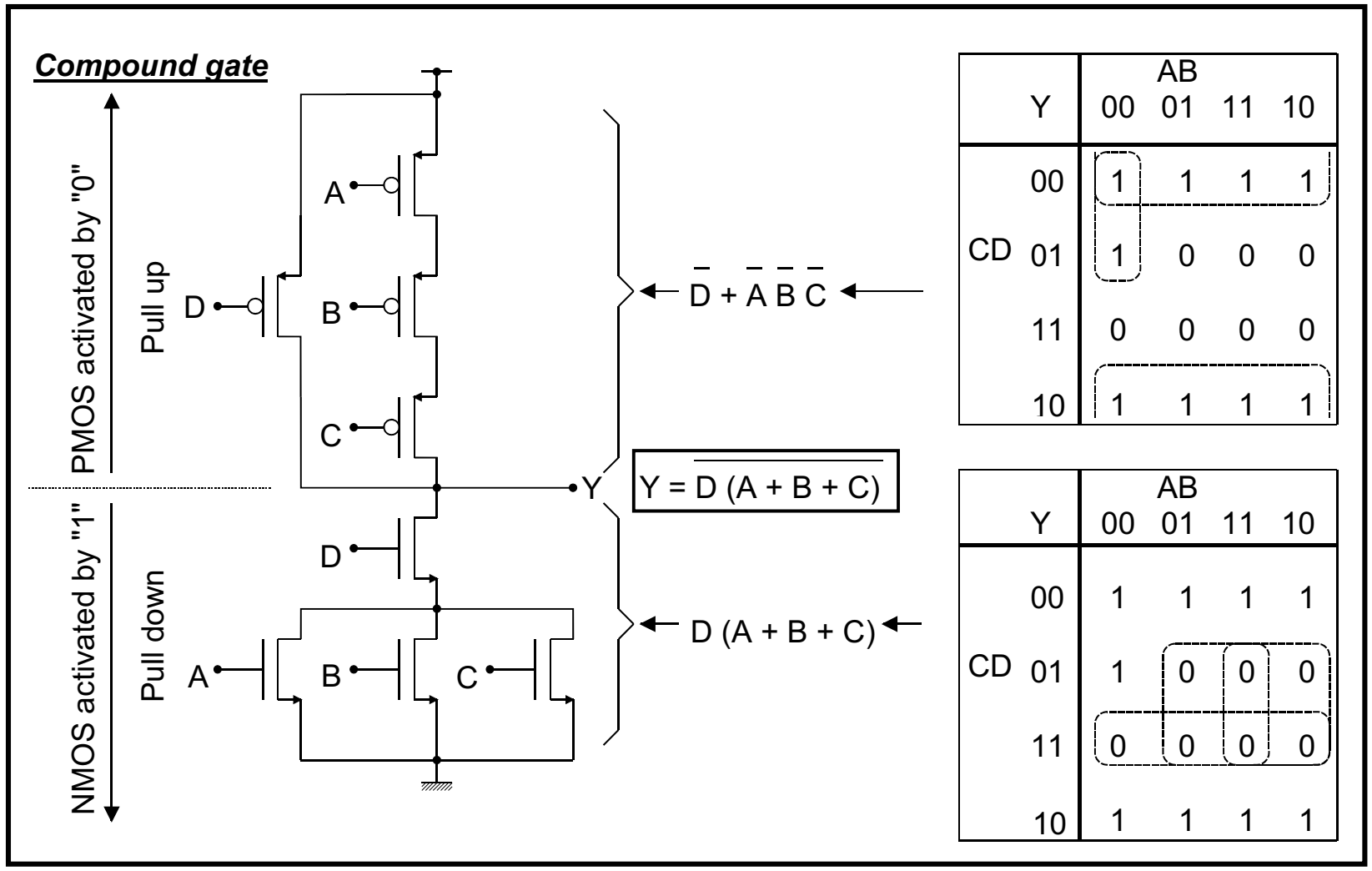


"Reading" CMOS gates



Designing CMOS gates



Y	AB 00	01	11	10
CD 00	1	1	1	1
CD 01	1	0	0	0
CD 11	0	0	0	0
CD 10	1	1	1	1

Y	AB 00	01	11	10
CD 00	1	1	1	1
CD 01	1	0	0	0
CD 11	0	0	0	0
CD 10	1	1	1	1

Complex CMOS gates

- Can a compound gate be arbitrarily complex?
  - NO, propagation delay is a strong function of fan-in:

$$t_p = a_0 \cdot FO + a_1 \cdot FI + a_2 \cdot (FI)^2$$

  - FO $\Rightarrow$ Fan-out, number of loads connected to the gate:
    - 2 gate capacitances per FO + interconnect
  - FI $\Rightarrow$ Fan-in, Number of inputs in the gate:
    - Quadratic dependency on FI due to "RC" signal path across the channels:
      - The resistance increases with the number of transistors in series
      - Each drain and source diffusion adds additional parasitic capacitance
  - Avoid large FI gates (Typically FI $\leq$ 4)