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First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Friday 27 June 2008

Laboratory Session. Implementation in the FPGA Development Platform. VHDL Package and Structural Design. Bidirectional Parallel Port Communication. (16:30-19:00)

time	title	presenter
16:30	Laboratory Session. Implementation in the FPGA Development Platform. VHDL Package and Structural Design. Bidirectional Parallel Port Communication.	MARIA LIZ CRESPO