Table of contents

i

First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977) / Programme

Monday 30 June 2008

First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Monday 30 June 2008

Laboratory Session. Implementation in the FPGA Development Platform. Bidirectional Parallel Port Communication. (12:00-13:00)

time	title	presenter
12:00	Laboratory Session. Implementation in the FPGA Development Platform. Bidirectional Parallel Port Communication.	MARIA LIZ CRESPO

First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977) / Programme

Monday 30 June 2008

Page 1