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Introduction to GPS Receiver Design Principles

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Session Outline

This introductory course on GPS receiver design principles is intended to familiarize the student with the internal components of any global navigation satellite system (GNSS) receiver architecture. Although every GNSS receiver design is uniquely tailored to its intended market and operational application, there is much in common with every GNSS receiver design. This course is taught in the context of the first civil user code and currently the most widely used GNSS signal in space, the GPS coarse/acquisition (C/A) code. As the name implies and as an interesting historical fact, the GPS C/A code was originally intended only to be the "stepping stone" signal into the GPS precision (P) code and was not originally intended to be a steady state satellite navigation signal. Fortunately, the C/A code was so well designed that it became the de-facto civil code after the U.S. Department of Defense (DoD) decided to encrypt the P code, beginning with the GPS Block II satellites. This was done to deny access to enemy military forces and to make it more difficult for an enemy to spoof (falsify) the resulting military P(Y) code signal.

The course consists of six sessions beginning with a high level description of the GPS signals that are processed using a "Generic digital GPS receiver" design as the teaching architecture. This is followed by "GPS receiver baseband processes" that take place after the signal is digitized. Within these baseband processes, there is more design elaboration on the following important topics: "Code tracking loop design;" "Carrier tracking loop design;" "Code and carrier loops filter design;" and, "Extracting measurements from code and carrier loops." These six sessions should provide each student a sound foundation for understanding the principles of operation of all GNSS receivers.

Session Outline

- I - Generic digital GPS receiver
- II- GPS receiver baseband processes
- III - Code tracking loop design
- IV - Carrier tracking loop design
- V- Code and carrier loops filter design
- VI - Extracting measurements from code and carrier loops

Session I

Session I
Generic digital GPS receiver

- Satellite signal modulation and acquisition overview
- Generic digital receiver block diagram
- Analog-to-digital (A/D) conversion
- Digital receiver channel block diagram
- Baseband processor code and carrier tracking loops block diagram
- Baseband signal processing
- Code phase assignments and initial code sequences for C/A-codes
- Code generator design: polynomials and initial states

Satellite signal modulation

The GPS space vehicles (SVs) transmit two carrier frequencies called L1, the primary frequency, and L2, the secondary frequency. The carrier frequencies are modulated by spread spectrum codes with a unique pseudo random noise (PRN) sequence associated with each SV and by the navigation data message. All SVs transmit at the same two carrier frequencies, but their signals do not interfere significantly with each other because of the PRN code modulation. Since each SV is assigned a unique PRN code and all of the PRN code sequences are almost uncorrelated with each other, the SV signals can be separated and detected by a technique called code division multiple access (CDMA). In order to track one SV in common view with several other SVs by the CDMA technique, a GPS receiver must replicate the PRN sequence for the desired SV along with the replica carrier signal, including Doppler effects. Two carrier frequencies are provided to permit the two-frequency user to measure the ionospheric delay since this delay is related by a scale factor to the difference in signal time of arrival for the two carrier frequencies. Single frequency (L1 only) users must estimate the ionospheric delay using modeling parameters which are broadcast to the user in the navigation message. The characteristics of these signals will be explained in more detail.

Satellite signal modulation

- GPS space vehicles (SVs) transmit two carrier frequencies
  - L1 = primary frequency = 1575.42 MHz
  - L2 = secondary frequency = 1227.60 MHz
- Carrier frequencies modulated by
  - Spread spectrum codes with unique pseudo random noise (PRN) sequence associated with each SV
  - Navigation data message = 50 bps

Frequencies and modulation format

The table below summarizes the frequencies and modulation that are used on the GPS satellites. Note that the code usually selected by the Control Segment on L2 is P(Y)-code, but it is possible that the C/A-code could be turned on instead of P(Y)-code on L2. Also note that the 50 Hz navigation data message is usually modulated on L2 P(Y)-code, but can be turned off by the Control Segment to improve jamming performance. This is because a pure PLL carrier tracking loop has a 6 dB higher threshold than a Costas PLL carrier tracking loop and because the predetection integration time can be increased by more than 20 ms, which increases the tracking thresholds of both the code and carrier tracking loops. We will discuss these techniques in detail in this course. For now, just remember that for the L2 link there are three possibilities: P(Y)-code with data, P(Y)-code with no data and C/A-code with data.

Frequencies and modulation format

Signal Priority	Primary	Secondary
signal designation	L1	L2
carrier frequency (Hz) $f_0 = 10.23 \times 10^6$	1575.42×10^6 $154\ f_0$	1227.60×10^6 $120\ f_0$
PRN codes chipping rate (chips/s) $R_0 = 10.23 \times 10^6$	$P(Y) = R_0$ and $C/A = R_0/10$	$P(Y) = R_0$ or $C/A = R_0/10$
navigation message (bps)	50	50

GPS signal acquisition overview

In practice, a GPS receiver must replicate the PRN code that is transmitted by the SV that is being acquired by the receiver, then it must shift the phase of the replica code until it correlates with the SV PRN code. The same correlation properties occur when cross-correlating the transmitted PRN code with a replica code as occurs for the mathematical autocorrelation process for a given PRN code. When the phase of the GPS receiver replica code matches the phase of the incoming SV code, there is maximum correlation. When the phase of the replica code is offset by one chip or more on either side of the incoming SV code, there is minimum correlation. This is indeed the manner in which a GPS receiver detects the SV signal when acquiring or tracking the SV signal in the code-phase dimension. It is important to understand that the GPS receiver must also detect the SV in the carrier-phase dimension by replicating the carrier frequency plus Doppler (and usually eventually obtains carrier phase lock with the SV signal by this means). Thus, the GPS signal acquisition and tracking process is a two-dimensional (code and carrier) signal replication process.

In the code or range dimension, the GPS receiver accomplishes the cross-correlation process by first searching for the phase of the desired SV and then tracking the SV code state by adjusting the nominal chipping rate of its replica code generator to compensate for the Doppler-induced effect on the SV PRN code due to line-of-sight relative dynamics between the receiver and the SV. There is also an apparent Doppler effect on the code tracking loop caused by the frequency offset in the receiver's reference oscillator with respect to its specified frequency. This error effect, which is the time bias rate determined by the navigation solution, is quite small for the code tracking loop and is usually neglected. The code correlation process is implemented as a real-time multiplication of the phase-shifted replica code with the incoming SV code, followed by an integration and dump process. The objective of the GPS receiver is to keep the prompt phase of its replica code generator at maximum correlation with the desired SV code phase.

However, if the receiver has not simultaneously adjusted (tuned) its replica carrier signal so that it matches the frequency of the desired SV carrier, then the signal correlation process in the range dimension is severely attenuated by the resulting frequency response roll-off characteristic of the GPS receiver. Consequently, the receiver never acquires the SV. If the signal is successfully acquired because the SV code and frequency are successfully replicated during the search process, but then the receiver subsequently loses track of the SV frequency, then the receiver subsequently loses code track as well. Thus, in the carrier Doppler frequency dimension, the GPS receiver accomplishes the carrier matching (wipe-off) process by first searching for the carrier Doppler frequency of the desired SV and then tracking the SV carrier Doppler state. It does this by adjusting the nominal carrier frequency of its replica carrier generator to compensate for the Doppler induced effect on the SV carrier signal due to line-of-sight relative dynamics between the receiver and the SV. There is also an apparent Doppler error effect on the carrier loop caused by the frequency offset in the receiver's reference oscillator with respect to its specified frequency. This error, which is common with all the satellites being tracked by the receiver, is determined by the navigation filter as the time bias rate in units of seconds per second.

The two-dimensional acquisition and tracking process can best be explained and understood in progressive steps. The clearest explanation is in reverse sequence from the events that actually take place in a real-world GPS receiver. The two-dimensional search and acquisition process is easier to understand if the two-dimensional steady-state tracking process is explained first. The two-dimensional code and carrier tracking process is easier to understand if the carrier tracking process is explained first. This is the explanation sequence that will be used. The explanation will first be given in the context of a generic GPS receiver architecture with minimum use of equations. This high-level overview will then be followed by more detailed explanations of the carrier and code tracking loops, including the most useful equations.

GPS signal acquisition overview

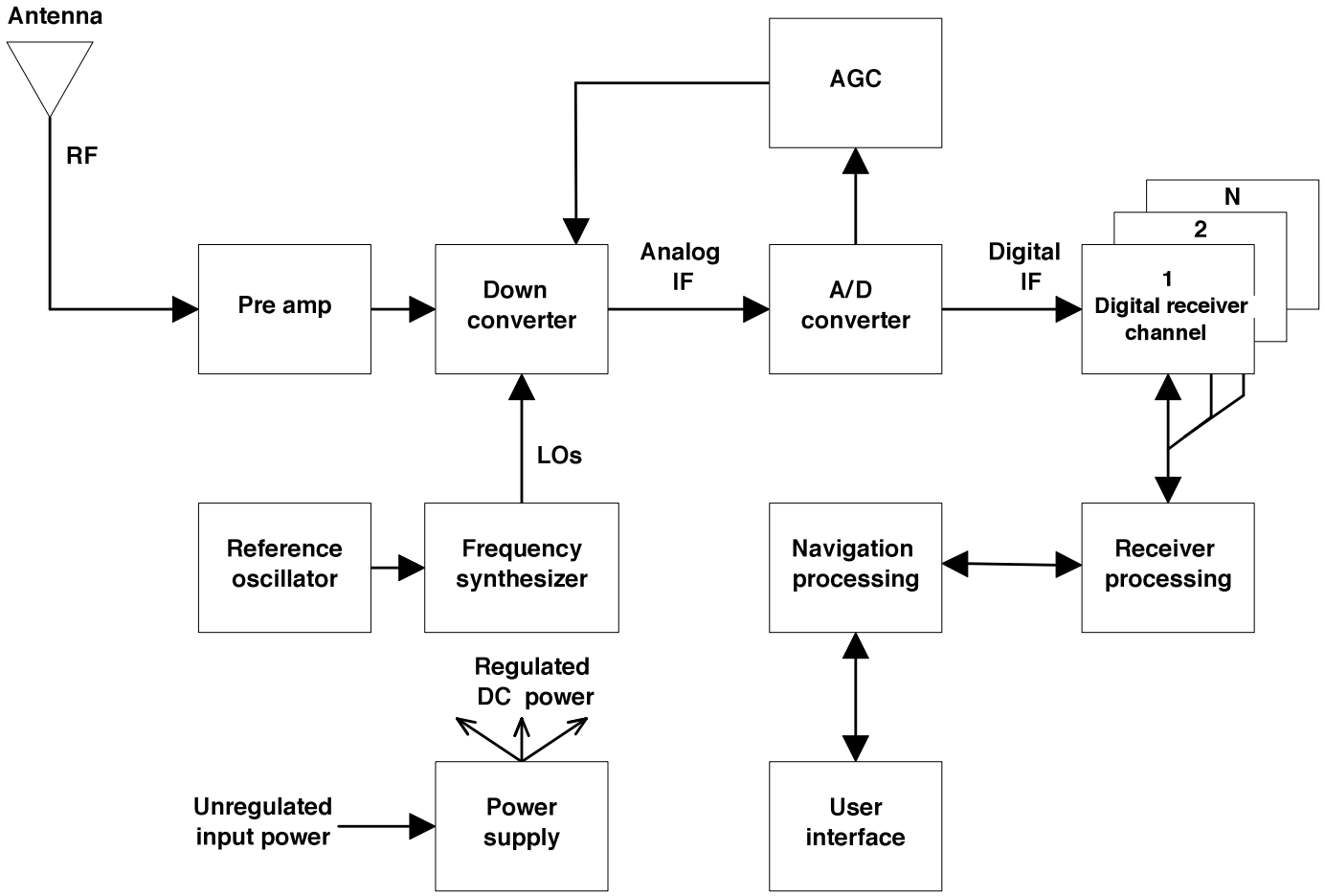
- GPS receiver signal acquisition
  - Receiver must replicate PRN code transmitted by SV
  - Receiver must shift phase of replica code until it correlates with SV PRN code as received at GPS receiver antenna
  - Receiver simultaneously adjusts (tunes) replica carrier to match desired SV carrier frequency (two-dimensional search) as received at GPS receiver antenna

Generic digital GPS receiver block diagram

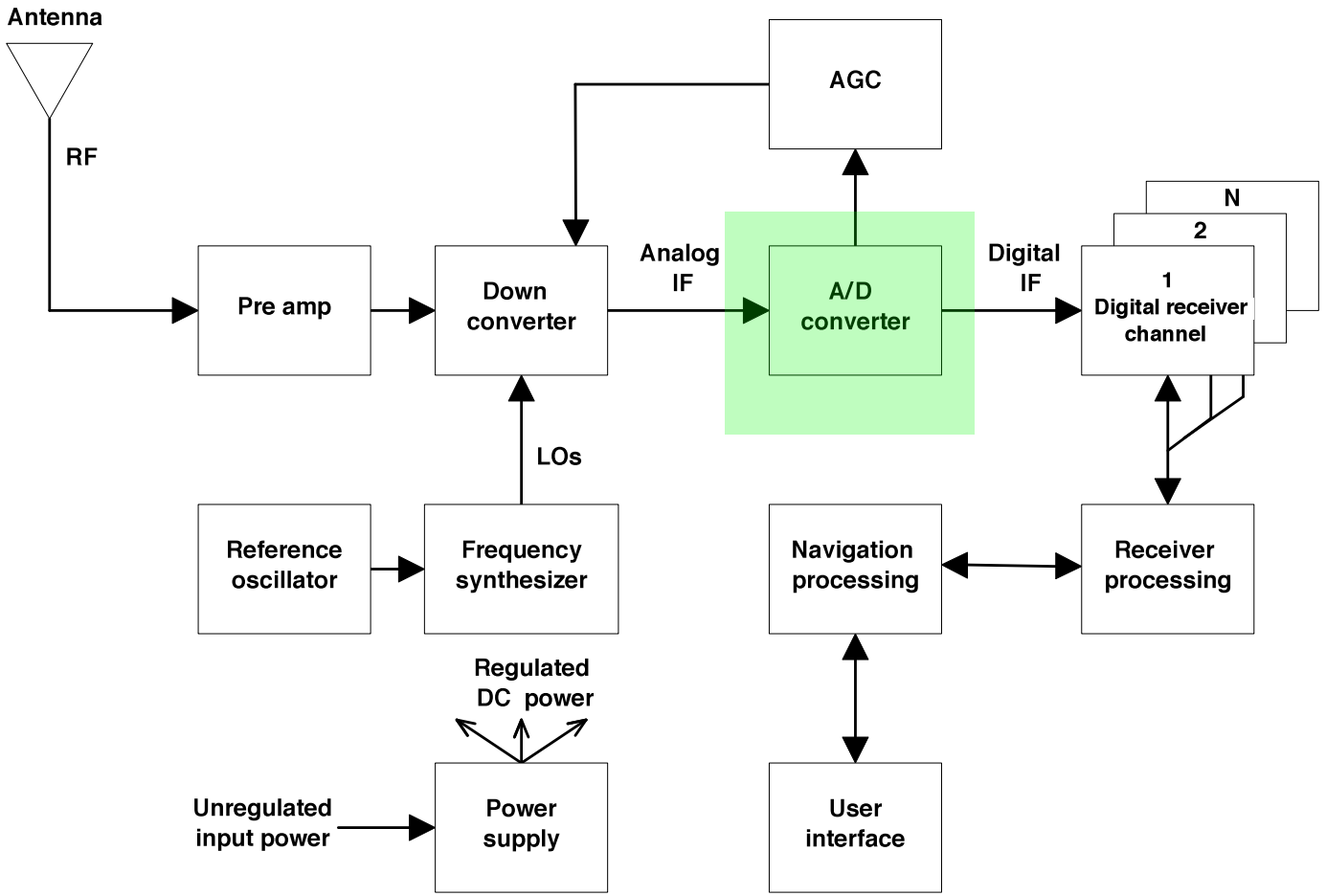
In the figure below, the GPS radio frequency (RF) signals of all SVs in view are received by a right hand circularly polarized antenna with nearly hemispherical gain coverage. These RF signals are amplified by a low noise preamplifier (preamp) which effectively sets the noise figure of the receiver. There may be a passive bandpass prefilter between the antenna and preamp to minimize out-of-band RF interference. These amplified and signal conditioned RF signals are then down-converted to an intermediate frequency (IF) using signal mixing frequencies from local oscillators (LOs). The LOs are derived from the reference oscillator by the frequency synthesizer based on the frequency plan of the receiver design. One LO per down converter stage is required. Two-stage down conversion to IF is typical, but one-stage down conversion and even direct L-band digital sampling have also been used. The LO signal mixing process generates both upper and lower sidebands of the SV signals, so the lower sidebands are selected and the upper sidebands and leak-through signals are rejected by a postmixer bandpass filter. The signal Dopplers and the PRN codes are preserved after the mixing process. Only the carrier frequency is lowered. The analog-to-digital (A/D) conversion process and automatic gain control (AGC) functions take place at IF. Not shown in the block diagram are the baseband timing signals that are provided to the digital receiver channels by the frequency synthesizer phase locked to the reference oscillator's stable frequency. The IF must be high enough to provide a single-sided bandwidth that will support the PRN code chipping frequency. An anti-aliasing IF filter must suppress the stopband noise (unwanted out-of-band signals) to levels that are acceptably low when this noise is aliased into the GPS signal passband by the A/D conversion process. All of the visible GPS signals are buried in the thermal noise at IF.

At this point the digitized IF signals are ready to be processed by each of the N digital receiver channels. No demodulation has taken place, only signal conditioning and conversion to the digital IF. These digital receiver channel functions are usually implemented in one or more application specific integrated circuits (ASICs). This is why these functions are shown as separate from the receiver processing function in the block diagram of the figure below. The name "digital receiver channel" is somewhat misleading since it is not the ASIC but the receiver processing function which usually implements numerous baseband functions such as the loop discriminators and filters, data demodulation, C/N_0 meters, phase lock indicators, etc. The receiver processing function is usually a microprocessor. The microprocessor not only performs the baseband functions, but also the decision-making functions associated with controlling the signal preprocessing functions of each digital receiver channel. It is common that a single high-speed microprocessor supports the receiver, navigation and user interface functions.

Generic digital receiver block diagram



Generic digital receiver block diagram – A/D converter



Analog-to-digital (A/D) converter

The analog-to-digital (A/D) converter performs two processes on the incoming analog signal: (1) sampling and (2) quantization.

The sampling process must be chosen by the design engineer to be consistent with the Nyquist criteria. Nyquist proved that if there is at least two samples per cycle at the frequency above which there is no data (including noise), then no information is lost in the sampling process. The adverse consequence of disobeying this criteria is that any analog information that is present above the Nyquist frequency will be aliased (folded) back into the sampled data that can never be removed by any subsequent digital signal processing. Long ago, Norbert Weiner proved that the Nyquist criteria is theoretically impossible to achieve, but practically speaking, it is possible to design anti-aliasing filters that suppress the unwanted signals, including noise, to a sufficiently low level that the aliasing that results contributes negligible distortions.

The quantization level is usually the focus of design attention (often to the neglect of the Nyquist sampling theorem). Earlier versions of GPS receivers used analog correlators when digital technology was not fast enough to A/D convert and process the IF signals at appropriate sampling rates. These A/D converters were implemented at baseband just after the code wipeoff process with analog anti-alias filtering that also provided a portion of the predetection integration process. Typically, these were 8-bit A/D converters (256 quantization levels) and a multiplicity of them were required for each receiver channel. These are called post-correlation A/D converters and the receivers designed in this manner were called analog receivers. Currently, all GNSS receiver designs employ the A/D converter in the location shown in the generic GPS receiver design. These are called pre-correlation A/D converters and the receives are called digital receivers. The vast majority of these A/D converters are 1, 2 and 3-bit converters with 2, 4 and 8 levels of precision, respectively. There is little to be gained with quantization precision above 3-bits provided that the intended operational environment is benign (no RF interference (RF)) or jamming).

For RFI or jamming environments, very high resolution A/D conversion is required, typically 10 to 12 bits or more, in order to implement RFI or jamming mitigation either with spectral excision for narrowband emitters or with a controlled reception pattern antenna (CRPA) for wideband emitters. The CRPA uses a multiple antenna element array that requires a separate RF front end per element. Each RF front end contains a high-quantization precision A/D converter.

A low-cost non-linear three-level flash A/D converter (ADC) can be very effective in some RFI environments [1]. When used in combination with a digital gain controlled automatic gain control (AGC) design, this ADC can effectively suppress continuous wave (CW) narrow-band jammers. It can also detect the presence of any RFI, then measure and characterize it as either narrowband or wideband. This part of the GNSS receiver continues to operate effectively even when the interference level is so high that the receiver cannot acquire and track the GNSS signals.

[1] Ward, Philip, "Simple Techniques for RFI Situational Awareness and Characterization in GNSS Receivers," Proceedings of The Institute of Navigation National Technical Meeting 2008, San Diego, CA, January 28-30.

Analog-to-digital (A/D) conversion

- Most receivers today digitize after down-conversion and prior to correlation
  - Post-correlation A/D was norm long ago
- Vast majority of commercial receivers use between 1-3 bits (2 - 8 output levels)
  - In benign environments, no gain from additional levels
  - For interference excision (anti-jam) applications, 10 to 12 bit A/D converters are required
  - For continuous wave (CW) interference mitigation, non-linear 1.5 bit A/D converters are very effective

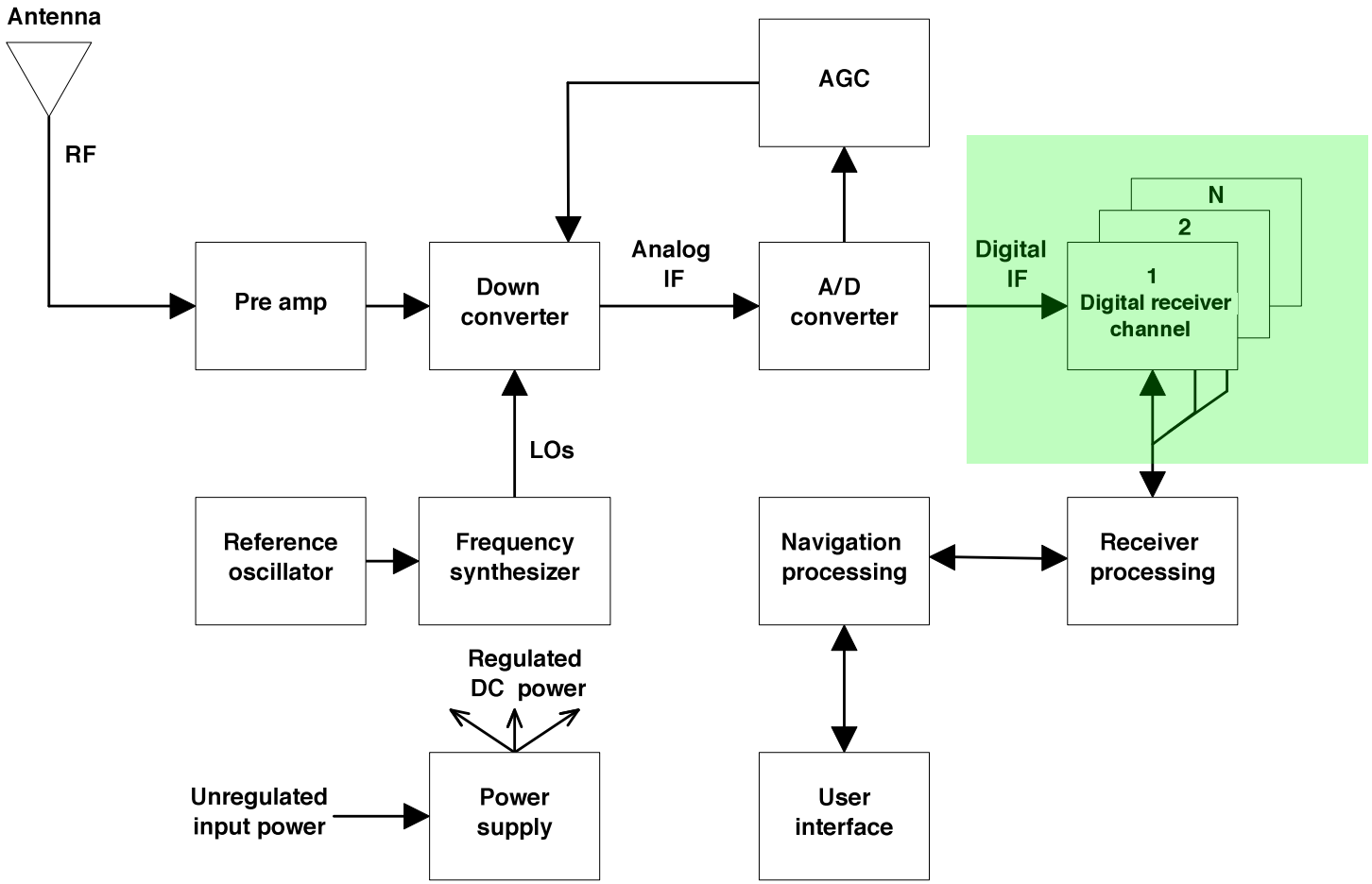
GPS receiver code and carrier tracking

Most modern GPS receiver designs are digital receivers. These receiver designs have evolved rapidly toward higher and higher levels of digital component integration. This trend is expected to continue. For this reason, a high-level block diagram of a modern digital GPS receiver will be used to represent a generic GPS receiver architecture as shown in the following figure. There will be similarities and differences between this generic design and other military or commercial GPS receiver designs. The differences are often simply due to the origin of the design; i.e., the functional partitioning of the first design was driven by a different situation in available components at the time. Other differences are due to the evolution of the design. In both cases the design is driven in large part by cost. Even though high level integration can reduce parts count without a reduction in complexity, there are usually constraints at every technology generation which cause changes in the original architecture. Especially in commercial GPS receiver design, there is a significant emphasis on reducing design complexity as well as reduction on parts count. Many commercial GPS receiver manufacturers have found clever ways to greatly simplify their GPS receiver designs, but there is usually a performance penalty when the functions shown in this generic architecture are altered excessively.

GPS receiver code and carrier tracking

- Most modern GPS receiver designs are digital (signal is digitized prior to detection)
- Receiver designs have evolved rapidly toward higher levels of digital component integration
- Modern GPS receiver is represented by a generic digital GPS receiver architecture
- GPS receiver code and carrier tracking explained in context of this generic digital architecture
- Modern digital receivers similar to generic architecture but designs driven by origin/evolution/cost
  - Performance penalties result if cost reduction focus is primarily on component reduction instead of technology advances

Generic digital receiver block diagram – Digital receiver channels



Digital receiver channel block diagram

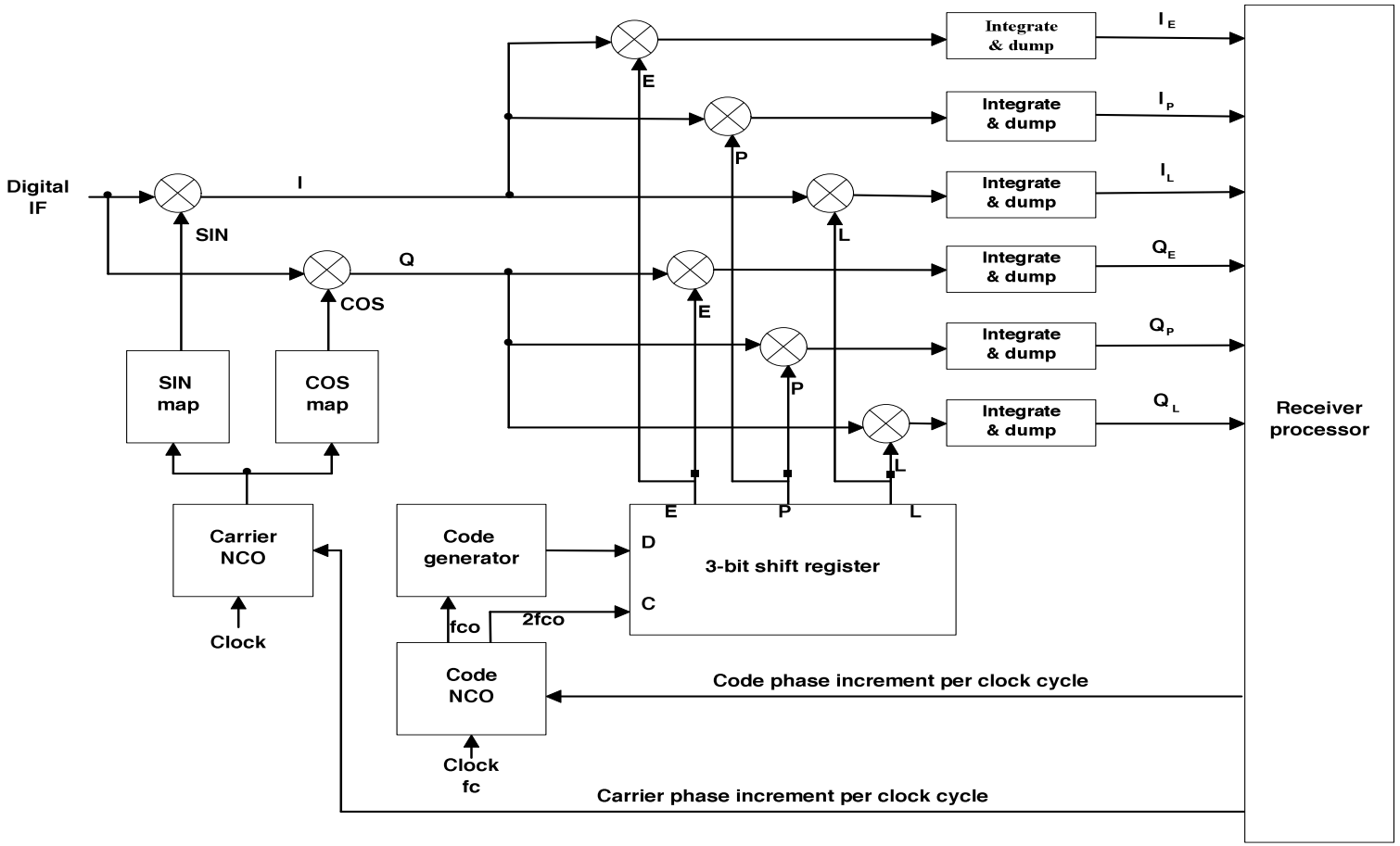
The digital receiver channel block diagram represents one channel of the receiver where the digitized intermediate frequency (IF) signals are applied to the input. For simplification, only the functions associated with the code and carrier tracking loops are illustrated and the receiver channel is assumed to be tracking the SV signal in steady state. First, the digital IF signal of the SV being tracked is stripped of the carrier (plus carrier Doppler) by the replica carrier (plus carrier Doppler) signal to produce in-phase (I) and quadra-phase (Q) signals. Note that the replica carrier signal is being mixed with all of the GPS SV signals (buried in noise) at the digital IF. Also note that this is the first digital process associated with the sampled and quantized analog IF data; i.e., A/D converted IF data. The I and Q signals at the outputs of the mixers have the desired phase relationships with respect to the detected carrier of the desired SV. However, the code stripping processes which collapse these signals to baseband have not yet been applied. Therefore, the I signal at the output of the in-phase mixer would be mostly thermal noise multiplied by the replica digital sine wave (to match the SV carrier at IF) and the Q signal at the output of the quadra-phase mixer would be the product of mostly thermal noise and the replica digital cosine wave (to match the SV carrier at IF). The desired SV signal remains buried in noise until the I and Q signals are collapsed to baseband by the code stripping process which follows. The replica carrier (including carrier Doper) signals are synthesized by the carrier numerical controlled oscillator (NCO) in combination with the discrete sine and cosine mapping functions.

The NCO generates an internal digital staircase function whose period is the desired replica carrier plus Doppler period. The sine and cosine map functions convert the NCO internal digital staircase amplitudes into the corresponding digital amplitudes of the respective sine and cosine functions. Buy producing I and Q component phases 90 degrees apart, the resultant signal amplitude can be computed from the vector sum of the I and Q components and the phase angle with respect to the I-axis can be determined from the arctangent of Q/I. In closed loop operation, the carrier NCO is controlled by the carrier tracking loop in the receiver processor. In phase lock loop (PLL) operation, the objective of the carrier tracking loop is to keep the phase error between the replica carrier and the incoming SV carrier signals at zero. Any misalignment in the replica carrier phase with respect to the incoming SV signal carrier phase is detected in the receiver processor as a non-zero error in the phase angle of the prompt I and Q vector magnitude, then corrected in the carrier NCO output so the I signals are maximum and the Q signals are nearly zero.

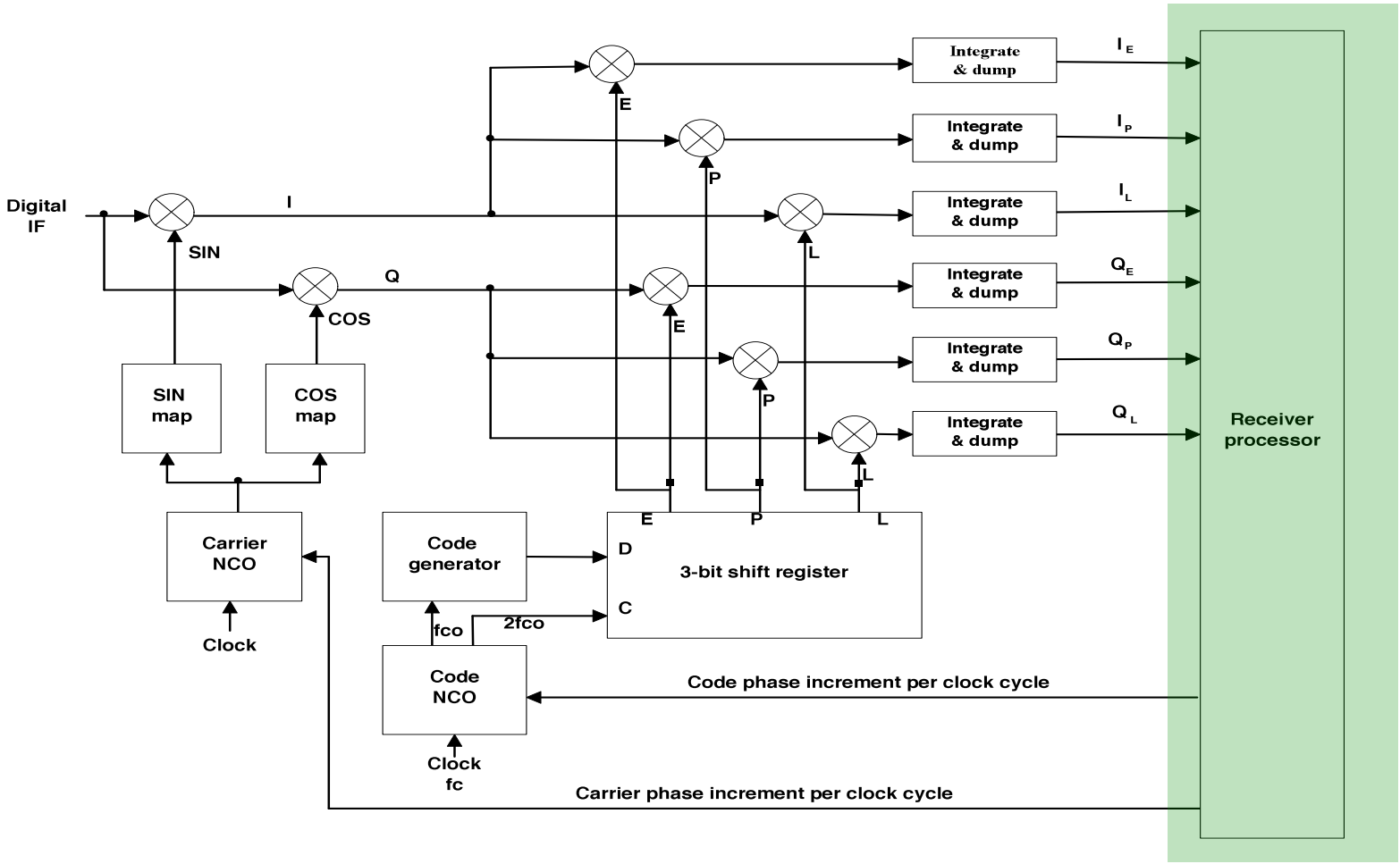
The I and Q signals are then correlated with early, prompt and late replica codes (plus code Doppler) synthesized by the code generator, a 2-bit shift register, and the code NCO. These six correlated outputs are then filtered by integrate and dump circuits, then fed to the receiver processor. In closed loop operation, the code NCO is controlled by the code tracking loop in the receiver processor. In this design, the code NCO produces twice the code generator clocking rate, $2f_c$, and this if fed into the 2-bi shift register. The code generator clocking rate, f_c, which contains the code chipping rate (plus code Doppler) is fed into the code generator. With this combination, the shift register produces three phases of the code generator output, each phase shifted by ½ chip apart. Not shown are the controls to the code generator which permit the receiver processor to preset the initial code tracking phase states which are required during the code search and acquisition process.

The prompt replica code phase is aligned with the incoming SV code phase producing maximum correlation if it is tracking the incoming SV code phase. In this design, the early phase is aligned ½ chip early and the late phase is alighted ½ chip late with respect to the incoming SV code phase and these correlations produce about half the maximum correlation. Any misalignment in the replica code phase with respect to the incoming SV code phase produces a difference in the vector magnitudes of the early and late correlated outputs so that the amount and direction of the phase change can be detected and corrected by the code tracking loop.

Digital receiver channel block diagram



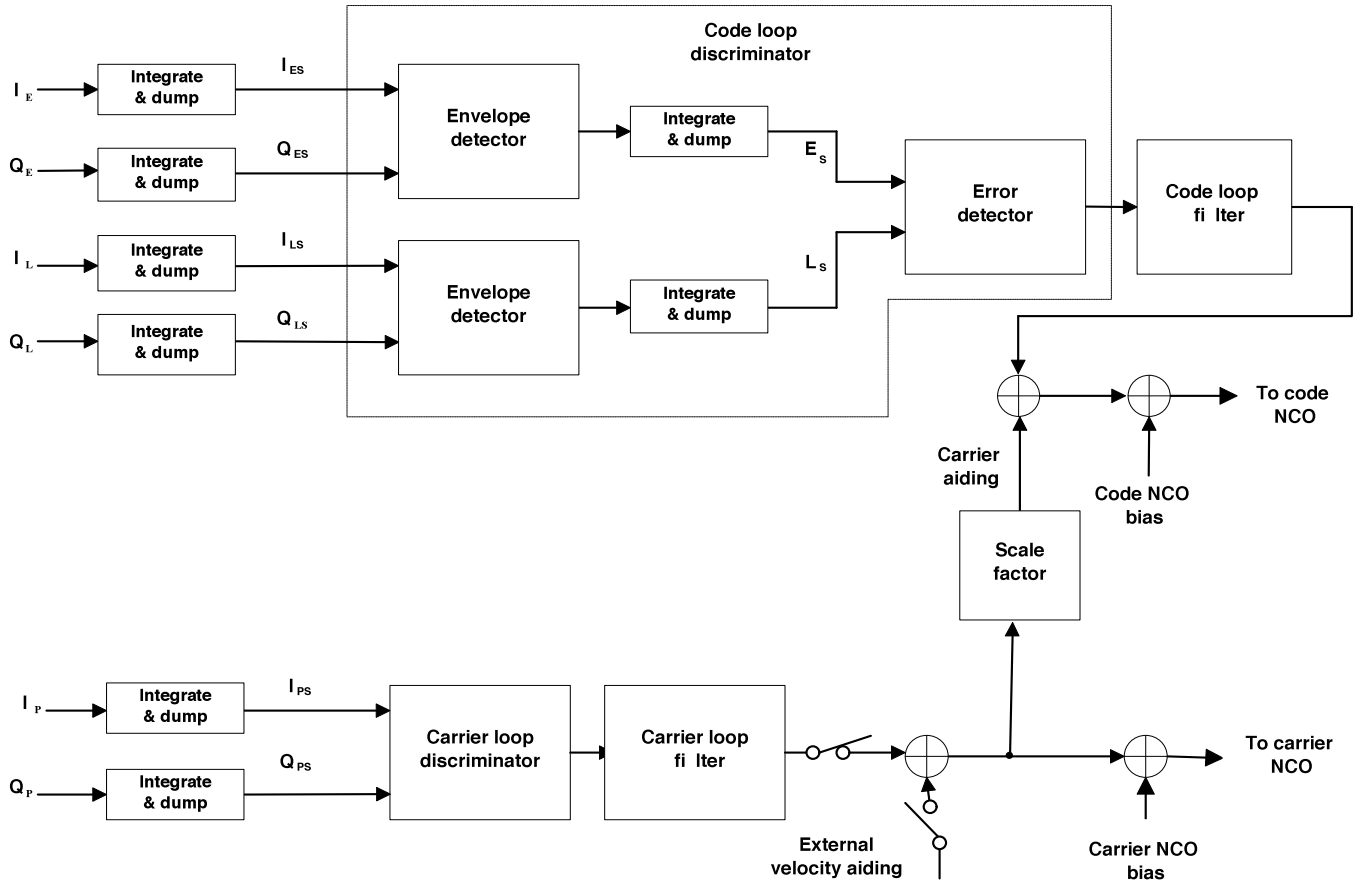
Digital receiver channel block diagram – code and carrier tracking loops



Baseband signal processing for code and carrier tracking loops

The receiver processor shown in the previous figure receives the I and Q signals from the signal digital receiver channel, performs the baseband signal processing (which includes code and carrier tracking loops) and then sends the resulting code and carrier update signals to the code/carrier replica signal generation circuits (specifically the NCOs). The figure below provides more detail on the code and carrier tracking loops which are implemented in the receiver processor

Baseband processor code and carrier tracking loops block diagram



Baseband signal processing

The previous figure illustrates typical baseband code and carrier baseband signal processing functions for one receiver channel in the closed loop mode of operation. The functions are typically performed by the receiver processor. The combination of these code and carrier tracking baseband signal processing functions and the digital receiver channel code and carrier wipe-off and predetection integration functions form the code and carrier tracking loops of one GPS receiver channel.

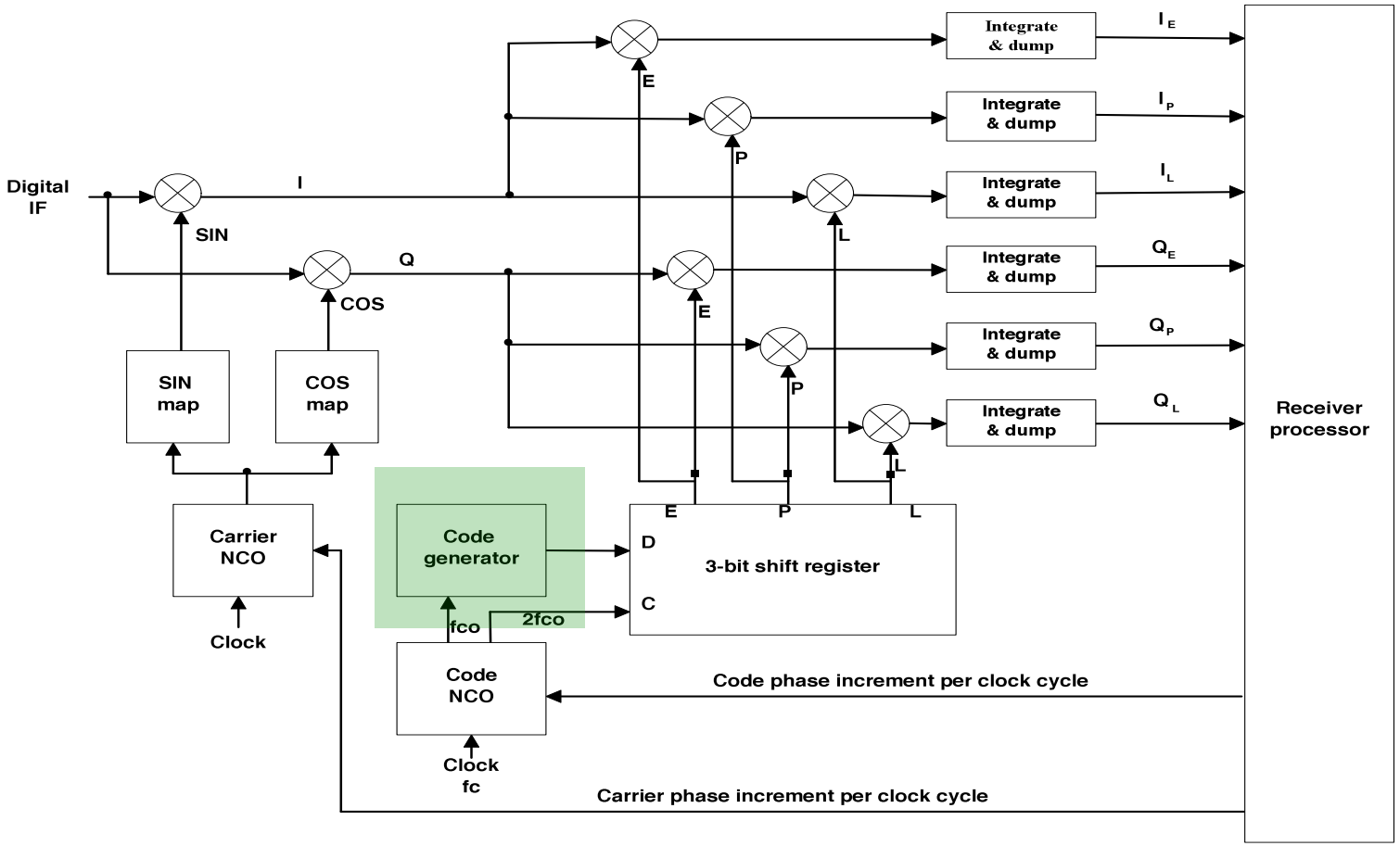
The baseband signal processing functions are usually implemented in firmware. Note that the firmware need only be written once since the microprocessor runs all programs sequentially (as opposed to the simultaneous parallel processing that takes place in the digital receiver ASIC(s)). Therefore, the microprocessor program can be designed to be reentrant with a unique variable area for each receiver channel so that only one copy of each algorithm is required to service all receiver channels. This reduces the program memory requirements and ensures that every receiver baseband processing function is identical.

The three complex pairs of baseband I and Q signals from the digital receiver may be resampled again by the integrate and dump accumulators. The total combined duration of the receiver and processor integrate and dump functions establishes the predetection integration time for the signal. Normally, this cannot exceed 20 milliseconds which is the 50 Hz navigation message data period (50 Hz message has a 20 ms period between potential data bit transitions). After carrier and code wipe-off have taken place, only the 50 Hz navigation message data modulation signal remains at baseband.

Baseband signal processing

- Baseband signal processing functions are typically performed by the receiver processor
- Software code/carrier tracking at baseband driving code/carrier wipe-off hardware followed by predetection integration functions form code/carrier tracking loops of one receiver channel
- Digital receiver channel hardware ASICs run in parallel
- Microprocessor runs all baseband signal processing programs sequentially

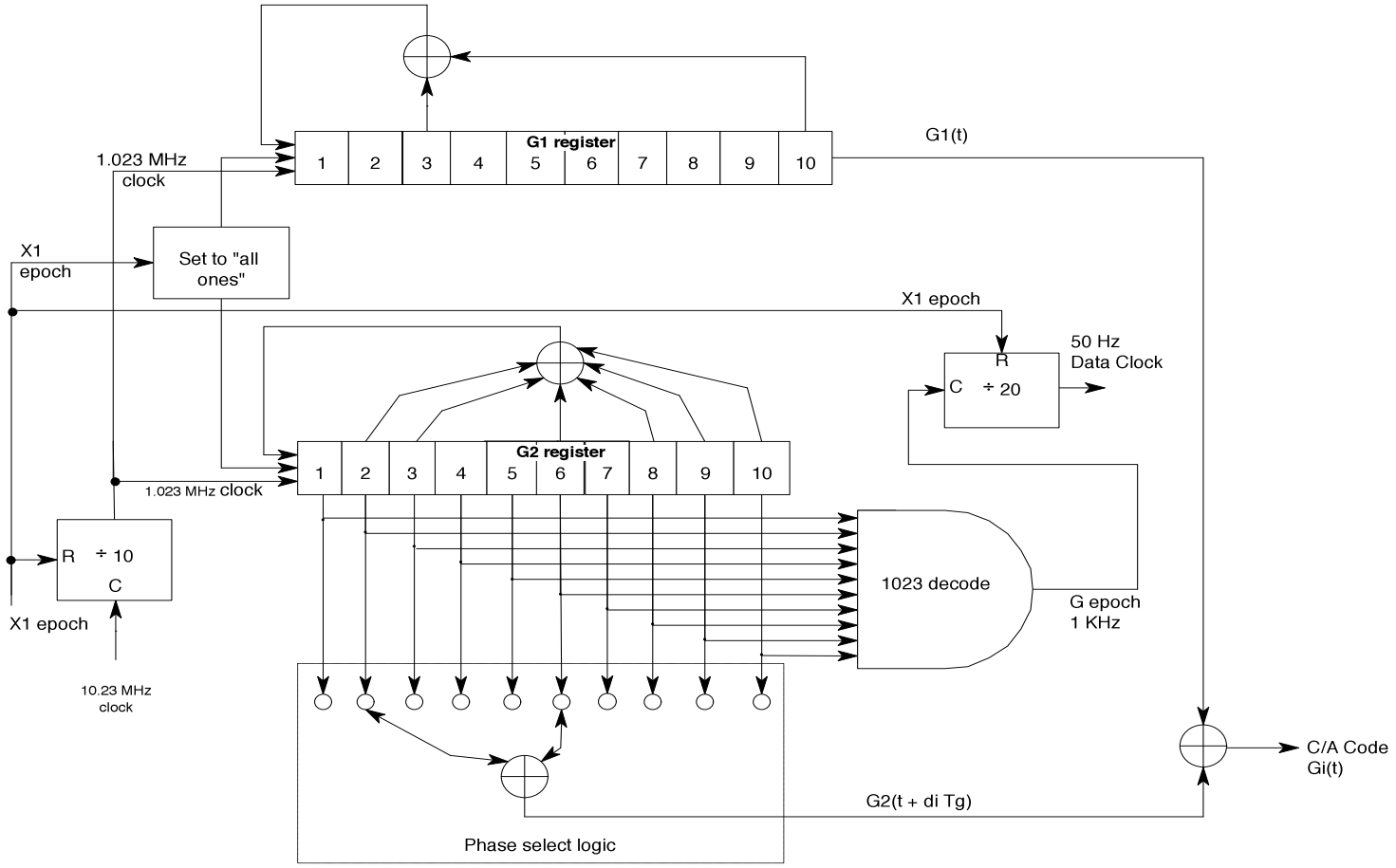
Digital receiver channel block diagram – code generator



C/A-code generator

The GPS C/A-code is a Gold code [2] with a sequence length of 1023 bits (chips). Since the chipping rate of the C/A-code is 1.023 MHZ, then the repetition period of the pseudo random sequence is 1023/1.023 X 10^6 or one millisecond. The figure below illustrates the design architecture of the GPS C/A-code generator. Not included in this diagram are the controls necessary to set or read the phase states of the registers or the counters. There are two 10-bit shift registers, G1 and G2, which generate maximum length pseudo noise (PN) codes with a length of 2^{10} - 1 = 1023 bits. (The one state that the shift register must not get into is the all-zero state). It is common to describe the design of linear code generators by means of polynomials of the form 1 + Γ x^i, where x^i means that the output of the ith cell of the shift register is used as the input to the modulo-2 adder (exclusive or) and the 1 means that the output of the adder is fed to the first cell [3]. The design specification for C/A-code calls for the feedback taps of the G1 shift register to be connected to stages three and 10. These register states are combined with each other by an exclusive-or circuit and fed back to stage one. The polynomial which describes this shift register architecture is: G1 = 1 + X^3 + X^{10}. The polynomials and initial states for both the C/A-code and P-code generator shift registers are summarized in the table which follows the figure below. The unique C/A-code for each SV is the result of the exclusive-or of a delayed version of the G2 output sequence and the G1 direct output sequence. The delay effect in the G2 PN code is obtained by the exclusive-or of the selected positions of the two taps whose output is called G21. This is because a PN code sequence has the property that, when added to a phase shifted version of itself, it does not change but simply obtains another phase. The function of the two taps on the G2 shift register in the figure below is to shift the code phase in G2 with respect to the code phase in G1 without the need for an additional shift register to perform this delay. Each C/A-code PRN number is associated with the two tap positions on G2. The previous table describes these tap combinations for all defined GPS PRN numbers and also specifies the equivalent delay in C/A-code chips. The first 32 of these PRN numbers are reserved for the space segment. Five additional PRN numbers, PRN 33 to PRN 37, are reserved for other uses such as ground transmitters (GTs). GTs were used during Phase I (concept demonstration phase) of GPS to validate the operation and accuracy of the system before satellites were launched. The GT C/A-codes 34 and 37 are identical.

C/A-code generator



Code phase assignments and initial code sequences for C/A-code and P-code

The delays associated with the C/A-code and P-code PRN sequences are summarized in the table below taken from ICD-GPS-200 [1]. The C/A-code delay can be implemented by a simple, but equivalent, technique which eliminates the need for a delay register. The C/A-code tap selection column describes the two-tap combinations associated with each SV PRN number. This two-tap delay technique used for the C/A-code generator is explained in more detail when the C/A-code generator is described. Note that the P-code delay in chips is identical to its PRN number, but that the C/A-code delay does not bear a mathematical relationship to the PRN number (either the two-tap combination or the delay must be obtained by table look-up). Also note that the first 10 C/A-chips from the beginning of each C/A-code epoch (every 1 ms) and the first 12 P-chips from the beginning of the GPS week are shown in octal notation in this table. The octal notation is explained both here and in the footnotes. In the octal notation for the first 10 chips of the C/A-code, the first digit (1) represents a “1" for the first chip and the last three digits are the conventional octal representation of the remaining nine chips. For example, the first 10 chips of the SV PRN number 1 C/A-code are 1100100000. The footnotes also describe that PRN codes 33 through 37 are reserved for other uses; e.g., ground transmitters (GTs). These were the GT PRN codes used for the Yuma Proving Ground inverted range in the early test phases of the GPS concept demonstration program which started before the first Block I SVs were launched. Note that C/A-codes for PRN 34 and PRN 37 are identical GT C/A-codes, but are different P-codes. This was because no more two-tap C/A-code combinations with the desirable cross correlation properties were left. However, numerous other C/A-code combinations with acceptable properties are available. These will be used in the FAA Wide Area Augmentation System (WAAS) for the Geostationary C/A-code only satellites. The WAAS C/A-code generator requires a design extension in the two-tap scheme.

Code phase assignments and initial code sequences for C/A- and P-code

SV PRN number	C/A-code tap selection	C/A-code delay (chips)	P-code delay (chips)	First 10 C/A-chips(octal)*	First 12 P-chips (octal)*
1	2⊕6	5	1	1440	4444
2	3⊕7	6	2	1620	4000
3	4⊕8	7	3	1710	4222
4	5⊖9	8	4	1744	4333
5	1⊖9	17	5	1133	4377
6	2⊕10	18	6	1455	4355
7	1⊕8	139	7	1131	4344
8	2⊕9	140	8	1454	4340
9	3⊕10	141	9	1626	4342
10	2⊕3	251	10	1504	4343
11	3⊕4	252	11	1642	"
12	5⊕6	254	12	1750	"
13	6⊕7	255	13	1764	"
14	7⊕8	256	14	1772	"
15	8⊕9	257	15	1775	"
16	9⊕10	258	16	1776	"
17	1⊕4	469	17	1156	"
18	2⊕5	470	18	1467	"
19	3⊕6	471	19	1633	"
20	4⊕7	472	20	1715	"
21	5⊕8	473	21	1746	"
22	6⊕9	474	22	1763	"
23	1⊕3	509	23	1063	"
24	4⊕6	512	24	1706	"
25	5⊕7	513	25	1743	"
26	6⊕8	514	26	1761	"
27	7⊕9	515	27	1770	"
28	8⊕10	516	28	1774	"
29	1⊕6	859	29	1127	"
30	2⊕7	860	30	1453	"
31	3⊕8	861	31	1625	"
32	4⊕9	862	32	1712	"
33**	5⊕10	863	33	1745	"
34**	4⊕10***	950***	34	1713***	"
35**	1⊕7	947	35	1134	"
36**	2⊕8	948	36	1456	"
37**	4⊕10***	950***	37	1713***	4343

* In the octal notation for the first 10 chips of the C/A-code as shown in this column, the first digit (1) represents a "1" for the first chip and the last three digits are the conventional octal representation of the remaining 9 chips. For example, the first 10 chips of the SV PRN number 1 C/A-code are 1100100000. **PRN codes 33 through 37 are reserved for other uses; e.g., ground transmitters. ***C/A-codes 34 and 37 are identical.

GPS code generator polynomials & initial states

Continuing from the previous discussion, there is also a phase precession between the X2A/X2B shift registers with respect to the X1A/X1B shift registers. This is manifested as a phase precession of 37 chips per X1 period between the X2 epochs as the output of the divide by 37 counter) and the X1 epochs. This is caused by adjusting the X2 period to be 37 chips longer than the X1 period. The details of this phase precession are as follows. The X1 epoch is defined as 3750 X1A cycles. When X1A has cycled through 3750 of these cycles or 3750 X 4092 = 15,345,000 chips, a 1.5 second X1 epoch occurs. When X1B has cycled through 3749 cycles of 4093 chips per cycle, it is kept stationary for 343 chips by halting its clock control until the 1.5 second X1 epoch causes it to continue. Therefore, the X1 registers have a combined period of 15,345,000 chips. X2A and X2B are controlled in the same way as X1A and X1B, respectively, but with one difference: when 15,345,000 chips have completed in exactly 1.5 seconds, both X2A and X2B are kept stationary for an additional 37 chips by halting their clock controls until the X2 epoch or the start of the week causes it to continue. Therefore, the X2 registers have a combined period of 15,345,037 chips, which is 37 chips longer than the X1 registers.

Note that if the P-code was generated by X1 —X2 and was not reset at the end of the week, it would have the potential sequence length of 15,345,000 X 15,345,037 = 4.1547 X 10^{14} chips. With a chipping rate of 10.23 X 10^{6}, this sequence has a period of 266.41 days or 38.058 weeks. However, since the sequence is truncated at the end of the week, each SV uses only one week of the sequence and 38 unique one-week PRN sequences are available. As in the case of C/A-code, the first 32 PRN sequences are reserved for the Space Segment and PRN 33 to 37 are reserved for other uses. The PRN 38 P-code is sometimes used as a test code in P(Y)-code GPS receivers as well as to generate a reference noise level (since, by definition, it cannot correlate with any used SV PRN signals). The unique P-code for each SV is the result of the different delay in the X2 output sequence. The previous table shows this delay in P-code chips for each SV PRN number. The P-code delays (in P-code chips) are identical to their respective PRN numbers for the SVs, but the C/A-code delays (in C/A-code chips) are different from their PRN numbers. The C/A-code delays are typically much longer than their PRN numbers. The replica C/A-codes for a conventional GPS receiver are usually synthesized by programming the tap selections on the G2 shift register. Future generation C/A-code generators may require the use of the variable chip delay (or an equivalent alternative design) if more C/A-codes are added to accommodate geostationary satellites or ground transmitters which transmit differential and integrity information.

The table below shows the polynomials and initial states associated with the two C/A-code generator registers, G1 and G2, and the four P-code registers, X1A, X1B, X2A and X2B. Note that the exponents of the polynomials are identical to the stage numbers of the shift registers which feedback to the input of the input (first stage).

C/A code generator design: polynomials and initial states

Register	Polynomial	Initial State
C/A-code G1	$1 + X^3 + X^{10}$	1111111111
C/A-code G2	$1 + X^2 + X^3 + X^6 + X^8 + X^9 + X^{10}$	1111111111
P-code X1A	$1 + X^6 + X^8 + X^{11} + X^{12}$	001001001000
P-code X1B	$1 + X^1 + X^2 + X^5 + X^8 + X^9 + X^{10} + X^{11} + X^{12}$	010101010100
P-code X2A	$1 + X^1 + X^3 + X^4 + X^5 + X^7 + X^8 + X^9 + X^{10} + X^{11} + X^{12}$	100100100101
P-code X2B	$1 + X^2 + X^3 + X^4 + X^8 + X^9 + X^{12}$	010101010100