# Table of contents

# Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis | (smr 2065)

## Tuesday 17 November 2009

### Laboratory Session. RVI Projects. Digital Signal Processing with FPGA.

### - Adriatico Guest House Informatics Lab. (09:30-10:30)

| time | title | presenter |
|---|---|---|
| 09:30 | Laboratory Session. RVI Projects. Digital Signal Processing with FPGA. | |