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Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis | (smr 2065)

Wednesday 28 October 2009

Digital Design III (more complex elements: RAM, ROM, buses, pipeline concept, etc) - Adriatico Guest House Kastler Lecture Hall (09:30-10:30)

time	title	presenter
09:30	Digital Design III (more complex elements: RAM, ROM, buses, pipeline concept, etc)	P. BAZARGAN-SABET