The Abdus Salam
International Centre for Theoretical Physics

United Nations
Educational, Scientific and
Cultural Organization

IAEA
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**2065-10**

# Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis

***26 October - 20 November, 2009***

## Digital Arithmetic (contd)

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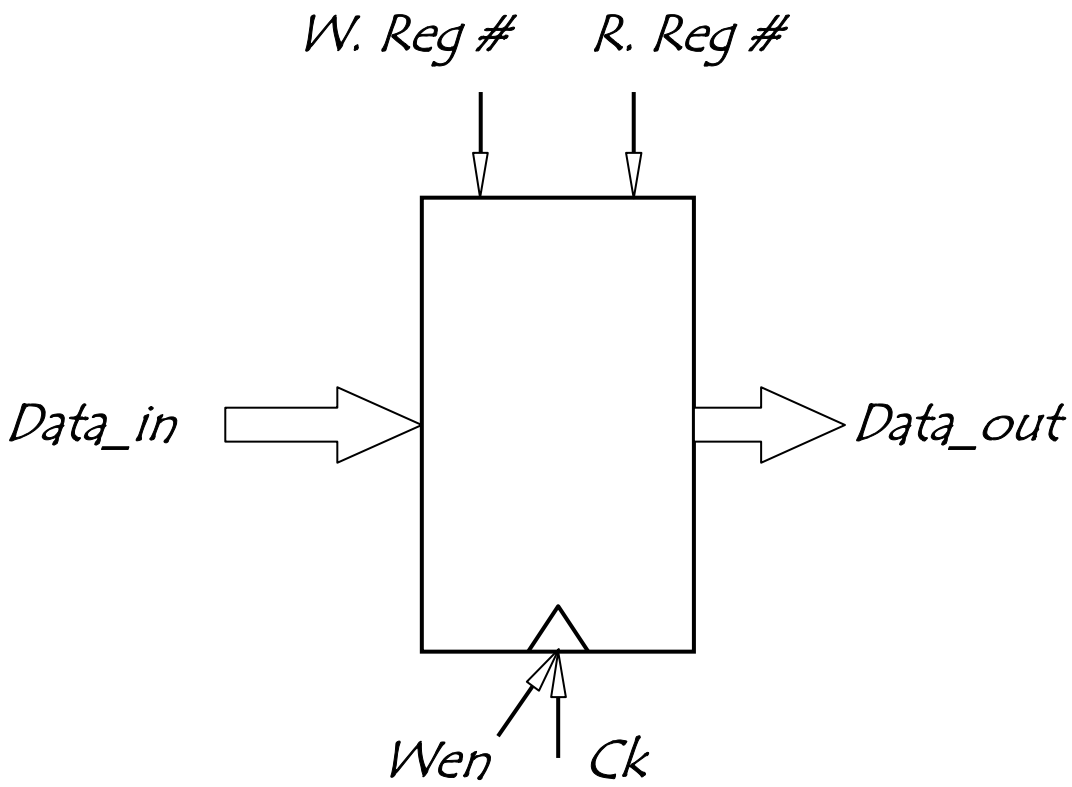
# Outline

- Digital CMOS Design
- Arithmetic Operators
- Sequential Blocs
  - Register Files
  - Fifos

# Register files

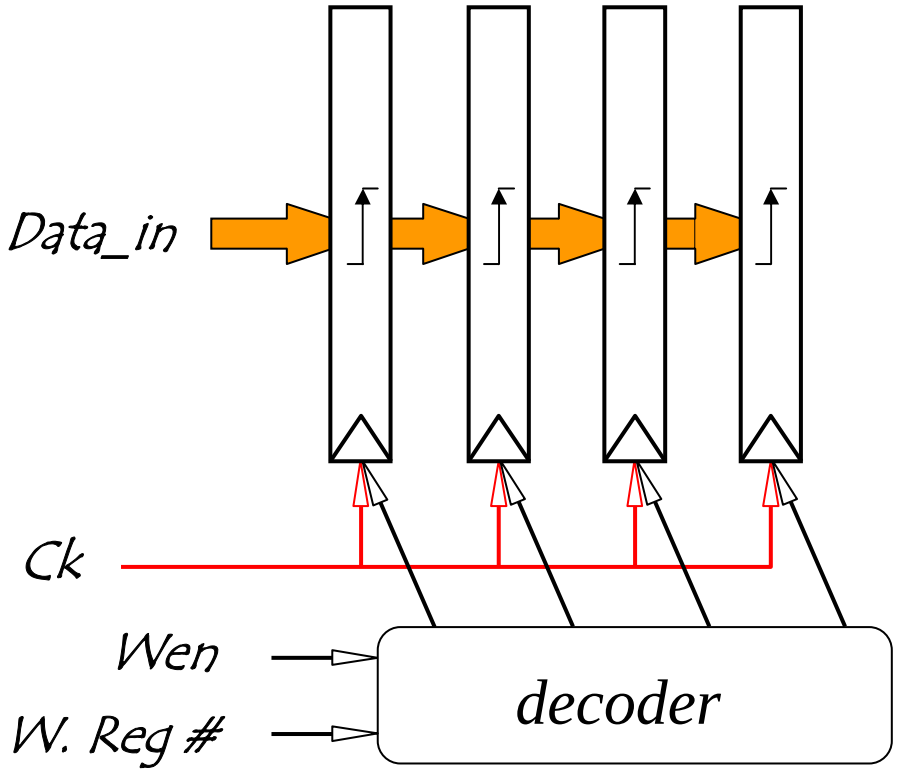
- A set of registers with the same size n-bit
- At each cycle a data can be written into one register
- At each cycle a data can be read from one register

# Register files



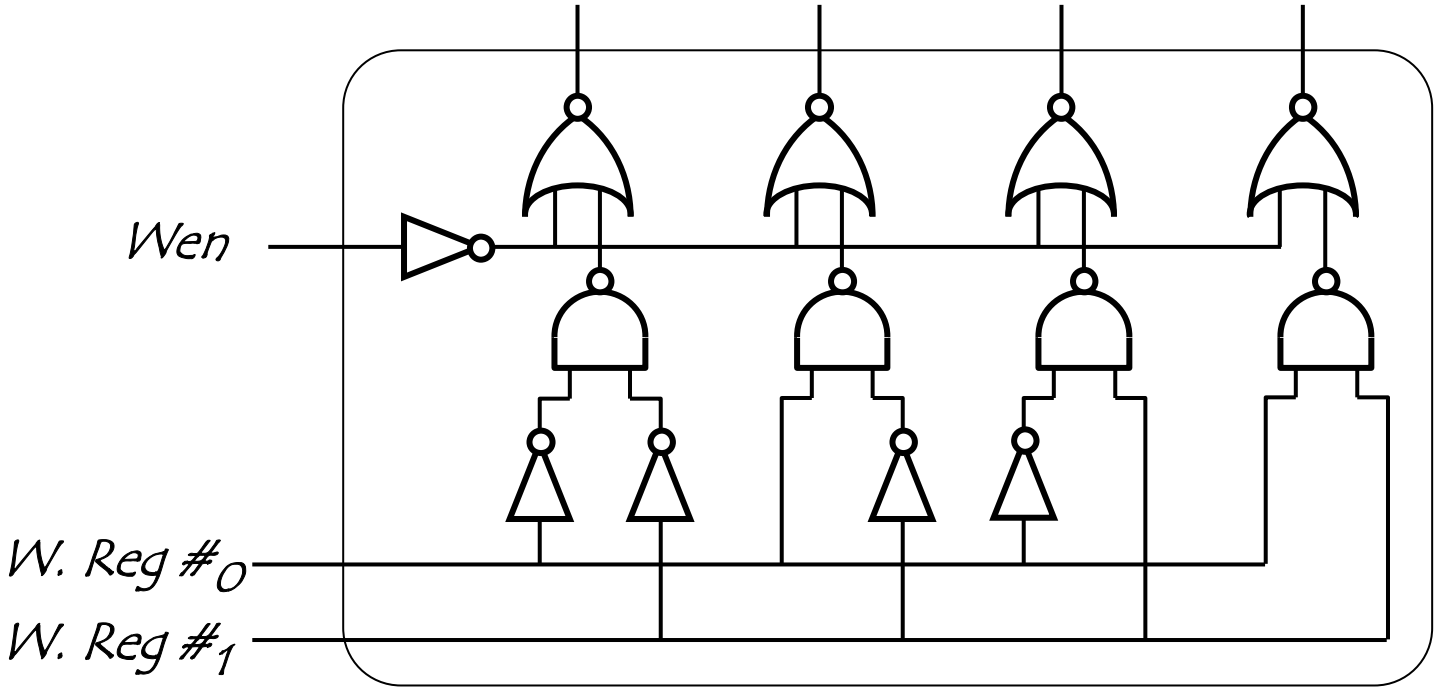
# Register files

## Write function



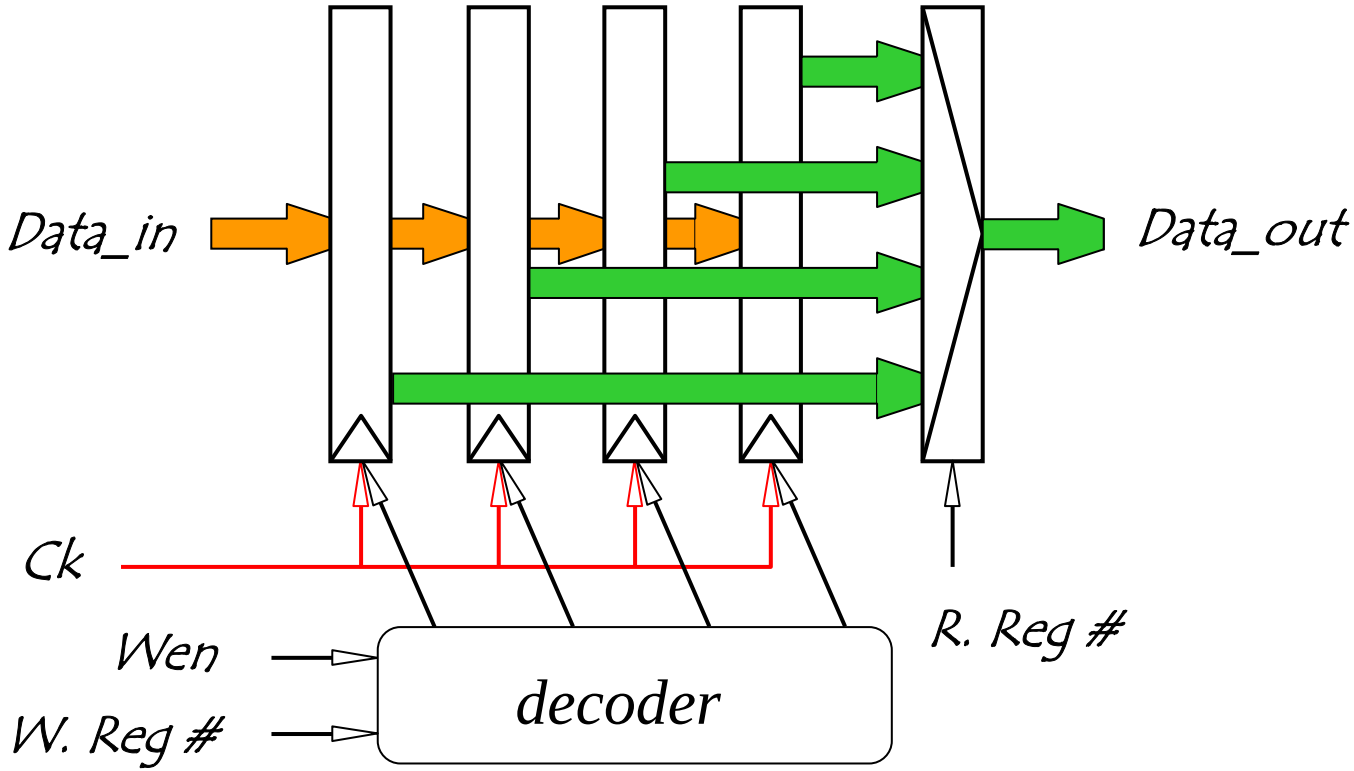
# Register files

## Write function



# Register files

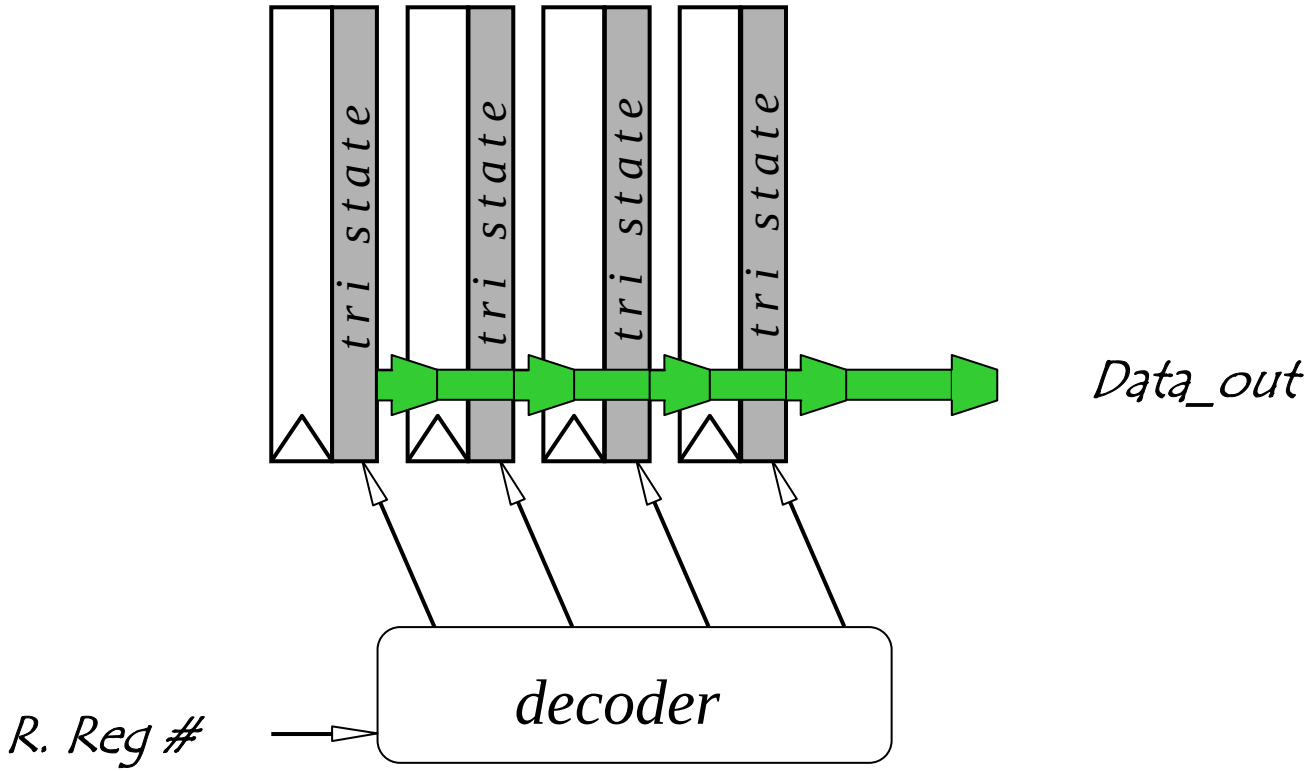
## Read function




## Hardware implementation

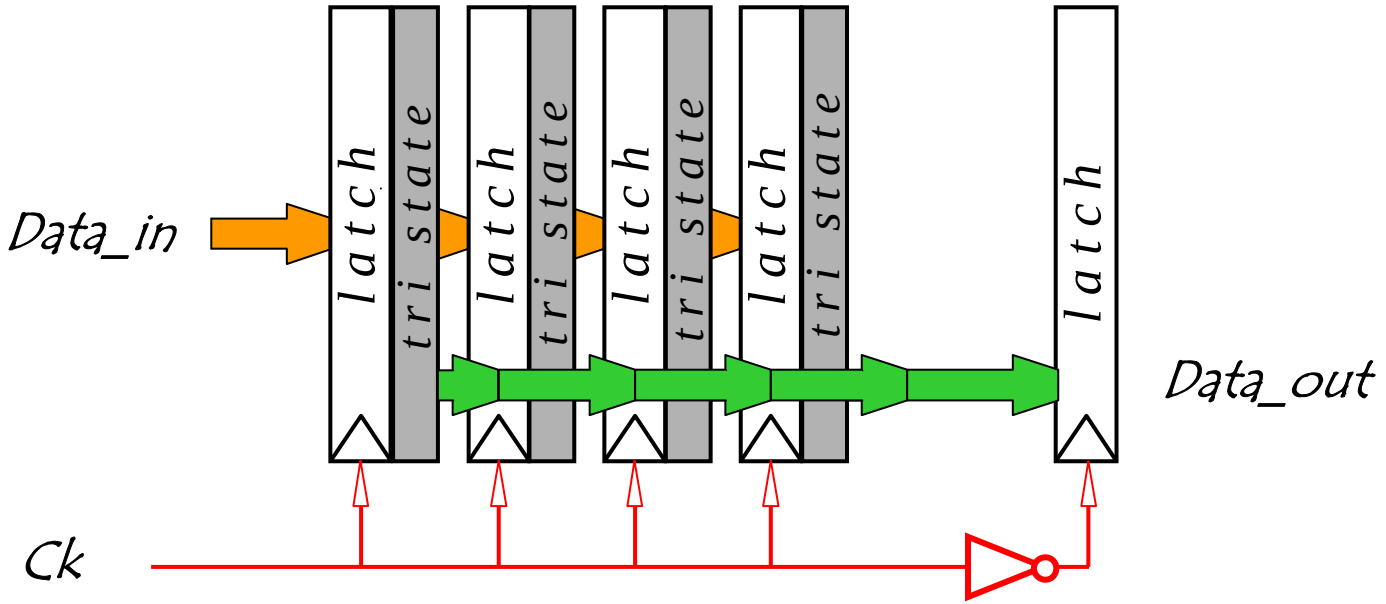
# Register files

## Read function



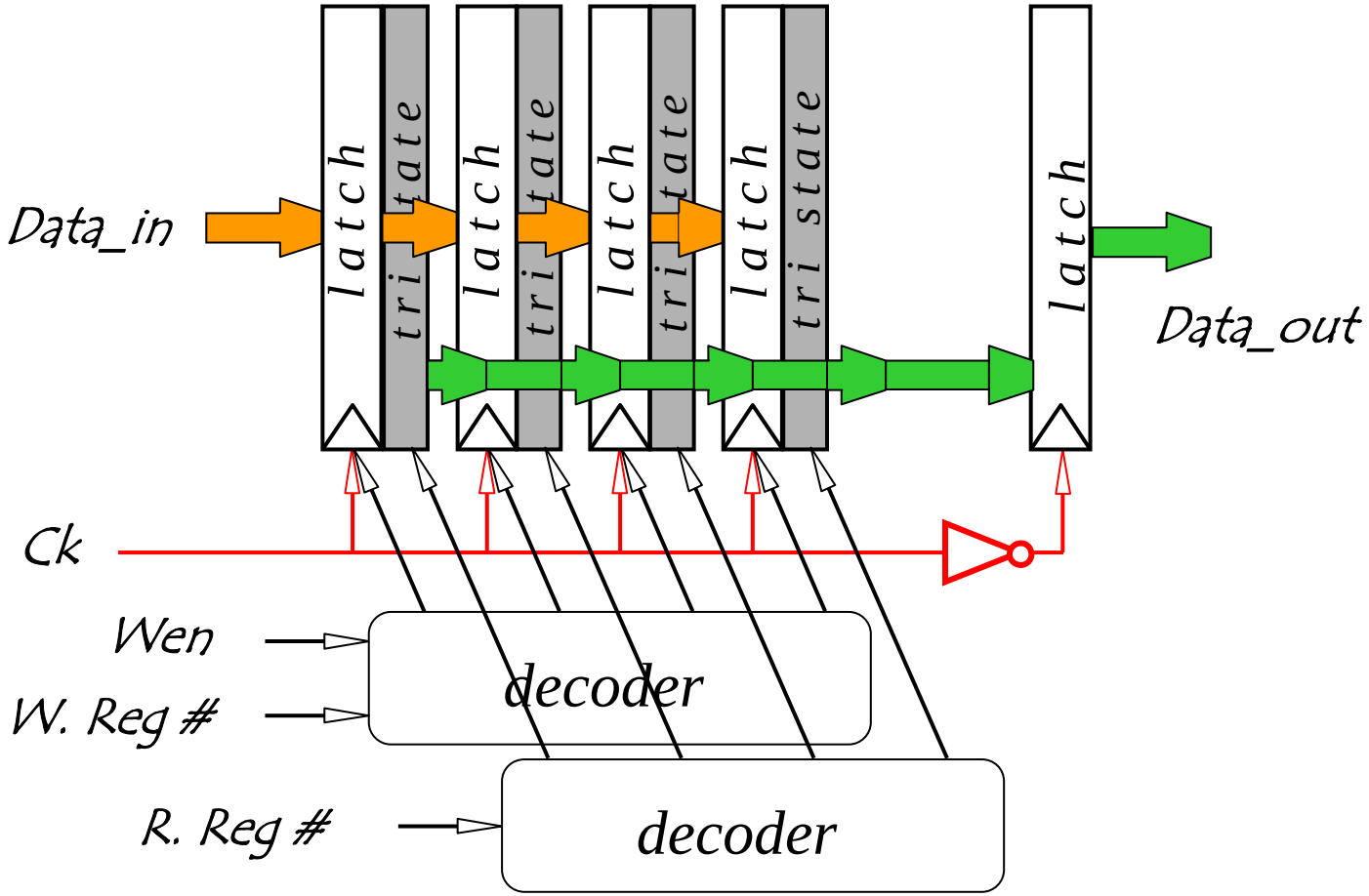
# Register files

There is no move of data inside the register file



# Register files

## Putting all together



# Outline

- Digital CMOS Design
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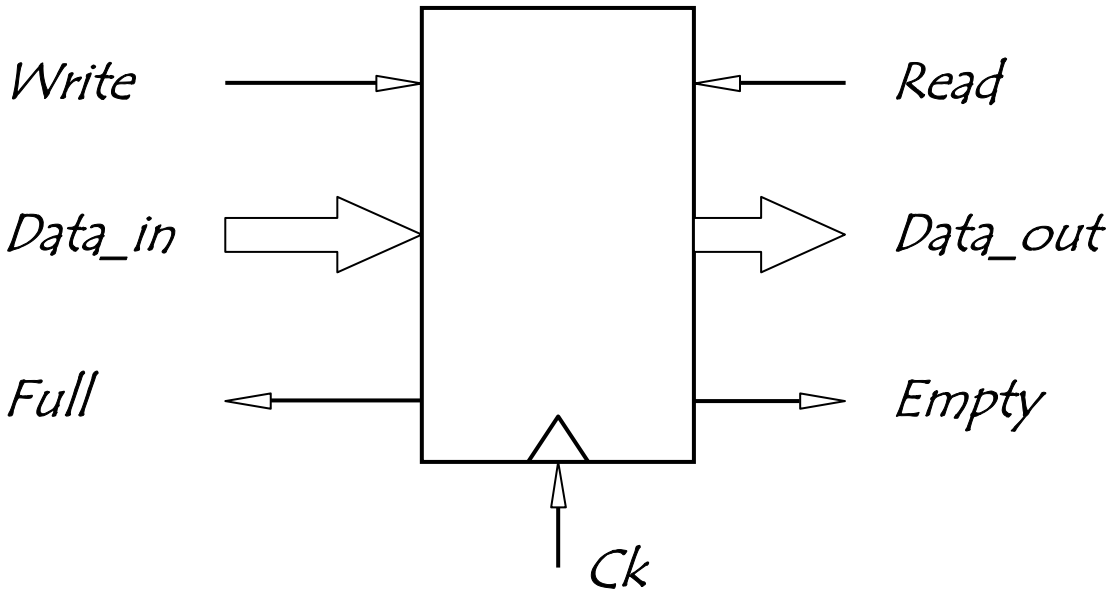
  - Fifos

# FiFos

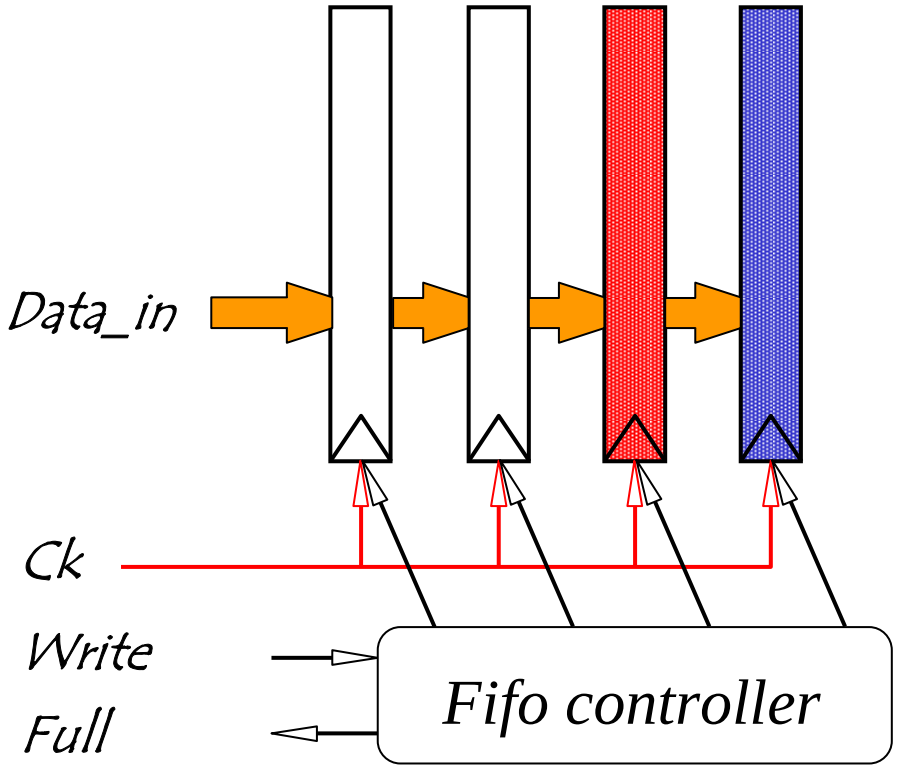
- A set of registers with the same size n-bit
- At each cycle a data can be written into the Fifo
- At each cycle a data can be read from the Fifo
- Data are read in the same order as they are written

# Fifos



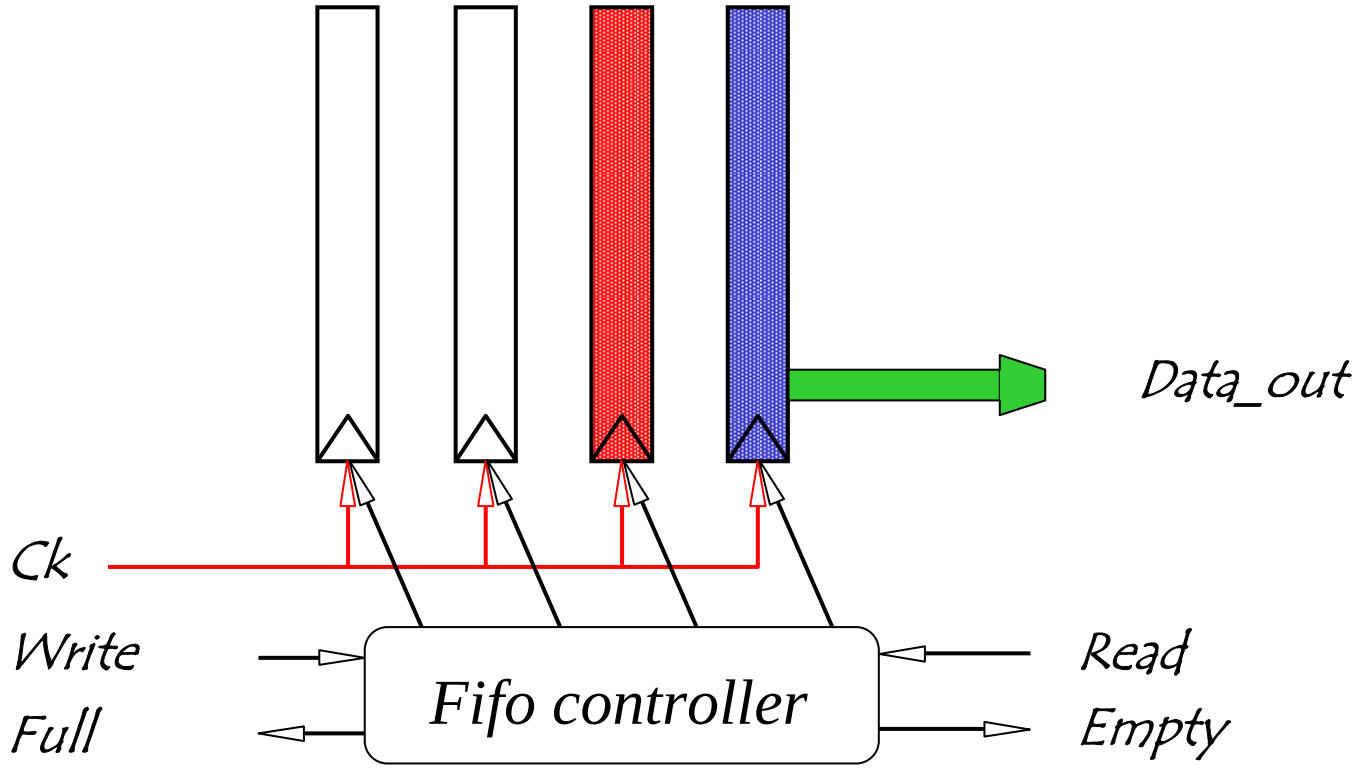
# Fifos

## Write function



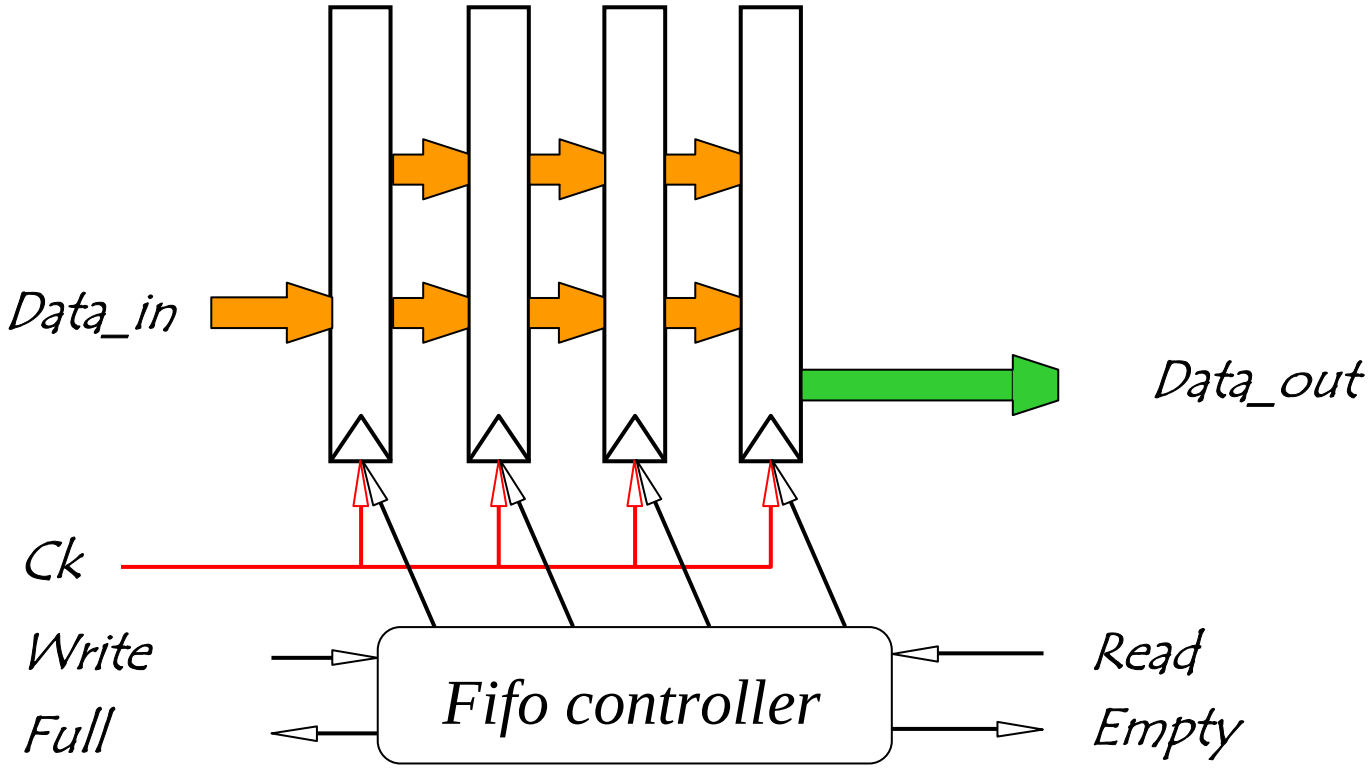
# Fifos

## Read function



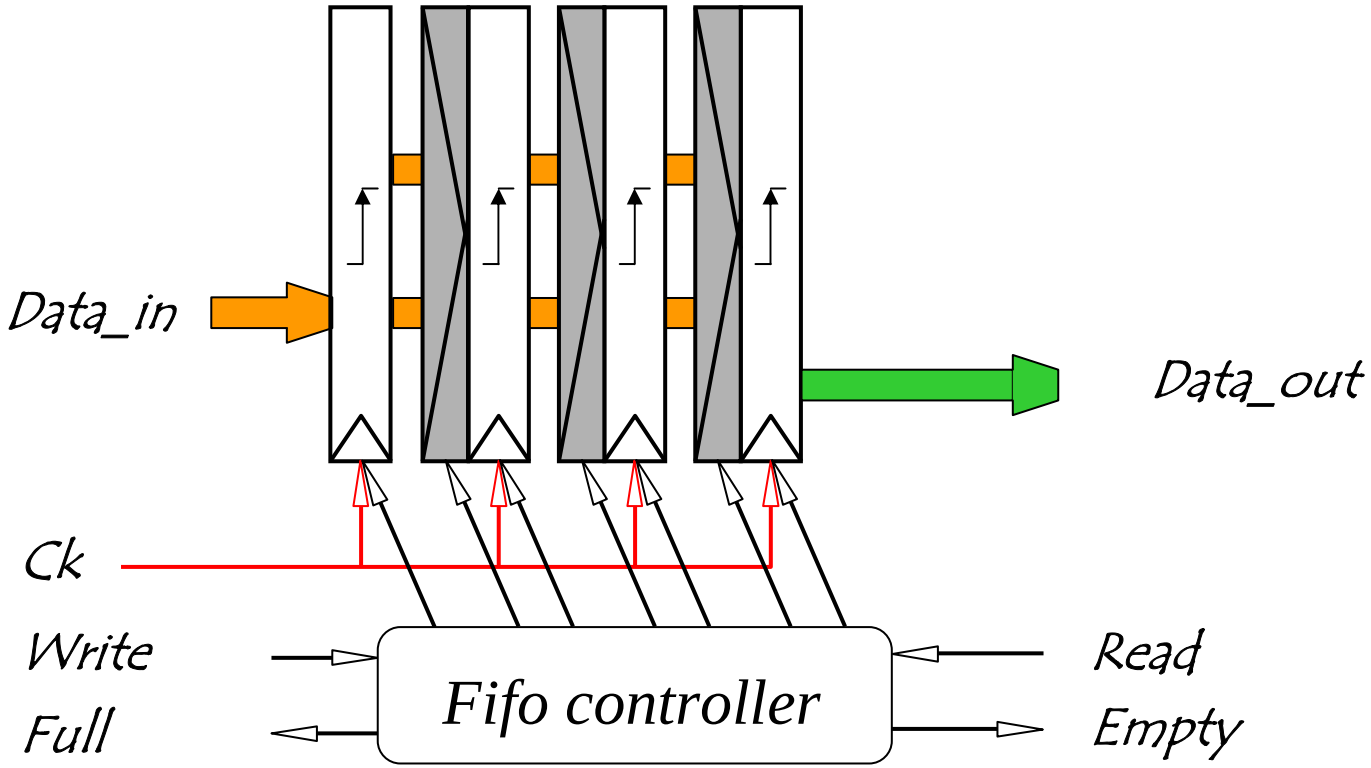
# Fifos

## Read function



# Fifos

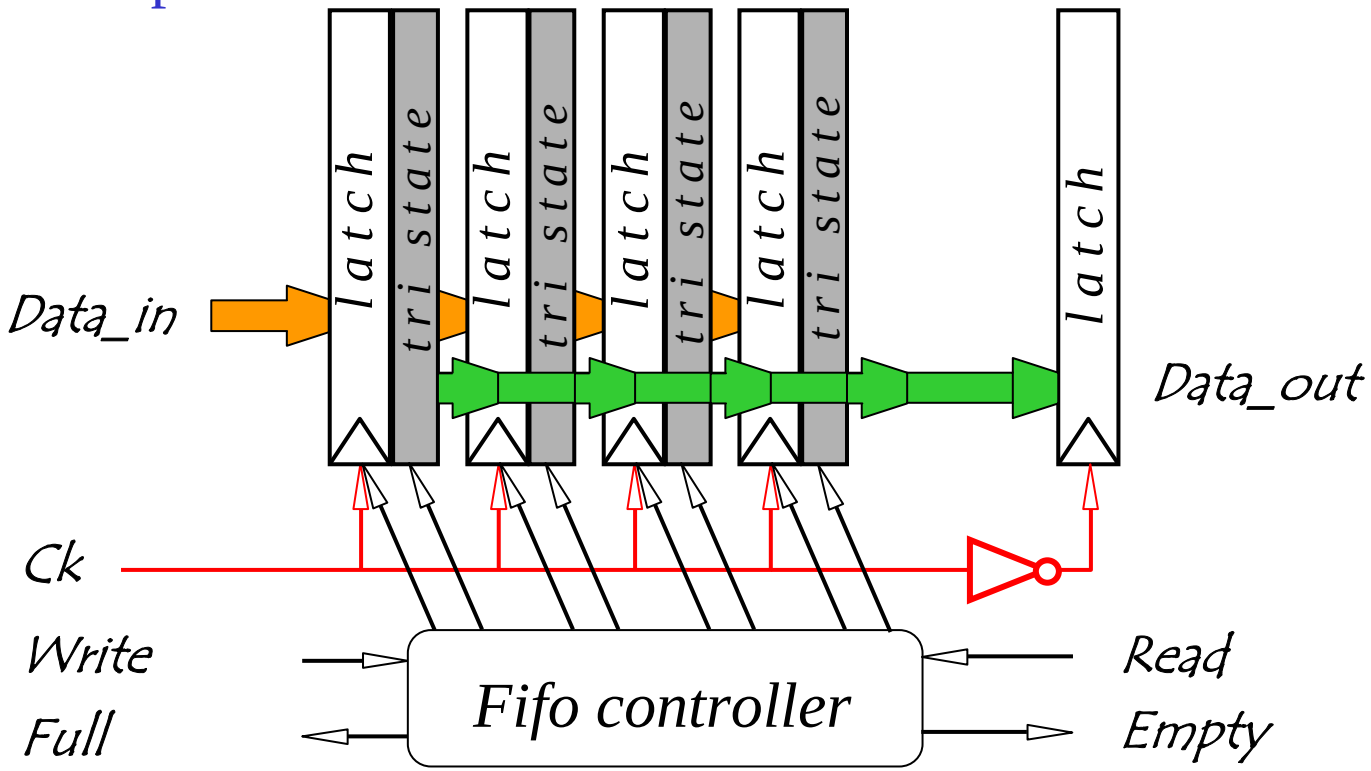
## Read function




Data are moved inside the Fifo

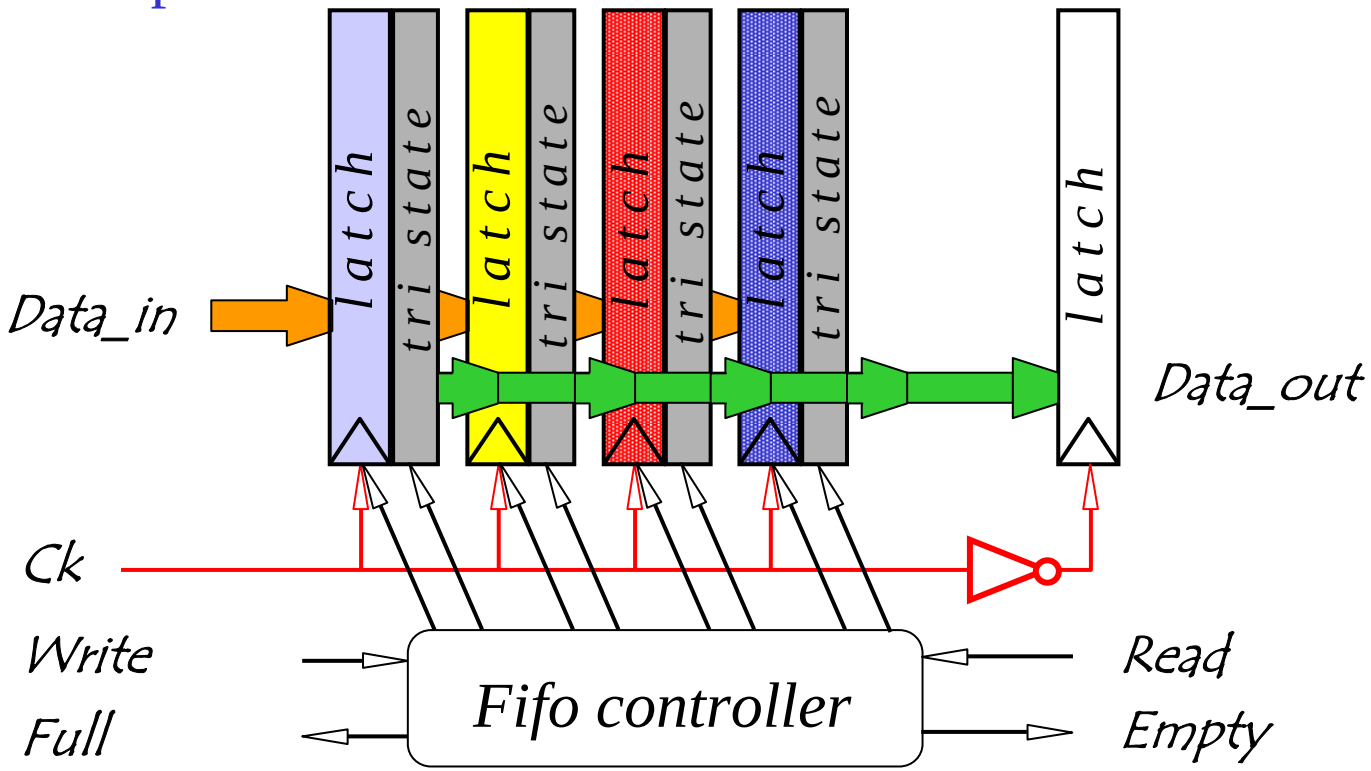
# Fifos

## Improved implementation



# Fifos

## Improved implementation




## Circular Fifo