



2065-4

#### Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis

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Digital CMOS Design (contd.)

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## Outline

- Digital CMOS design
  - ─ Boolean algebra
  - ─ Basic digital CMOS gates
  - Combinational and sequential circuits
    - Coding Representation of numbers



How can I design a digital circuit?

A set of gates (cell library)

combinational gates memory elements



How can I design a digital circuit?

Method to design combinational circuits
 Karnaugh table (local optimization)
 no method for global optimization





How can I design a digital circuit?

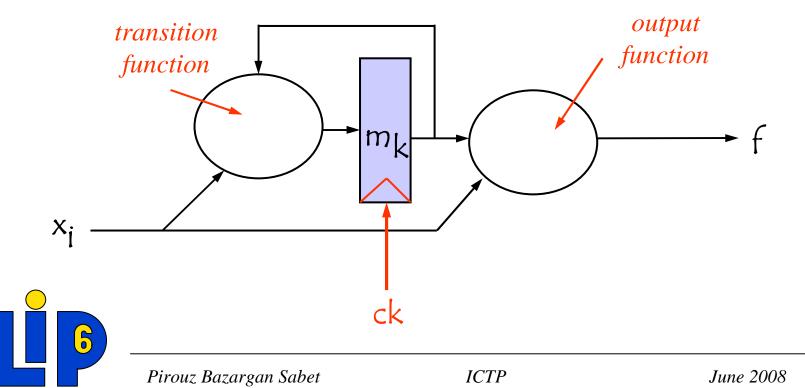
Specify the circuit

Combinational circuit: Boolean functions

Sequential circuit?

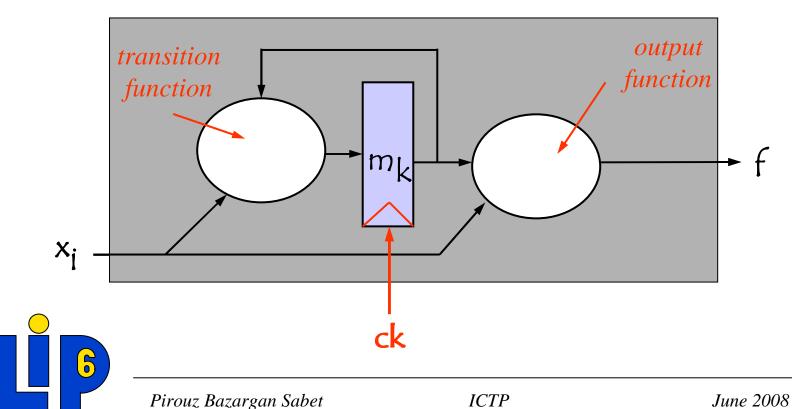


Sequential Circuit



How can I design a sequential circuit?

I need a method to go from a black box to a white box



How can I design a sequential circuit?

The starting point (what I know)

What the circuit is supposed to do

Capture this knowledge into a representation that can be transposed into Boolean functions



The aim

How it will do it

number of required memory elements



Representation of a sequential circuit?

State graph

$$G = (X, Y, S, T,$$

O) X : input variables

Y : output variables

5 : states

T: transitions

O : output set conditions



$$\mathbf{G} = (X, Y, S, T,$$

O)

T : set of transitions

$$t \in T$$
,  $t = (s, s', f)$ 

 $s \in S$  : source state

 $s' \in S$ : target state

 $f \in \mathbf{B}_n$ : transition condition



$$\mathbf{G} = (X, Y, S, T,$$

O)

O: output set conditions

$$o \in O$$
,  $o = (y, s, c)$ 

 $y \in Y$  : output variable

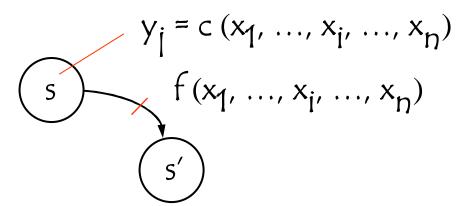
 $s \in S$  : state

 $c \in \mathbf{B}_n$ : output set condition



• Let consider a graph  $\mathbf{G} = (X, Y, S, T, O)$ 

Graphic representation of **G** 





Representation of a sequential circuit?

State graph

Transpose into a graphic representation the expected behavior of a sequential system

$$G = (X, Y, SS, TT, O)$$





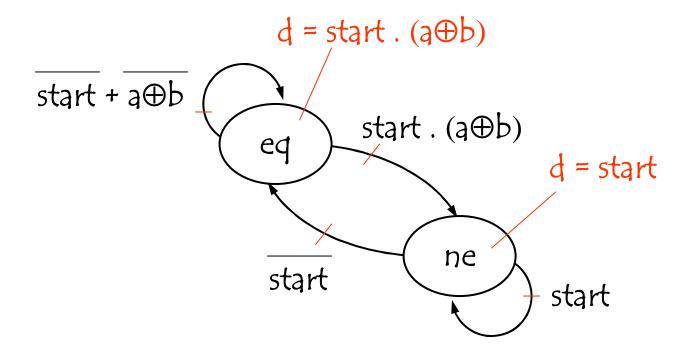
Two signals a, b each transmitting a series of bits (1 bit at a cycle)

Design a system that sets a flag d if the value transmitted by a is different than b





# Example





Representation of a sequential circuit?

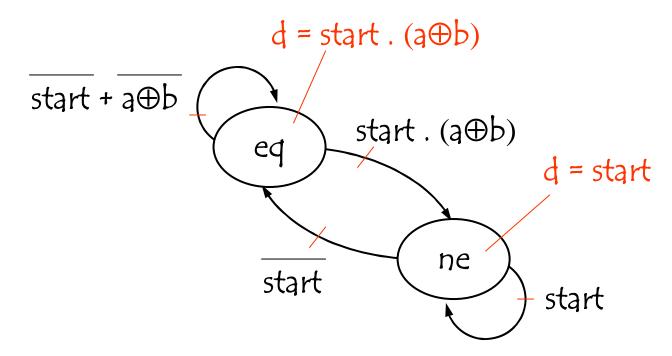
State graph

$$G = (X, Y, SS, TT, O)$$

define the number of memory elements required to represent S : M



# Example





2 states  $\longrightarrow$  1 memory element

Representation of a sequential circuit?

State graph

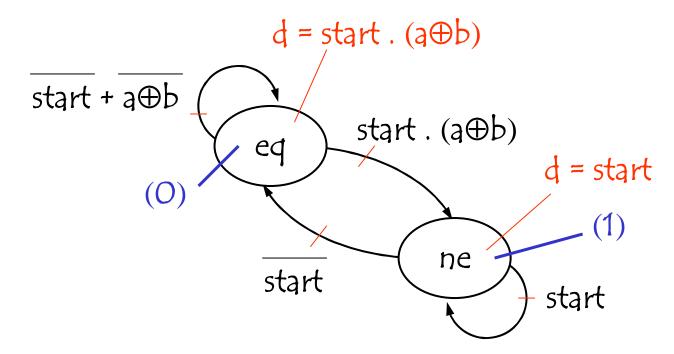
$$G = (X, Y, S, T,$$

define the number of memory elements required to represent S : M

represent each state s by a vector of M



# Example





2 states  $\longrightarrow$  1 memory element

Representation of a sequential circuit?

State graph

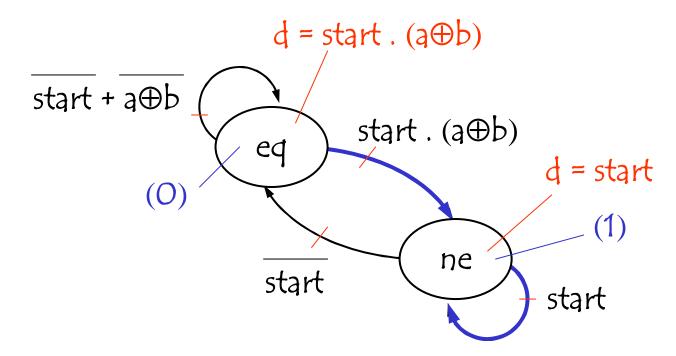
$$G = (X, Y, S, T,$$

define the transition function: mk

 $m_k$  = sum of the Boolean function of the transitions that have as target a state where  $m_k$ =1



# Example





 $m_1 = \overline{m_1}$ .start.(a $\oplus$ b) +  $m_1$ .start

Representation of a sequential circuit?

State graph

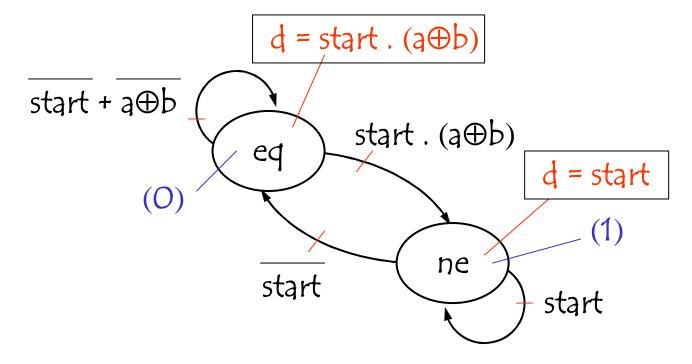
$$G = (X, Y, S, T,$$

define the output function : y<sub>j</sub>

 $y_i = \text{sum of the output conditions concerning } y_i$ 



# Example





$$d = \overline{m_1}.start.(a \oplus b) + m_1.start$$

Representation of a sequential circuit?

State graph

$$G = (X, Y, S, T,$$

implement the Boolean functions:  $m_k$ ,  $y_j$ 

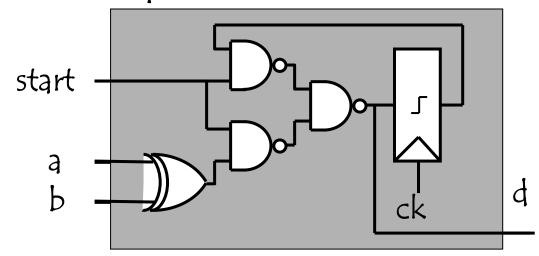


## Example

$$m_1 = \overline{m_1}$$
.start.(a $\oplus$ b) +  $m_1$ .start

$$d = \overline{m_1}.start.(a \oplus b) + m_1.start$$

$$m_1 = \text{start.}(a \oplus b) + \text{start.}m_1$$





How can I design a sequential circuit (summary)?

$$\mathbf{G} = (X, Y, S, T, S,$$

- O) graphic representation the behavior
  - define the number of memory elements required to represent S: M
  - represent each state by a vector of M
  - define the *transition function*
  - define the *output function*



