Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis

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FPGA Applications in High Energy Physics

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FPGA applications in High Energy Physics

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Outline

CERN – electronics system concepts
a project cycle

Application: Data selection

Application: Data processing
CERN
Application overview CERN

CERN, experiments
Aim
General detector concept
Examples

Principle of data acquisition & data flow

data selection: trigger
data processing
Experiments
Principle of detectors

- tracking
- precision position
- calorimetry
- (missing) energy
- muon chamber
- position and momentum
- time of flight
- particle identification
100 million sensors
22 m diameter
position resolution: > 10 µm
4T magnet field
Detector: ALICE
Principle of Data acquisition
Data selection

Collision → Particle

40 MHz → Detector electronics → L1 Trigger

100 kHz → Zero suppression & event builder → L2 Trigger

100 Hz → Data storage

100 Tbyte/s

100 Gbyte/s

100 Mbyte/s
Data selection

Process probability \(10^{-11}\)

**Diagram:**

- **Detector**
  - Particle Identification + Location (40 MHz)
  - Track Reconstruction + Process Indication (100 kHz)

**Flowchart:**

1. **Detector**
   - Pipeline Memory
   - Level 1 Trigger
   - Yes/No + Location of properties of interesting events

2. **Level 2 Trigger**
   - Yes/No
   - Flow to **Level 1 Trigger**

- **Data Flow:**
  - 10..100 Hz
Principle of data acquisition

Data selection: trigger - FPGA

Front end: data taking-ASICs

Read out electronics-FPGA
Trigger processor
Challenge/Specifications

- **Fast**
  - the faster, the less data needs to be pipelined/stored

- **Compact**
  - Many data channels are going into one processor system

- **Connectivity**
  - High number
  - Transmission delay on cables (5ns/m -> 200 m -> 1µs)

- **Reliability**
  - Physics processes with a probability of $10^{-11}$ need to be recorded
  - Processing and data transmission error rate $>> 10^{-11}$
**Challenge/Specifications**

- **Quality control**
  - Processes are verified in hardware and software processors

- **Radioactive environment**

- **Data volume/rate**
  - Many (100,000) parallel inputs in 25 ns interval

- **Parallel processing – pipelined processing**
  - FPGA
  - Highly parallel because of many IOs and interconnectability
Example: Tracal Trigger

- Specifications
  - Calculate how many out of 1000 binary sensor inputs are active
  - Each 25 ns a new set of 1000 bits
  - Result required within 100 ns

- Solution possibilities
- Today and 10 years ago
Challenge/Specifications

System topology

• high number of inputs ->
  – operation to simplify data and reduce data amount

• reduced number of inputs ->
  – connected to more complex processing units

• at the end of processing chain ->
  – interest to integrate as much information into 1 FPGA to reduce interconnection
Challenge/Specifications

System topology: Interconnection:

- delay
  - (clock to pin, transmission outside FPGA, setup time)
Challenge/Specifications

System topology: Interconnection:

- Parallel interconnection:
  - high number of IOs, problem moved to board level
  - reliability impact due to solder joints or connectors
Challenge/Specifications

System topology: Interconnection:

- Serial interconnections at high speed
  - reduce reliability impact and increases delay
    (trigger needs to be fast)
**Challenge/Specifications**

**System topology: Interconnection:**

- **delay**
  - (clock to pin, transmission outside FPGA, setup time)

- **Parallel interconnection:**
  - high number of IOs, problem moved to board level
  - reliability impact due to solder joints or connectors

- **Serial interconnections at high speed**
  - reduce reliability impact but increase delay (trigger needs to be fast)

- **Interest to keep as much as possible within the same FPGA**
Muon Track Finder
Trigger Processor
Muon track finder trigger
Principle of data acquisition

trigger detector

collision 40 MHz

precision detector

central trigger

DAQ

Sensor-elektronics

readout-elektronics

100 m = 0.5 µs

10^-11

100 m = 0.5 µs

10^-11

100 m = 0.5 µs

100 m = 0.5 µs

Particle
## Muon track finder trigger

- **Size of detector system**
  - \( r = 14 \text{ m}, \text{ length} = 20 \text{ m} \)
  - cable delay \( \sim 5 \text{ ns/m} \) -> synchronisation

- **Each 25 ns new data set**

- **240 detector modules – 200,000 detector cells**

- **Identify particles (muons)**

- **Measure curvature = momentum of particles within 400 ns**

- **Find 4 particles with highest momentum**
Muon track finder trigger
200.000 sensors ->

240 chambers x 2 track segments = 480 track segments

1 track segment
  position (phi): 12 bits
  angle (phi_b): 10 bits
  quality code: 3 bits

25 bits * 480 track segment = 12000 bits
12000 bits * 40 MHz = 480 Gbit/s
Muon track finder trigger

How?
Muon track finder trigger
Muon track finder trigger

- Track segment in $\eta \phi$ plane
- Position of the track segment and angle
- Track projected in $\eta \phi$ plane
- Interaction point

Muon stations 1 to 4
Muon track finder

trigger

2 * extrapolation threshold

track segment

muon station 4

muon station 3

muon station 2

muon station 1

$\phi_2 - \phi_1$
Muon track finder trigger

- **Muon station 4**
- **Muon station 3**
- **Muon station 2**
- **Muon station 1**

2 \* extrapolation threshold

\[ \sum \text{blue} = N_{\text{bin}} \]
\[ \sum \text{red} = N_{\text{binmin}} \]

\(k\) reference cells
Muon track finder trigger

\[ \phi_{\text{source}} + \phi_{\text{qual_{source}}} \]

\[ \phi_{\text{b,source}} \]

\[ 12 \times \phi_{\text{target}} + \phi_{\text{qual_{target}}} \]

extrapolation quality (eq1)

extrapolation result (er1)

er2, eq2

er3, eq3

er11, eq11

er12, eq12

\[ \phi_{\text{C1..C comparator}} \]

\[ \phi_{\text{C11}} \]

\[ \phi_{\text{C12}} \]
Muon track finder trigger

Pairwise Matching - Extrapolation

Track Assembler

Pt-assignment

extrapolation window

track segment

muon station 2

μ2 - μ1

μ4 - μ3

track found
(TS1, TS2, TS3, TS4)

extrapolation result *1/0*

pt

TS1, TS2, TS3, TS4
Result of all extrapolation units is 180 bits

\[\rightarrow\text{ data reduction}\]

Track assembly unit is combinatorial and looks for the longest possible track combination
Muon track finder trigger

Parameter assignment unit: momentum (5 bits) based on difference in position of layer 1 and 2.
Muon track finder trigger
Muon track finder trigger
Muon track finder trigger

Extrapolation units:
EP20k400EFC672
Data pipeline: 3 x
EP1k100FC484
Track segment linker:
EP20k300

16 layer PCB
no pin level back annotation
no board level simulation
Soldering problems with ball grid
Muon track finder trigger
Muon track finder trigger

All in EP1S40F1020C7

8 layer PCB
pin level back annotation
board level VHDL simulation
full JTAG boundary scan
FPGA on daughter card
Muon track finder trigger

• Conclusion track finder:
  • Data reduction
  • Pipelining
  • Feasibility study on possible algorithms
  • Back annotation of Pins in FPGA after routing
  • Full board – multiple FPGA VHDL simulation
  • Stimulus files from (costumer) simulation
  • Planning at FPGA level has impact on system implementation
Example FPGA processors
Processor board with optical inputs

- 12 channels
  - Parallel optical receiver module
  - 12 closely packed G-link deserializer ASICs

Virtex 4 LX 60
Agilent HDMP-1034
Zarlink POFM
Connectors

84 mm
160 mm
Trigger system crate
Design cycle
Design cycle

- **System – Specifications**

- **Different approaches - possibilities**
  - ASICs, CAM -> FPGA
  - Pattern recognition / Analytical approach => Mixture => successive data reduction

- **Simulation - Feasibility - Forecast to future technologies**

- **Data flow simulation/calculation**
  - buffer sizes
  - dead times
Design cycle

- Implementation scheme – propose technology independent architecture
  - Do not push problems to a higher level - IO pins, PCB, system

- Technology independent Simulation
  - Full system: system input patterns – Qualification of data process
  - implement/integrate into system surrounding - work on FPGA code
  - Simulation together with environment
    - other FPGAs
    - input data
### Design cycle

<table>
<thead>
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<th>Step</th>
<th>Details</th>
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<td>Implementation - technology dependent</td>
<td>-</td>
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| Selection of components       | - Performance, features, evaluation, availability  
|                               | - Price, age/phase in product cycle,   
|                               |   - If very new -> support and access to high quantity difficult  
|                               |   - Close connection to distributor   |
| Define strategy on Maintenance and upgrades | - FPGA might get too full & slow after implementation of more and more functions  
|                               | - FPGA might get too old/obsolete during product cycle  |
**Design cycle**

- **FPGA simulation/synthesis/place&route/back-annotation**
- **Board Placing/routing**
  - FPGA -> board -> FPGA
  - FPGA Back annotation/Board level of pin position-Feedback on board layout
- **behavioral simulation of HDL code**
  - back annotated gate level after routing with board/system level
  - SEU simulation
Design cycle

- Problems which are not solved on component level (ASIC/FPGA)
  - are pushed to the system level, become expensive and time consuming

- System level considerations ->
  - System level simulation
  - Multi designer environment
  - Multi component environment
Example design

- Prototype no internal design constraints on pin assignment for board layout -> 16 layer board ->
  - with assignment clean and 8 layer board

- Missing board level simulation with two FPGAs
  - simulation of each FPGA is OK
together setup and hold time violations
board delay

- Evolution of FPGA technology:
  - more than 1 FPGA with board routing ->
  - 1 FPGA no board routing
Design cycle

- Software/Hardware development must go hand in hand

- Debugging features in FPGAs/system/history/status

- Remote control is often required
  - how to implement
  - always one FPGA not reprogrammable as communication processor
Design cycle

- Board production
  - JTAG boundary scan is mandatory for BGA
    - Full system JTAG especially with multiple FPGAs on board
    - reduces turn around time
    - gives proof of problems to manufacturer
    - X-ray tests are not always conclusive (example not even copper on pads)
  - Soldering problems with prototype series
  - Test points
Design cycle

• Define strategy on Reliability
  – which date may be corrupted and which data must not be corrupted
  – radiation, SEU, cosmic rays on ground level
  – sub micron ASICs/FPGA