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International Centre for Theoretical Physics**



2065-31

**Advanced Training Course on FPGA Design and VHDL for Hardware
Simulation and Synthesis**

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**Fast Time Tagging Silicon Pixel Tracker
The NA6₂ Gigatracker**

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Fast time tagging silicon pixel tracker, The NA62 Gigatracker

presented by A. Kluge
CERN/PH-ESE
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Outline

- Introduction
 - applications for time tagging
- NA62, introduction, challenge
- GigaTracker
 - specifications, module, beam/data rate, cooling
 - architecture
 - demonstrator ASICs
- Summary



Introduction



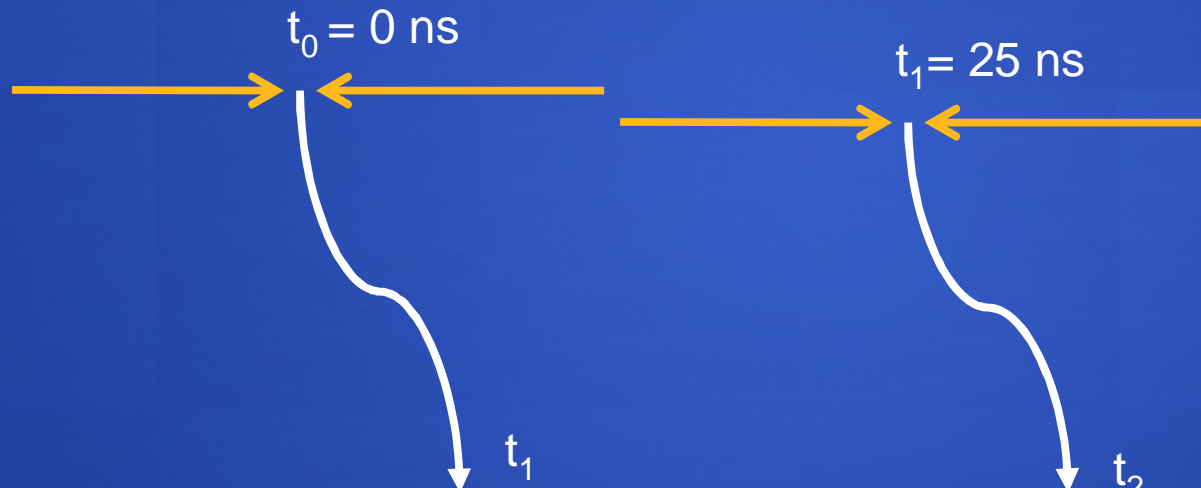
Why measure time?

- time-of-flight detectors:
- Particle identification, $t = f(m, p)$
(example ALICE TOF)
 - position resolution: centimeters
 - timing resolution: < 100 ps
 - based on resistive plate chambers (M)RPCs
 - high material budget, large elements
- measurement of asynchronous event



Why measure time?

- separation of particles belonging to different events

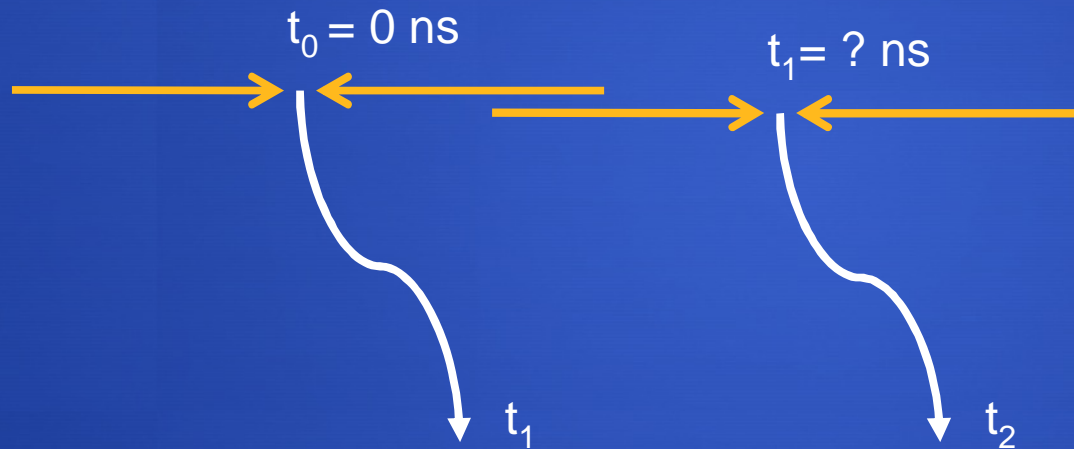


- from that point of view the LHC trackers are time tagging detectors with a time resolution of 25 ns, as they assign each hit to a bunch crossing
- Time tagging in synchronous system



Why measure time?

- separation of particles belonging to different events

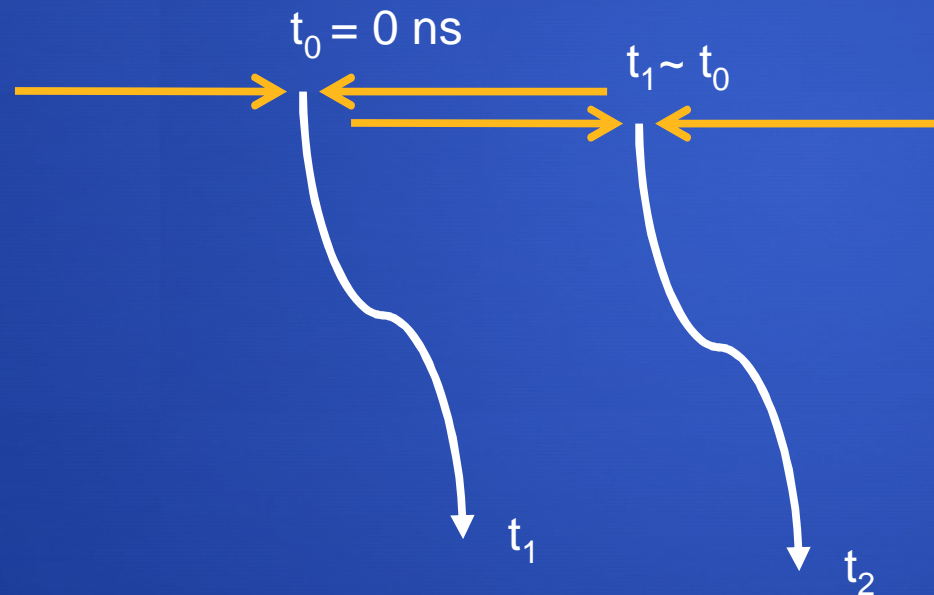


- Fixed target experiment: asynchronous arrival time
- Triggerless or late trigger & high particle rate:
 - high read-out data rate: hits time tagged



Why measure time?

- separating overlapping events

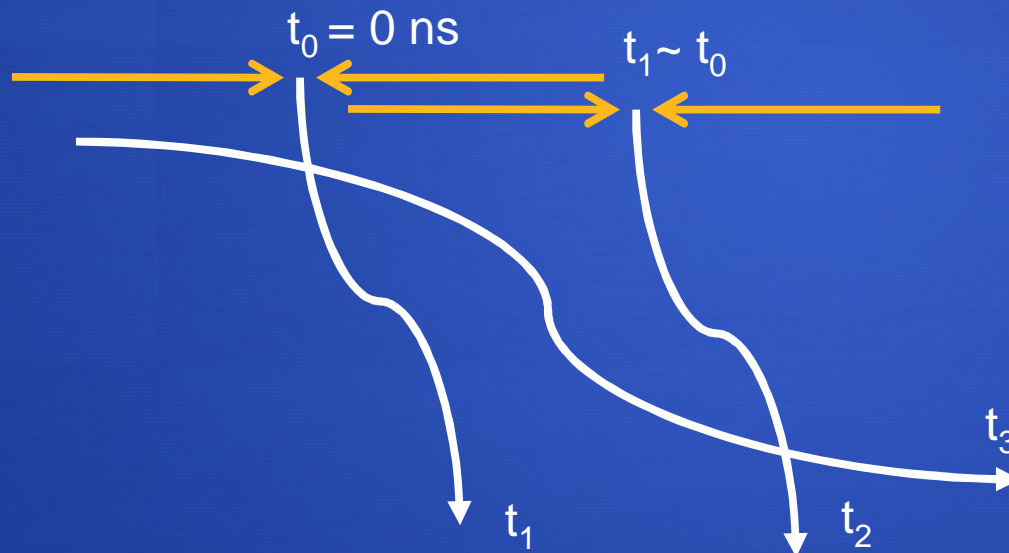


- Linear collider CLIC: bunch spacing 0.5 ns



Why measure time?

- suppressing particles not belonging to collision (noise, back ground suppression)



- CLIC: high back ground from machine
- LHC: beam gas suppression



Why measure time?

- **Overlapping in time**
 - Linear collider, CLIC
- **Asynchronous arrival time**
 - Fixed target experiments, TOF
- **Timepix**
 - TPC read-out



NA62 - Introduction



10⁻¹³



Experimental setup- NA62

hit correlation via matching of arrival times – 100 ps

selects particles with 75 GeV/c

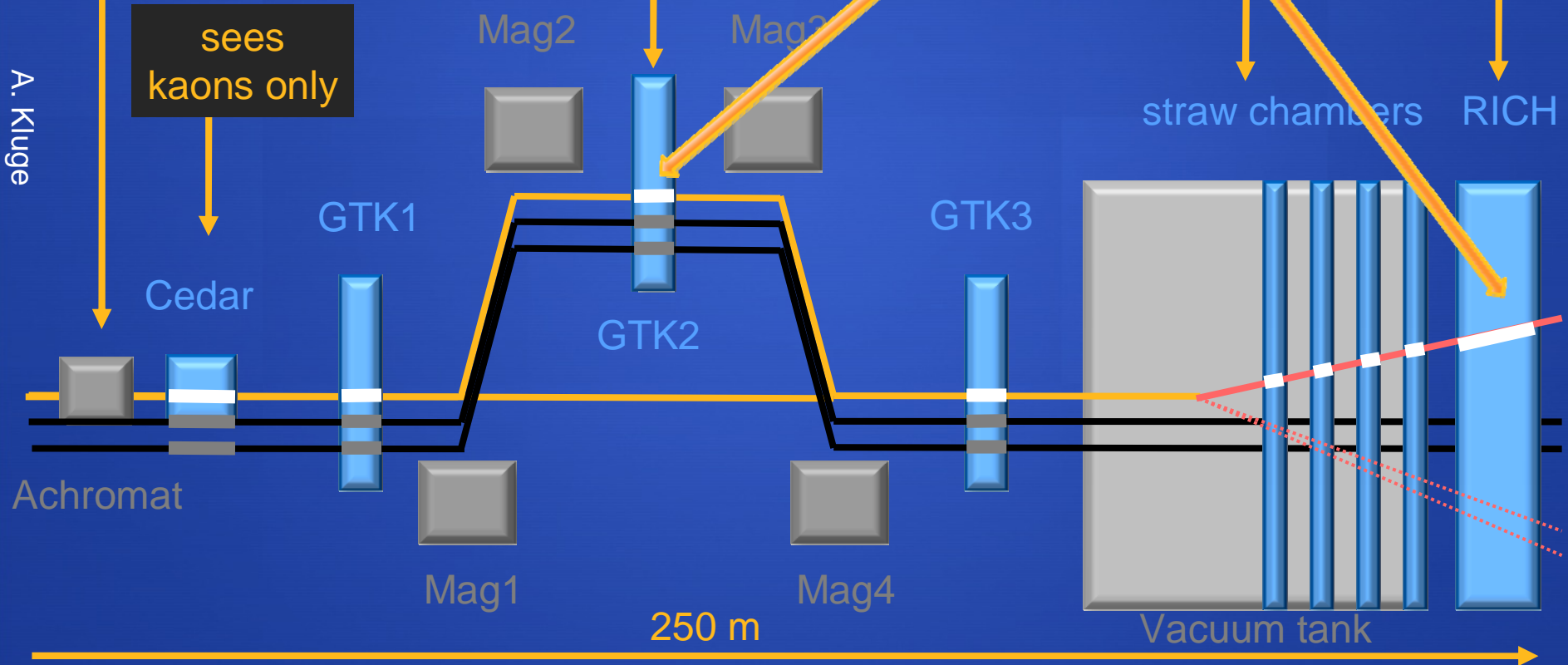
sees kaons only

GTK sees all particles

straw chambers measure position

RICH identifies pions

A. Kluge



beam: hadrons, only 6% kaons -> only 20% decay in the vacuum tank into a pion and 2 neutrinos -> out of which only 10^{-11} decays are of interest

A. Kluge

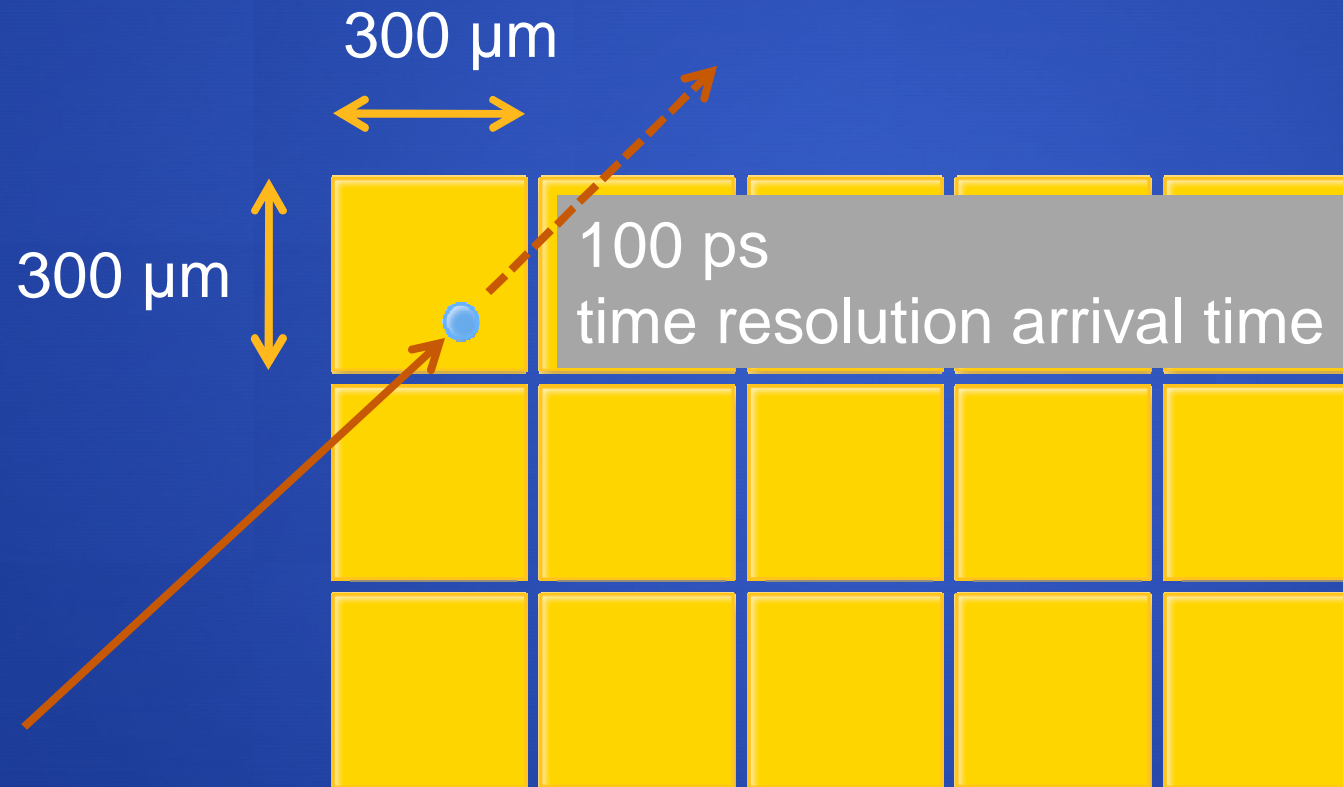


Experimental setup- NA62

beam: hadrons, only 6% kaons ->	0.06
only 20% decay in the vacuum tank into a pion and 2 neutrinos ->	0.20
out of which only 10^{-11} decays are of interest ->	10^{-11}
<hr/>	
total probability	1.2×10^{-13}



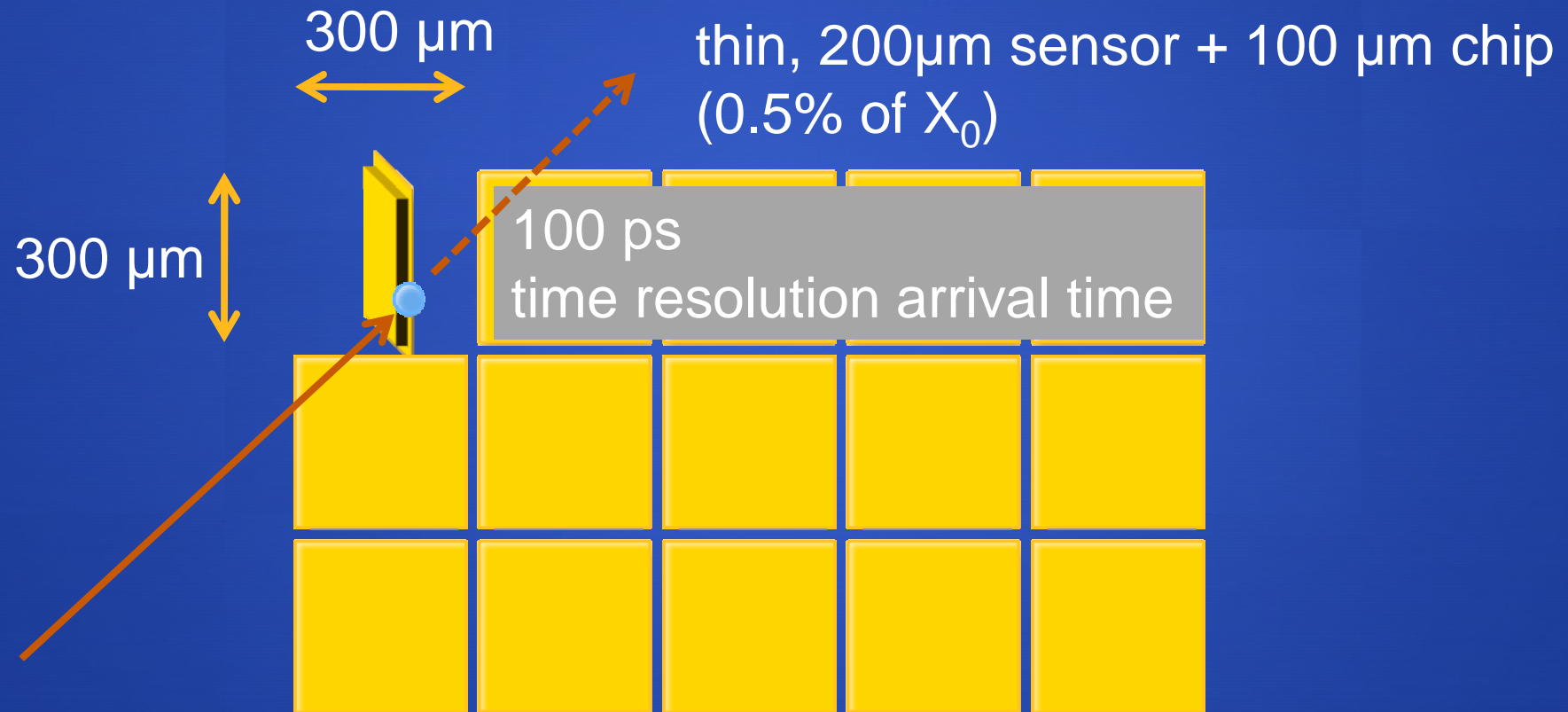
Experimental setup: GTK specifications



800 MHz particle rate



Experimental setup: GTK specifications



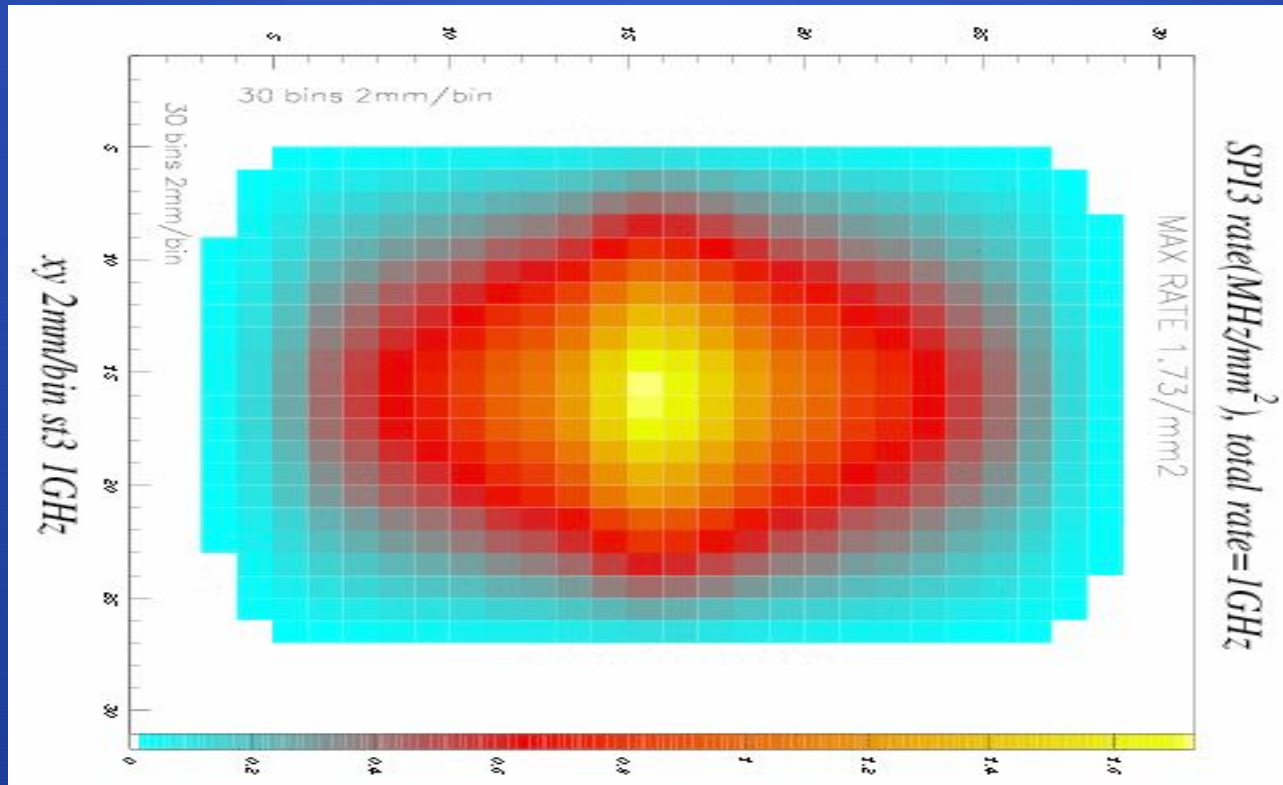


Beam & detector configuration



Beam profile

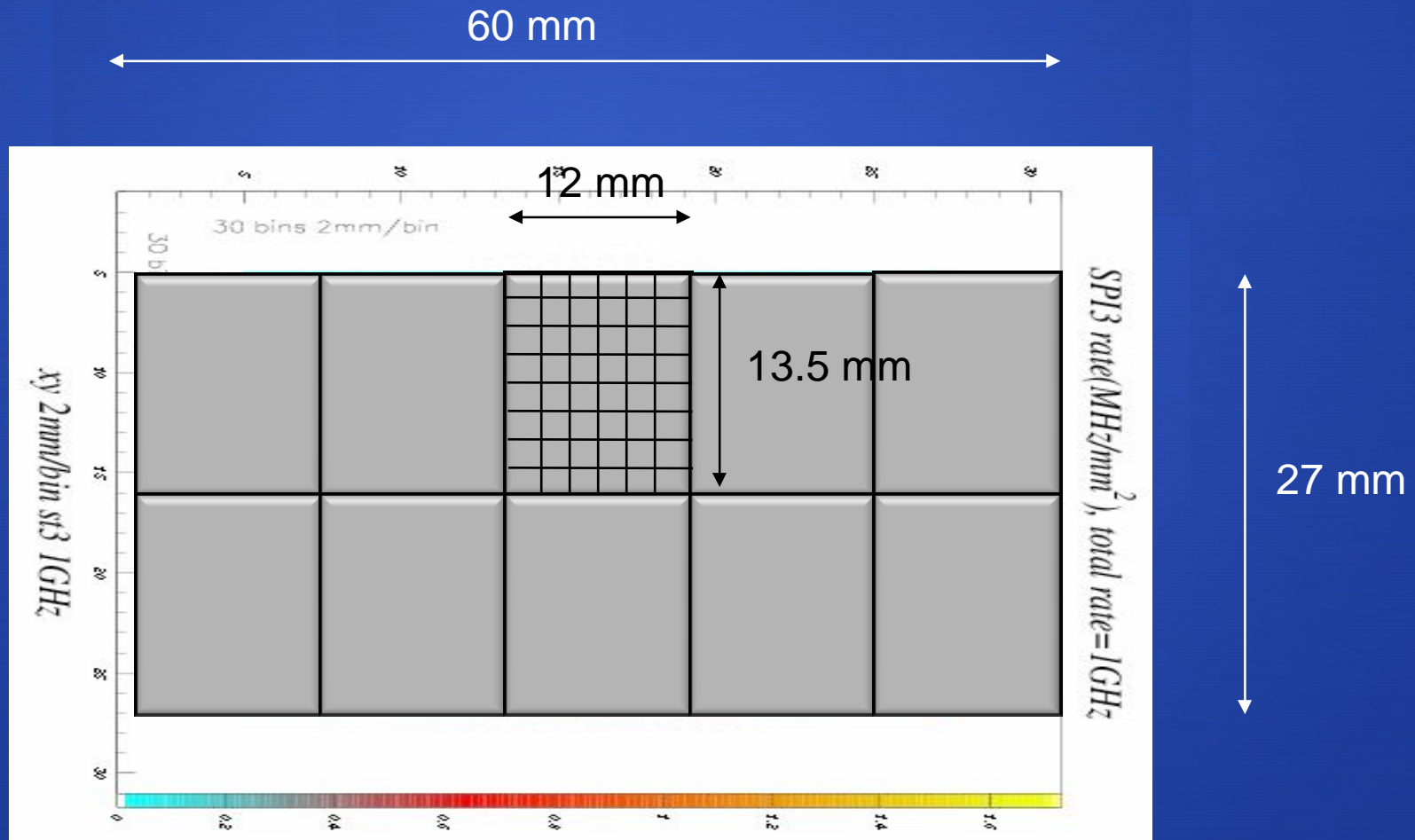
60 mm



27 mm

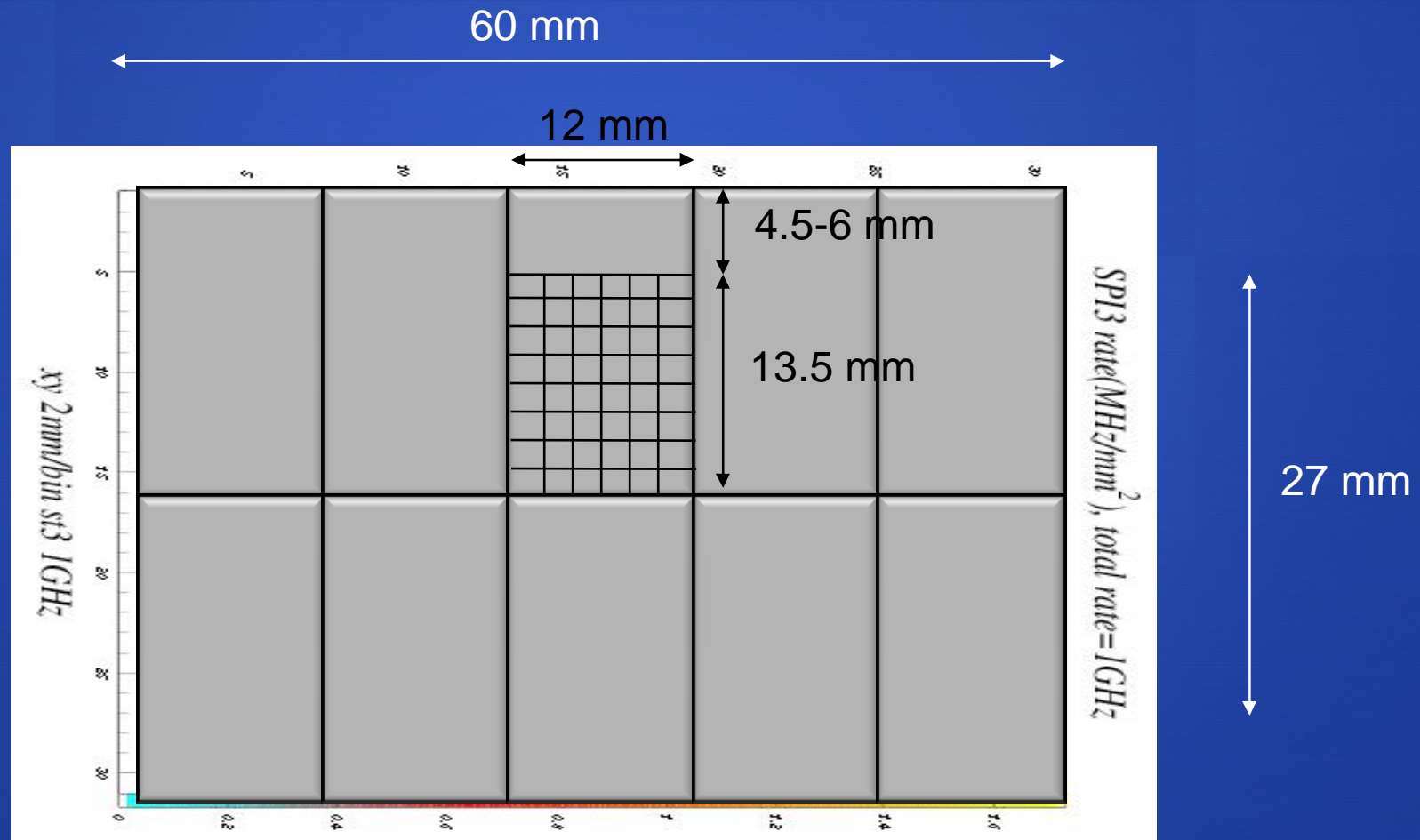


Giga Tracker setup





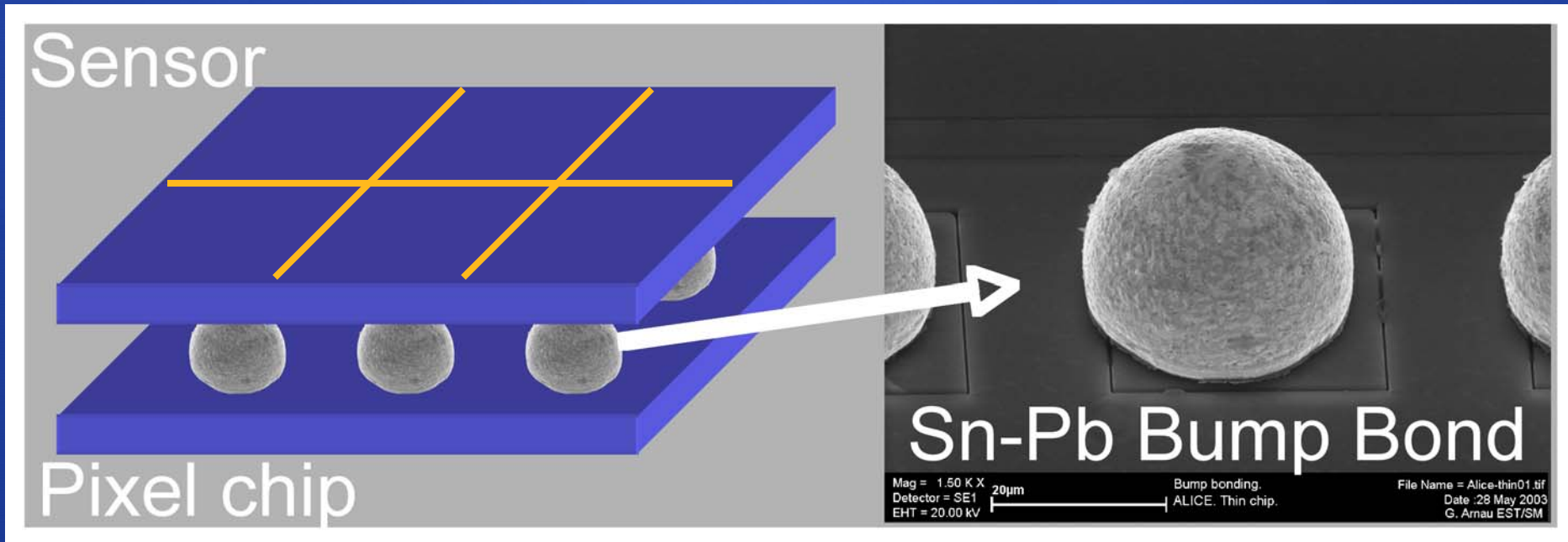
ASIC covering beam



45 rows times 40 columns per chip = 1800 pixels per chip

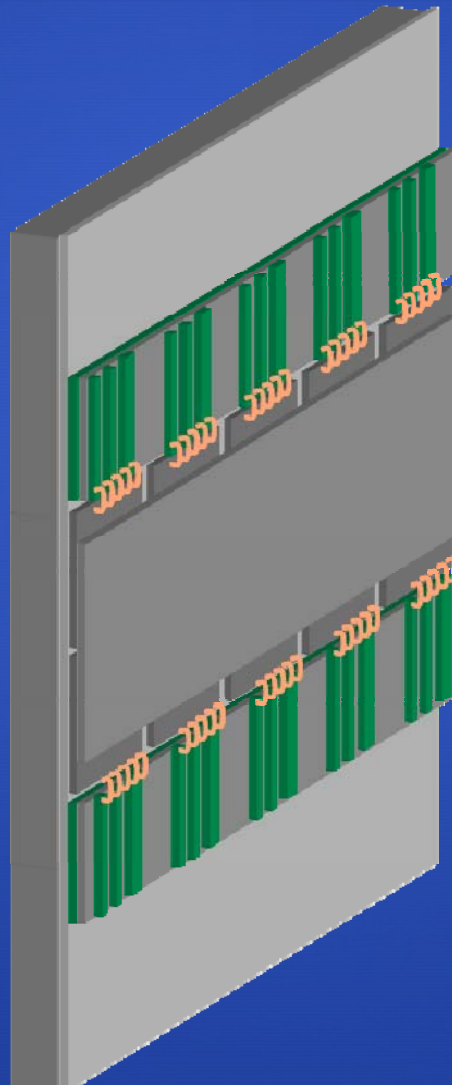


Hybrid pixel detector



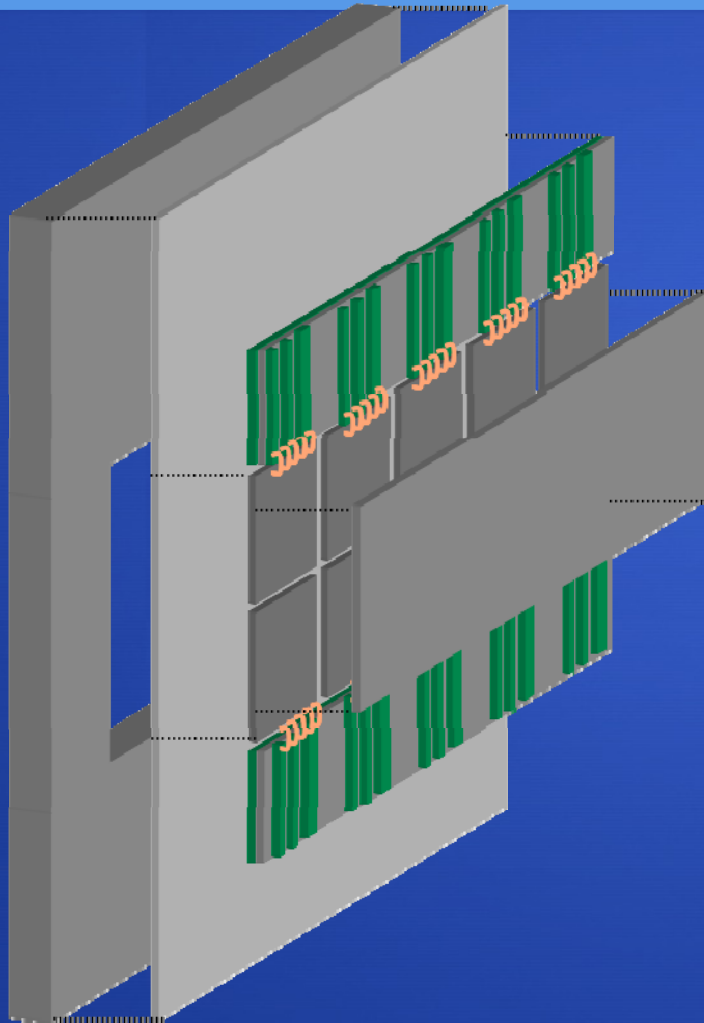


Configuration for beam 27-60

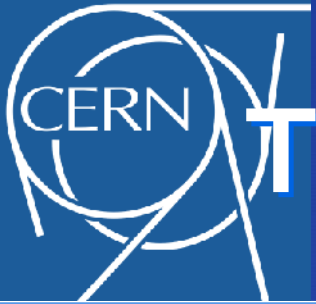




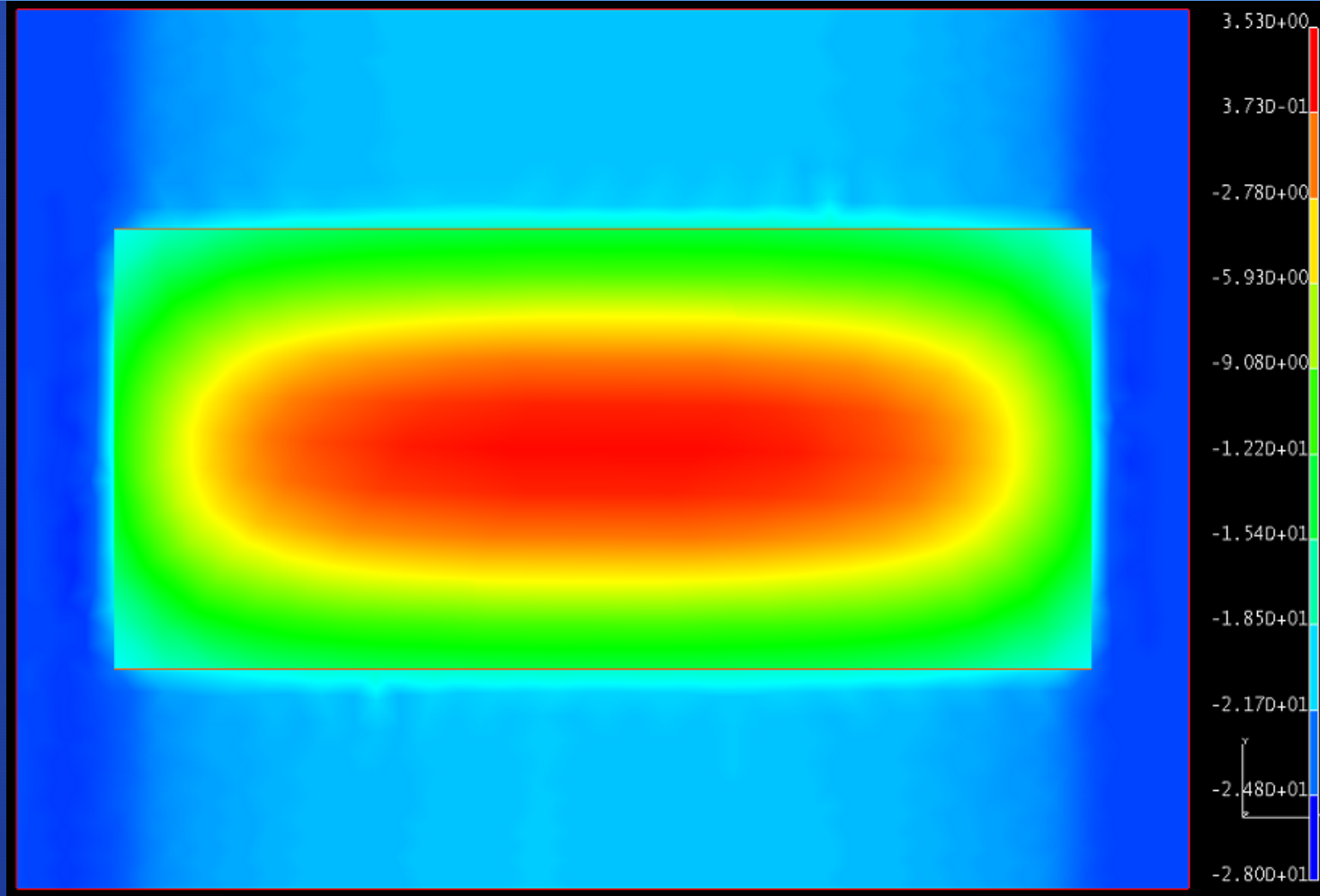
Giga Tracker setup



- Sensor&bonds: 0.24% X_0
(200 μm Silicon)
- RO chip: 0.11% X_0
(100 μm Silicon)
- Structure: 0.10% X_0
(100 μm Carbon fiber)
- Total: 0.45% X_0 uniform



Temperature distribution



Vittore Carassiti - INFN FE



Integration

- Module has very little mass
- It is cooled to < 0 degree C
- Possibly with cooling fluids of -173 degree C

- Integration challenge
 - temperature gradients
 - Safety systems in case of cooling failure, but now even
 - in case of power supply failure



The electronics specification



General: System Specifications

Number of pixels per chip	$1800 = 45 \times 40$
Size of pixels	$300 \mu\text{m} \times 300 \mu\text{m}$
Active area per chip	$12 \text{ mm} \times 13.5 \text{ mm} = 162 \text{ mm}^2$
Chip design time resolution	100 ps (rms)
Thickness of sensor	200 μm
Type of sensor	p in n
Thickness of read-out chip	100 μm
Dynamic input range	5000 – 60000 electrons



General: System Specifications

Design particle rate per chip	130 MHz
Rate of center pixel	140 kHz
Rate of center column	~ 3.3 MHz or 0.82 MHz/mm ²
Average rate per pixel	73 kHz
Maximum dead time	1 % (2 % in beam center)
Data transfer rate per chip	6 Gbit/s
Total dose in 1 year	~ 10 ⁵ Gy
Neutron flux in 100 days	2 x 10 ¹⁴ 1 MeV neutron equivalent cm ⁻²
Material budget/thickness	0.5 % X ₀ per station

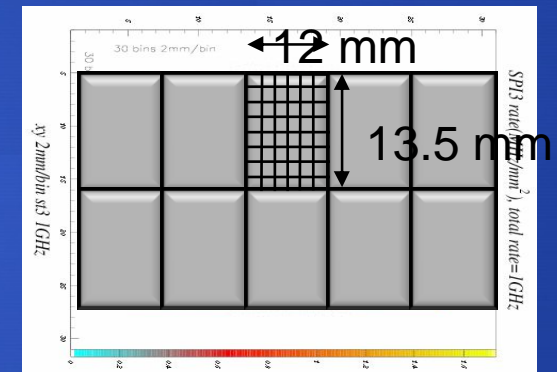


Data rate

- Rate of center column = chip design rate:

3.3 MHz/column
~ 82 MHz/cm²

- => avg rate 73 kHz/pixel
- => 132 MHz/chip



- => **132 MHz/chip * ~ 32 bit = ~4.2 Gbit/s**

- => max rate in beam center 140 kHz/pixel

- Example data word (11 bit address, 5 bit fine time, (5 bit fine time trailing), 11 bit coarse time)



Data rate & buffering

- 4.2 Gbit/s: Can we store the data on chip & send only data selected from NA62 trigger processor?
- Trigger latency: < 1ms, trigger window 10 ns
- 4.2 Gbit/s * 1 ms = 4.2 Mbit
 - 1 Flip-flop: $3.6 \times 7.2 \mu\text{m}^2 = 26 \mu\text{m}^2 \Rightarrow 10^8 \mu\text{m}^2 = 10 \times 10 \text{ mm}^2$
- As a result we cannot store the data
- We must ship it out without trigger
- Triggerless architecture
- Data selection off-detector in FPGA

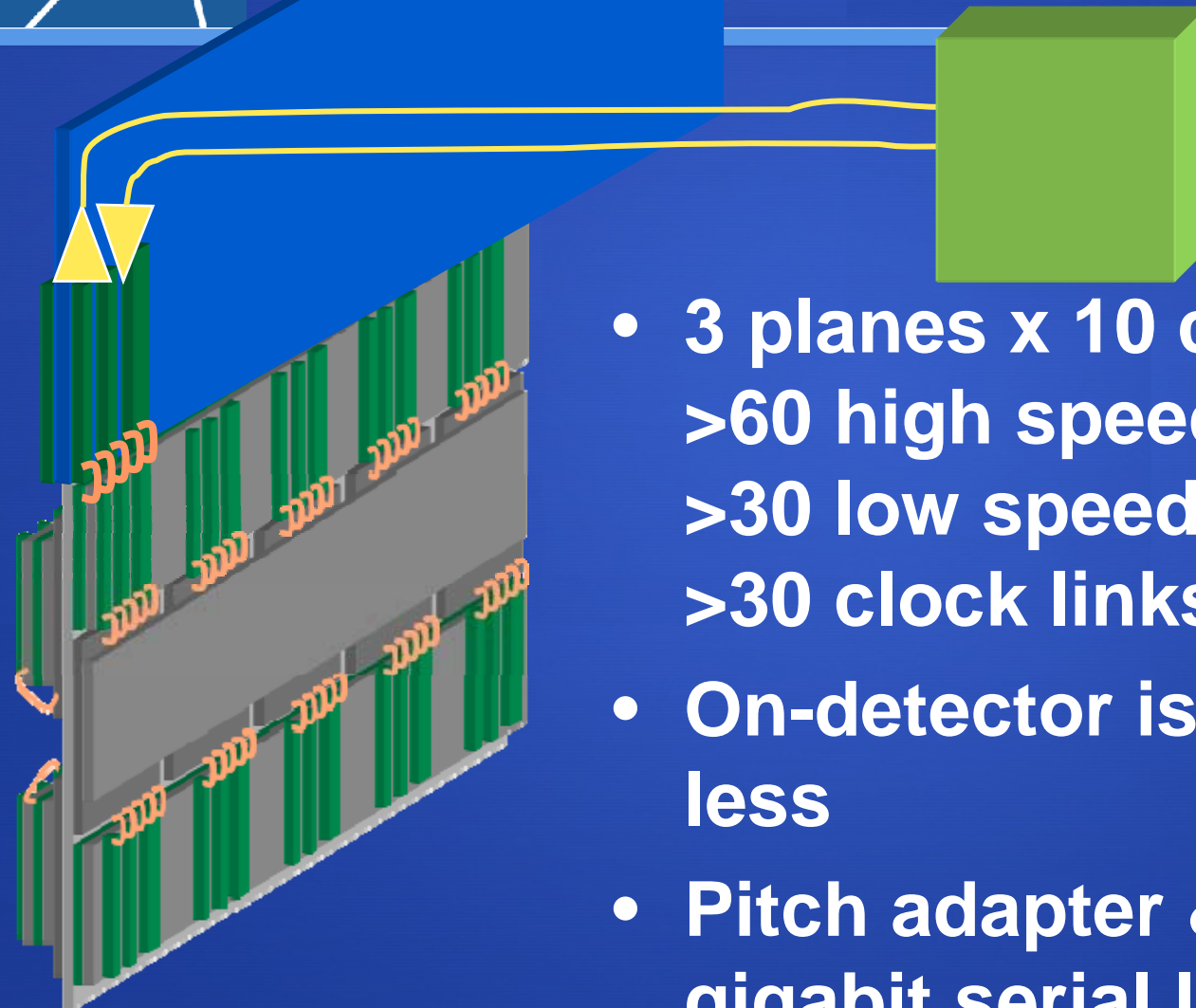


I/O block diagram of chip





Read out



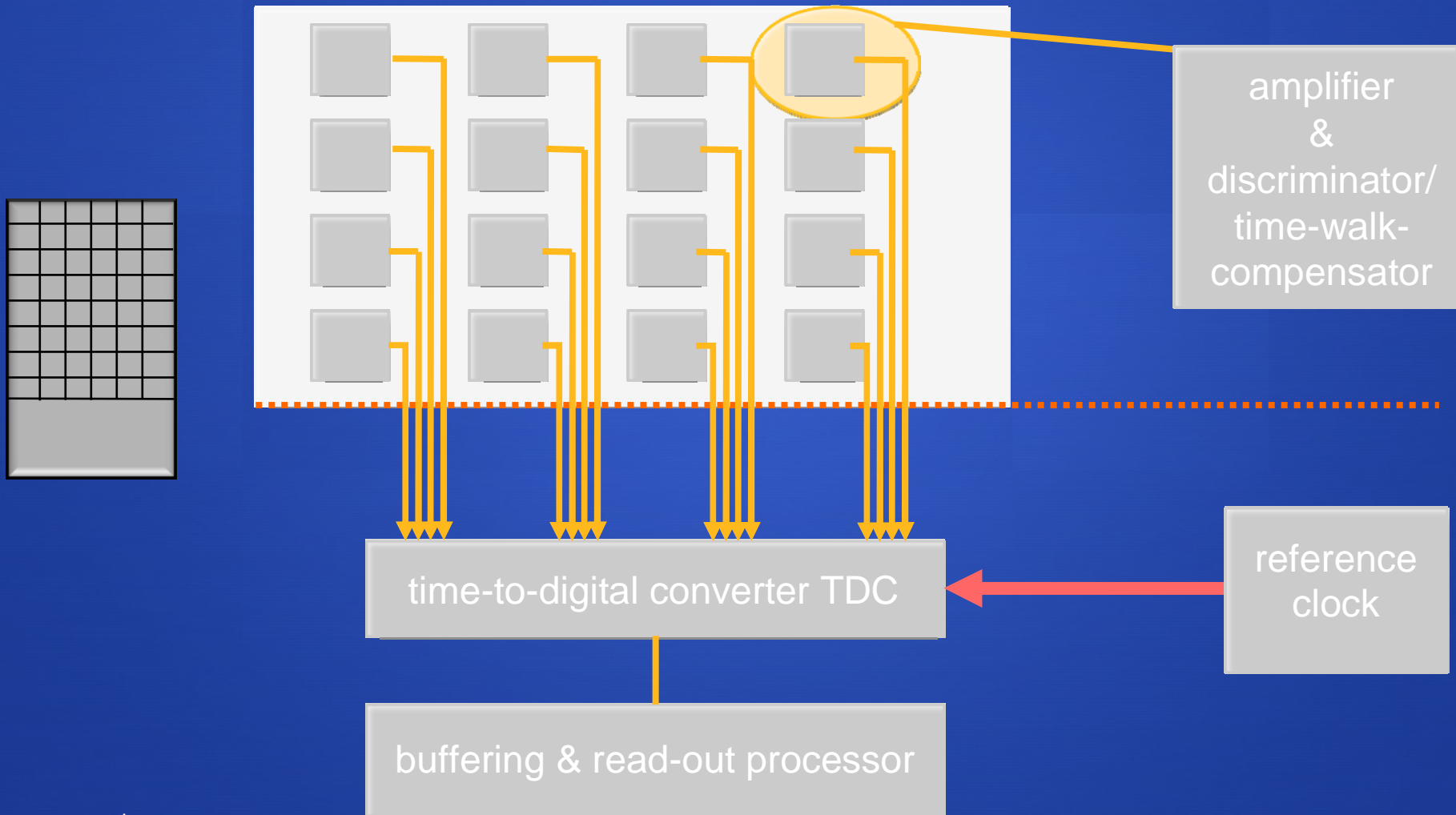
- 3 planes x 10 chips:
>60 high speed links +
>30 low speed links+
>30 clock links
- On-detector is trigger-less
- Pitch adapter & multi gigabit serial links



The architecture

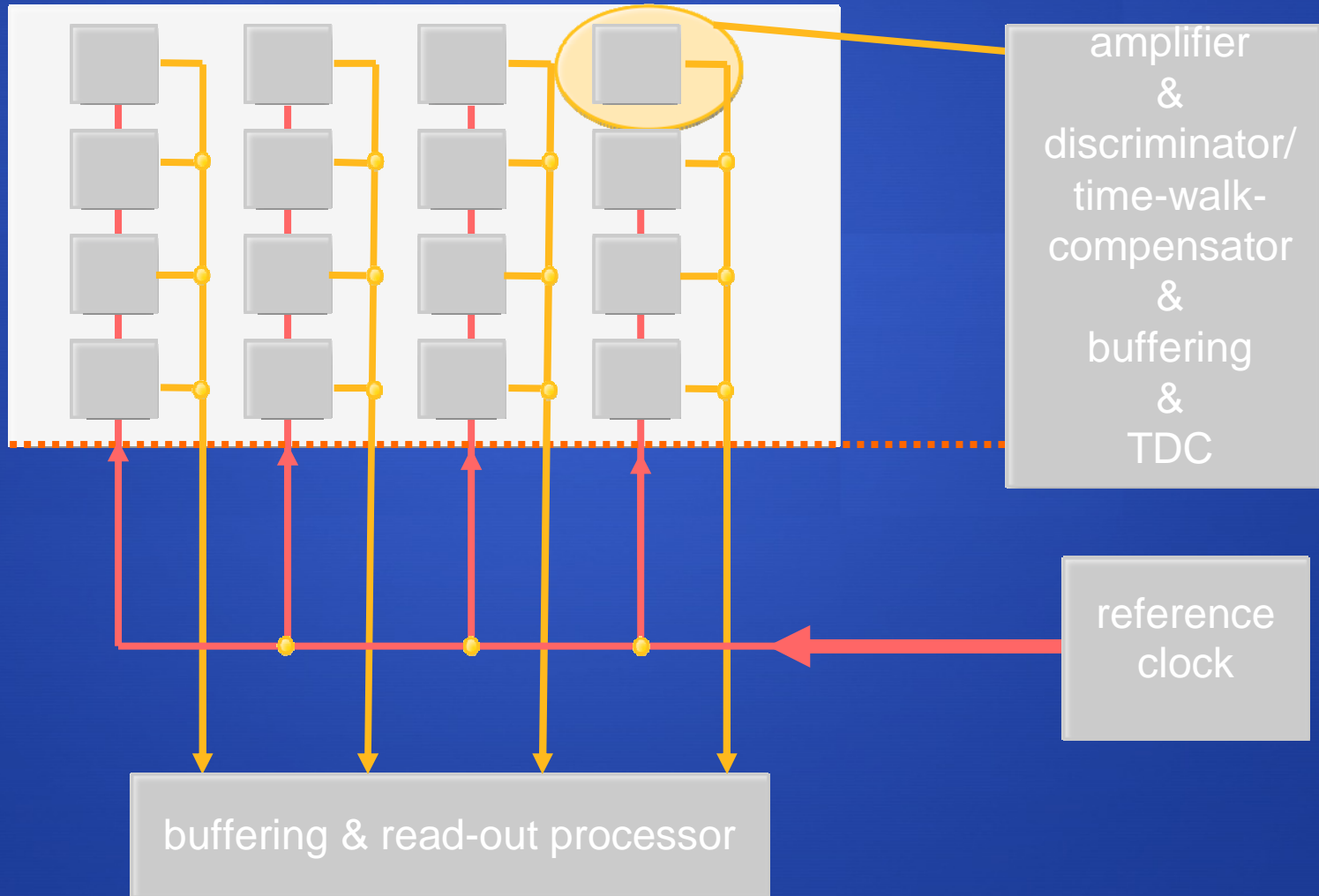
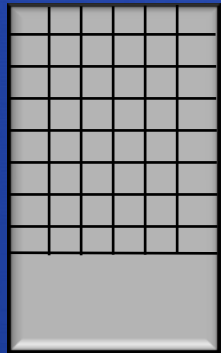


Jitter-free pixel signal to TDC in EOC





Precise clock signal to all pixels





EOC architecture

- simple basic concept
- improved analog/digital noise separation due to physical distance
- pixel cell not fully filled, possibility to make smaller
- TDC concept already tested
- no clock signals in matrix
- transmission of jitter-free hit signal along the matrix for each pixel
- transmission only when hits occur
- digital read-out electronics in EOC not in heavily radiated beam zone
- dead-time optimisation by number of multiplexed pixels in one TDC



TDC per pixel architecture

- advanced concept
- analog/digital noise separation more difficult
- pixel cell efficiently filled, difficult to make smaller
- clock signals all over matrix
- digital read-out bus in matrix, no individual transmission of signals
- digital electronics in heavily radiated beam zone
- dead time optimisation by choice of TDC conversion time and in pixel buffering



Which architecture to choose?

- Postpone after we discussed
 - How to measure the arrival time
- &
- How to compensate for time walk



The time-to-digital conversion



Delay locked loop based TDC

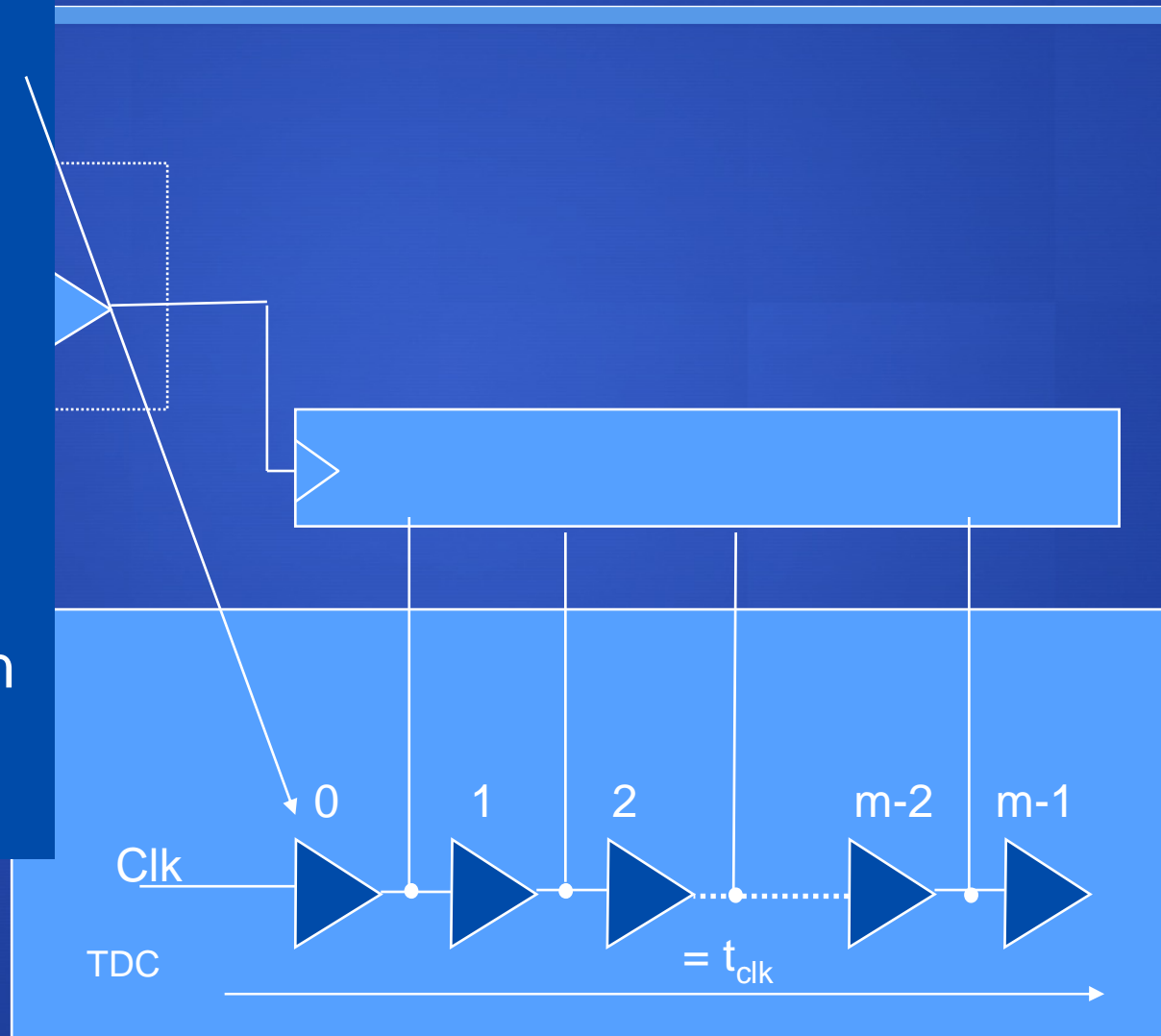
Differential buffers:

Low noise, higher power consumption

Good matching required, bigger than simple inverter

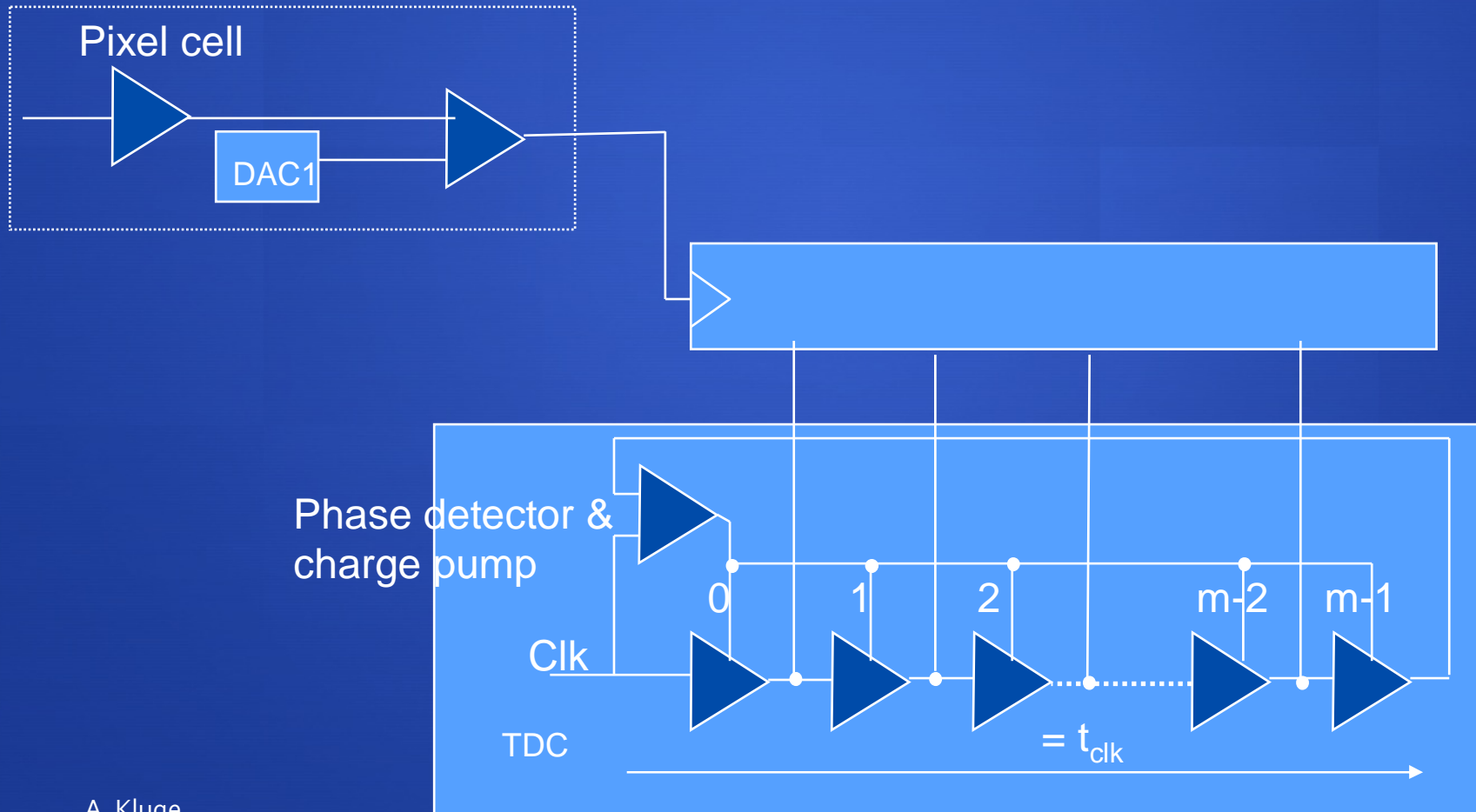
More than 32 in series (I.e. 128) non-linearity is an issue, calibration required

DLL based TDC



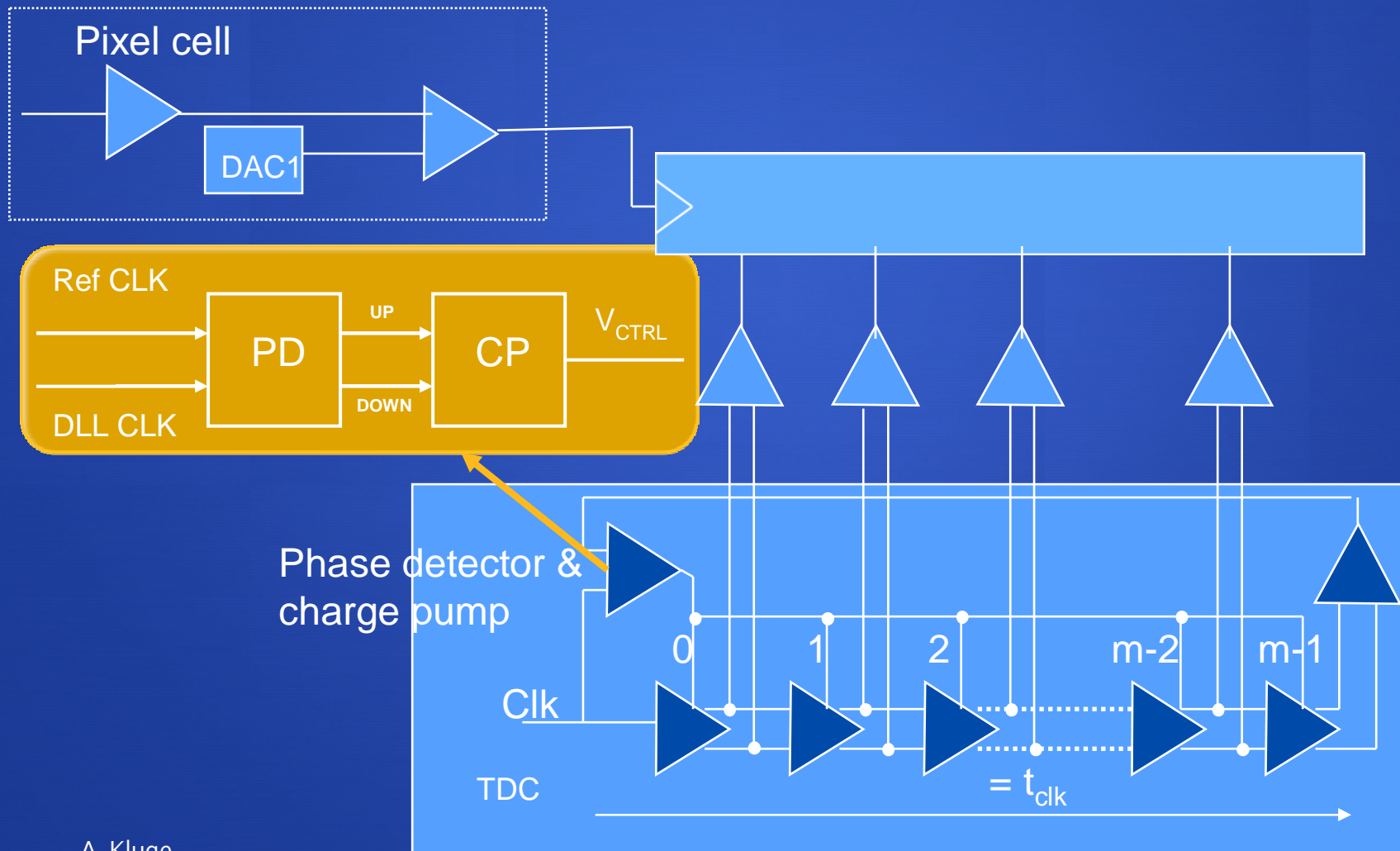


DLL based TDC





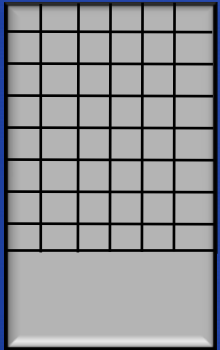
DLL based TDC





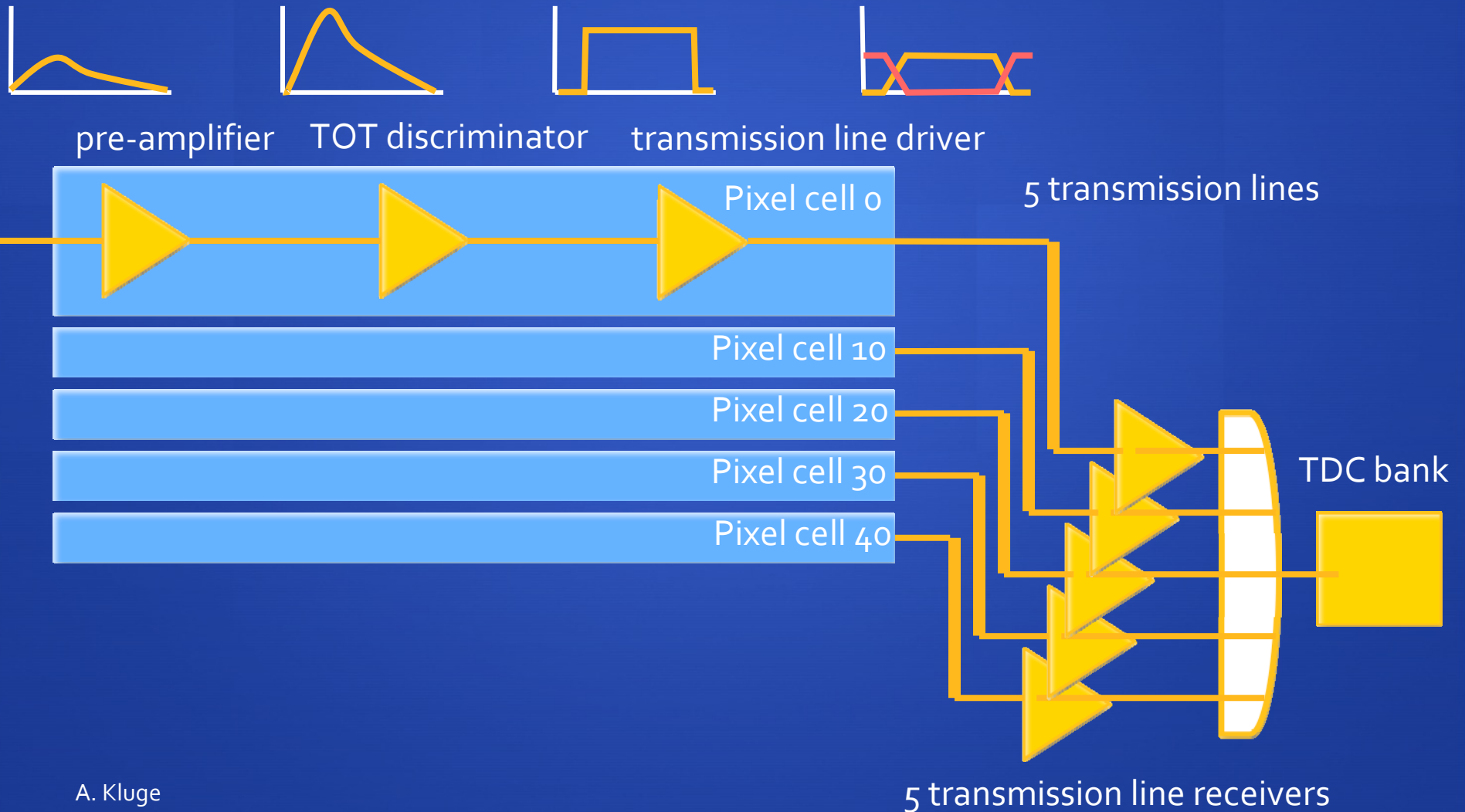
Time-to-digital converter - TDC

- in end of column – EOC
- space, but not space for one TDC each for all 1800 pixels



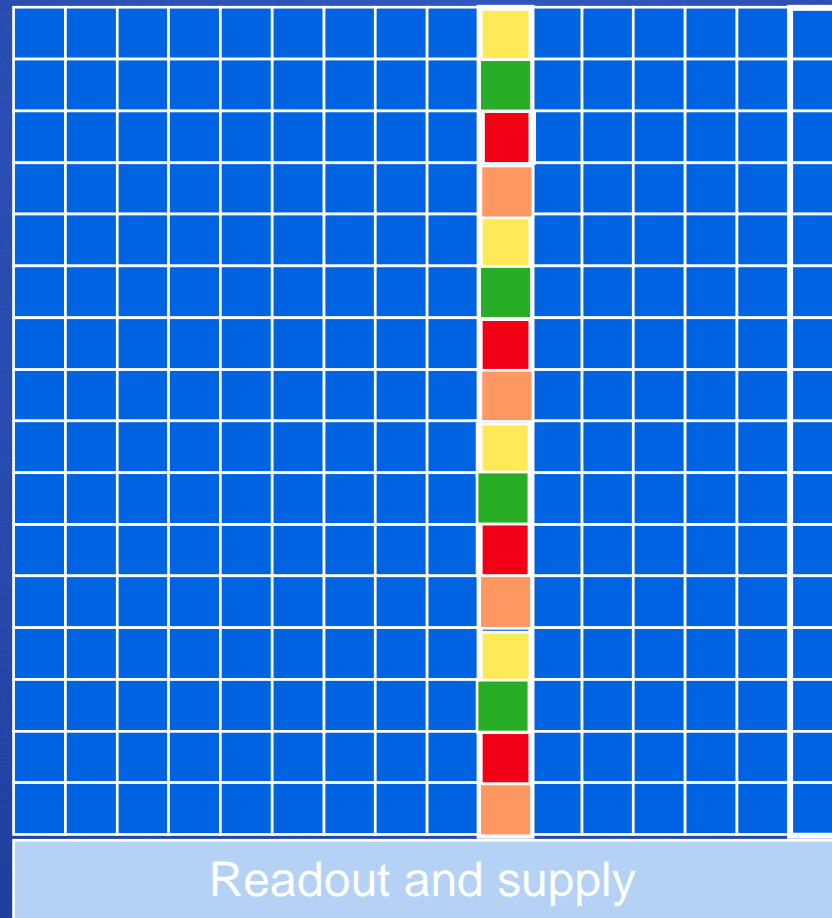
- choice -> DLL based TDC

grouping of pixels



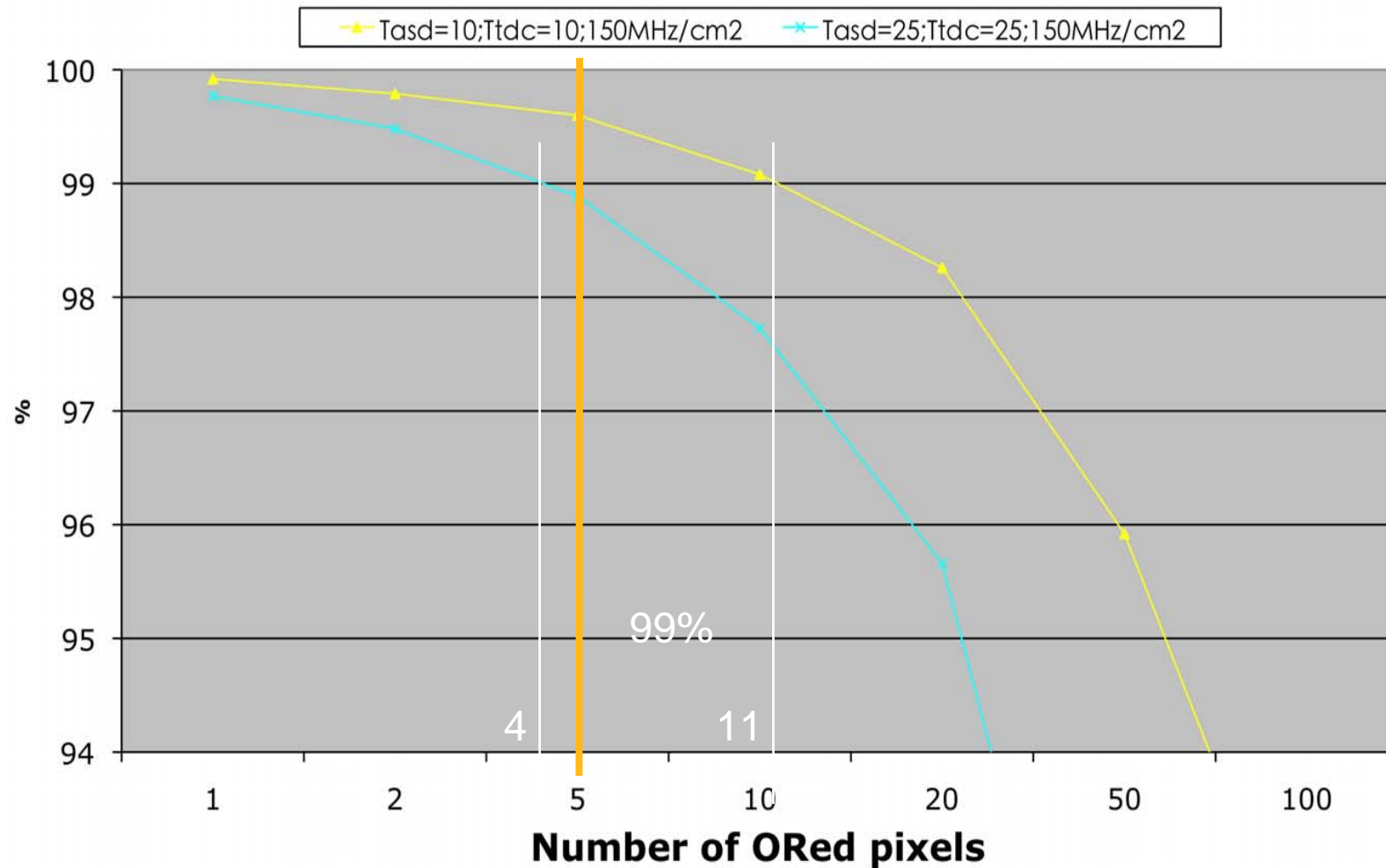


grouping of pixels



Pixel segmentation

Efficiency 150 MHz/cm² (corresponds to center pixel)
if pixels shared come from different parts in the column the rate decreases



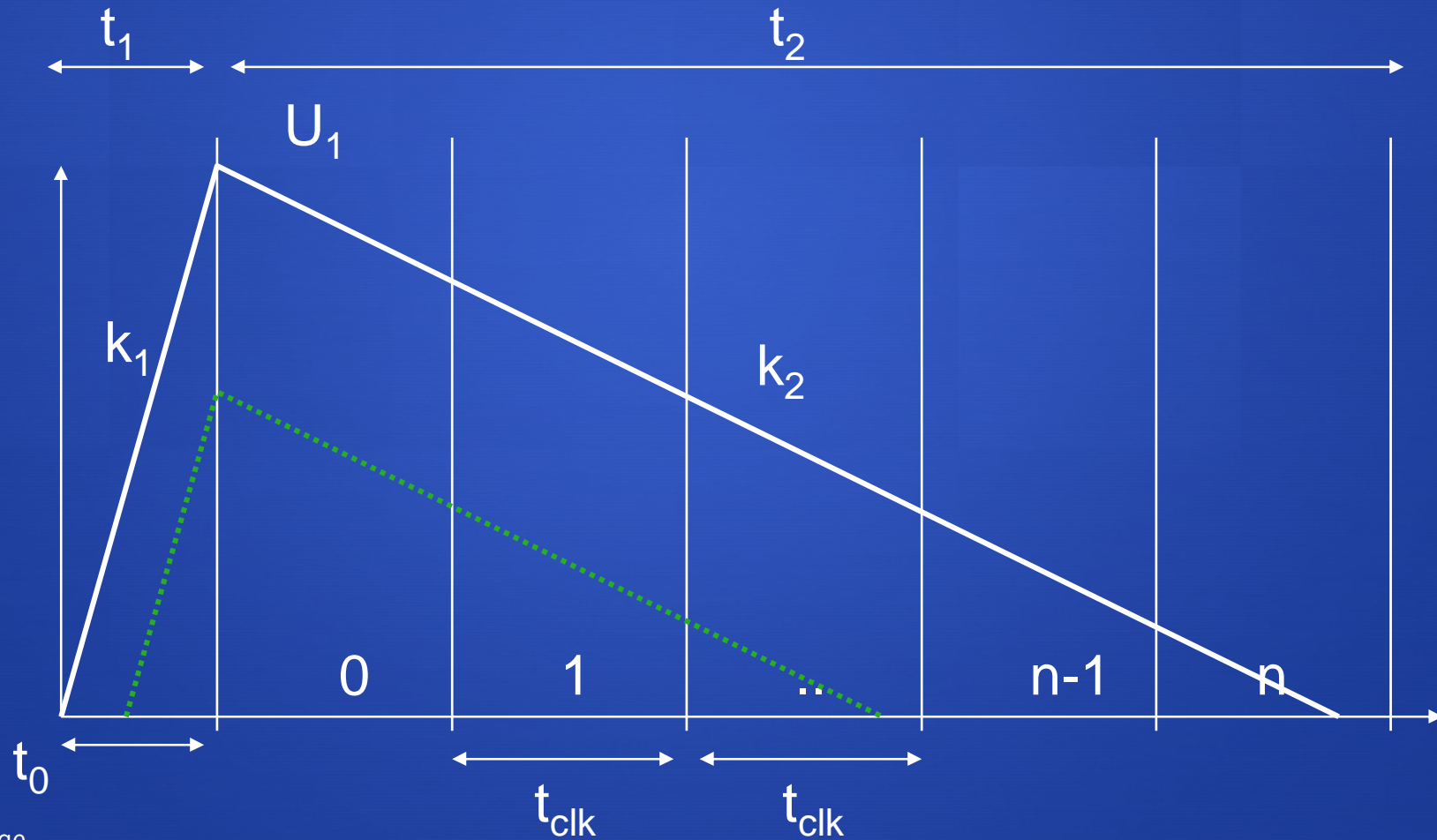


Dual slope TDC

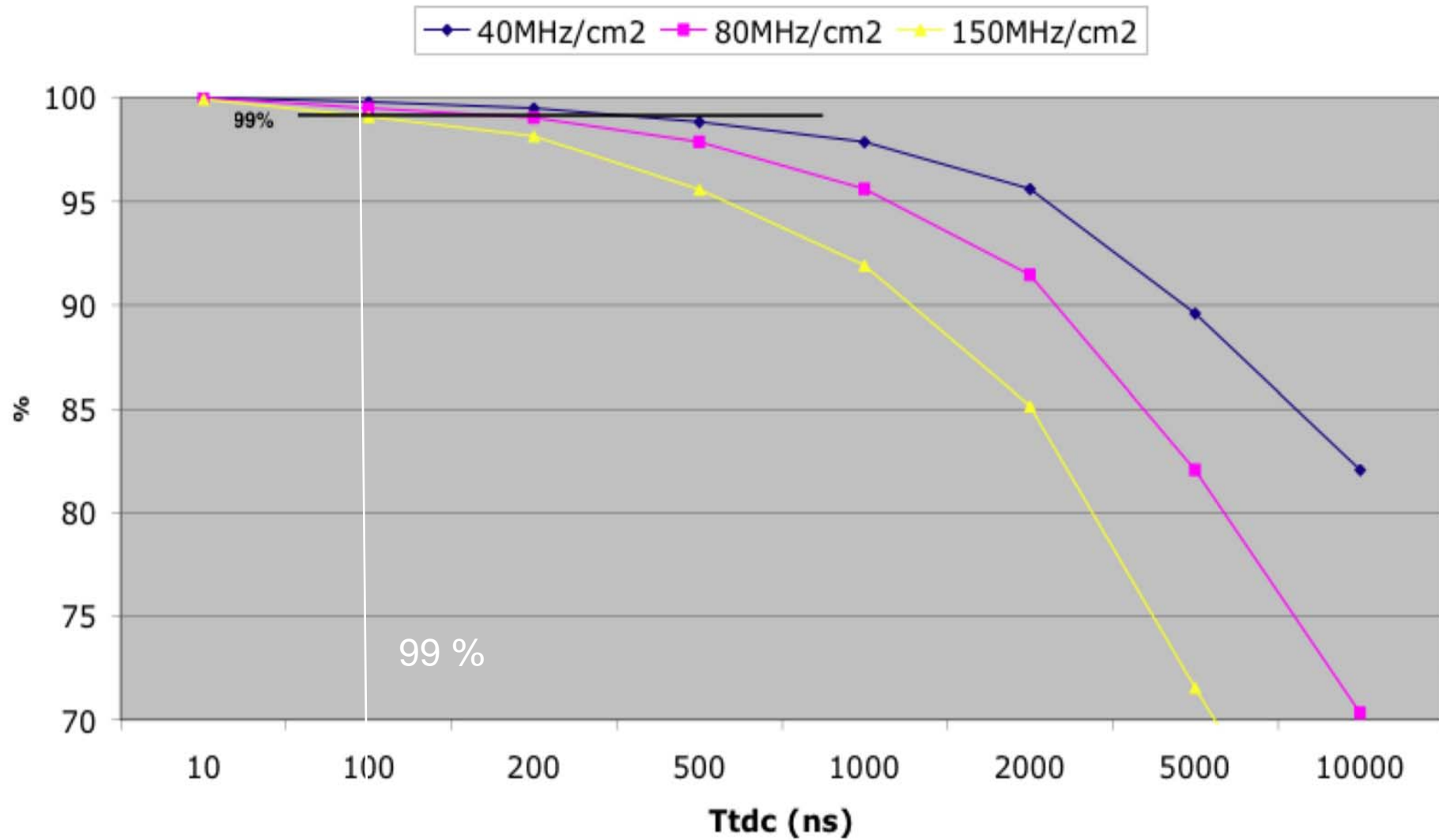


TDC Wilkinson (dual slope)

$$t_0 = n t_{\text{clk}} k_2 / k_1$$

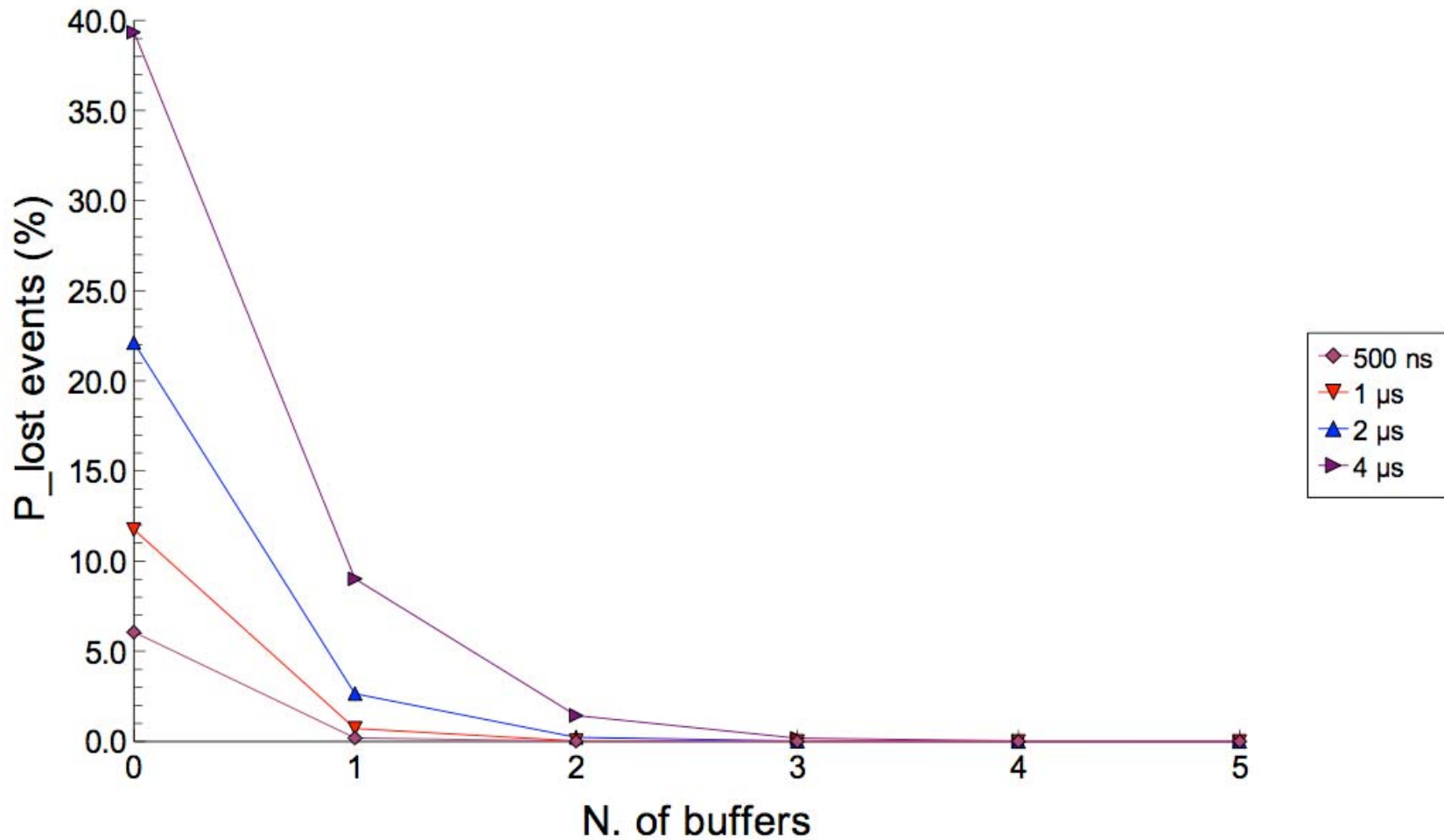


Efficiency for 1 TDC per pixel ($T_{asd}=10\text{ns}$, $N_{or}=1$)



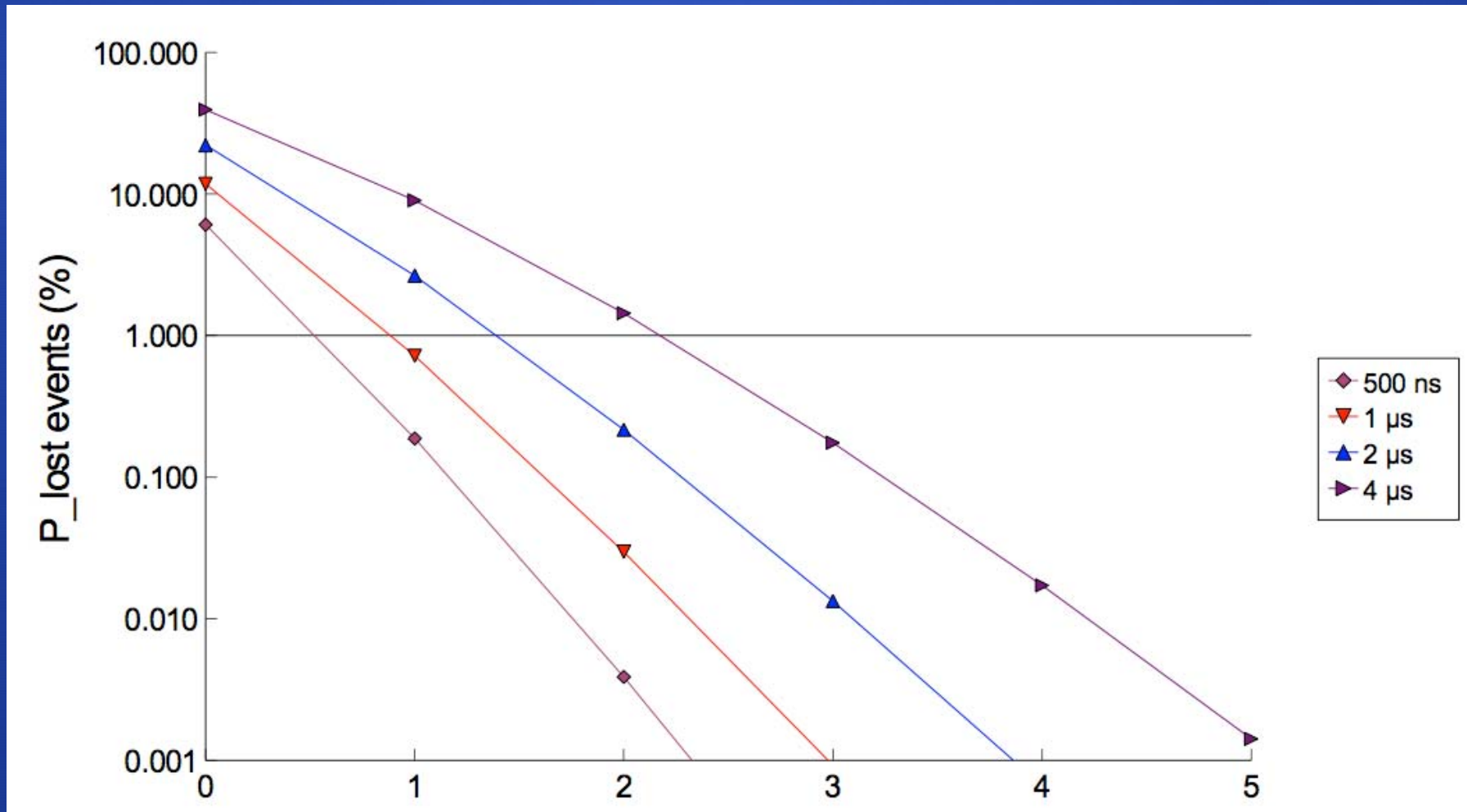


Dual slope with buffers





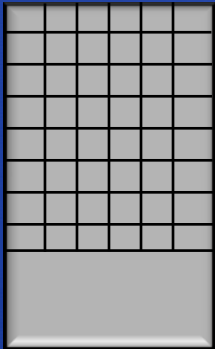
Dual slope with buffers





TDC per pixel

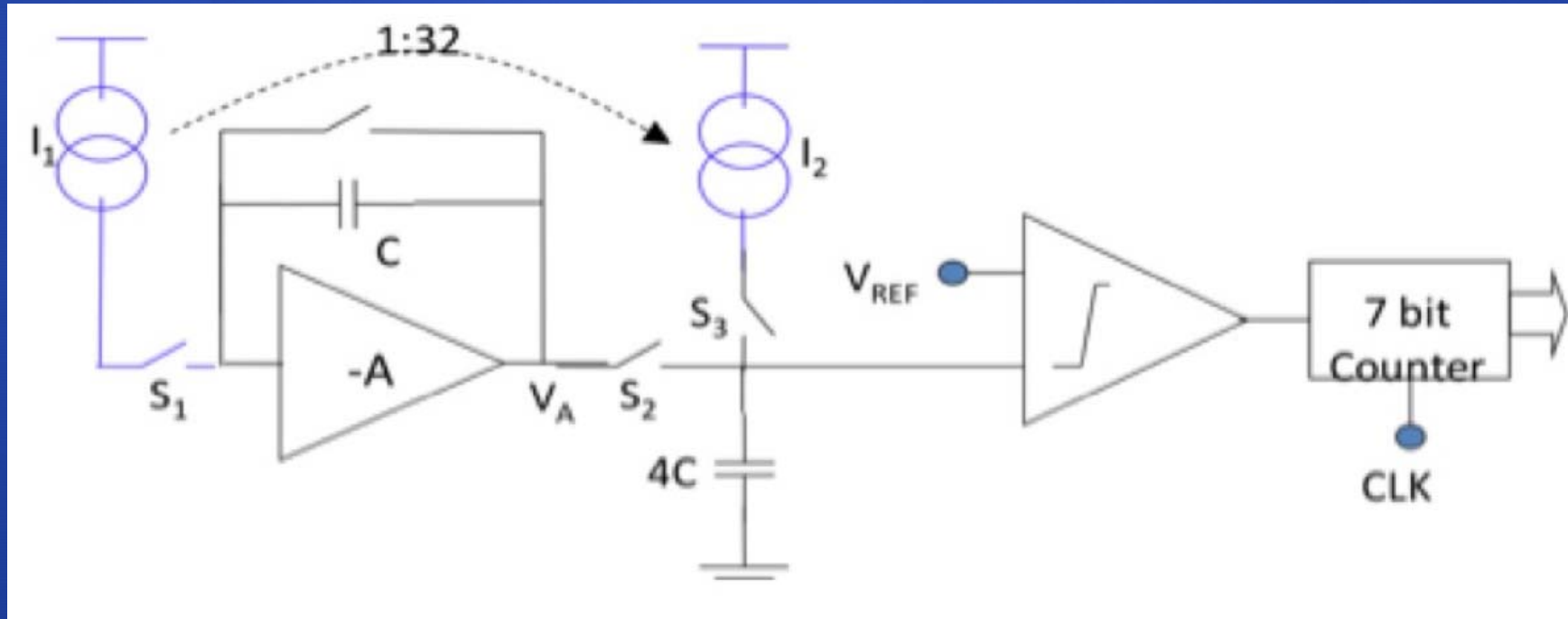
- in pixel cell
 - limited space, but space in each pixel cell



- choice -> Wilkinson – dual slope based TDC



Dual slope TDC

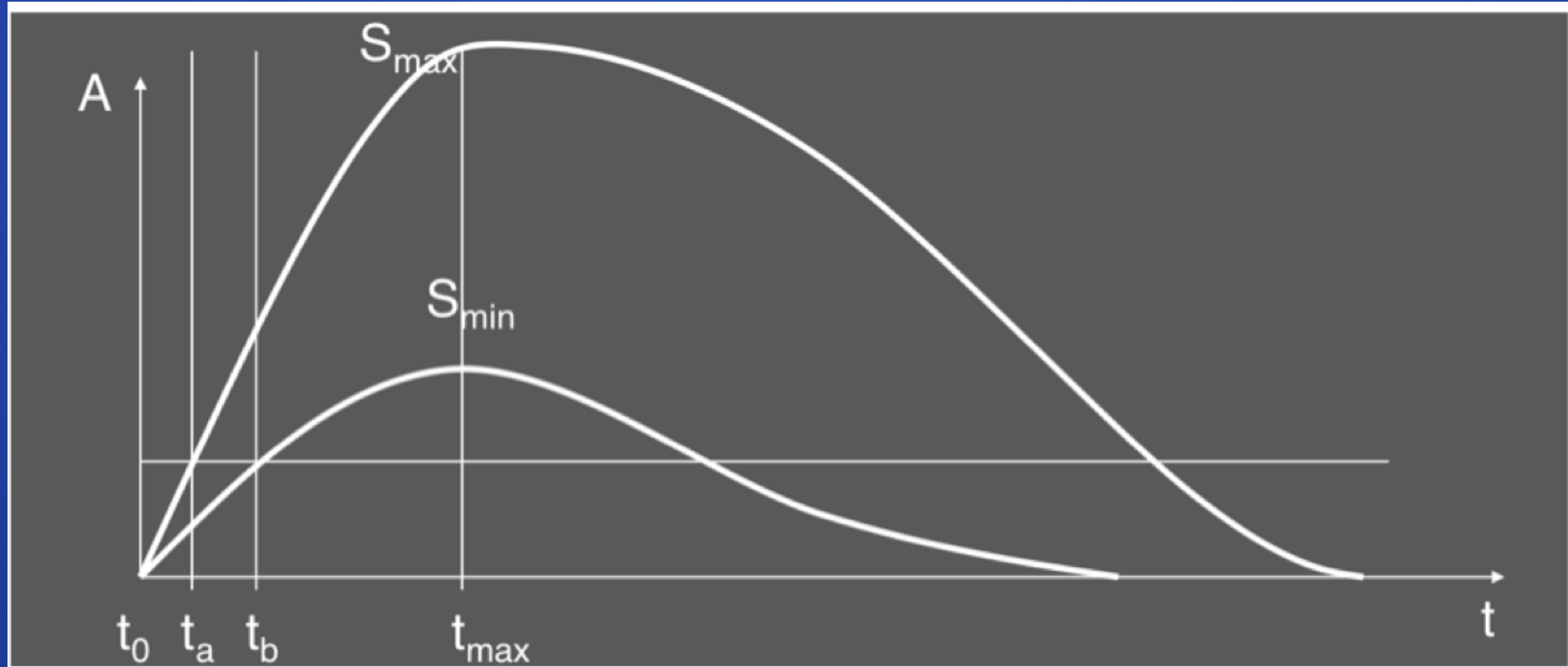




time walk



Time walk

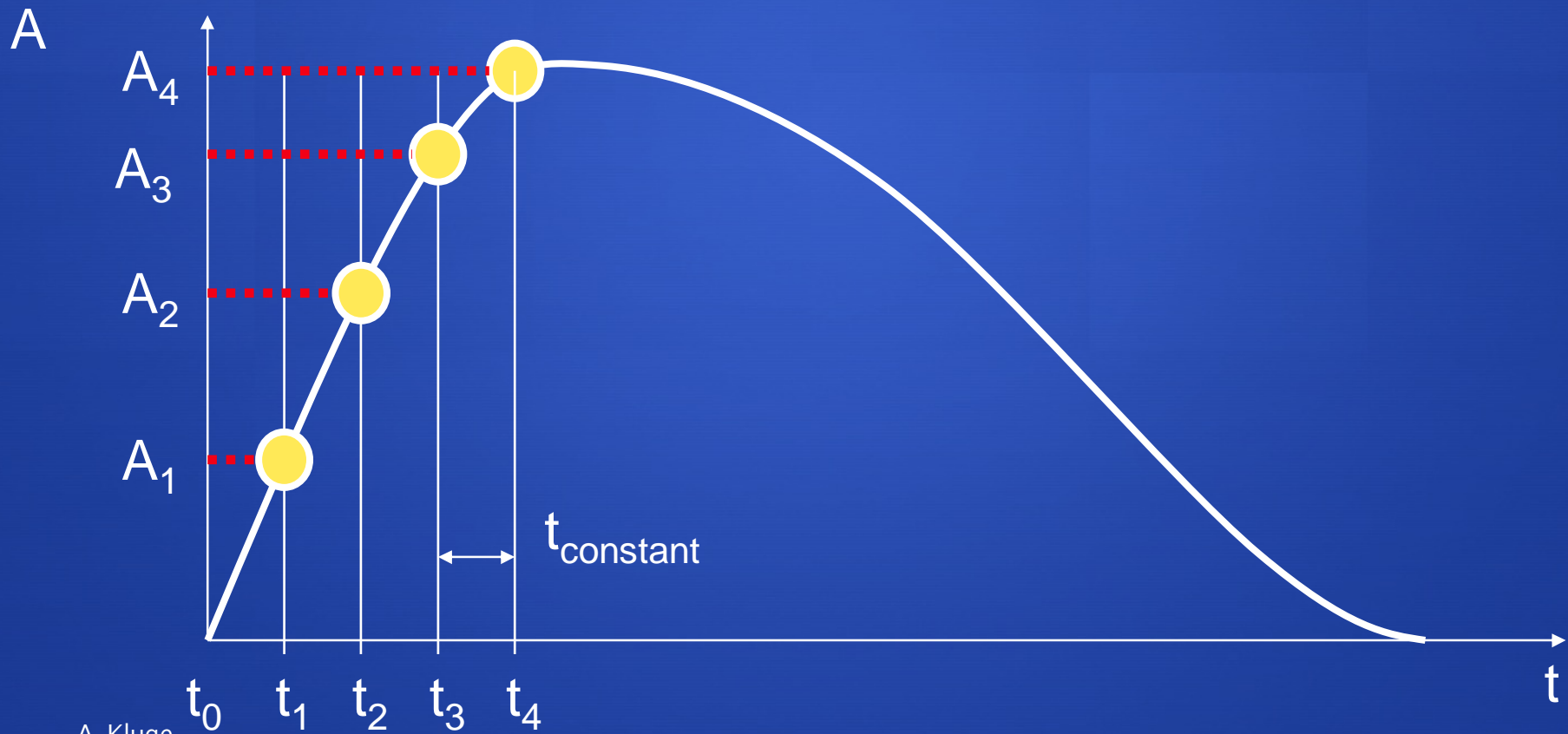


- Until now assumed ideal discriminator



Ideal: Sample signal

- at constant times
- Many high precision ADCs needed: unrealistic



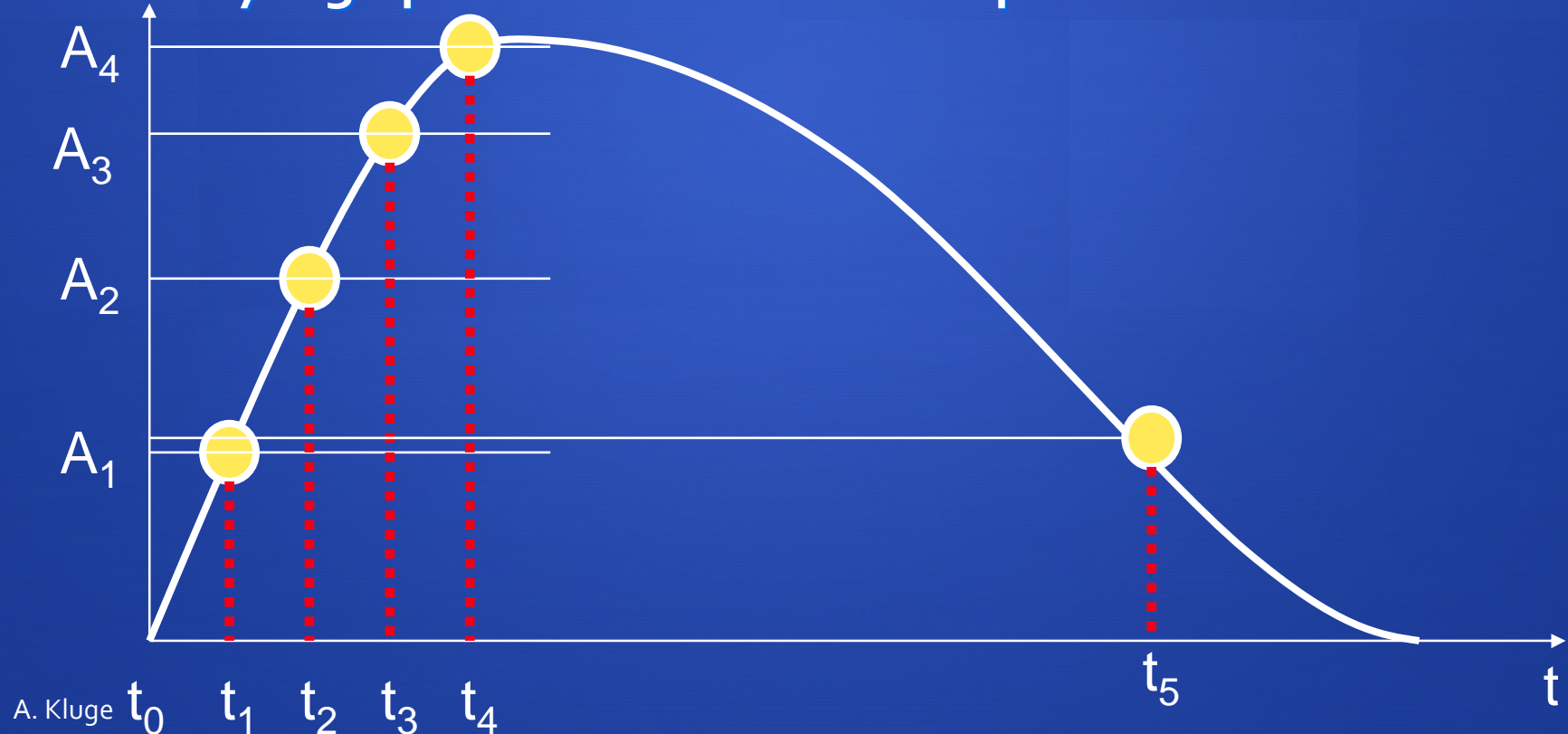


Ideal: Sample signal

- at discrete amplitude values with several single threshold discriminators

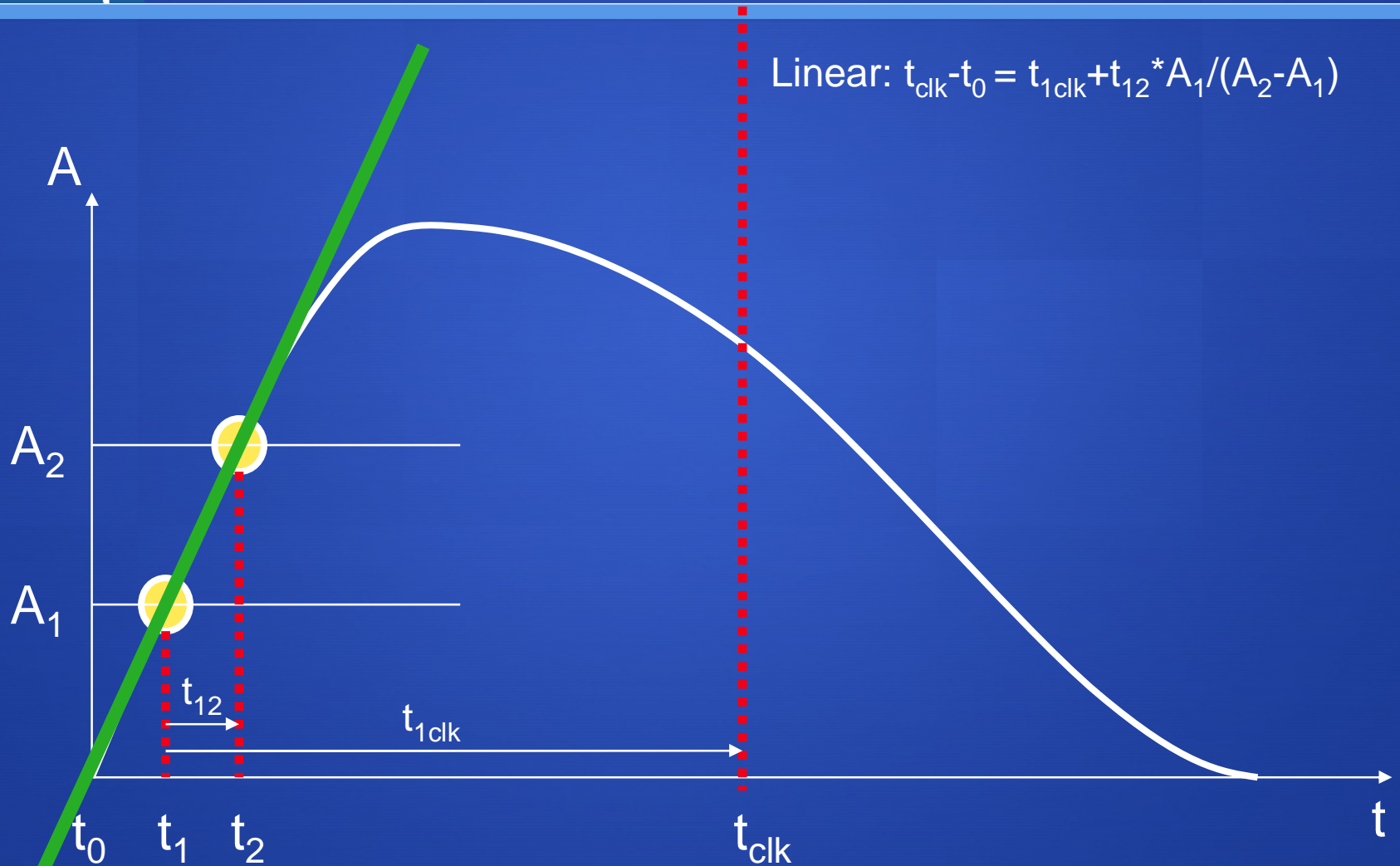
A

- Many high precision TDCs needed: possible?



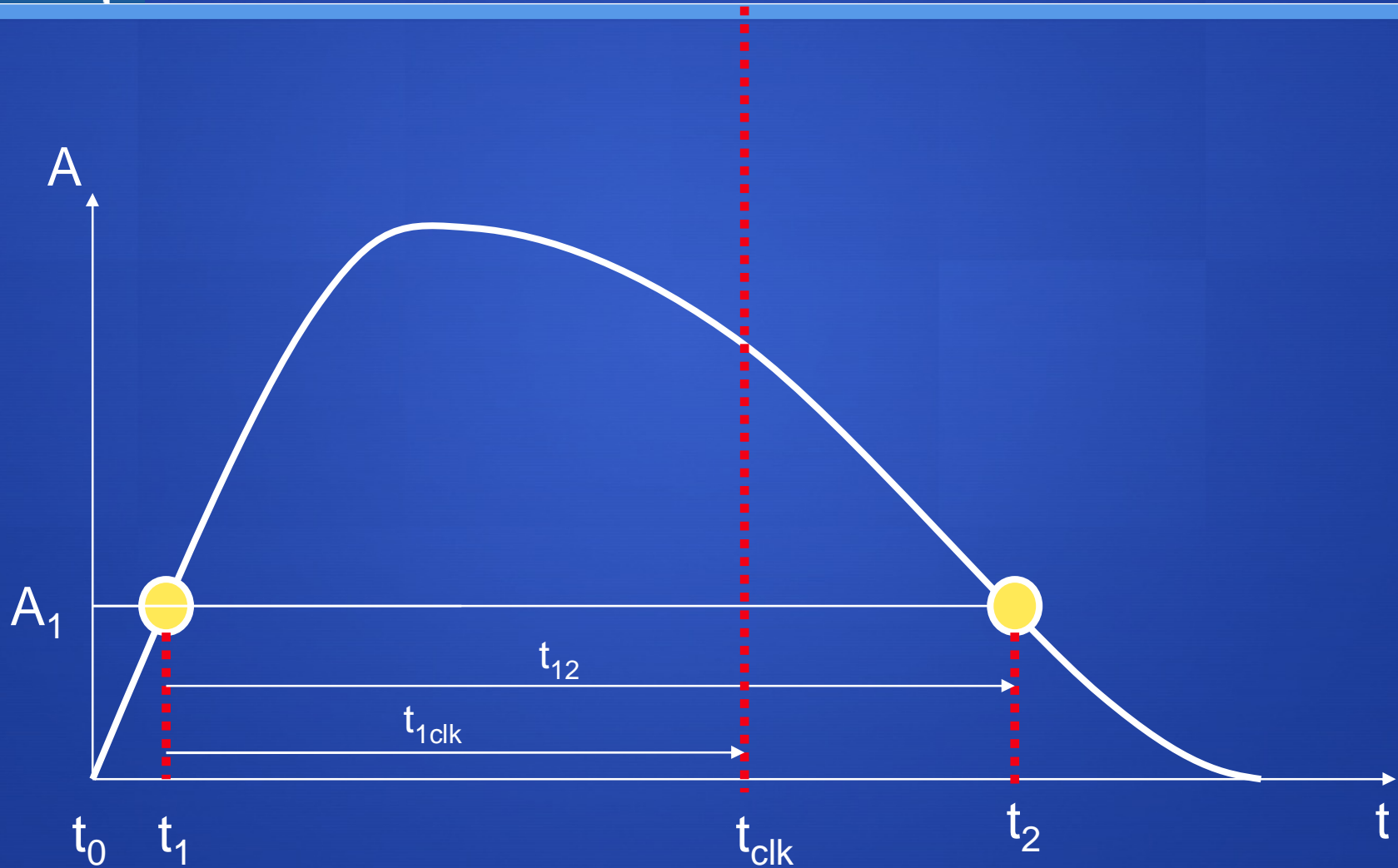


Double threshold



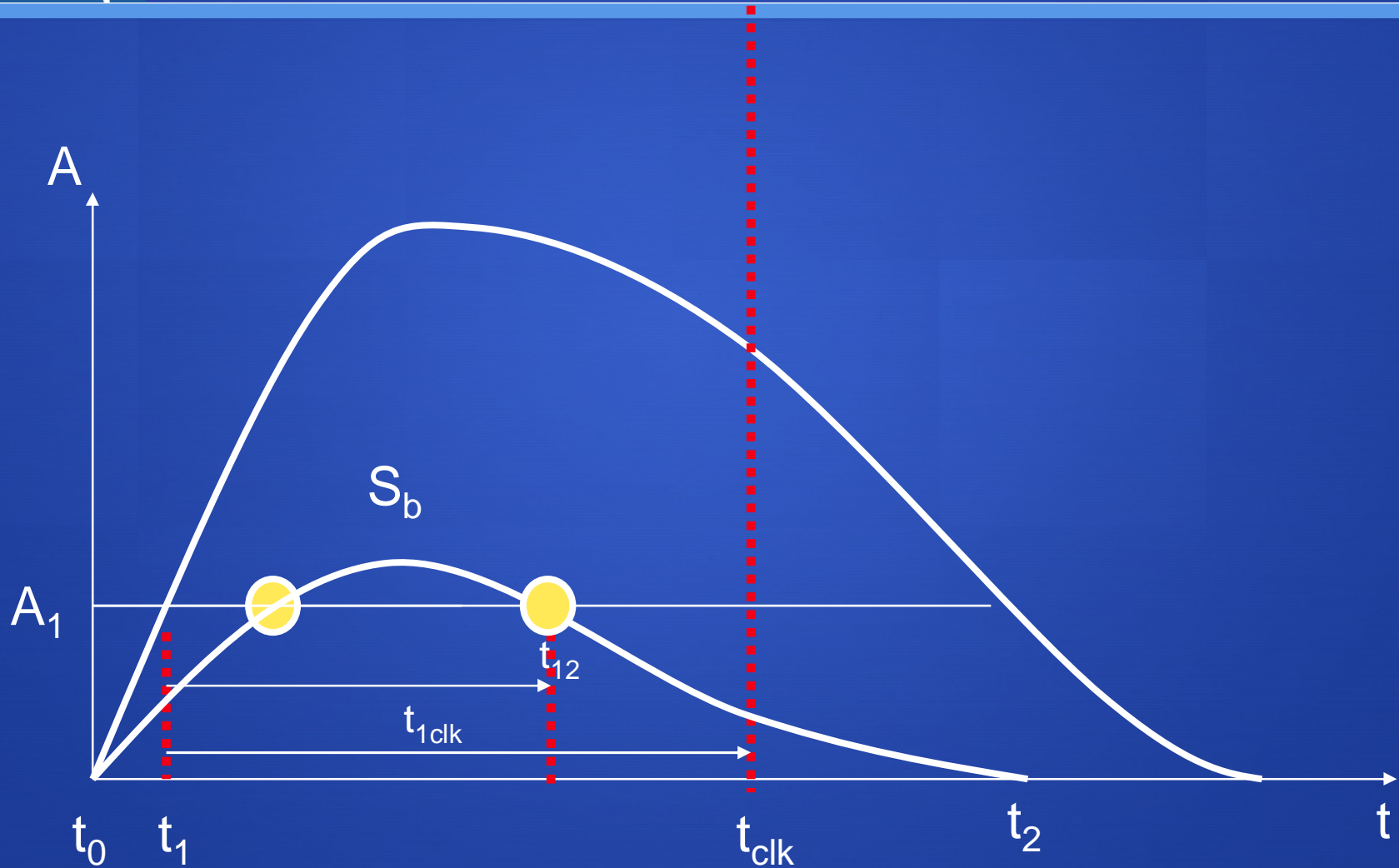


time-over-threshold



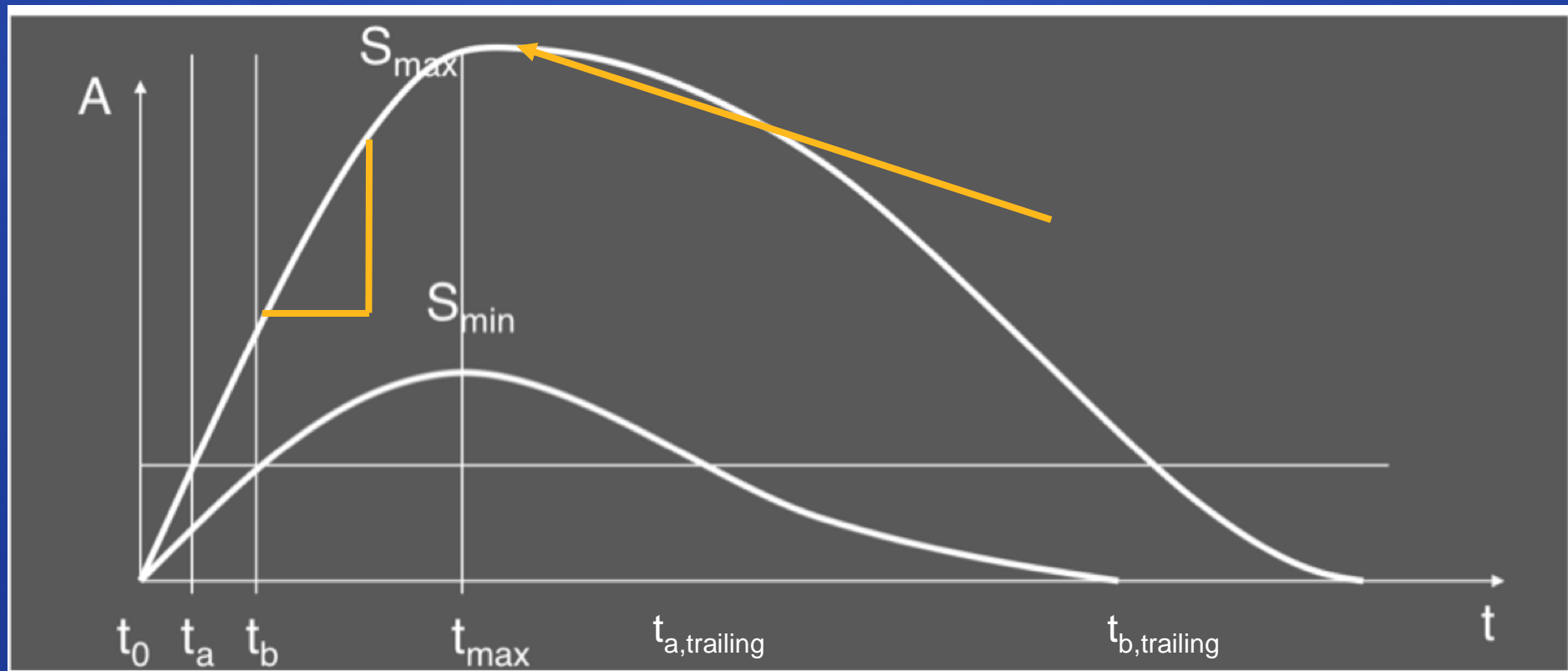


Time-over-threshold





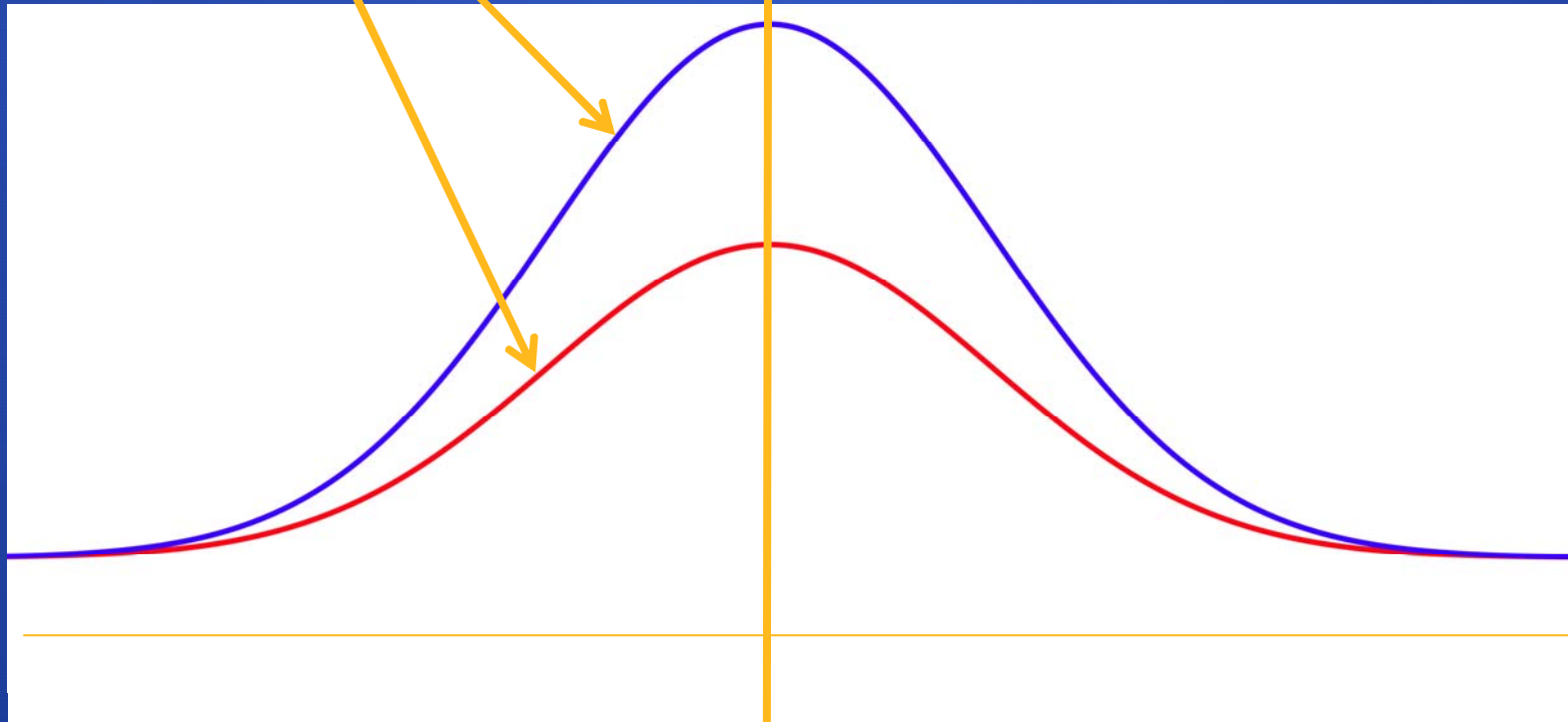
Constant fraction discriminator





Constant fraction discriminator

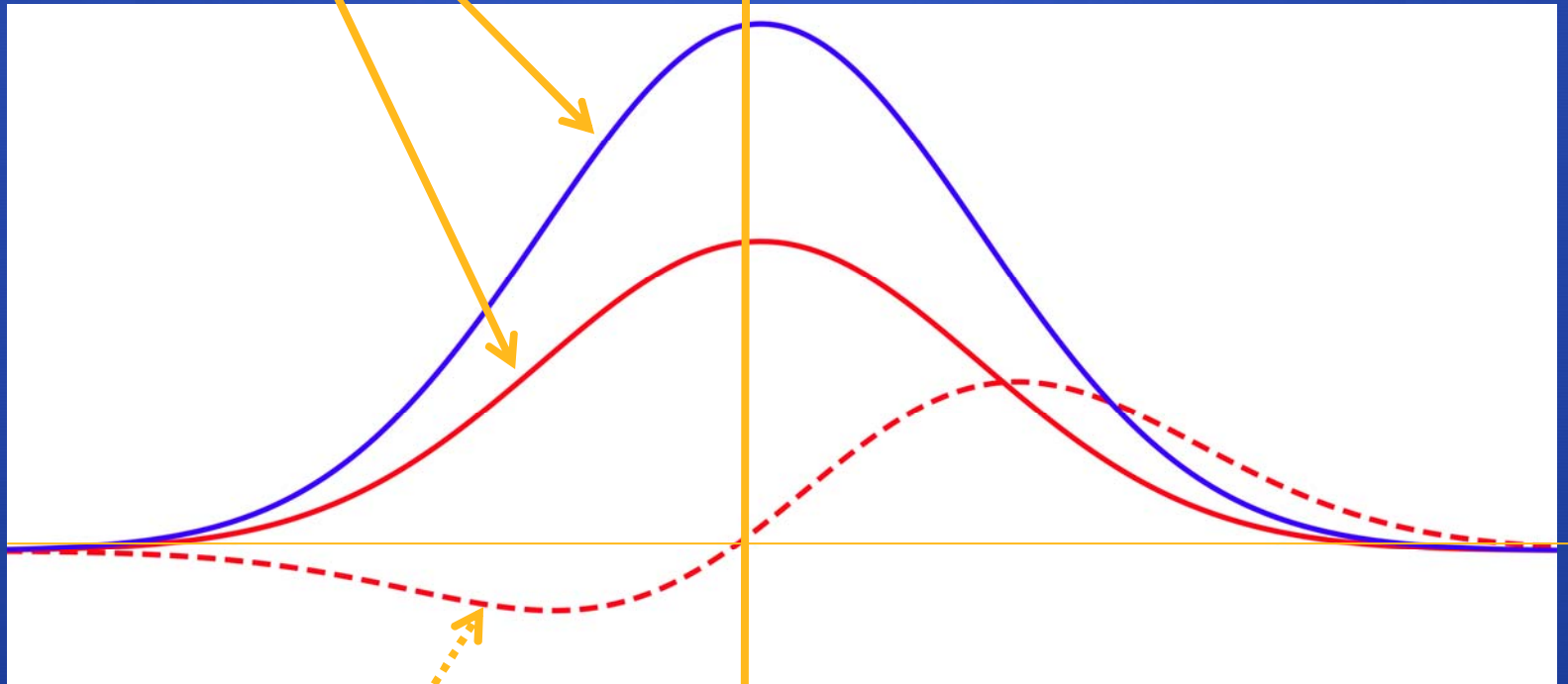
input pulse large/small amplitude





Constant fraction discriminator

input pulse large/small amplitude

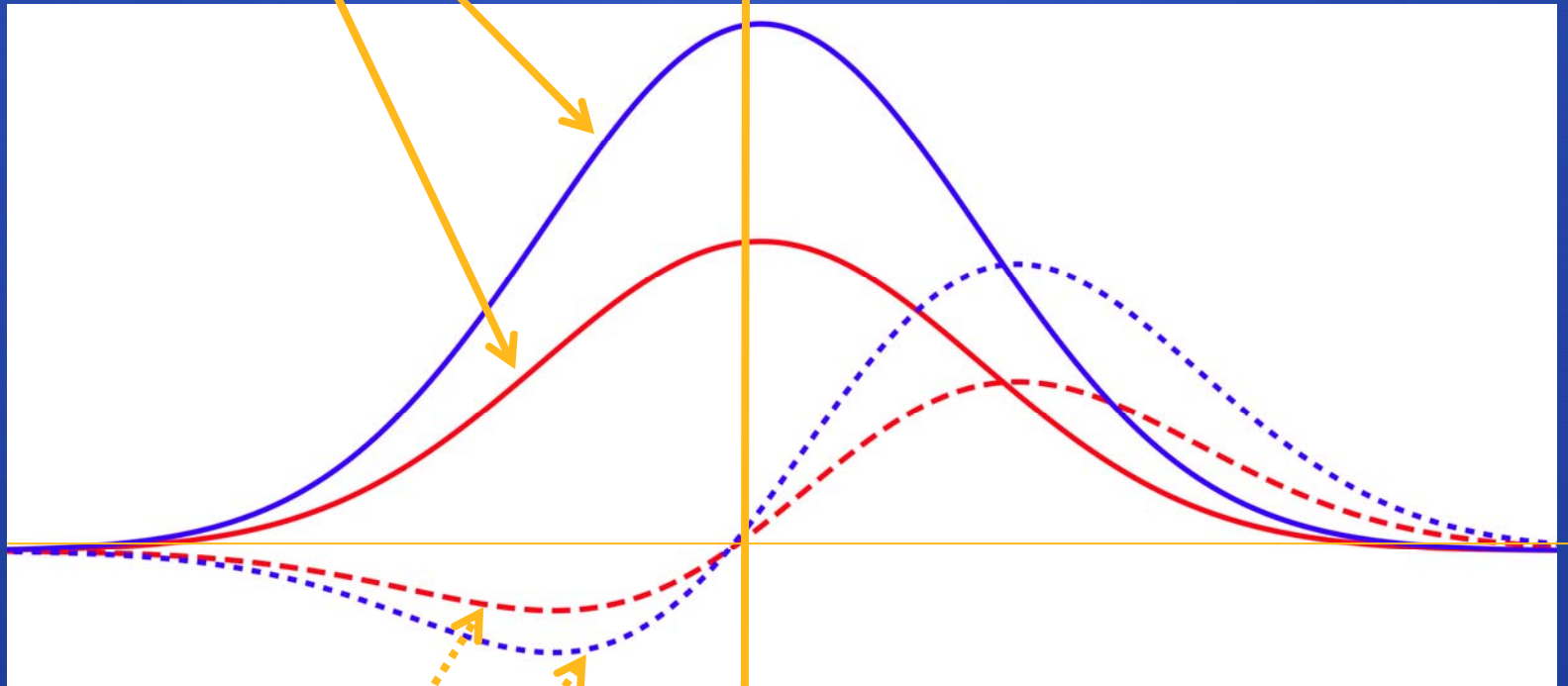


output = delayed input – attenuated input



Constant fraction discriminator

input pulse large/small amplitude



output = delayed input – attenuated input



Demonstrator



Demonstrator options

- TDC
 - On-pixel TDC -> Dual Slope TDC
 - Off-pixel TDC -> Delay locked loop (DLL) based TDC
- Time-walk
 - Time-over-threshold discriminator
 - Constant fraction discriminator (CFD)



Demonstrator

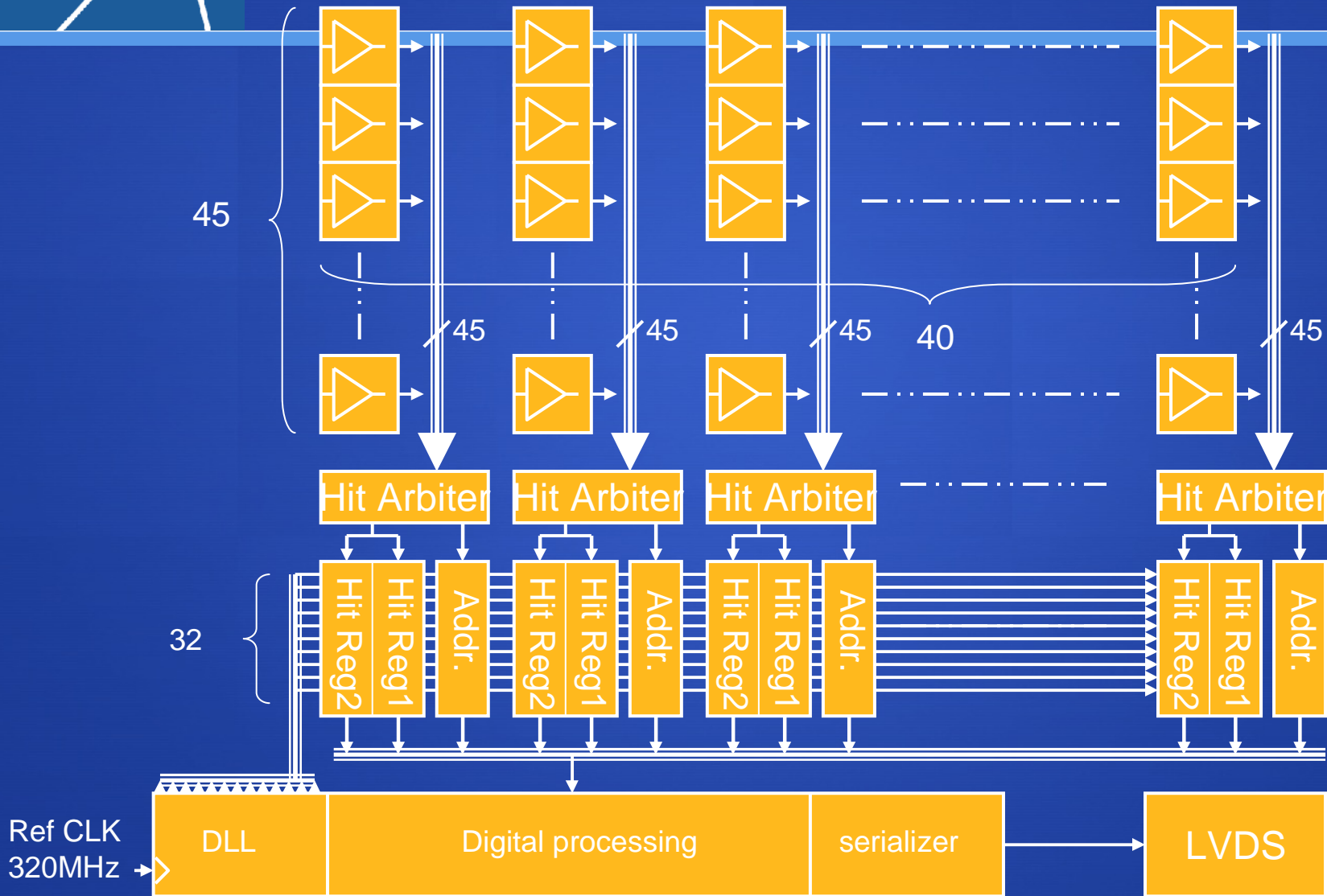
- On-pixel, dual slope TDC with CFD time walk compensation
- Off-pixel, DLL based TDC with time-over-threshold compensation
- 2 demonstrator ASICs
 - 45 pixel - folded column with full frontend
 - complete TDC system
 - reduced read-out and formatting functionality



EOC column architecture

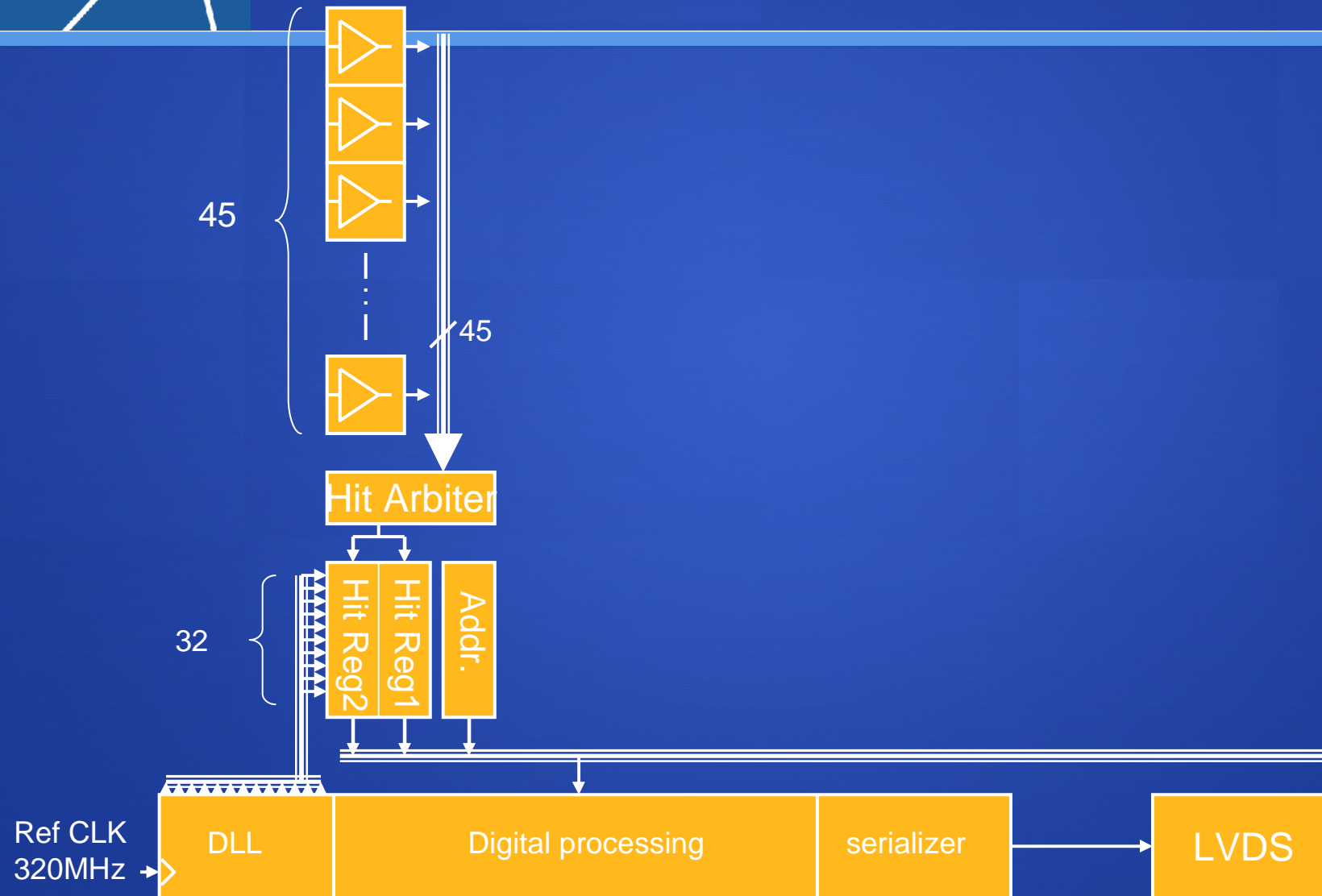


45 x 40 pixel final chip



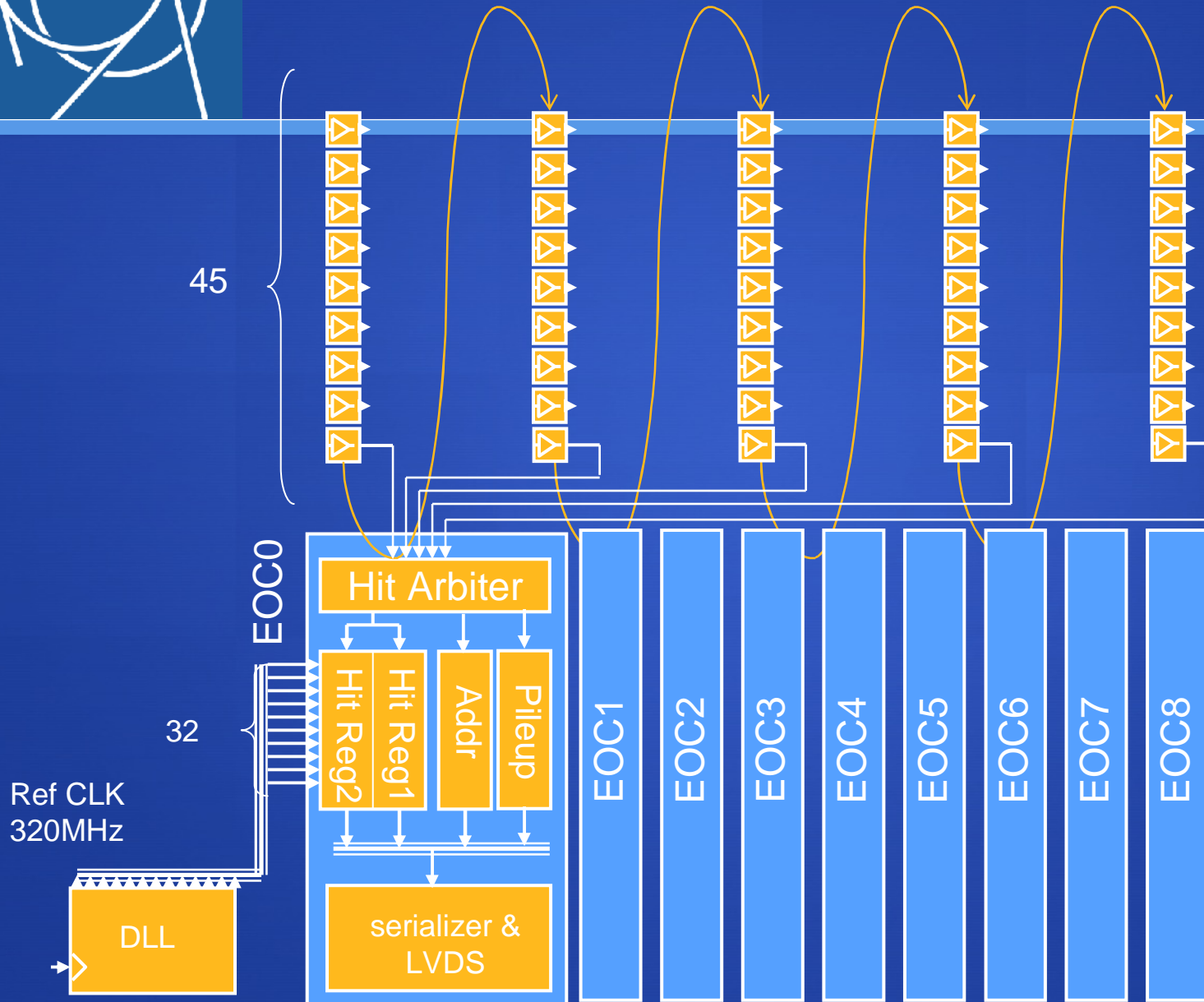


45 x 1 demonstrator



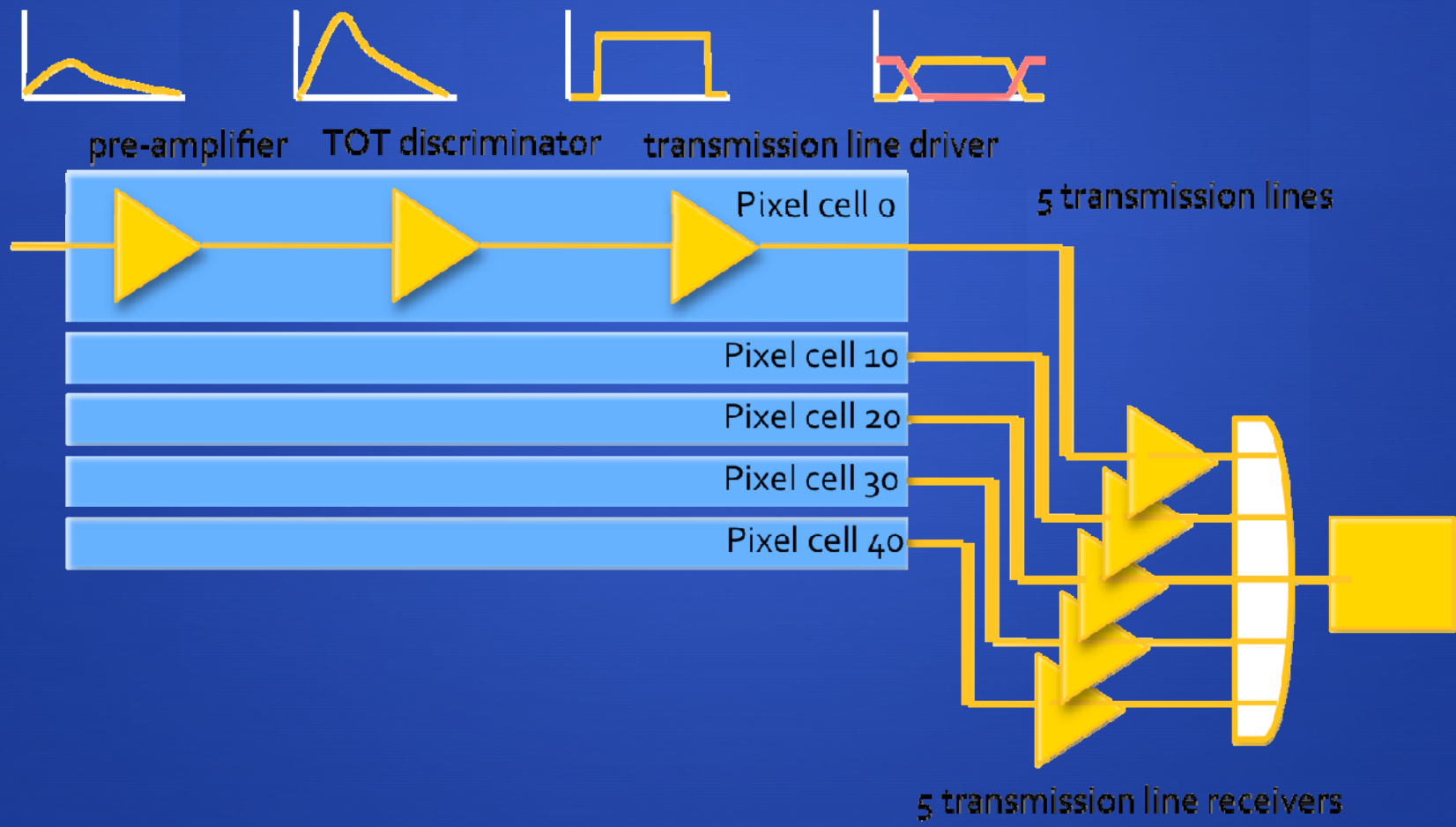


45 x 1 demonstrator



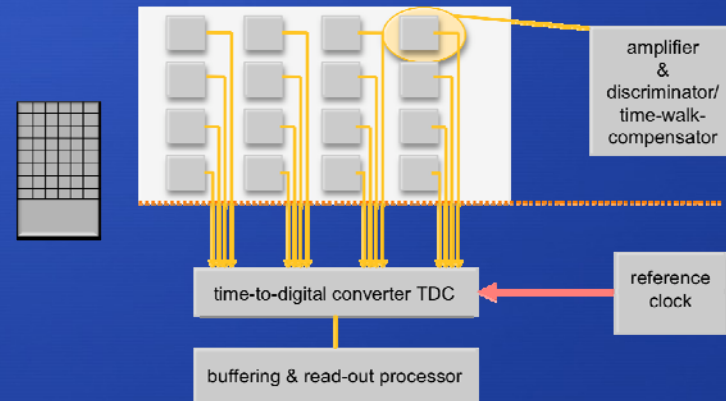
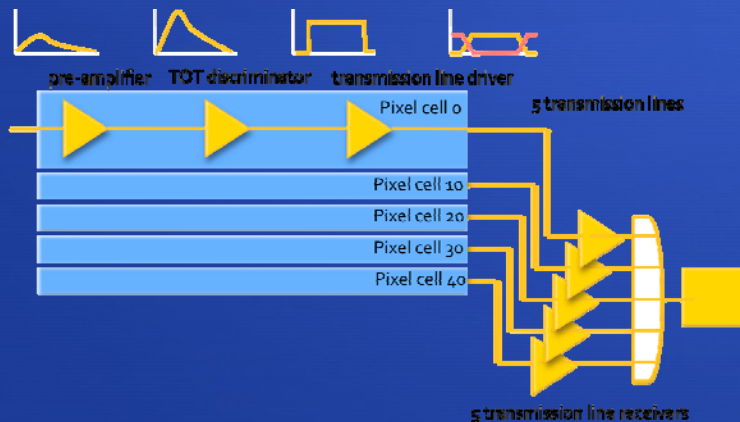
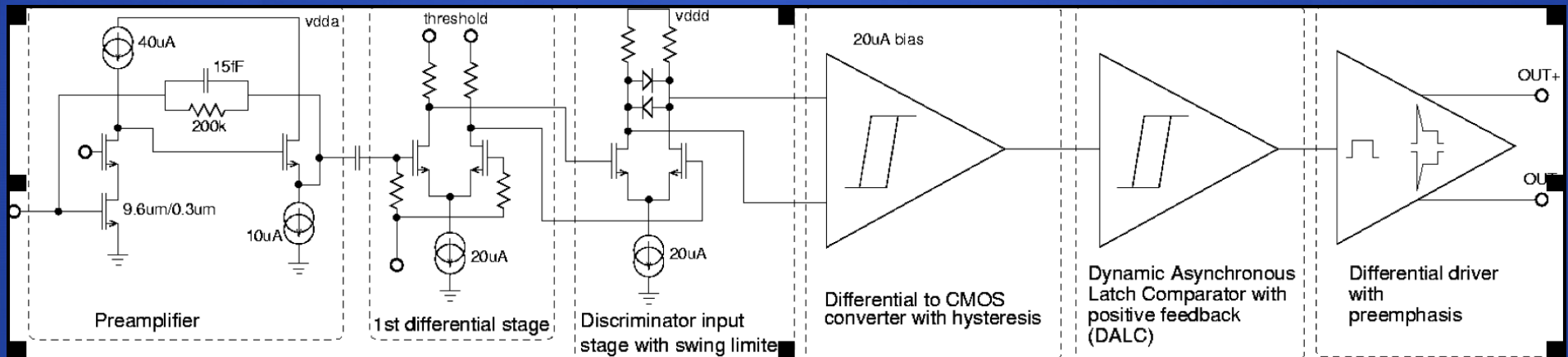


Pixel cell frontend



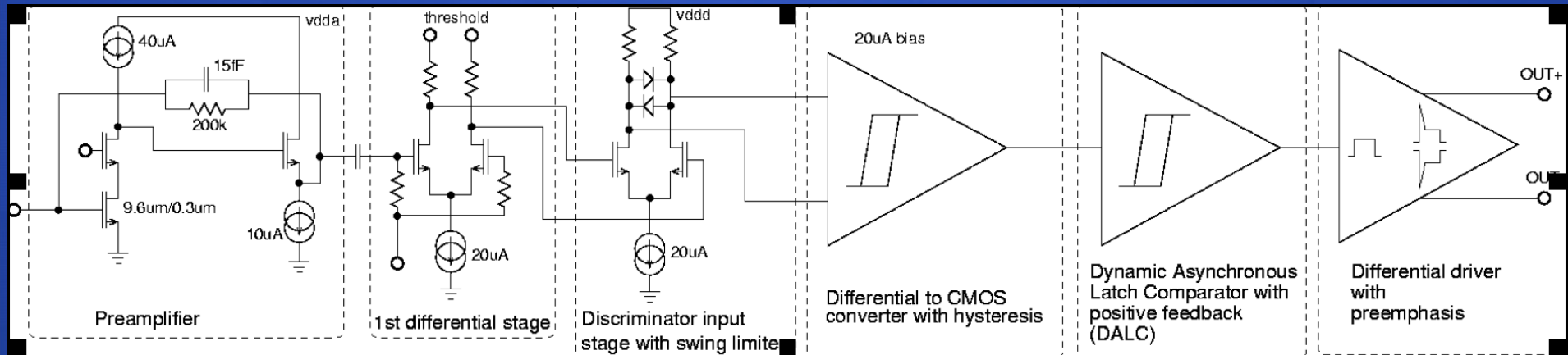


Pixel cell frontend





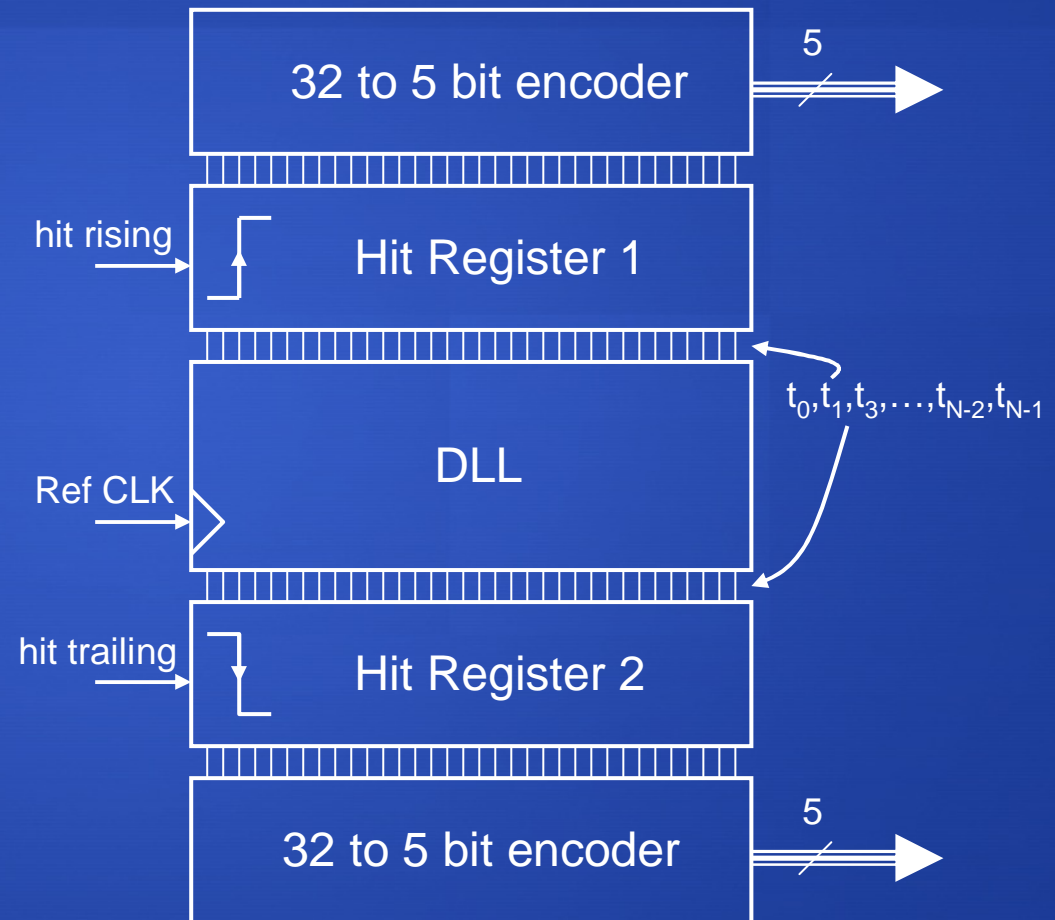
Pixel cell frontend



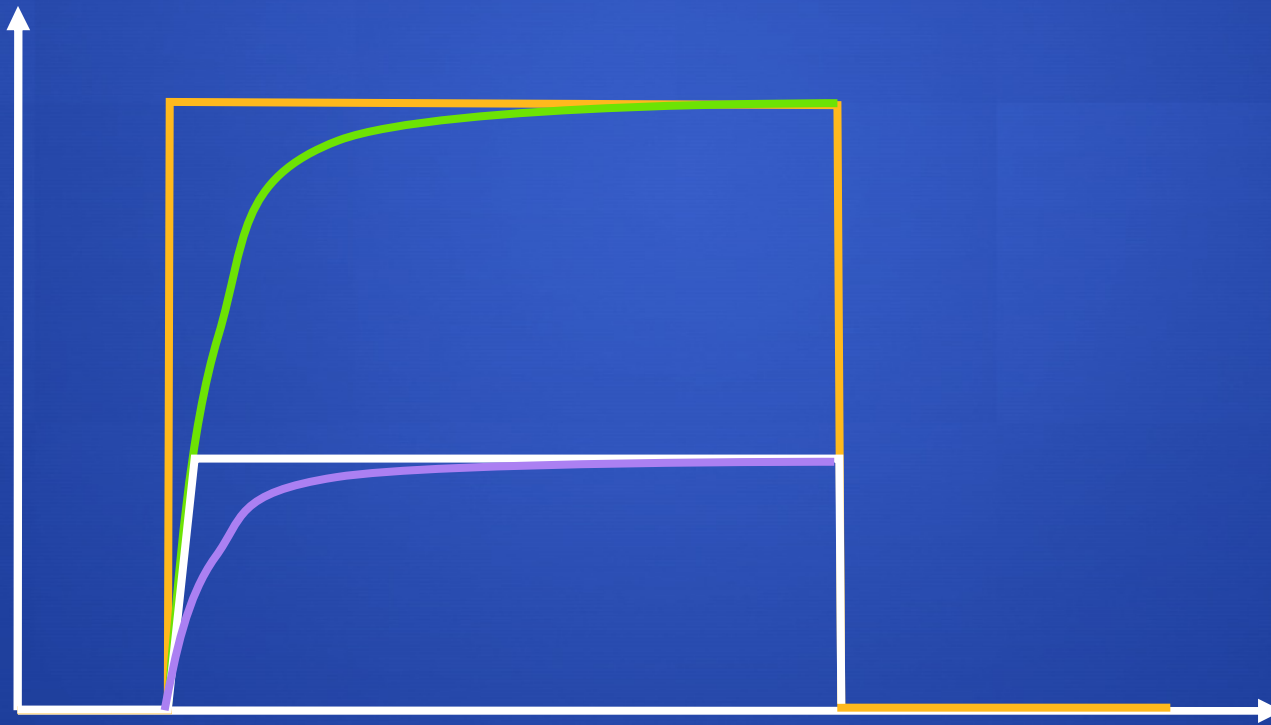
- Preamp; buffered cascode (NMOS input transistor), resistive feedback (200k)
- Gain; 70mV/fC (25mV/fC at preamp output)
- Preamplifier AC coupled to shaper and discriminator stages
- Consumption; 190 μ A/pixel (70 μ A in analog section, 40 μ A digital part of comparator, 80 μ A line driver)

Time to Digital Converter

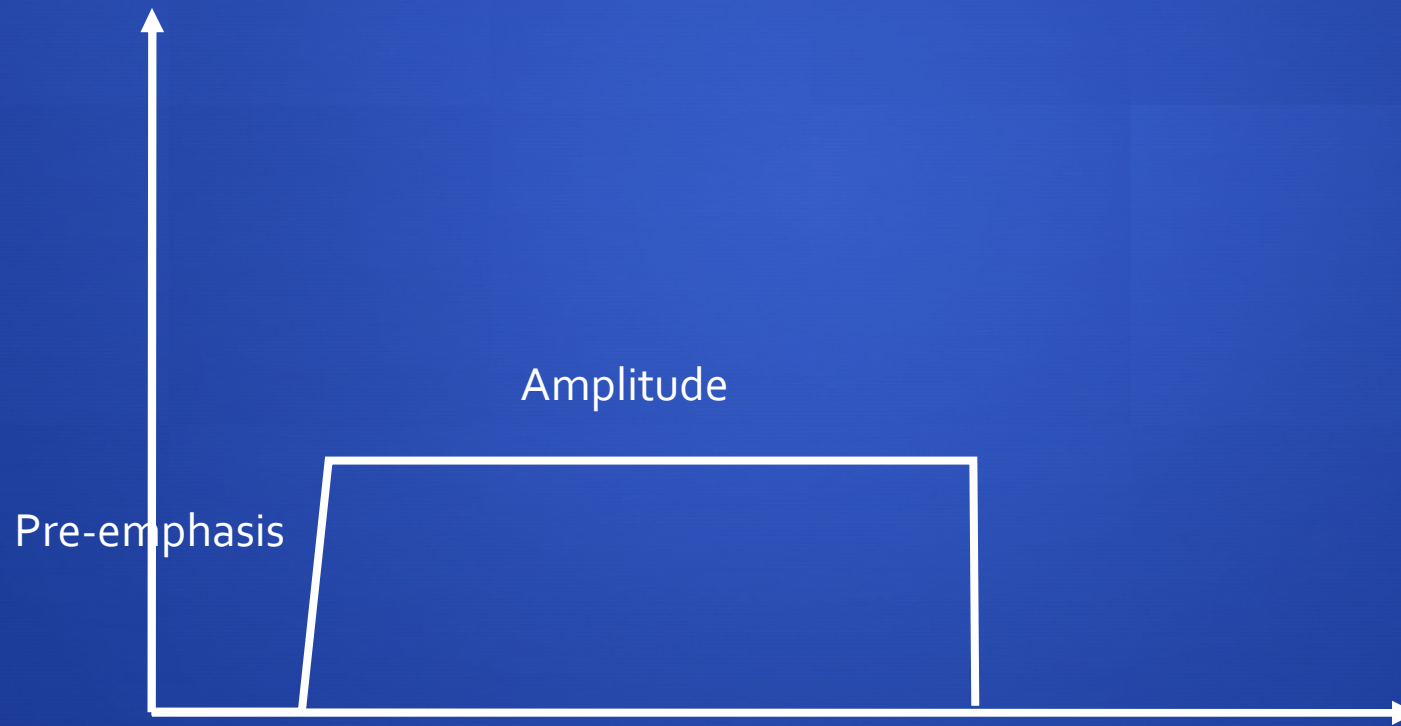
- Tapped delay line
 - 32 cells, 100ps
- Two hit registers
 - One per both leading and trailing edge
- 5 bit encoding



Optimisation of transmission line drivers – pre-emphasis

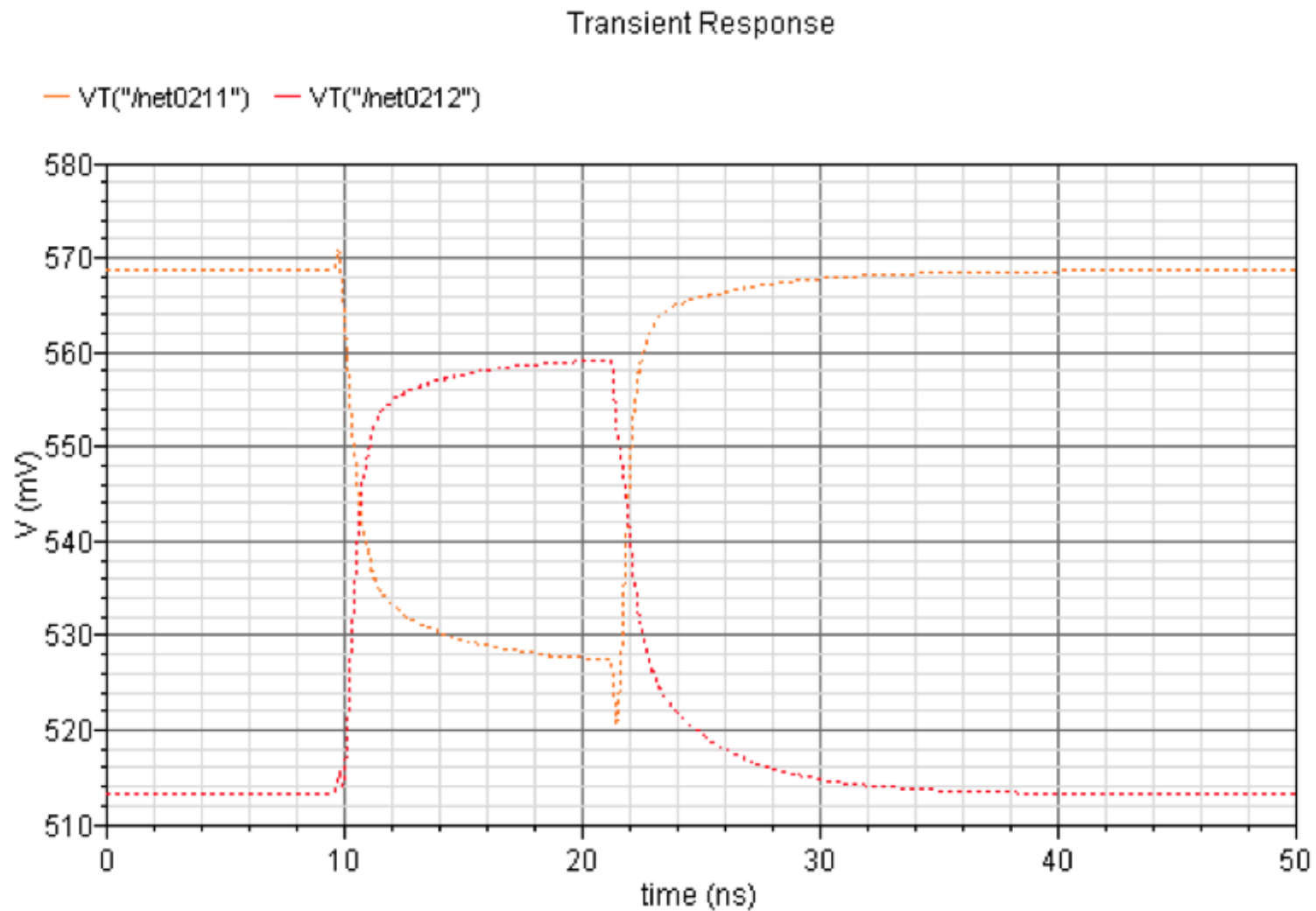


Optimisation of transmission line drivers



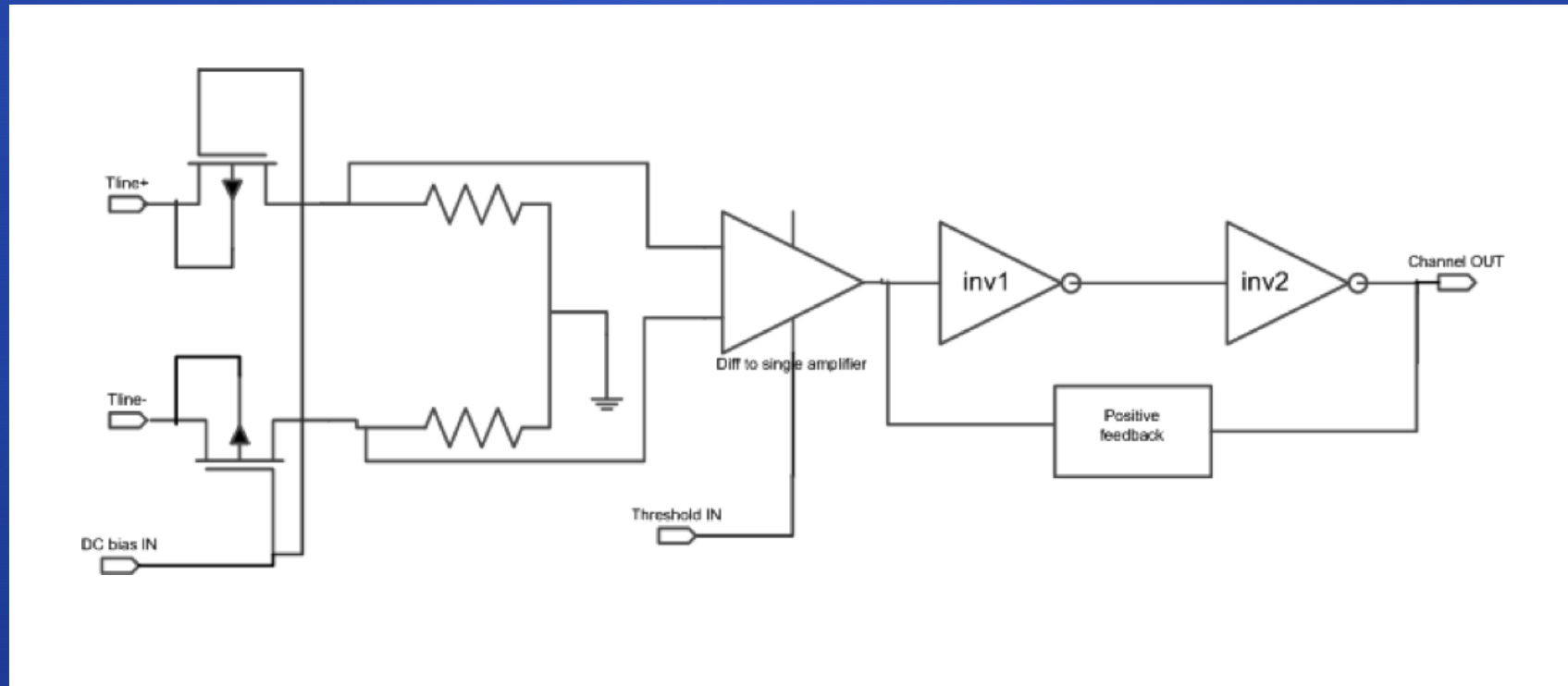


Transmission of pixel hit





Transmission of pixel hit



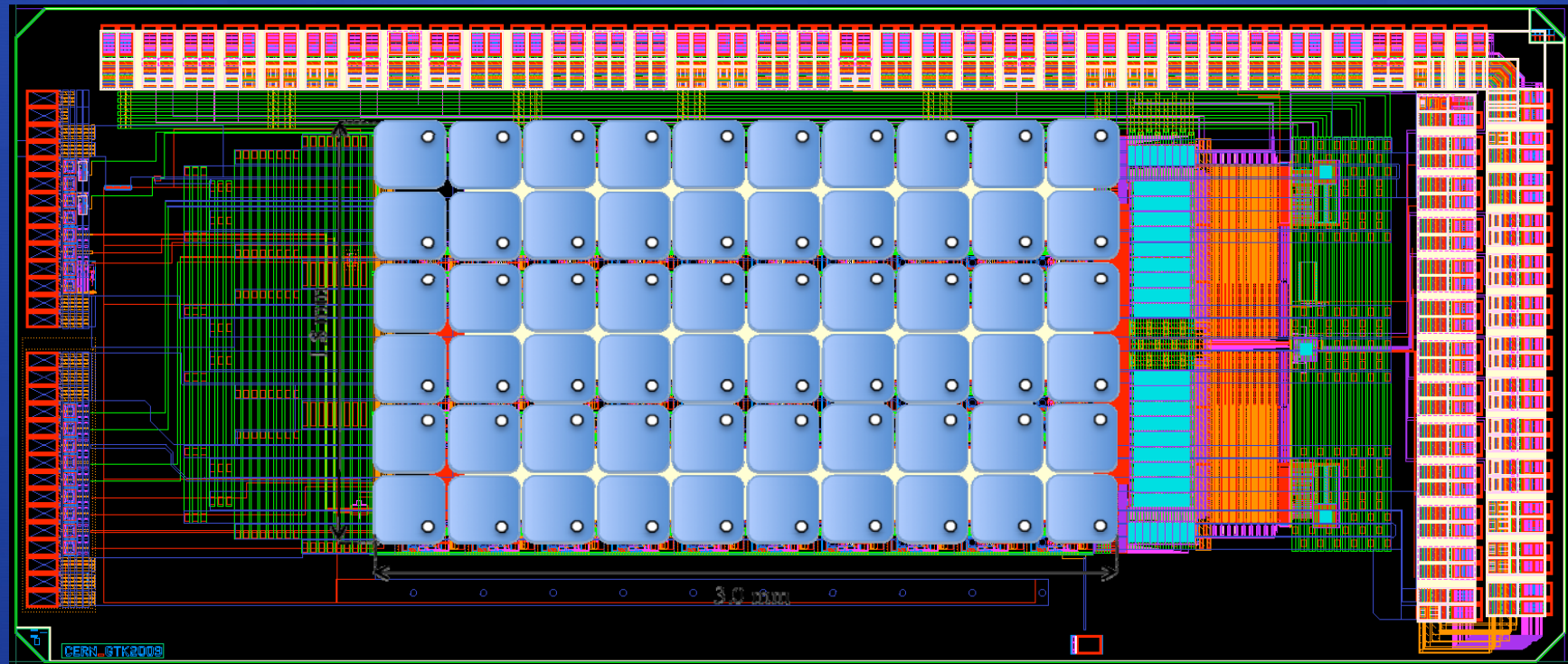


hit Arbiter

- **Aynchronous latch logic which**
 - **defines first arriving pixel hit out of 5 in one group**
 - **latches hit address unambiguously**
 - **during time-over-threshold time + TDC acquisition time: ~ 10 ns, address of additional (piled up) hits in same pixel group is stored**



Layout – EOC 130 μ m



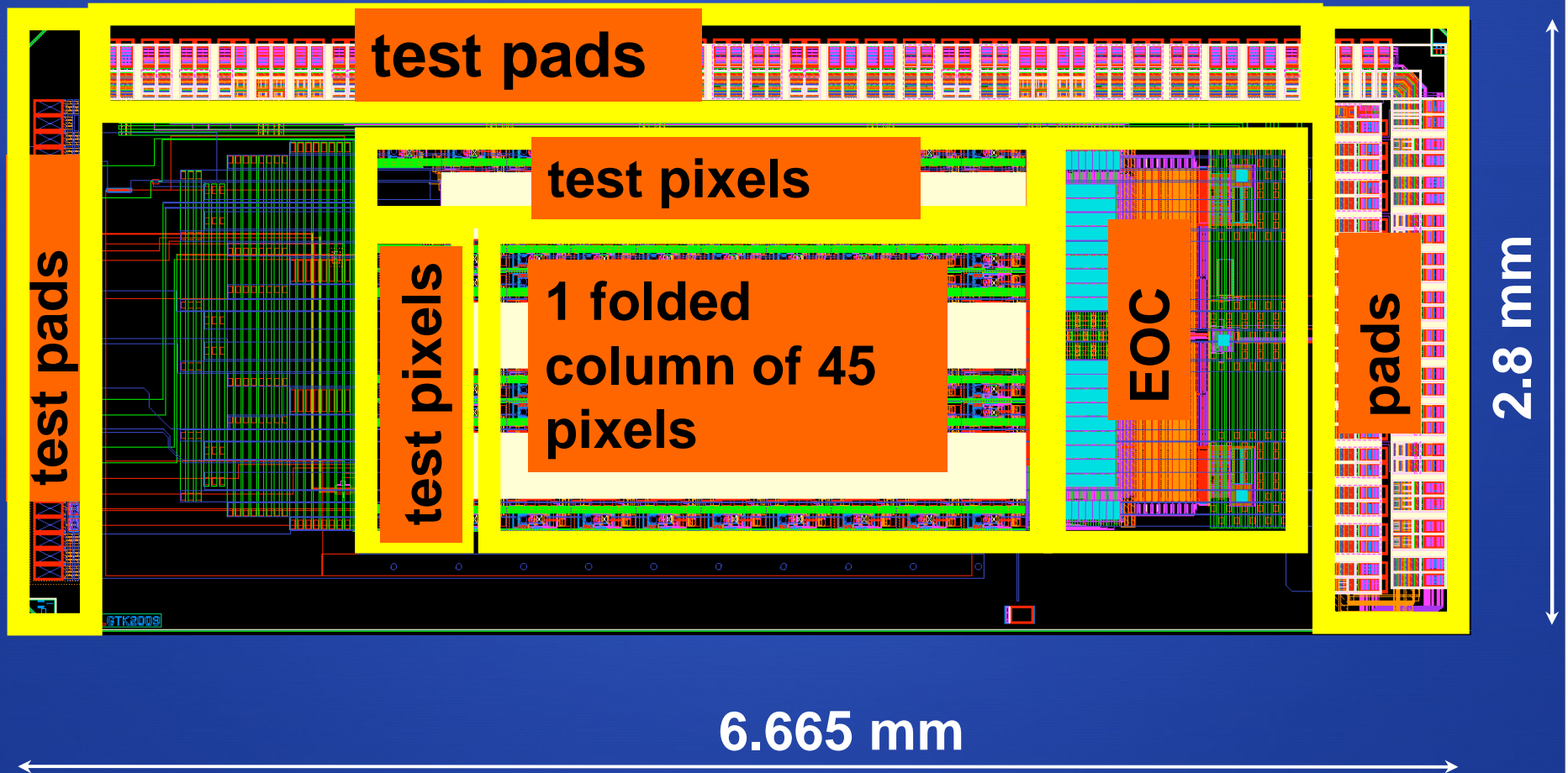
2.8 mm

6.665 mm

A. Kluge

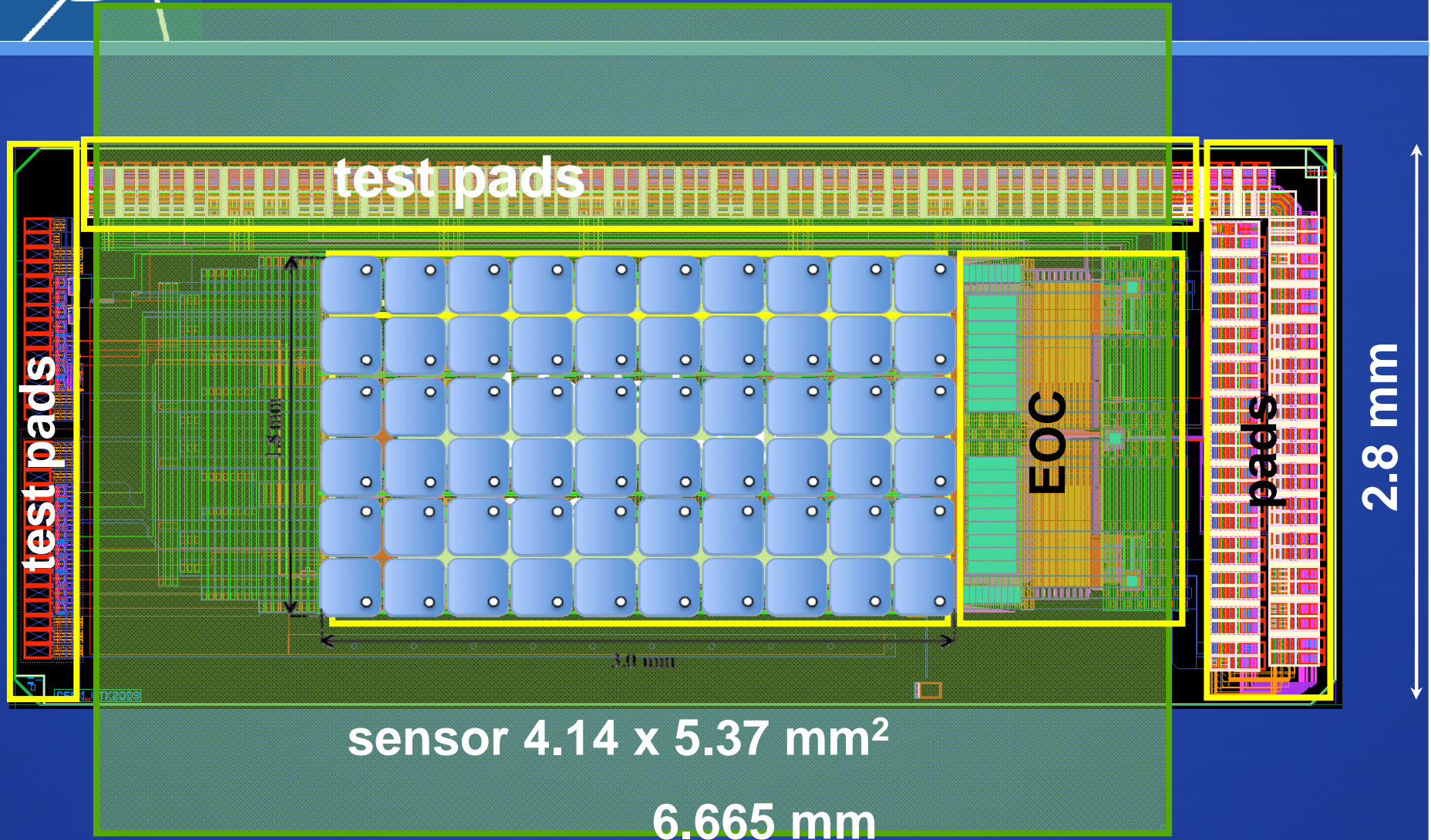


Layout – EOC 130 μ m





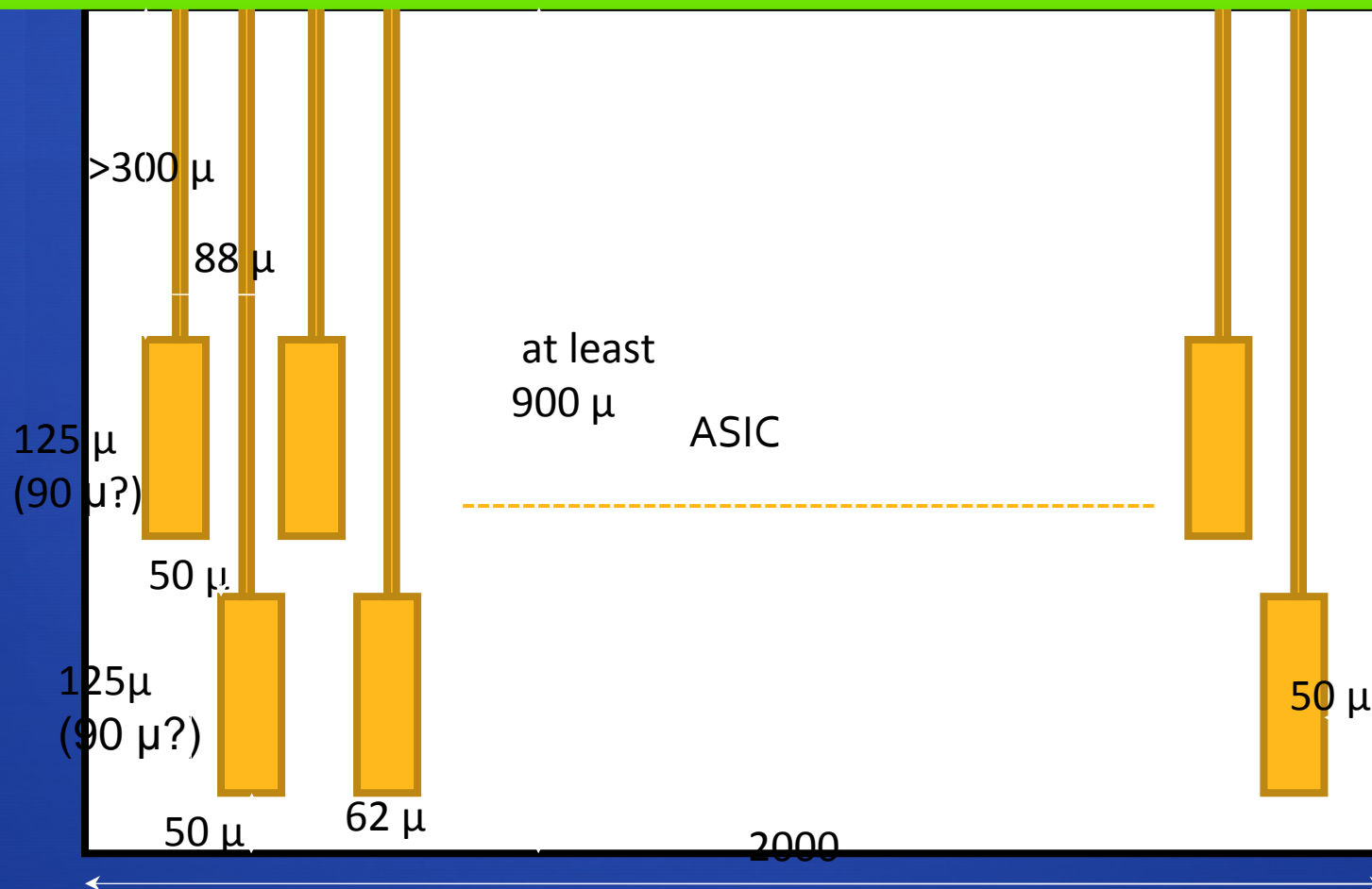
Layout – EOC 130 μ m





2 rows ASIC pads layout

Sensor edge



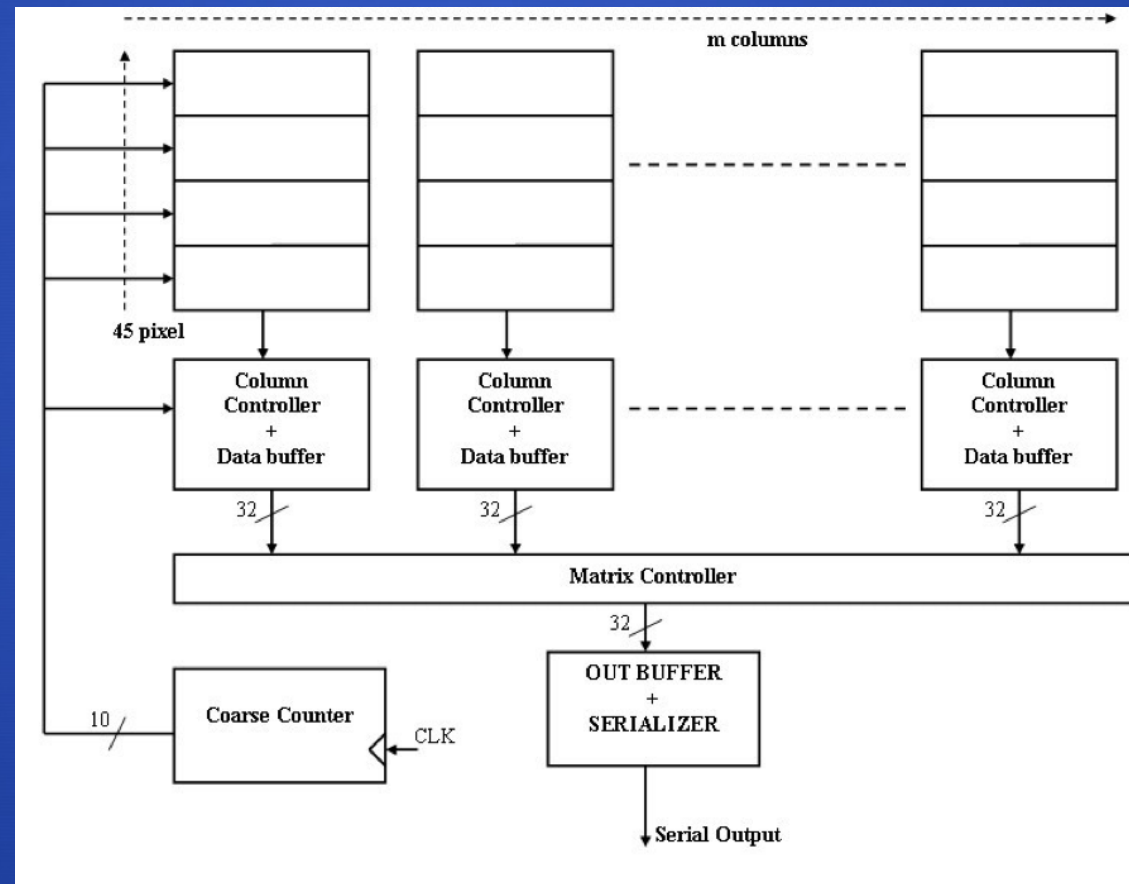


End of Column

- Time walk compensation using time-over-threshold
- Transmission of pixel with shielded wave guides on chip and optimized transmitter receiver pair
- Hit arbitration allows high efficiency and low number of TDC registers

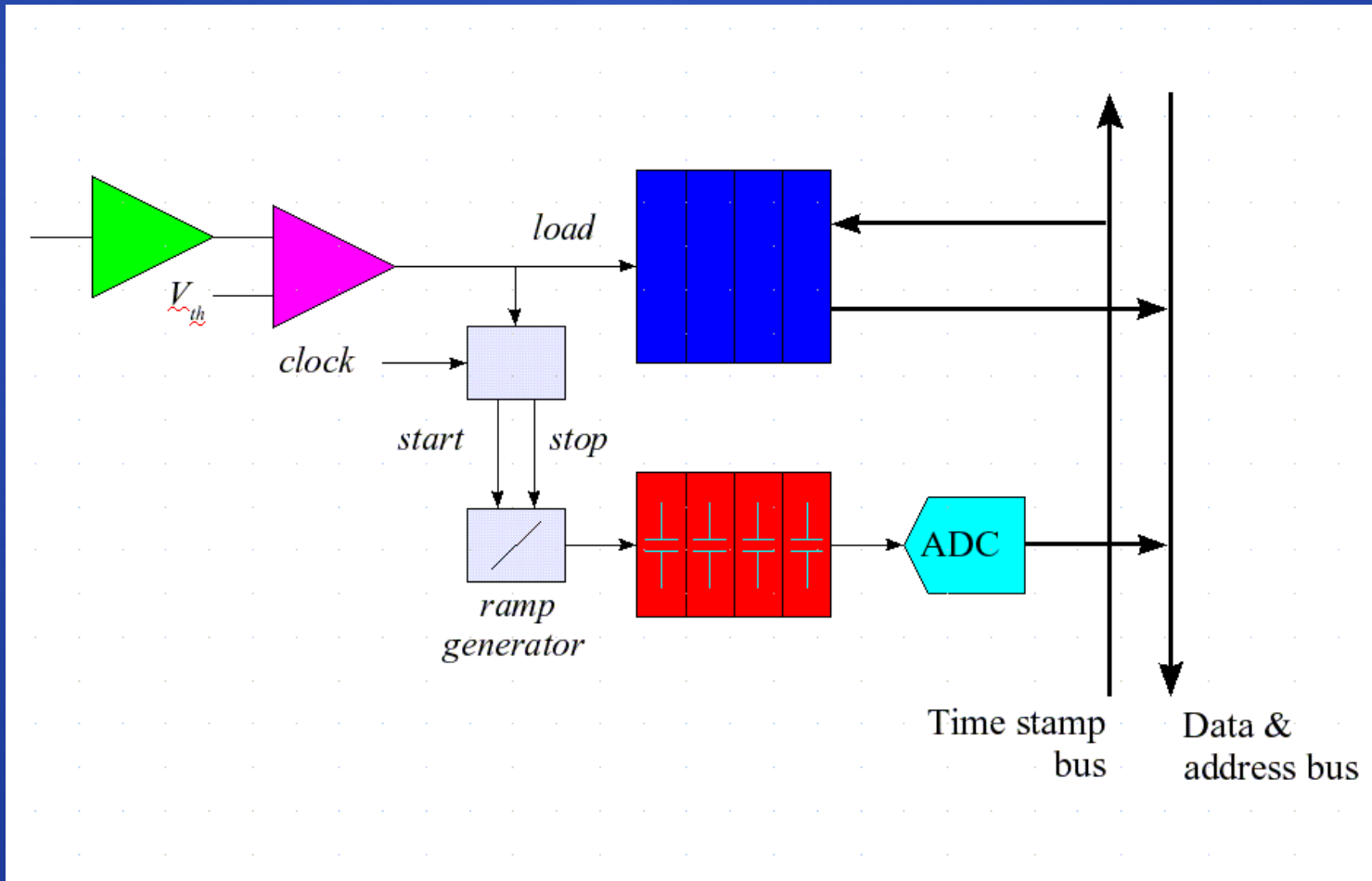


TDC per pixel architecture



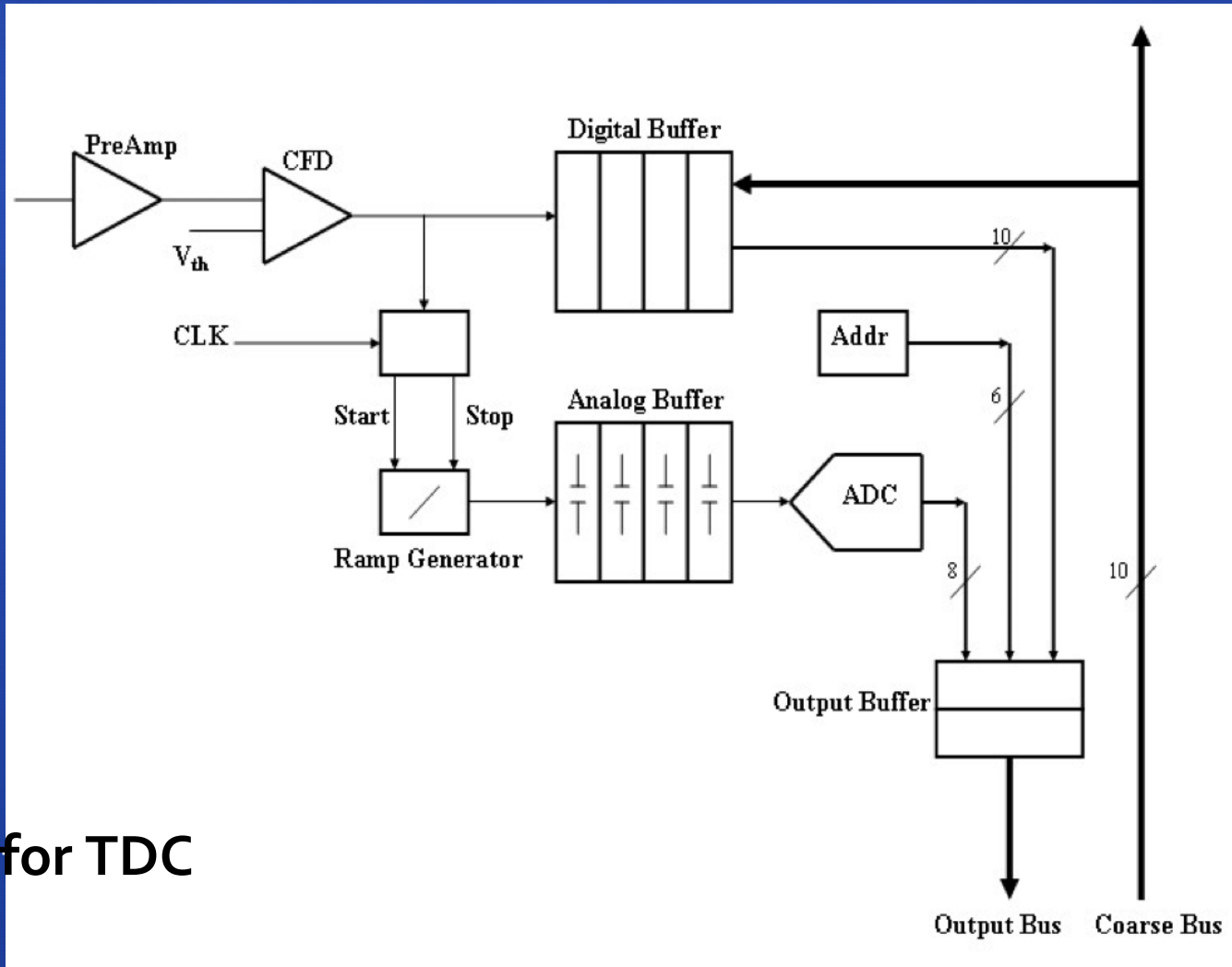


On pixel cell TDC





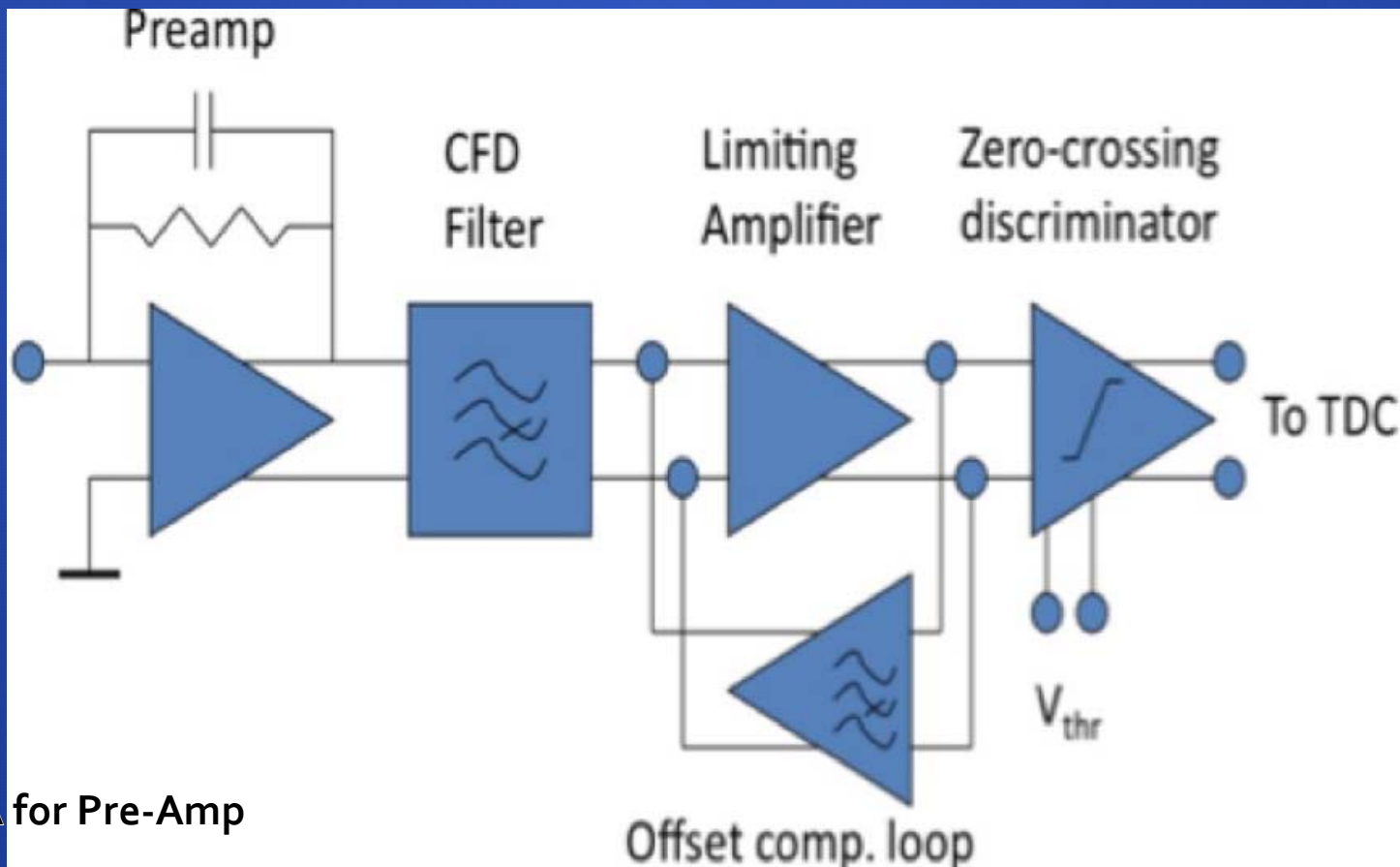
On pixel cell TDC



- 135 μA for TDC



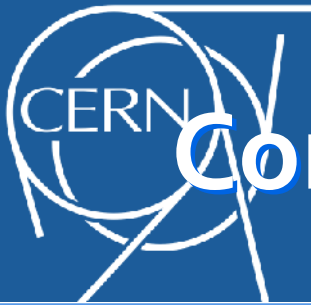
Constant fraction discriminator



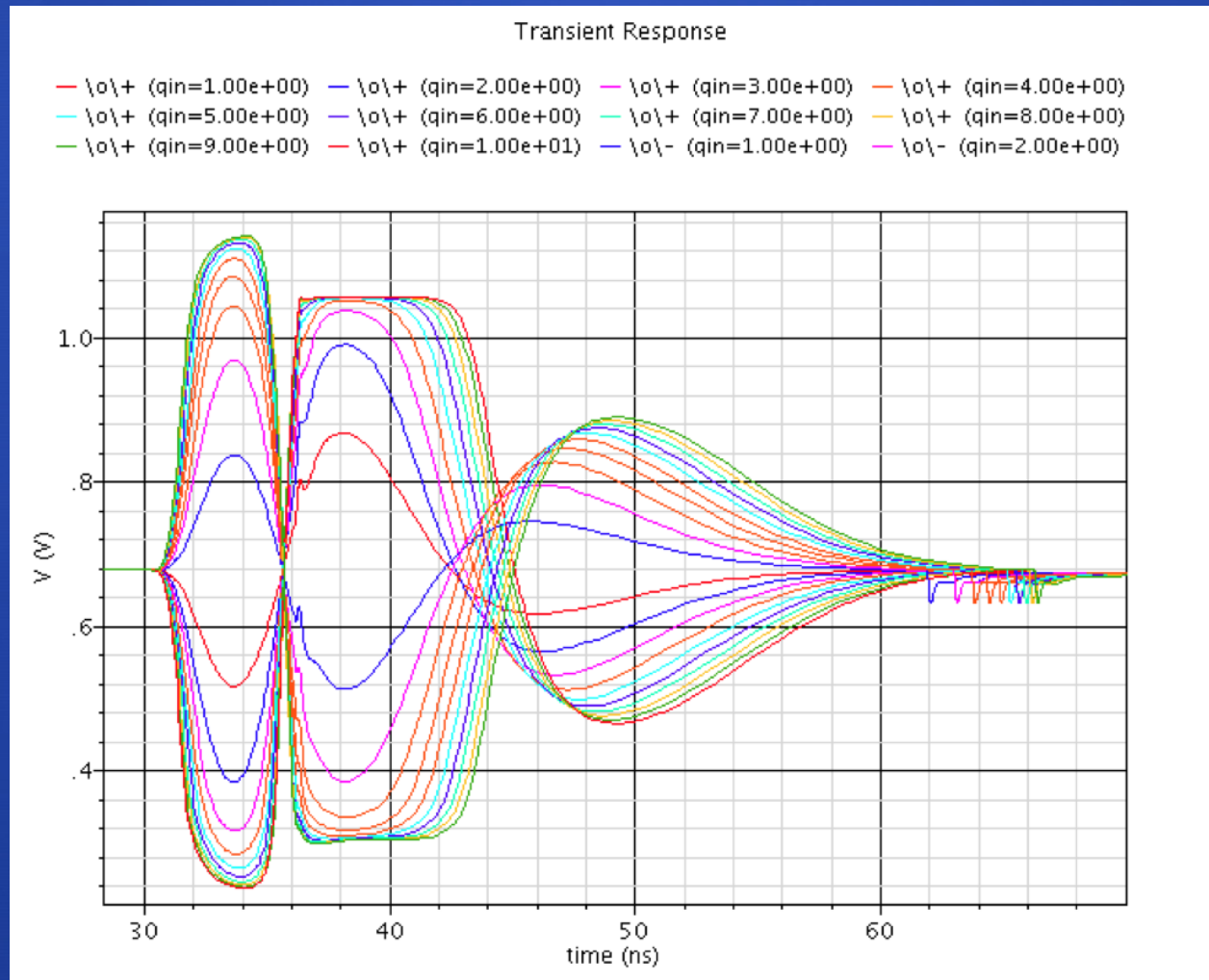
- 250 μA for Pre-Amp

- 500 μA for CDF

A. Kluge



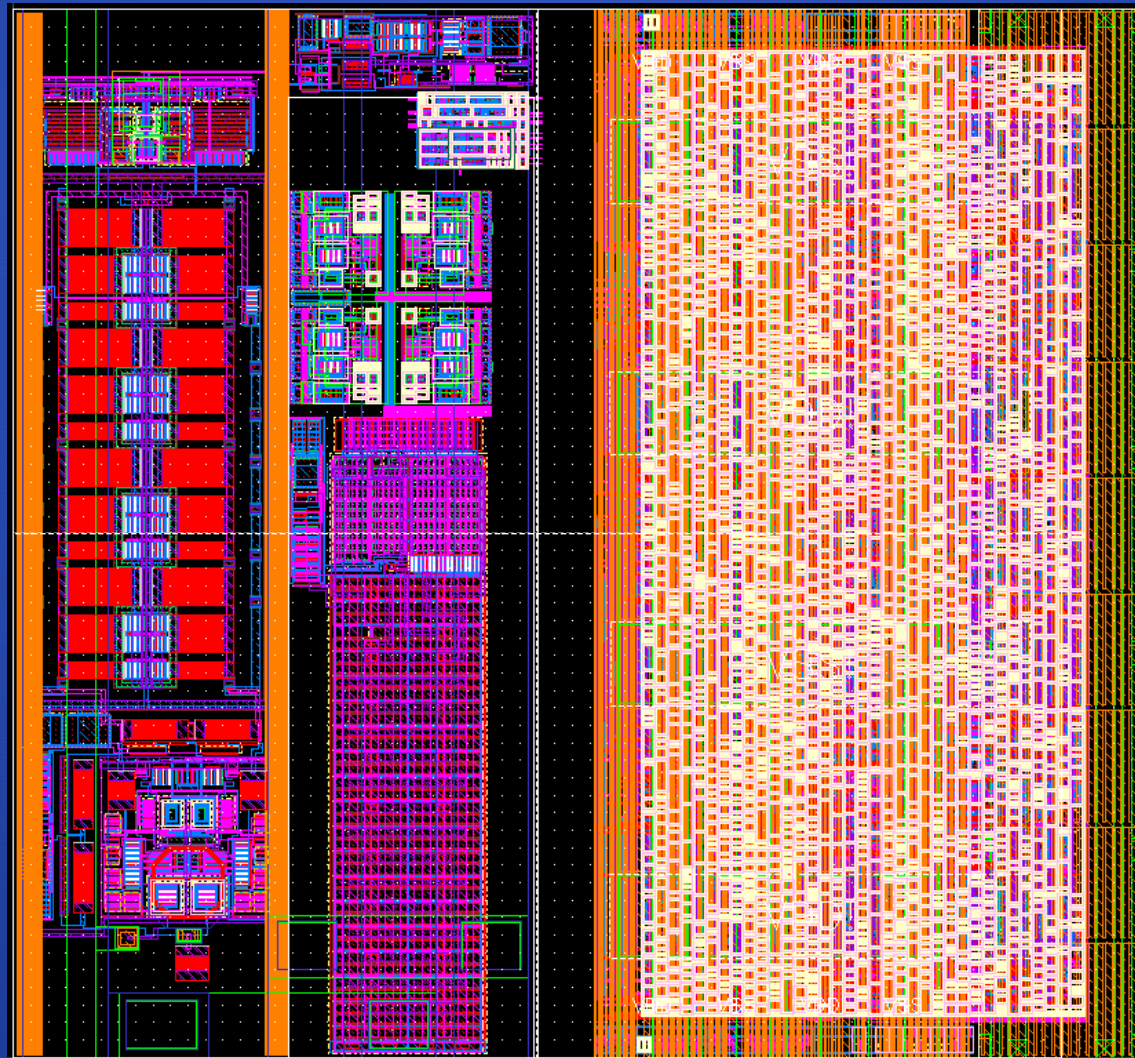
Constant fraction discriminator





Layout – on pixel TDC

130 μm





TDC per pixel

- Time walk compensation using constant fraction discriminator
- Transmission of clock with clock buffer pipeline
- In pixel cell buffers allows high efficiency



Summary

- 300 x 300 μm^2 , 100 ps pixel detector for NA62 GigaTracker
- Specifications challenging, demanding integration
- Specifications on material budget, cooling and time stamping => future, linear collider, fixed target, particle time tagging
- high data bandwidth, triggerless
- 2 Prototypes submitted
- options to be evaluated in demonstrator ASICs



- thanks