



**The Abdus Salam  
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**2132-5**

**Winter College on Optics and Energy**

***8 - 19 February 2010***

**Wafer Silicon Technologies**

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# **Wafer Silicon Technologies**

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  - Overview of PV technology
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  - High-efficiency Devices
  - New silicon sources

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# **Overview of PV technology**

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# What would we like to happen.....

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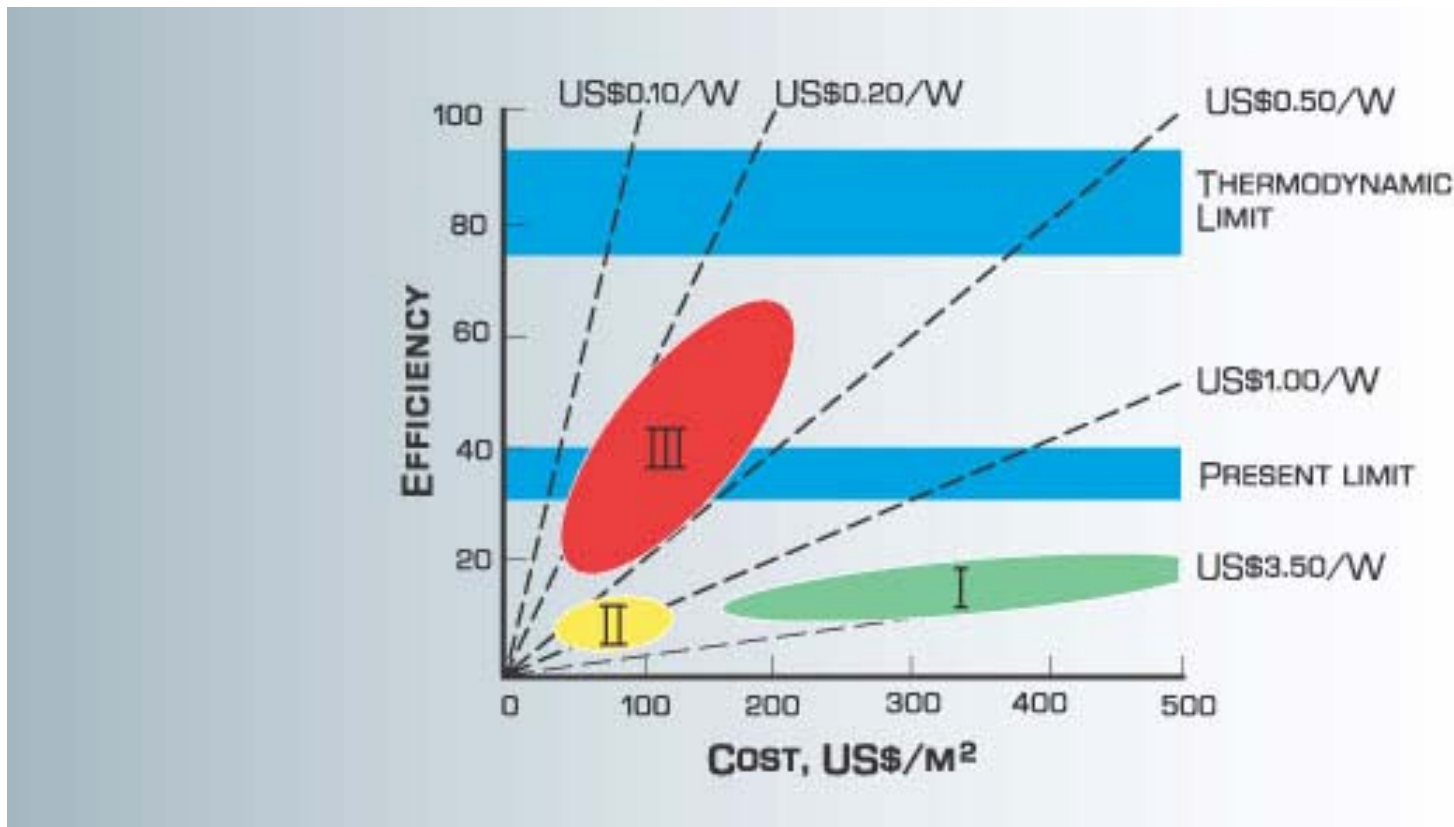
- PV to be affordable to all (and ubiquitous)
- PV to be much more efficient (for convenience)
- PV (along with wind, hydro and improved storage) to be significant part of a zero carbon economy)

## In reality:

- **PV needs to be commercially viable! (grid parity)**
- **We need to move away from subsidy and dependence on government policy**
- Inefficient factories/technologies will close (customers will become more discerning)
- Brand names (of companies and device types) will become important (PV industry will be comparable to car industry - there will be Rolls-Royce and AA)

# 3 “Generations” of PV

- Martin Green suggests 3 Generations of PV based on efficiency and cost



(M.A. Green, Prog. Photovolt: Res. Appl. 2001; 9:123-135)

# 3 “Generations” of PV

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## First Generation:

- Silicon wafer devices
- 10 to 20% efficient, expensive

## Second Generation:

- Thin film devices
- 5 to 10% efficient, cheap
- **Devices will become ubiquitous**

## Third Generation:

- Multi-junction devices (+other conceptual schemes)
- 20 to 60% efficient, expensive
- **Devices will become convenient**

# 3 “Generations” of PV

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## **First Generation:**

- Where we are now (70%)
- no grid parity

## **Second Generation:**

- Where are going (now 30%)
- approaching grid parity

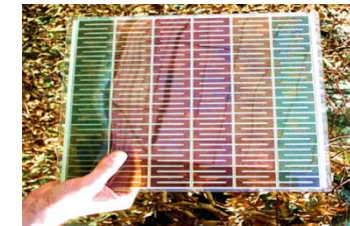
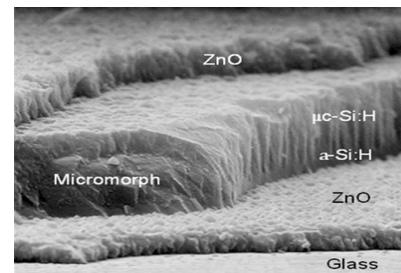
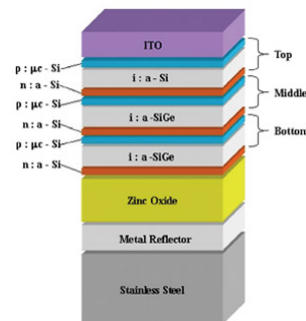
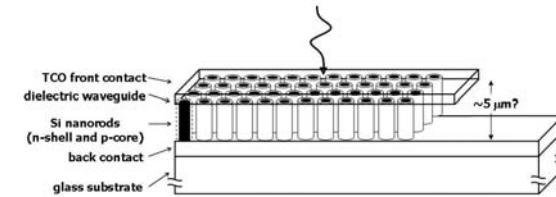
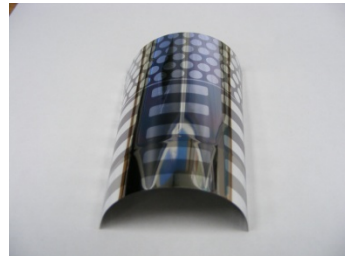
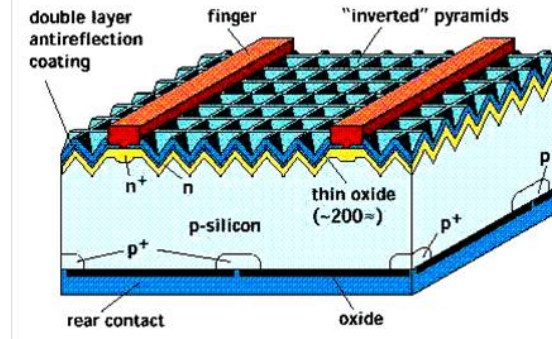
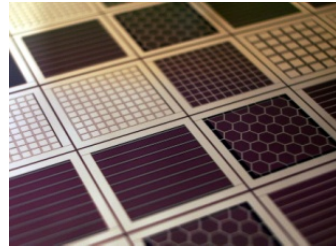
## **Third Generation:**

- Thin film devices
- (20 to 60% efficient, expensive)

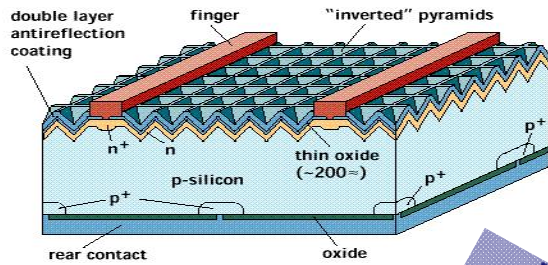


# Technologies

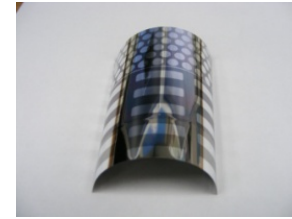
## “device technologies”



# Emerging Trends



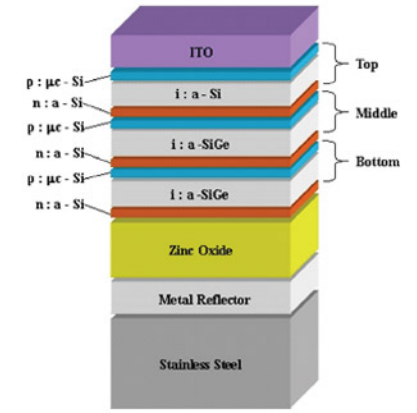
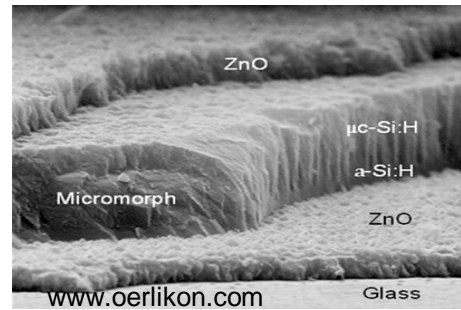
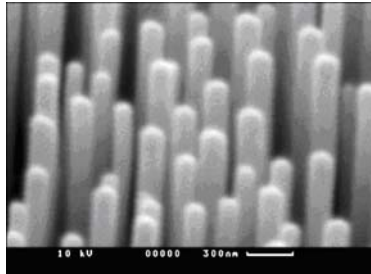
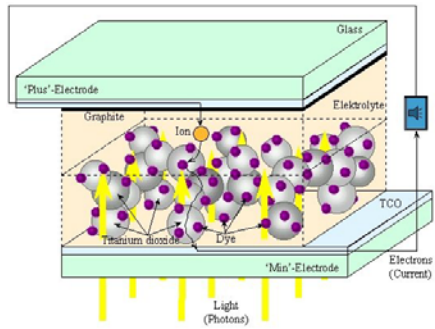
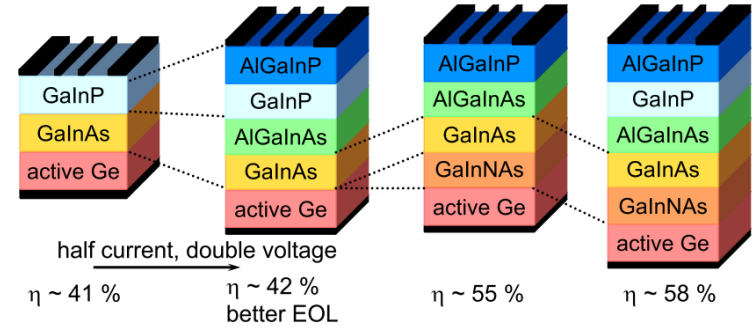
**Flexible Substrates** →



**Multi-junction (3G)** →

**Bulk hetero-junctions** ↓

**Thin film multi-junctions** ↘



# 3 “Generations” of PV

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## **First Generation:**

“Wafer Silicon Technologies” (me, now)

## **Second Generation:**

“Thin Film technologies” (me, at 5.00pm)

## **Third Generation:**

“High efficiency solar cells and 3<sup>rd</sup> Generation Concepts”

(Prof. Jenny Nelson – tomorrow at 9.00am)

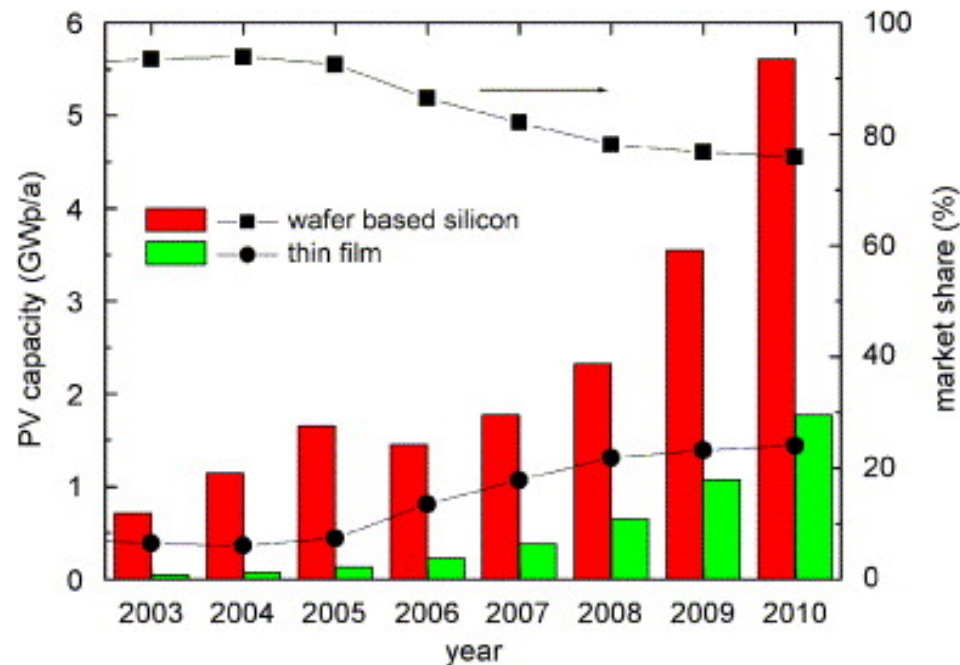
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# **Silicon Wafer Technologies**

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# Market Share

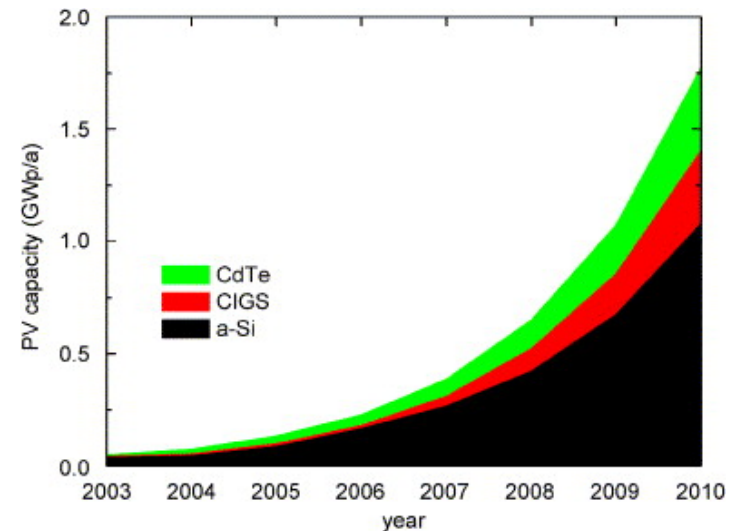
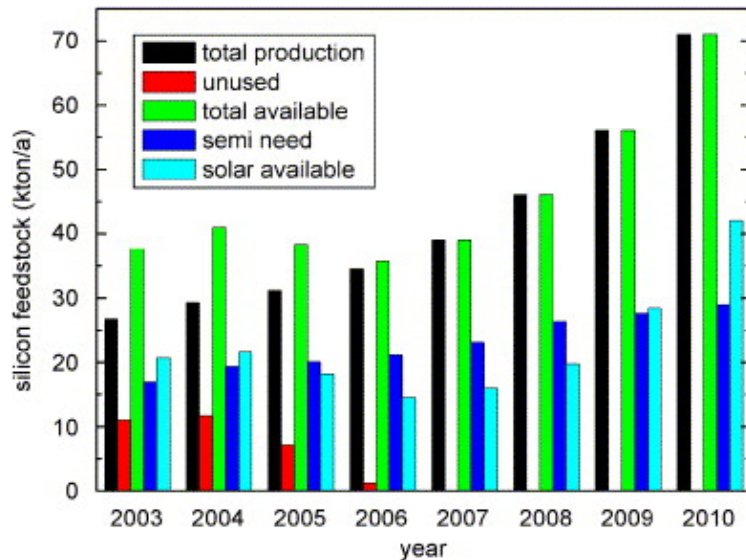
- The last few years have seen an unprecedented boom in PV production and installation
- C-Si and mC-Si remain the most important (80%) but thin film technologies are increasing market share



W.G.J.H.M. van Sark et al, Energy policy, [Volume 35, Issue 6](#), June 2007, 3120

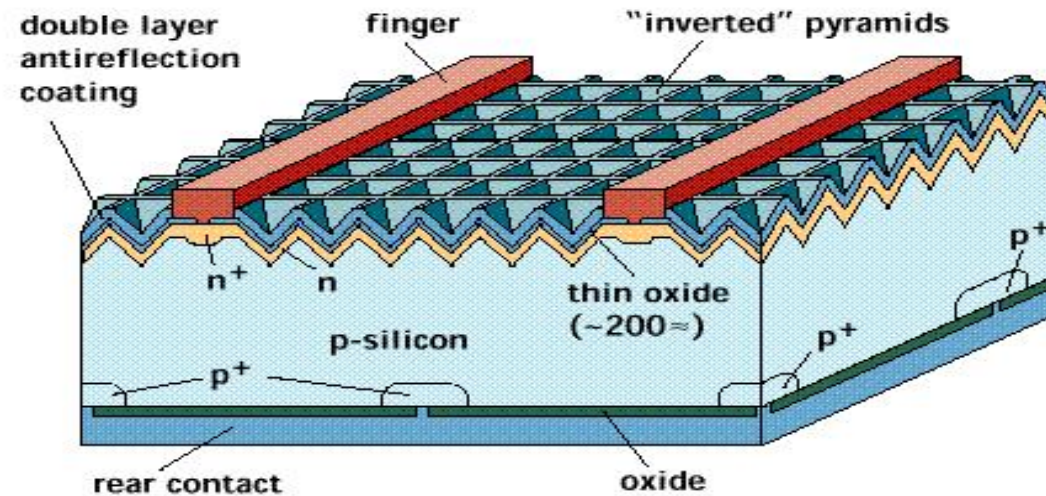
# Feedstock

- Until recently, increase in thin film technologies were largely due to shortage of wafer silicon
- More recently, CdTe (First Solar) has gained significance as first 1\$/W technology



(van Sark *et al*, Energy policy, Volume 35, June 2007, 3120)

# Silicon Wafer Devices

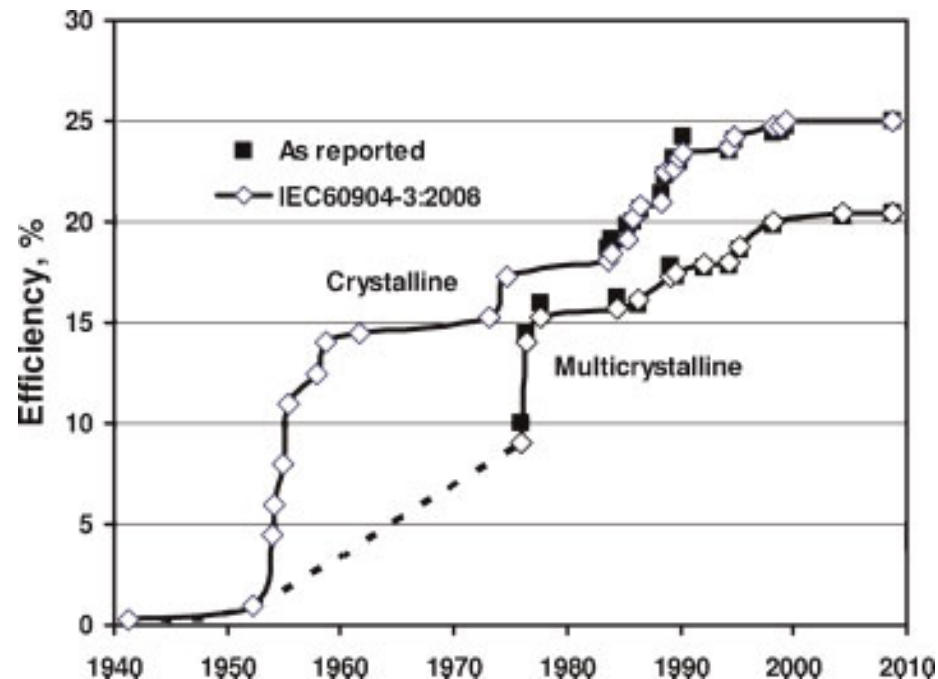


(M.A. Green, Prog. Photovolt: Res. Appl. 2009; 17:183)

- the PERC cells is a highly optimised 25% efficient silicon wafer cell
- commercial devices are much less efficient (and much cheaper)
- we will explore the commercial technologies and some of the techniques being used to **improve efficiency** and **reduce cost**

# Silicon Wafers

- two types of wafer silicon device
- Crystalline silicon (C-Si) devices are based on **single crystal wafers**
- Multicrystalline (mC-Si) devices are based on **multicrystalline wafers**
- mC-Si lag C-Si on efficiency but are cheaper



(M.A. Green, Prog. Photovolt: Res. Appl. 2009; 17:183)



# Silicon Wafers

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- in fact, around 50% of Si PV module cost is the wafer!
- poor absorption (indirect bandgap) requires thick samples and this in turn require long carrier diffusion lengths
- long carrier diffusion lengths require, low doping, low impurities and excellent crystal structure.

**Traditionally**, high quality single crystal wafers are made by Czochralski and float-zone techniques

- The ***Czochralski method***: involves slowly drawing an oriented seed from molten silicon in a pure quartz crucible

(Zulehner W. Czochralski Growth of Silicon. Journal of Crystal Growth. 1983;65(1-3):189-213.)

- The ***float zone*** method: involves passing a molten zone of silicon along a silicon rod to produce a purified single crystal ingot

(Wolf S, Tauber RN. Silicon Processing for the VLSI Era, Process Technology. Vol 1. Sunset Beach, California: Lattice Press; 1986)

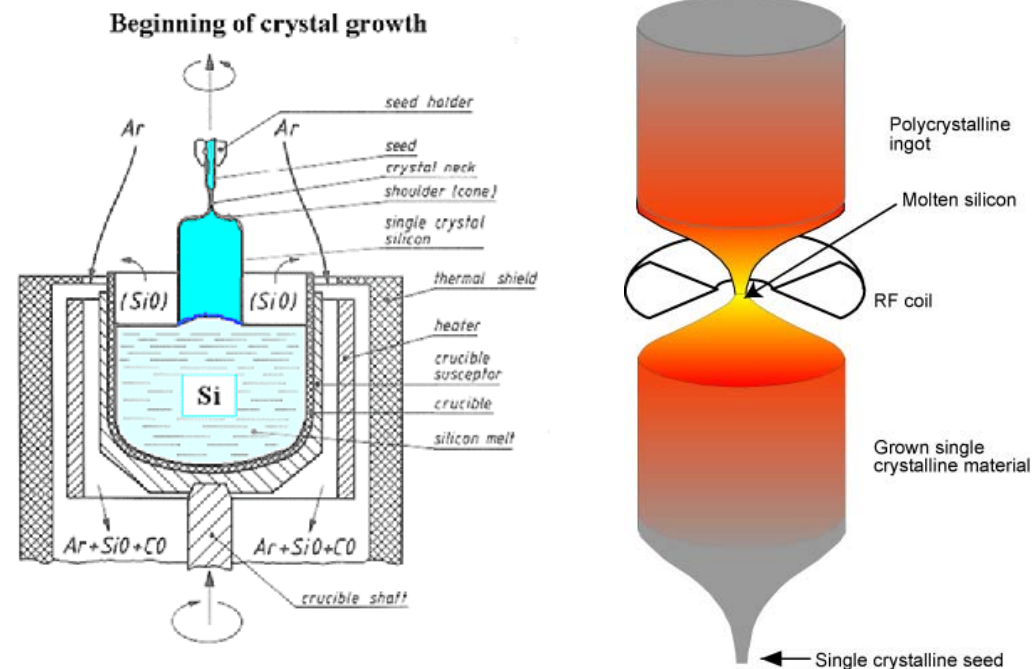
# Silicon Wafers

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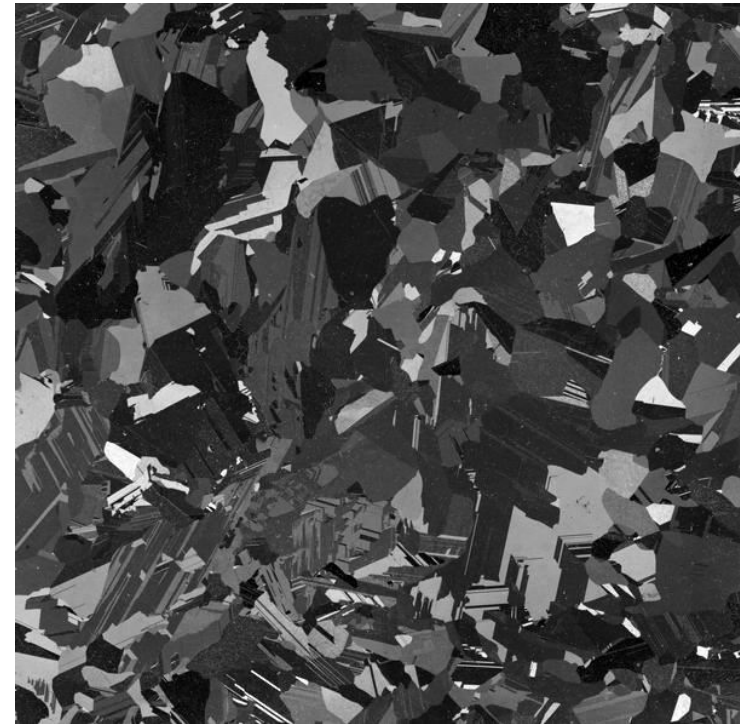
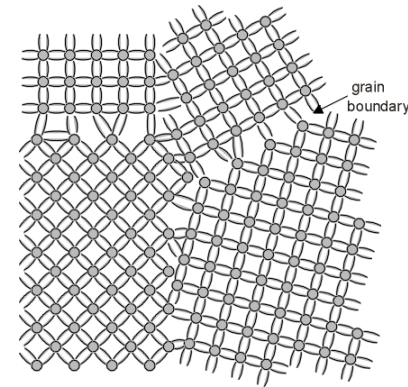
(Wolf S, Tauber RN. Silicon Processing for the VLSI Era, Process Technology. Vol 1. Sunset Beach, California: Lattice Press; 1986)



# mC-Wafers

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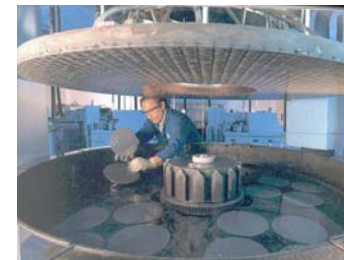
- Multicrystalline Wafers produced by careful control of recrystallization of molten silicon
- Grain boundaries are a source of carrier loss
- Large vertical grains are provided by suitable m-C cruxible/furnace conditions



# Silicon Wafer Processing

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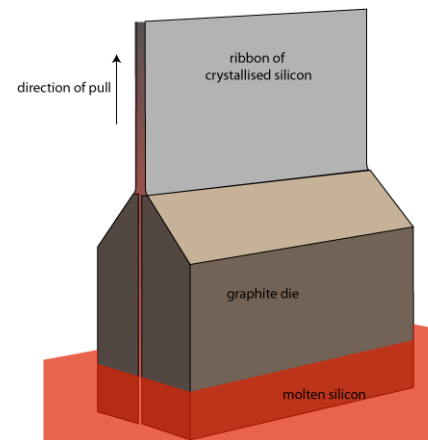
- Step 1: Obtain good sand
- Step 2: Refine ( $\text{SiO}_2 + \text{C} \Rightarrow \text{Si} + \text{CO}_2$ )
- Step 3: Prepare silicon bath
- Step 4: Grow ingot (FZ or CZ....)
- Step 5: Grind ingot (shaping for wafers)
- Step 6: Saw wafers (diamond saw)
- Step 7: Thickness sort
- Step 8: Lapping and etching
- Step 9: Sort and test
- Step 10: Polish
- Step 11: Qualify
- Step 12: sell to PV manufacturer.....



# Alternative silicon sources

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- Techniques were traditionally developed for microelectronics
- Money was (almost no object)
- Now PV demand is beginning to outstrip microelectronics demand
- New, cheap techniques are sought (for every part of process)



<http://pvcdrom.pveducation.org/index.html>

# Commercial Devices

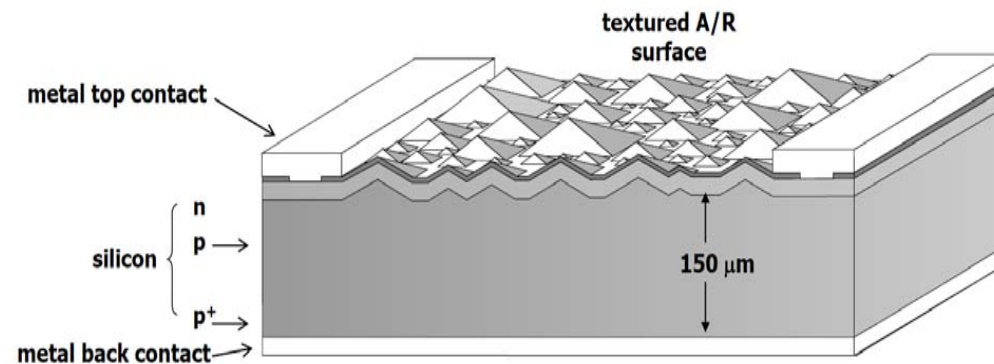
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- commercial C-Si wafer module efficiencies have reached 22.9% but are more typically in the range 14-17%

[King DL, et al "World's First 15% Efficiency Multicrystalline Silicon Modules". In: Procs of the 1st World Conference on Photovoltaic Energy Conversion; 1994; Hawaii. p. 1660-1662.]

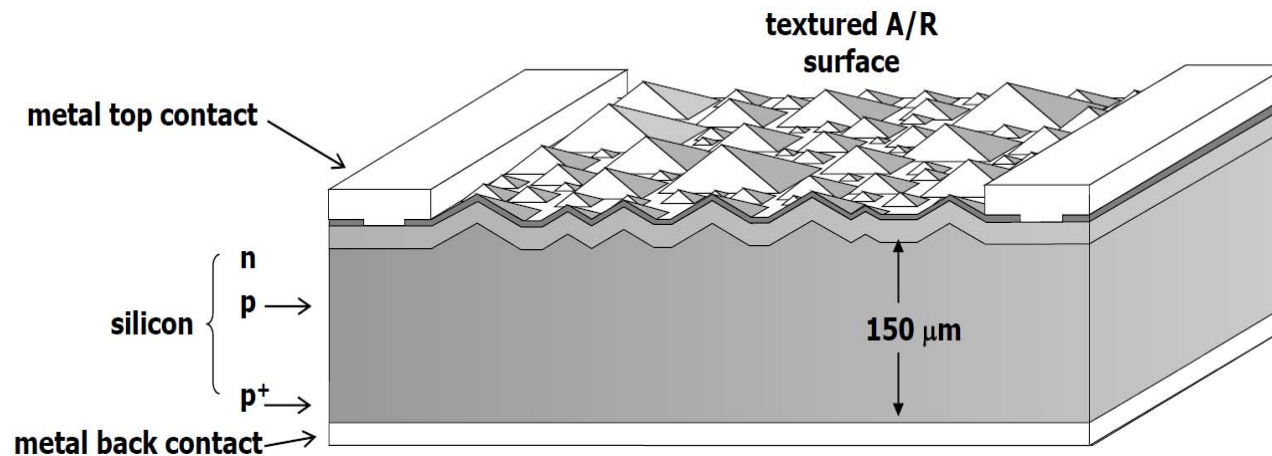
- mC-Si modules have reached up to 15.5% but are more typically sold as modules in the 10-14% range

[Blakers et al ."23% Efficient Silicon Solar Cell." In: Proceedings of the 9th European Communities Photovoltaic Science and Engineering Conference; 1989; Freiburg, Germany. p. 328-329]

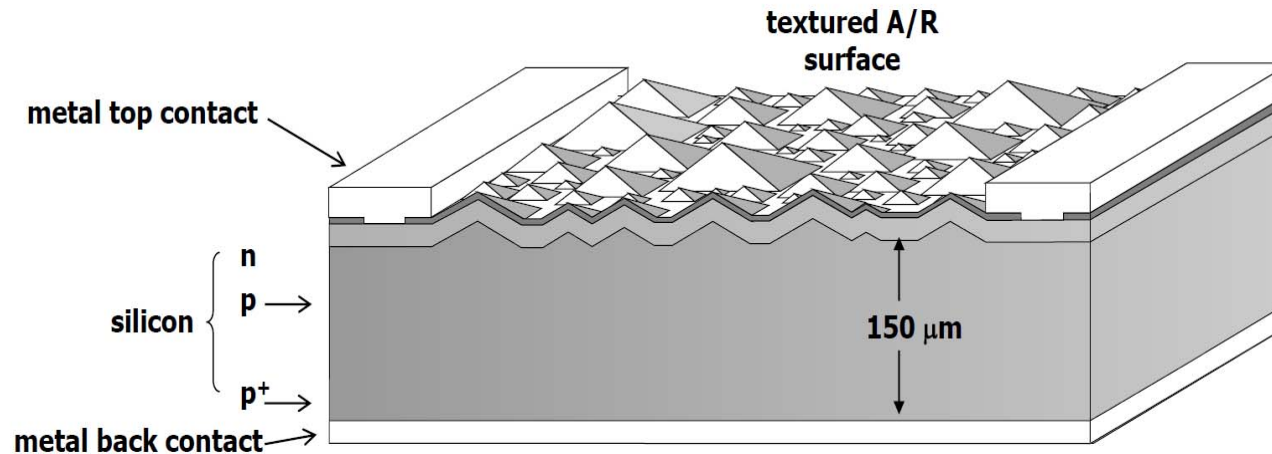


# Commercial Devices

- There is a large diversity of C-Si and mC-Si device types;
- Nearly all commercial C-Si and mC-Si devices have a shallow n-type region formed by the diffusion of phosphorous from  $\text{POCl}_3$  into a lightly doped p-type wafer to form the junction.
- The polished front surface of a C-Si solar cell is typically textured by a KOH etch to produce a randomized array of micron-scale inverted pyramids [40]. This provides a cost effective antireflection scheme.
- The textured surface is then covered by a single layer of a dielectric material, typically silicon oxide or silicon nitride
- This layer provides an antireflective coating and a passivation layer that reduces surface recombination.



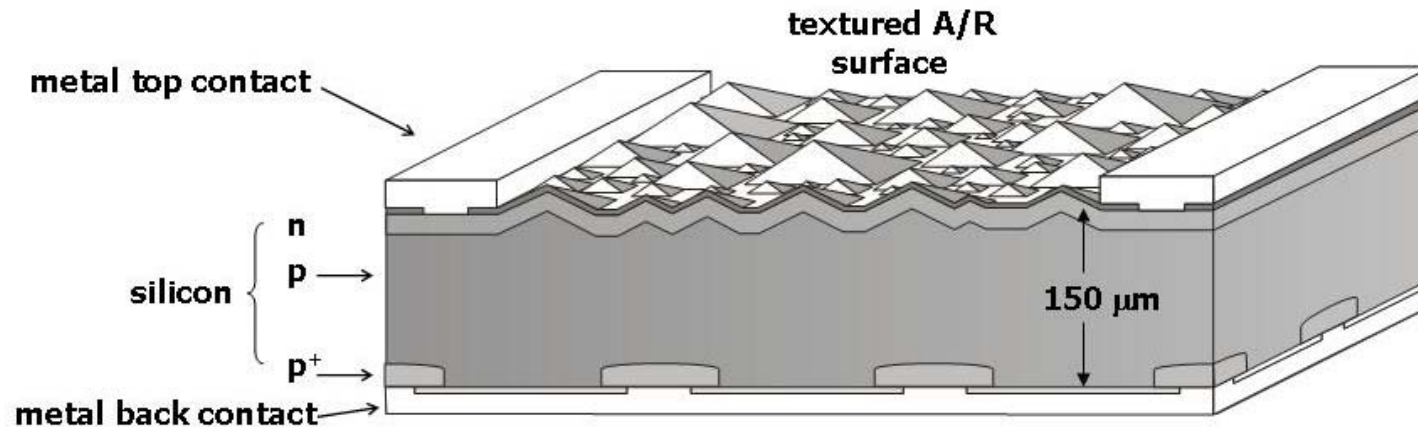
# Commercial Devices



- The polycrystalline form of the mC-Si wafers will not facilitate the formation of the inverted pyramid structure so mC-Si devices therefore rely solely upon 1/4 wavelength AR coatings.
- A large number of contacting materials and deposition schemes are employed.
- On the front surface a finger grid of titanium (protected by nickel or palladium) is deposited by evaporation through a shadow mask or by screen printing to form the top electrical contacts.
- Typically aluminium is screen-printed or evaporated onto the entire rear surface of the wafer to form the back electrical contact.



# Rear Passivation

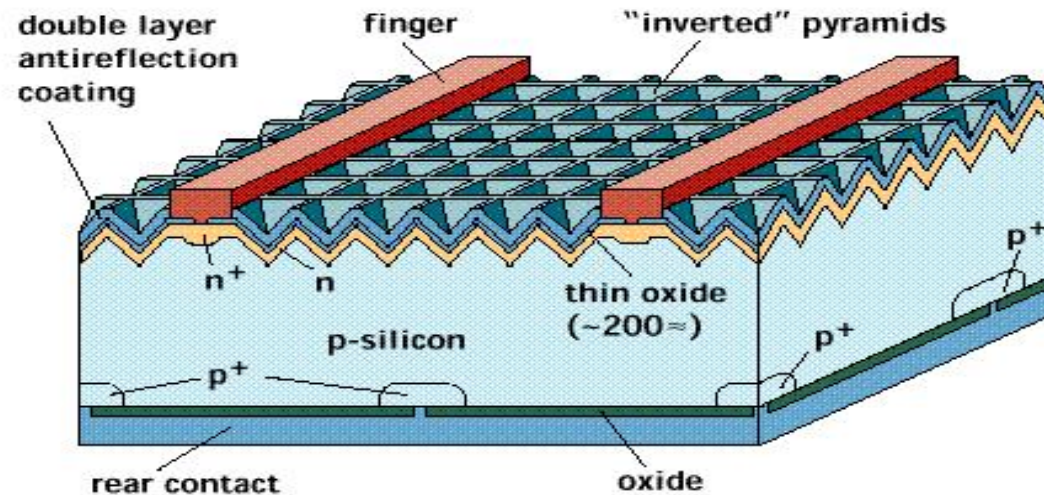


The **Passivated Emitter and Rear Contacts (PERC)** device uses:

- a thinner wafer, uses an oxide to passivate much of the rear surface of the device
- selectively heavy doping of regions where the metal contacts the silicon
- In this design, light is reflected back from the rear surface and carrier recombination is reduced

[Blakers et al. "23% Efficient Silicon Solar Cell." In: Proceedings of the 9th European Communities Photovoltaic Science and Engineering Conference; 1989; Freiburg, Germany. p. 328-329]

# PERL cell

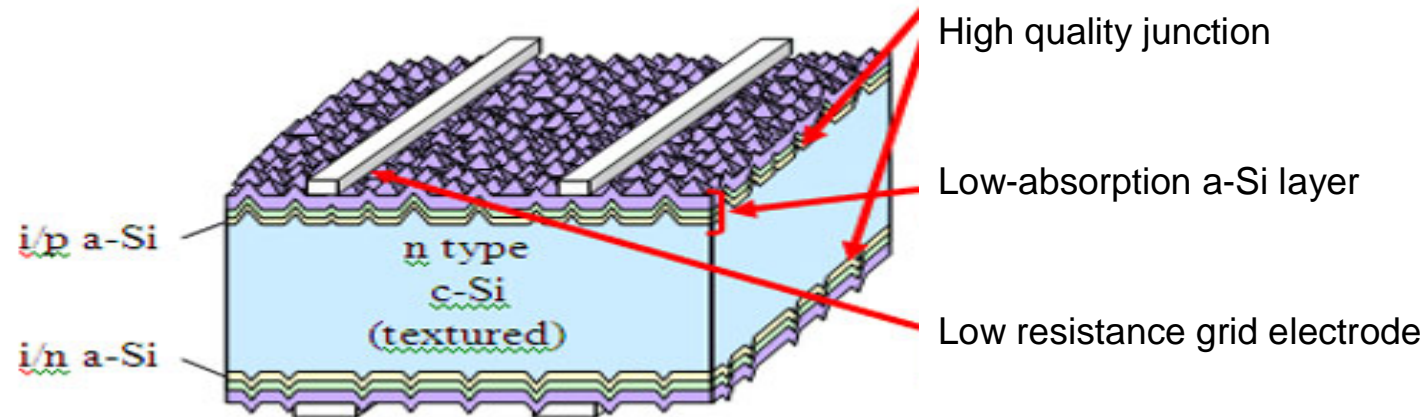


- The Passivated Emitter, Rear Locally-diffused (PERL) cell is the most efficient single-junction silicon solar cell reported [1].
- The most striking feature of the PERL cell is the lithographically defined “inverted pyramid” structure on the top surface that is covered with a thin passivating oxide and a double-layer antireflection coating.
- This structure not only provides low reflectance it also increases absorption lengths by ensuring that most of the absorbed light is directed obliquely into the device. Careful optical design, [2] reduces optical losses to only 6-7% of the incident light

[1] J. Zhao et al, “24% Efficient PERL Silicon Solar Cell: Recent Improvements in High Efficiency Silicon Cell Research”. *Solar Energy Materials and Solar Cells*. 1996;41-42:87-99

[2] P. Campbell P, M.A.Green “Light trapping properties of pyramidally textured surfaces” *Journal of Applied Physics*. 1987;62(1):243-249.

# Sanyo's HIT cell

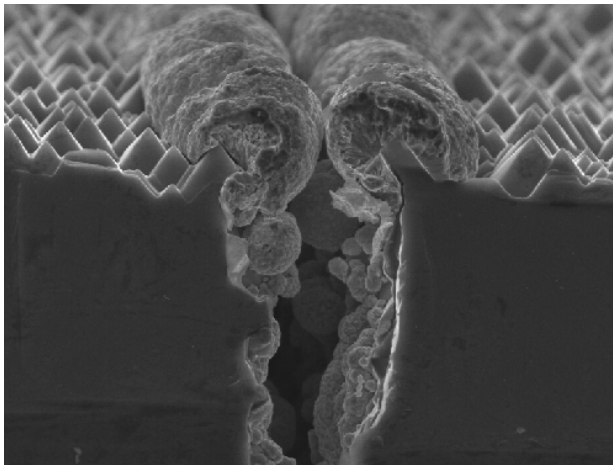
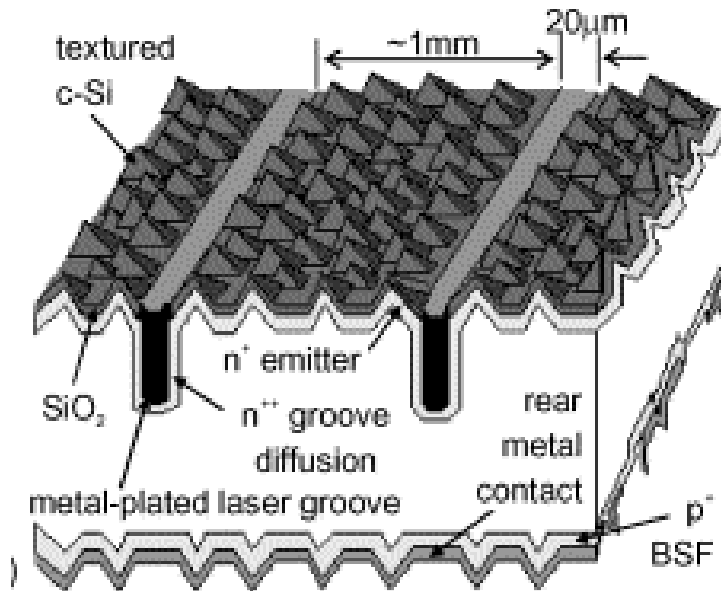


HIT (heterojunction with intrinsic layer) cells combine a-Si technology and C-Si technology.

- Unusually these devices start with an n-type substrate, but then surround the C-Si with p and n-type a-Si layers on the top and bottom of the device.
- These layers provide excellent passivation and low resistances, they ease contact formation and allow large open-circuit voltages,
- Although absorption in the a-Si cannot contribute minority carriers and device currents are reduced, impressive **22.8% efficient devices** have been demonstrated

E. Maruyama et al, "Sanyo's Challenges to the Development of High-efficiency HIT Solar Cells and the Expansion of HIT Business". In: Proceedings of the 4th World Conference on Photovoltaic Energy Conversion; 2006; Hawaii

# Buried Contact cells

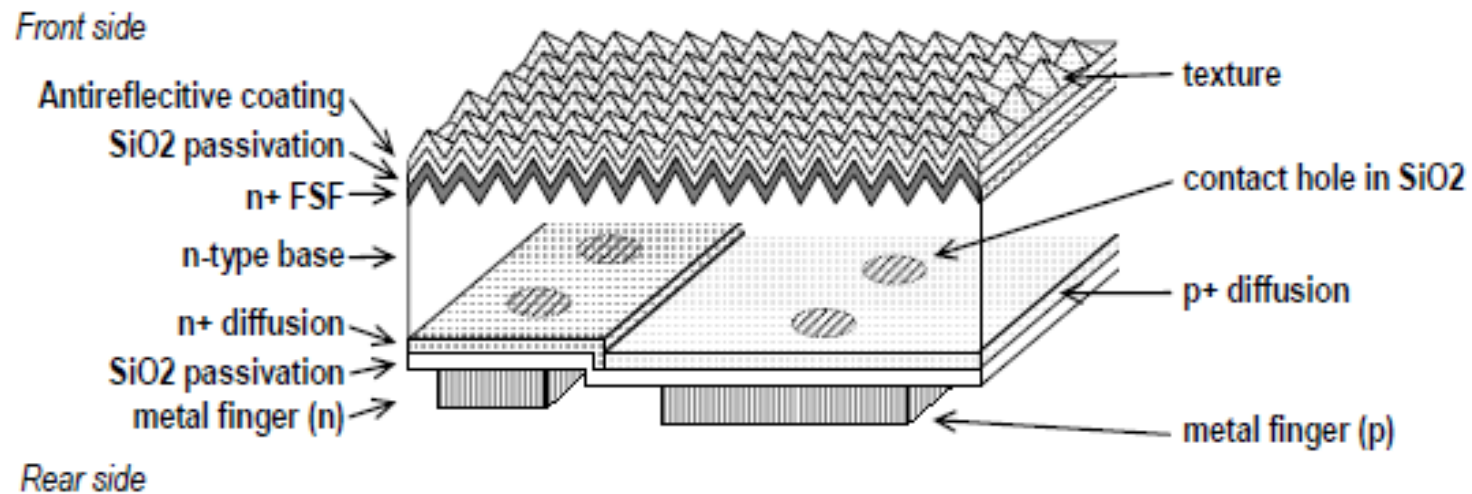


- The buried contact solar cell is on a plated metal contact inside a laser-formed groove.
- this technology overcomes many of the disadvantages associated with screen-printed contacts and this allowing performance up to 25% better than commercial screen-printed solar cells.
- A key high efficiency feature of the of the buried contact solar cell is that the metal is buried in a laser-formed groove inside the silicon solar cell.
- This allows a large volume of metal to be used in the contact finger, without having a wide strip of metal on the top surface. Shading losses are reduced to 2 to 3%, resistance losses are reduced.

[BP: Bruton, T.M., Procs. of 6th International Photovoltaic Science and Engineering Conference, p 11

B. Richards Solar Energy, Volume 76, Issues 1-3, January-March 2004, Pages 269-276 ]

# Rear Contact cells



- eliminate shading losses altogether
- electron-hole pairs generated by light that is absorbed at the front surface can still be collected at the rear of the cell
- especially useful in concentrator applications where the effect of cell series resistance is greater.
- an additional benefit is that cells with both contacts on the rear are easier to interconnect

Sunpower: K. McIntosh et al, 3<sup>rd</sup> World Conf. On PV energy Conversion 2003

Van Kerschaver and Beaucarne: Prog. Photovolt: Res. Appl. 2006;107

<http://pvcadrom.pveducation.org/index.html>

# Conclusions

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- **The best commercial wafer silicon module efficiencies are in the 20-23% range**
- **The worst are much lower than this**
- **There has been a great deal of scientific progress, efficiencies are not likely to increase significantly**
- **To reduce costs the best hopes are :**
  - **scaling (10% reduction each time production goes up 10x**
  - **improved wafer technology (thinner wafers, less waste)**

**Increasingly we might expect thin film technologies to gain market share over wafer technologies.**

[ D.M. Bagnall, M. Boreland “Photovoltaic technologies”, Energy Policy 36 (2008) 4390]