The Abdus Salam
International Centre for Theoretical Physics

United Nations
Educational, Scientific and
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IAEA
International Atomic Energy Agency

2177-6

ICTP Latin-American Basic Course on FPGA Design for Scientific Instrumentation

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**Gates**

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Outline

- **Introduction**
- **Transistors**
- **The CMOS inverter**
- **Technology**
- **Scaling**
- Gates
  - The NAND gate
  - "Reading" CMOS gates
  - Designing CMOS gates
- **Sequential circuits**
- **Storage elements**
- **Phase-Locked Loops**
- **Example**
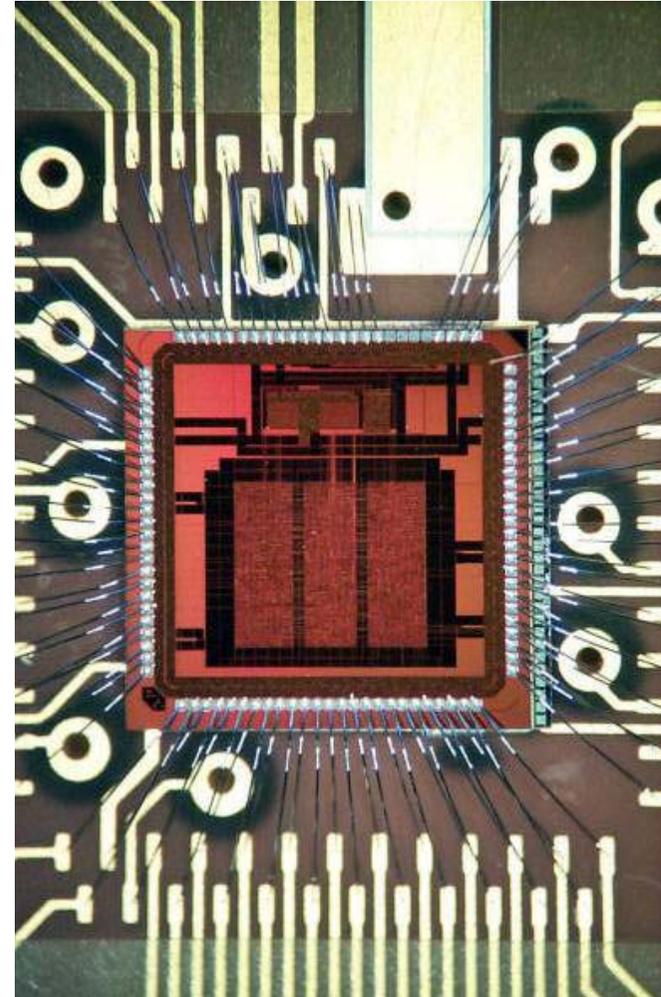
NAND 2-inputs
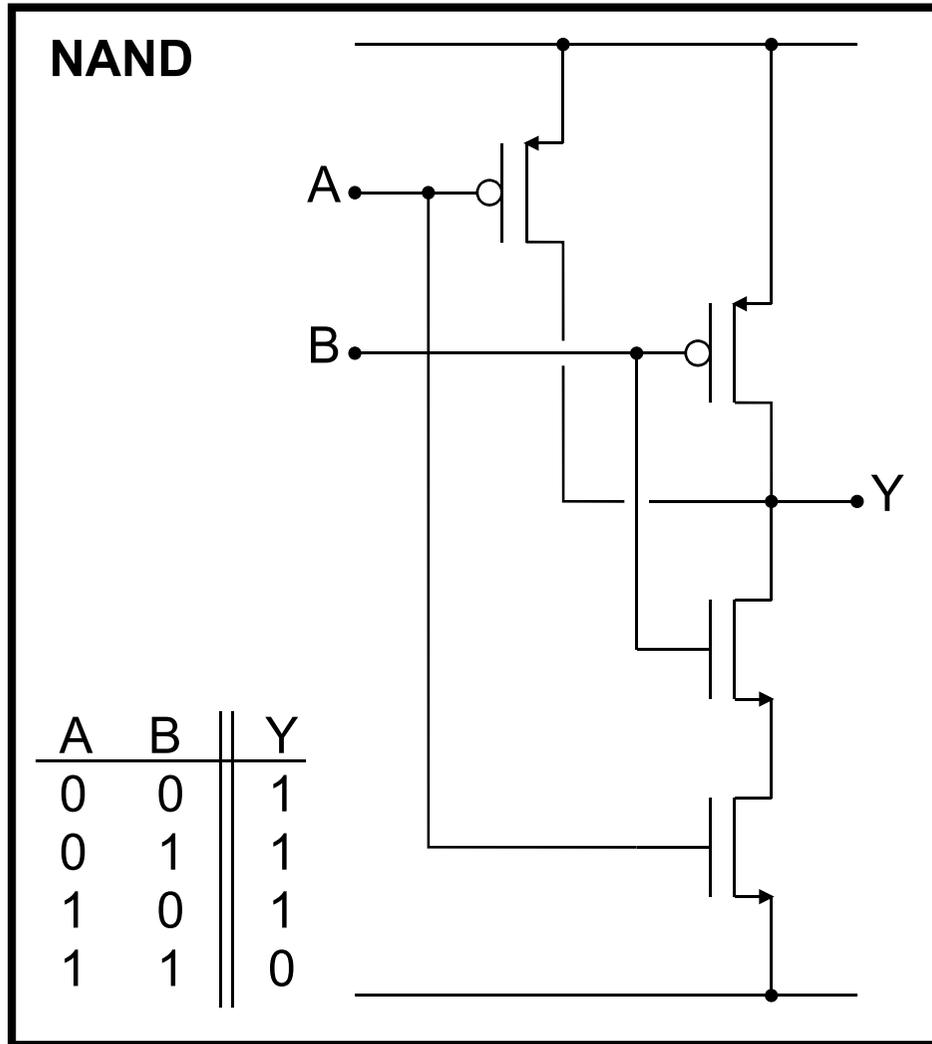
NAND

"Gates are inverters in disguise!"

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NAND 3-inputs

NAND 3 inputs

"Delay equivalent" inverter

NAND 3-inputs

NAND 3 inputs

Use transistors close to the output for critical signals

Bulk effect

Stray capacitance
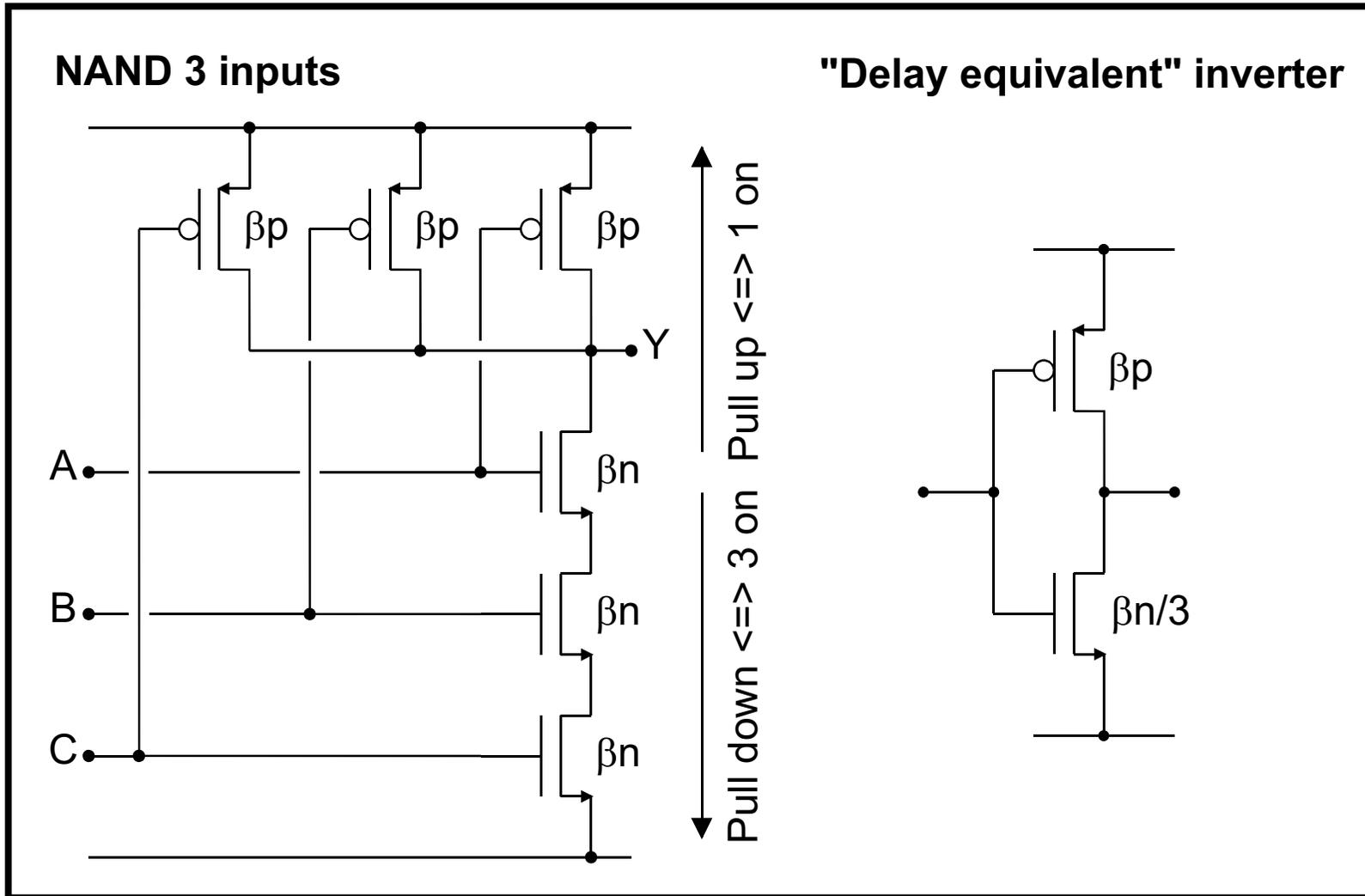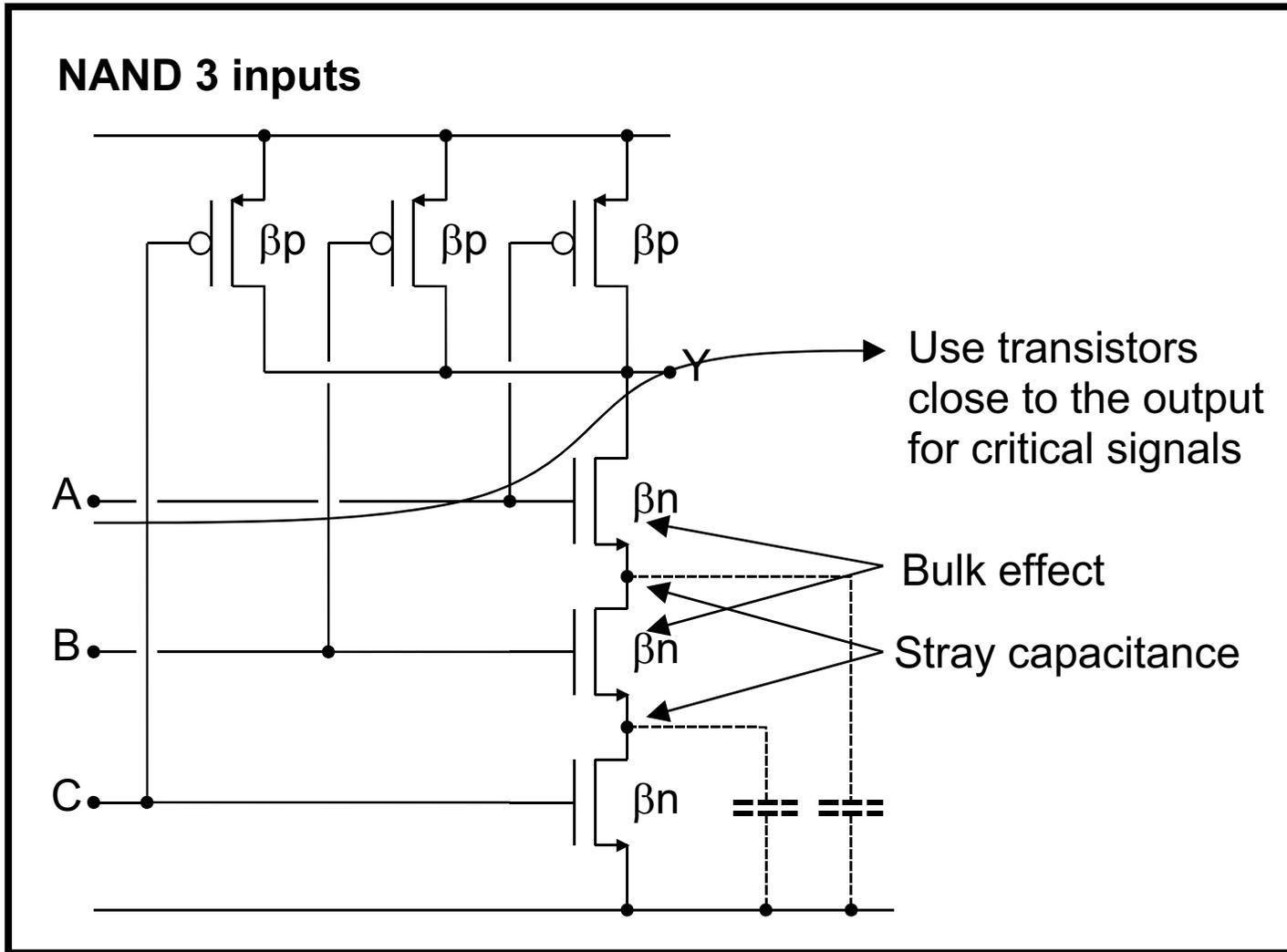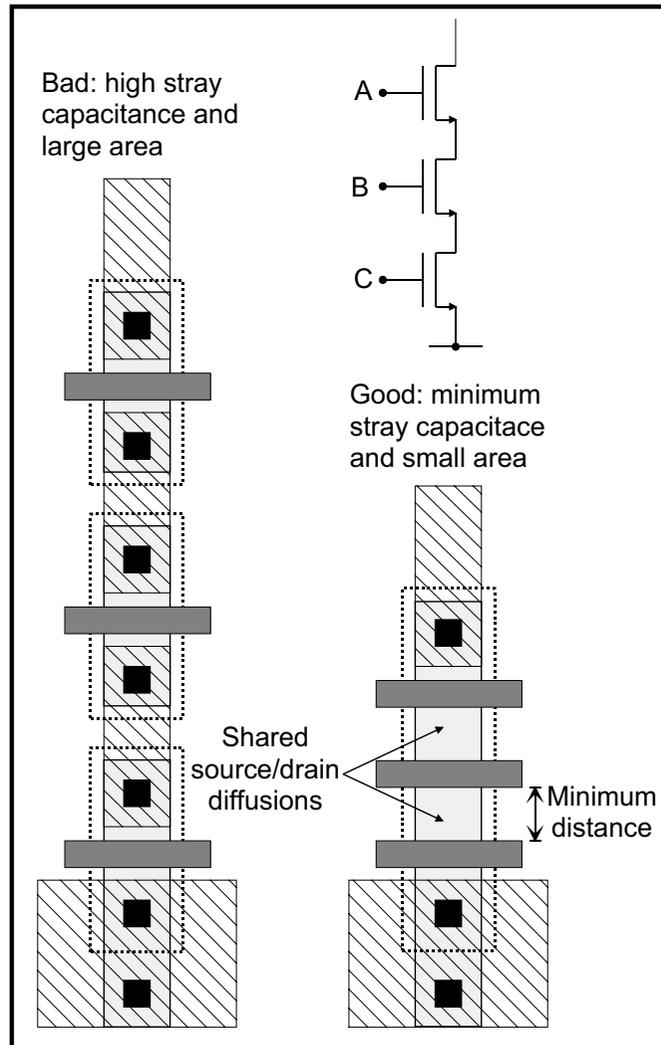
NAND 3-inputs

NAND 3-inputs

"Reading" CMOS gates

Designing CMOS gates

$$Y = \overline{D (A + B + C)}$$
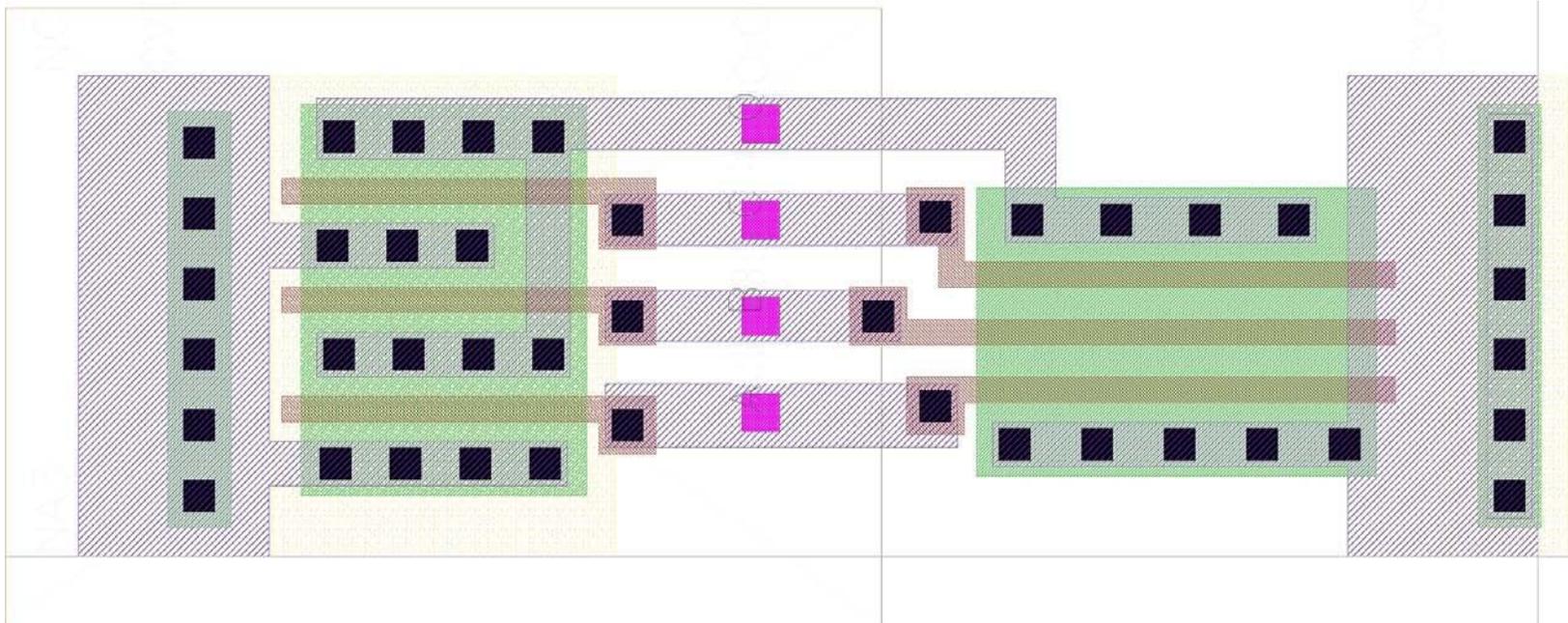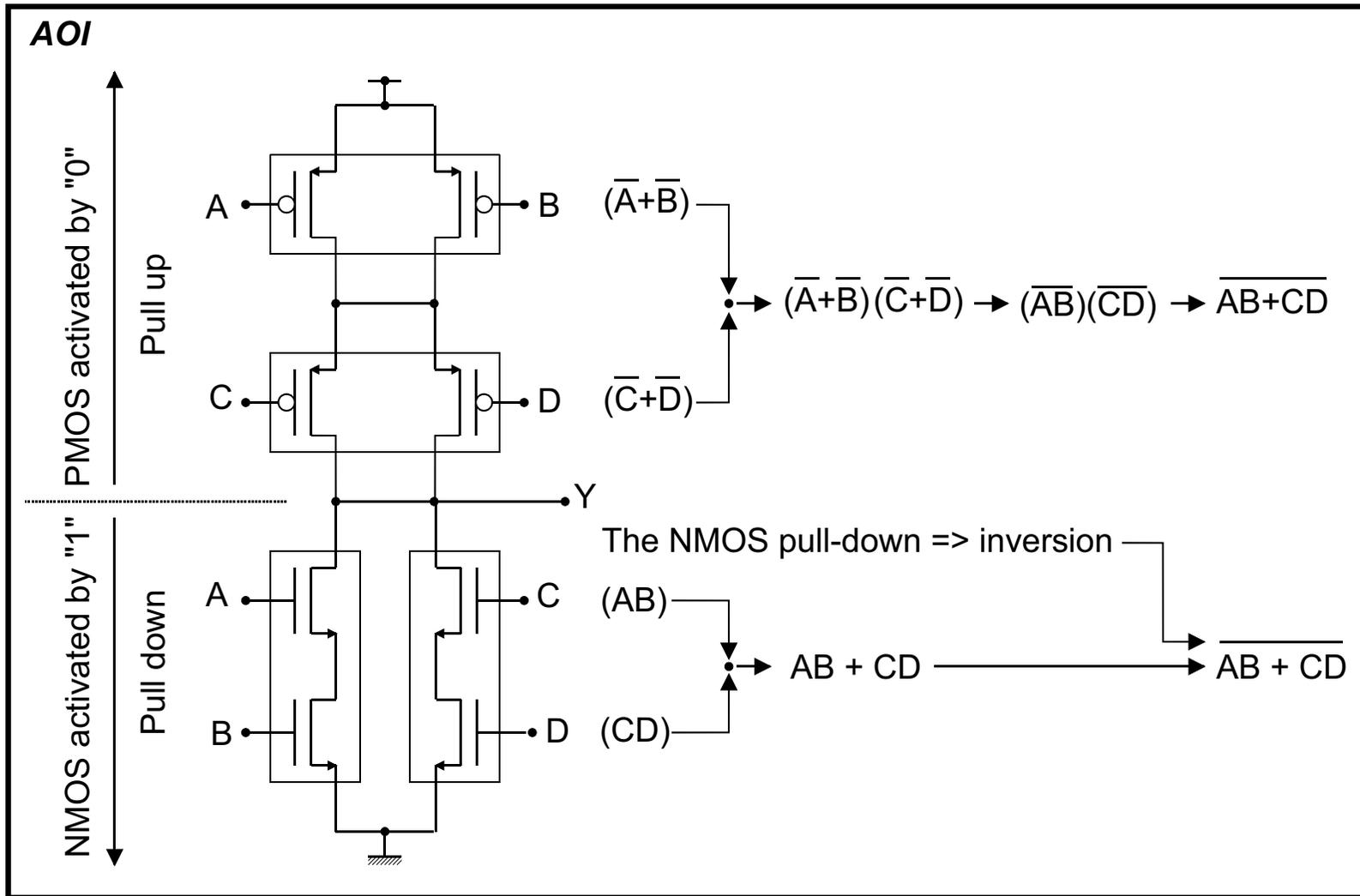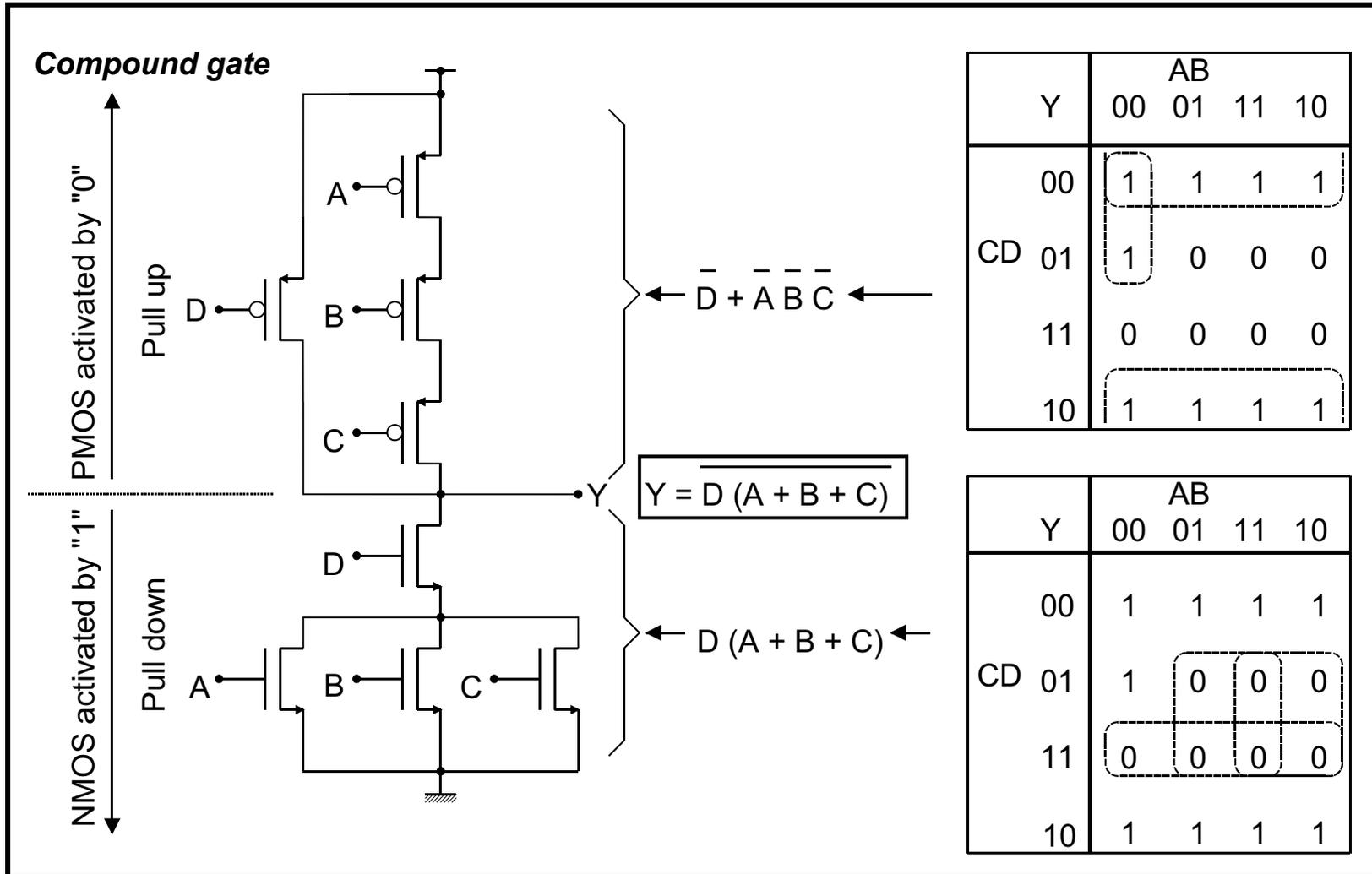
Complex CMOS gates

- Can a compound gate be arbitrarily complex?

    - <u>NO</u>, propagation delay is a strong function of fan-in:

$$t_p = a_0 \cdot FO + a_1 \cdot FI + a_2 \cdot \left(FI\right)^2$$

    - FO $\Rightarrow$ Fan-out, number of loads connected to the gate:
        - 2 gate capacitances per FO + interconnect

    - FI $\Rightarrow$ Fan-in, Number of inputs in the gate:
        - Quadratic dependency on FI due to "RC" signal path across the channels:
            - The resistance increases with the number of transistors in series
            - Each drain and source diffusion adds additional parasitic capacitance

    - <u>Avoid large FI gates</u> (Typically FI $\leq$ 4)