2177-7

ICTP Latin-American Basic Course on FPGA Design for Scientific Instrumentation

15 - 31 March 2010

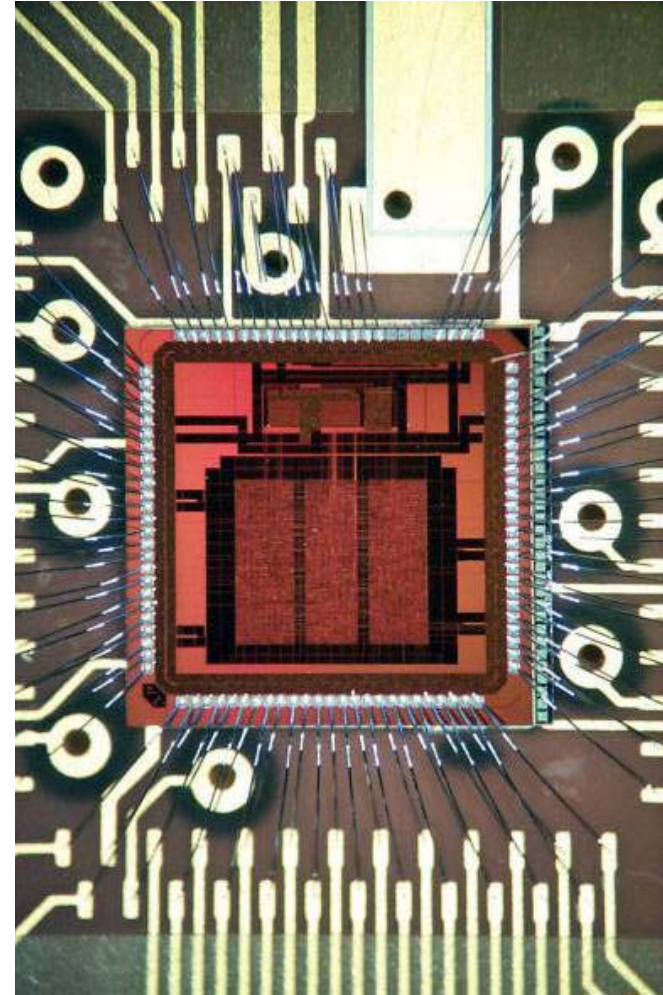**Sequential circuits**

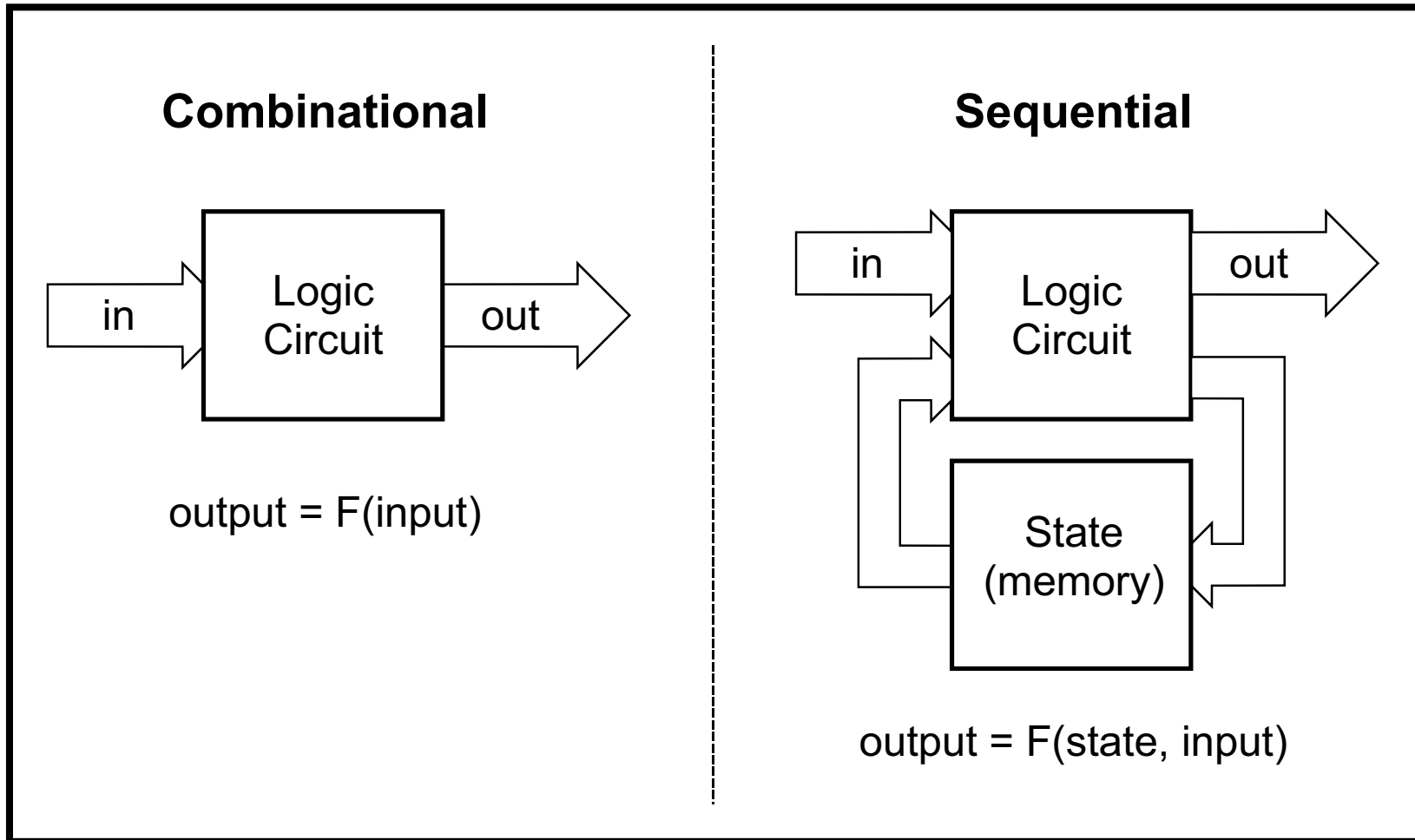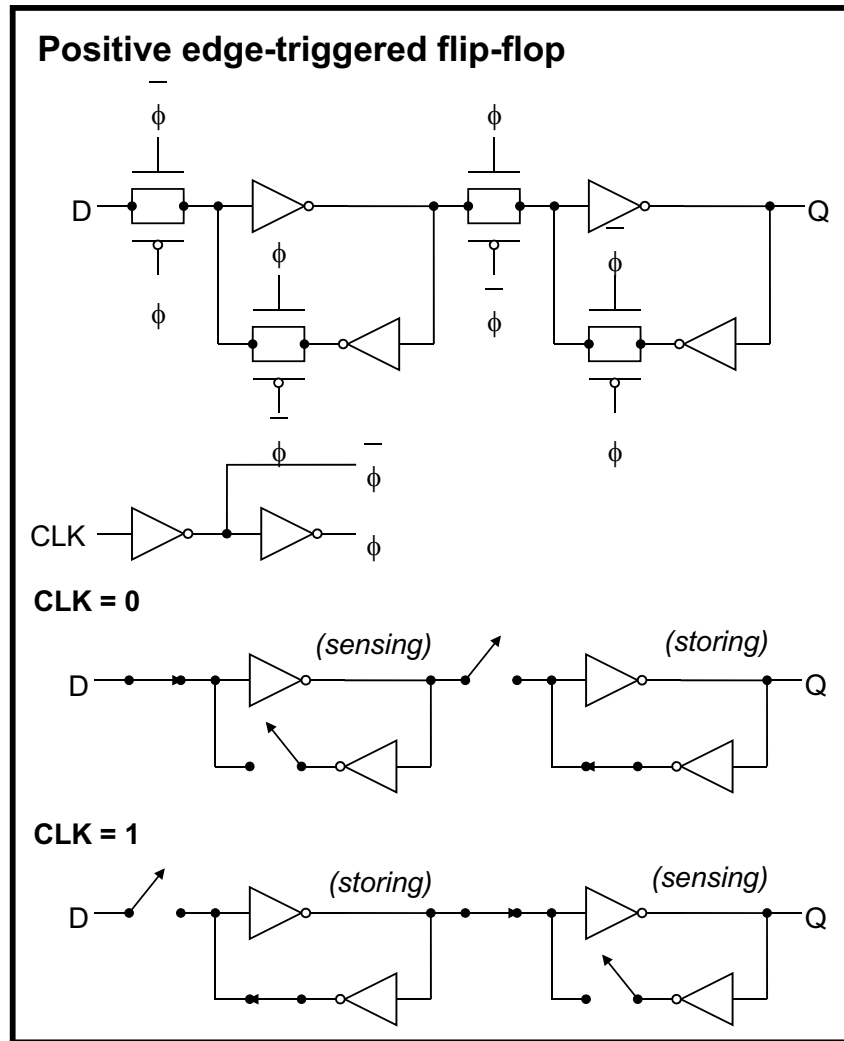MOREIRA Paulo Rodrigues S.
*CERN
Geneva
Switzerland*

Outline

- **Introduction**
- **Transistors**
- **The CMOS inverter**
- **Technology**
- **Scaling**
- **Gates**
- **Sequential circuits**
  - Time in logic circuits
  - D flip-flop
  - State machine timing
  - Interconnects
  - Clock distribution
- **Storage elements**
- **Phase-Locked Loops**
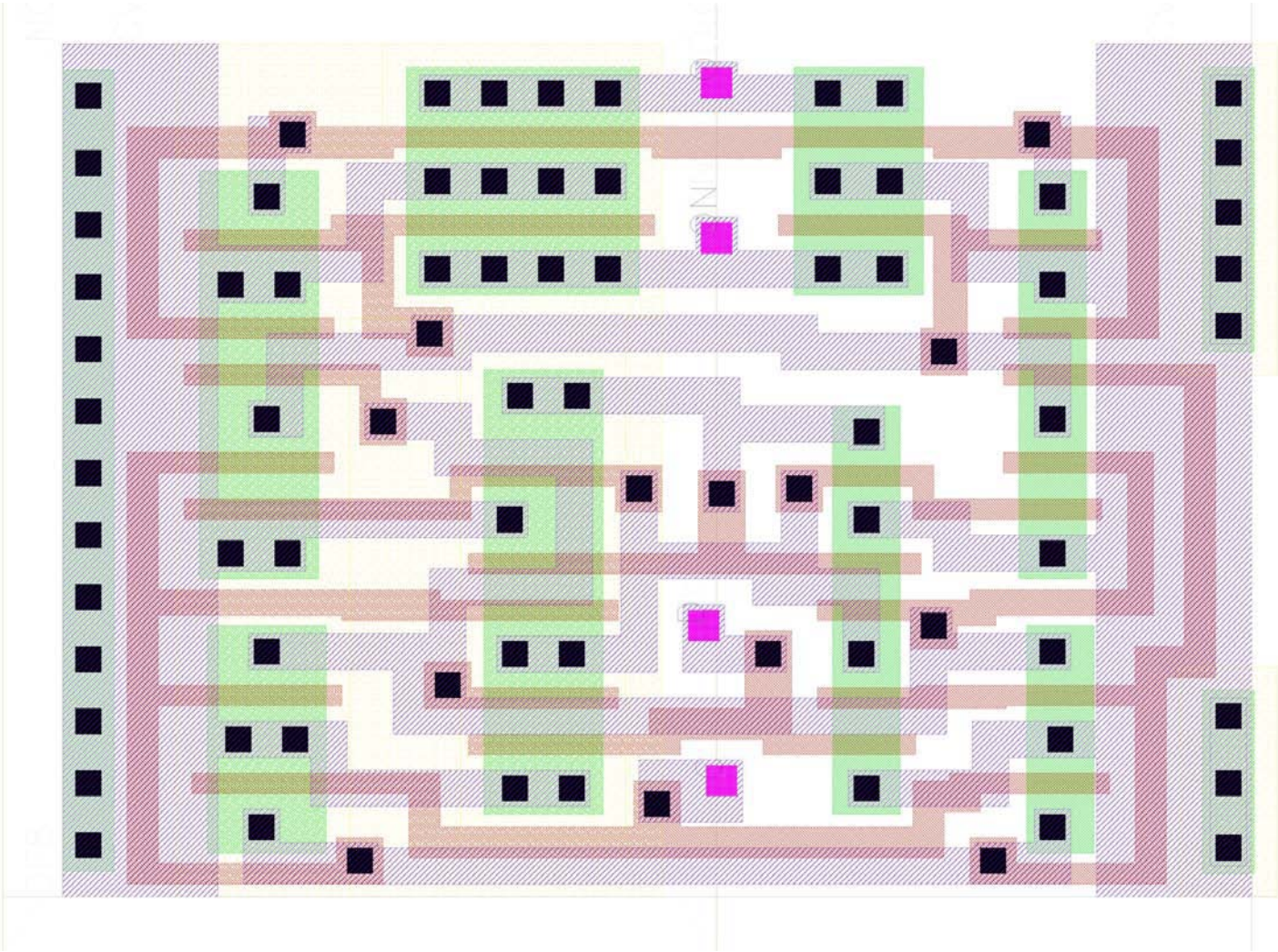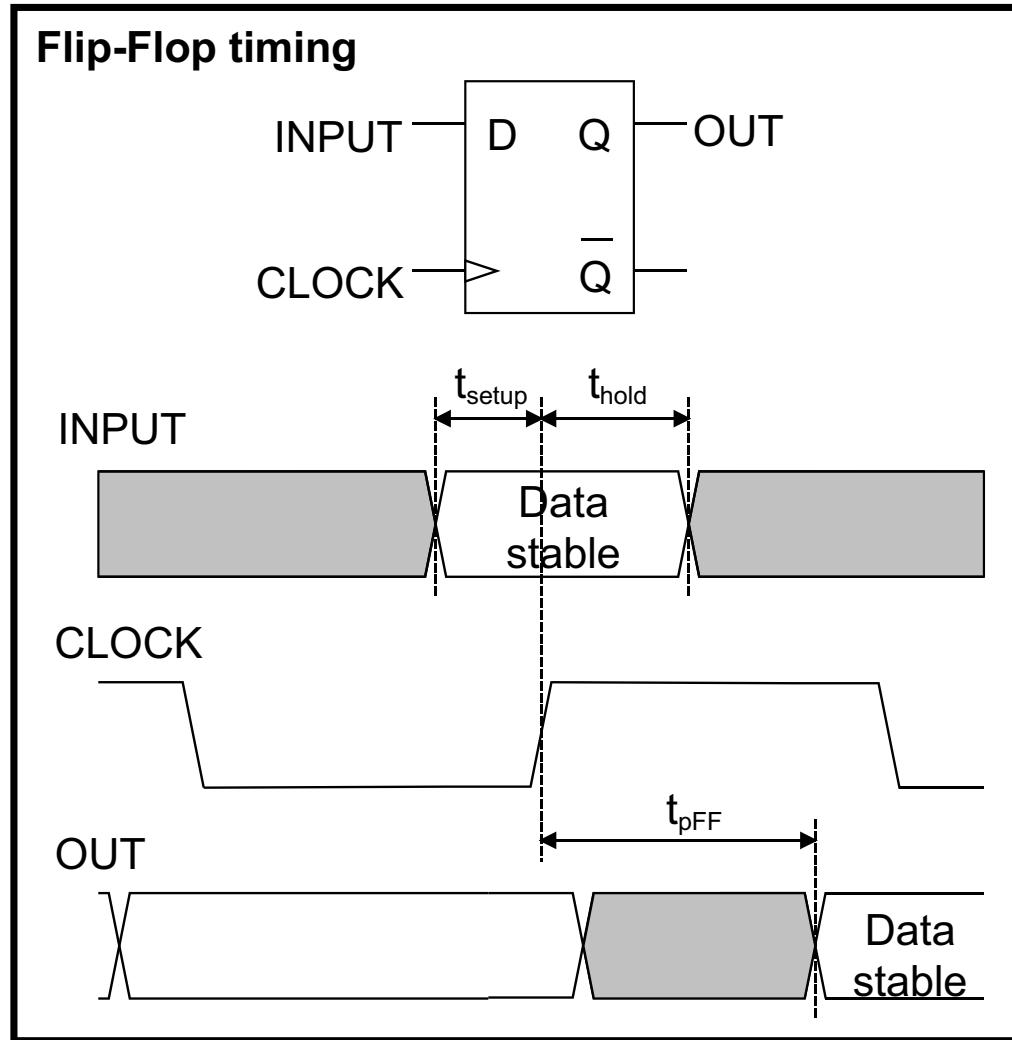- **Example**

"Time also counts"

Combinational

Logic Circuit

in

out

output = F(input)

Sequential

Logic Circuit

in

out

State (memory)

output = F(state, input)

D Flip-Flop

D Flip-Flop

State machine timing

State machine timing

Maximum clock frequency

in

Logic
Circuit

out

Q   D

clock

$$T_{min} > t_{pFF} + t_{p,comb} + t_{setup}$$

$$f_{max} = 1/T_{min}$$
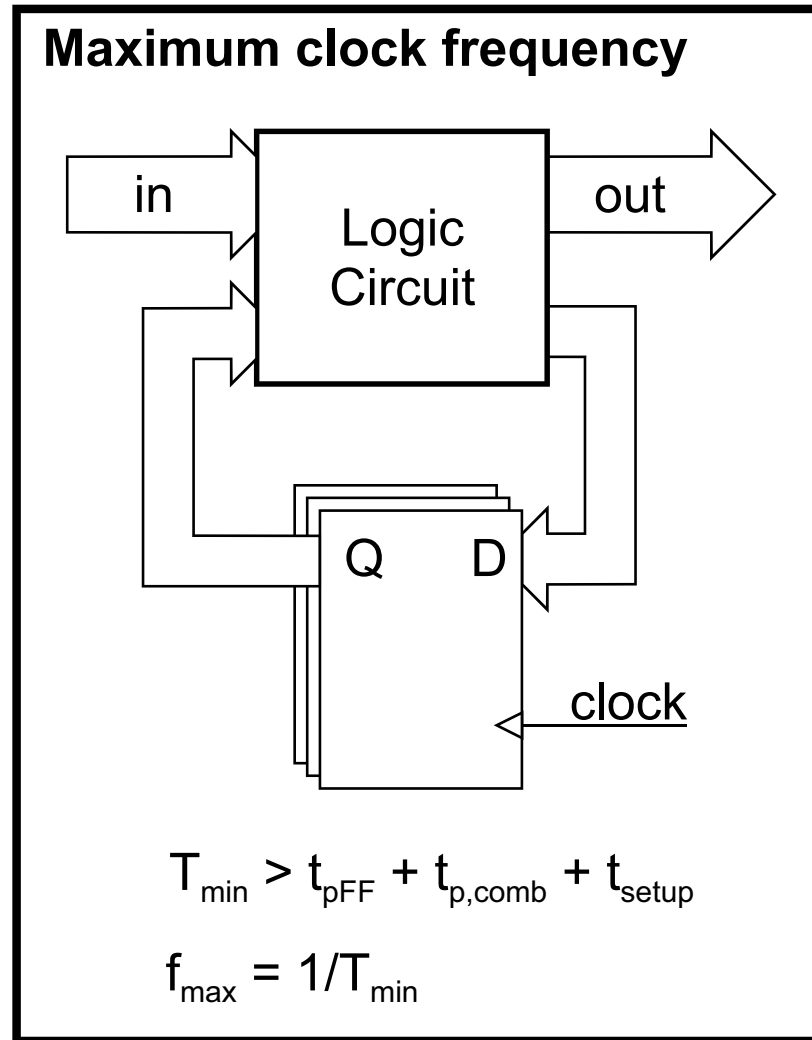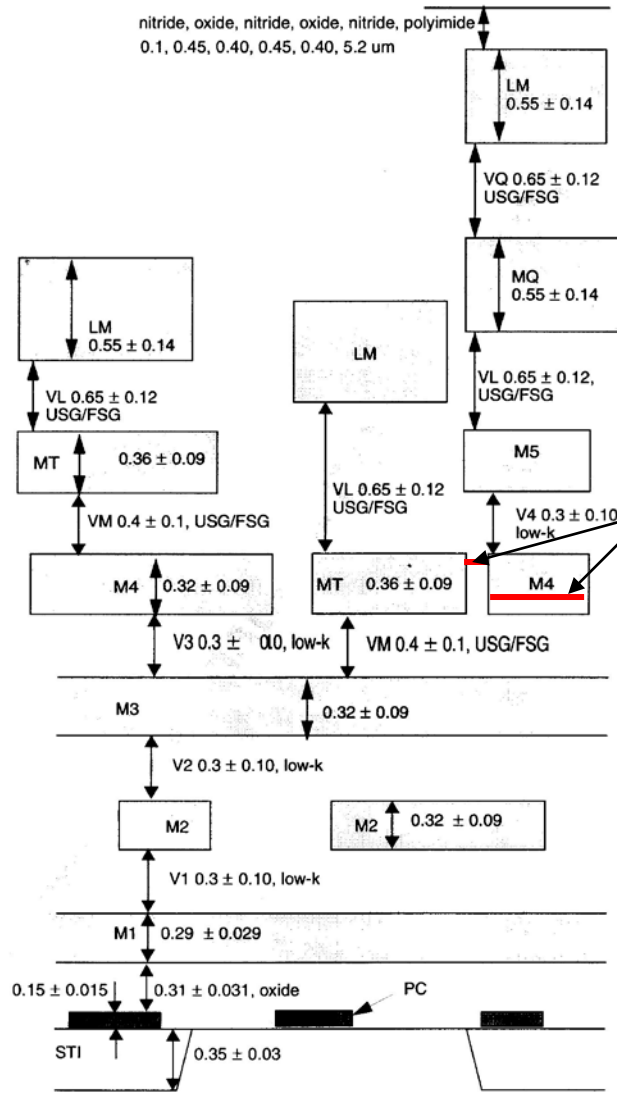
Interconnects

- The previous result assumes that signals can propagate instantaneously across interconnects

- In reality interconnects are metal or polysilicon structures with associated resistance and capacitance.

- That, introduces signal propagation delay that has to be taken into account for reliable operation of the circuit

Interconnects

Minimum Pitch: 0.2 μm
Minimum Width 0.2 μm
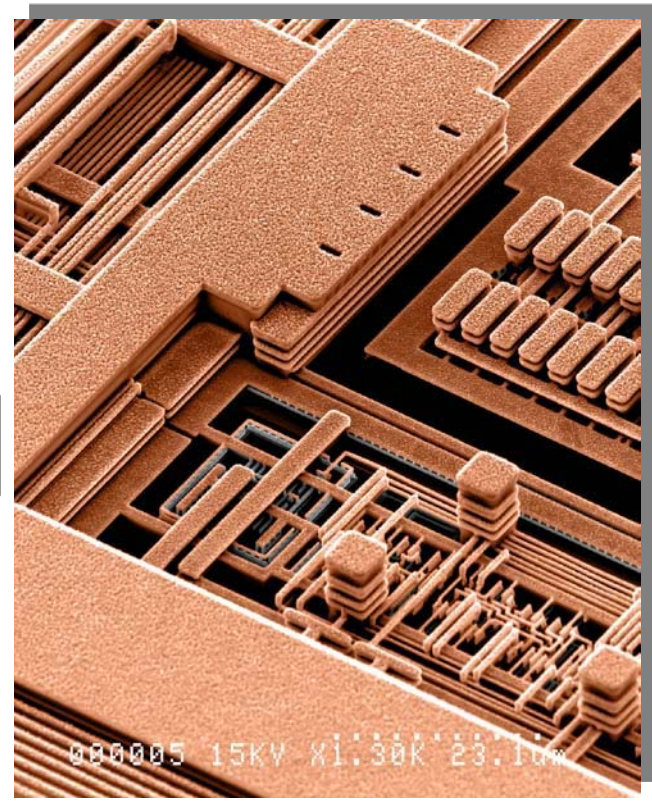
§ **Capacitance to substrate becomes irrelevant**
§ **Capacitance to neighboring signal becomes dominating**
§ **Noise to neighboring signal also not negligible**
§ **Extraction for Timing simulation horribly complicated: tools absolutely mandatory**
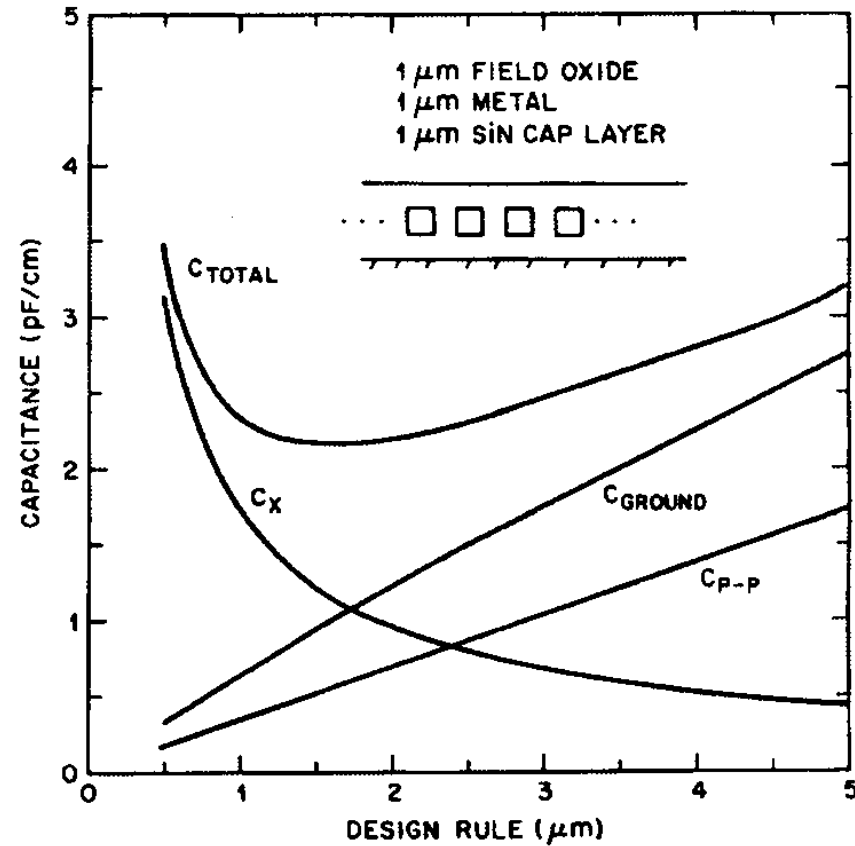
Interconnects

Figure 3.10: Interconnect capacitance including wire-to-wire capacitance [Schaper83]. (© 1983 IEEE)

Interconnects

Conductor

$$R = R_\square \frac{L}{W}$$
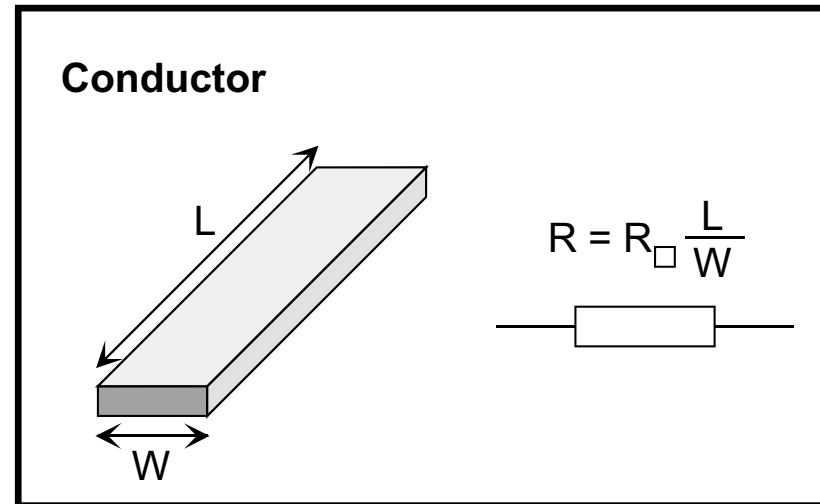
Film	Sheet resistance (Ω/square)
n-well	310
p+, n+ diffusion (salicided)	4
polysilicon (salicided)	4
Metal 1	0.12
Metal 2, 3 and 4	0.09
Metal 5	0.05
	(Typical values for an advanced process)

Interconnects

Via

Metal 1

Via

Metal 2

R_{via}
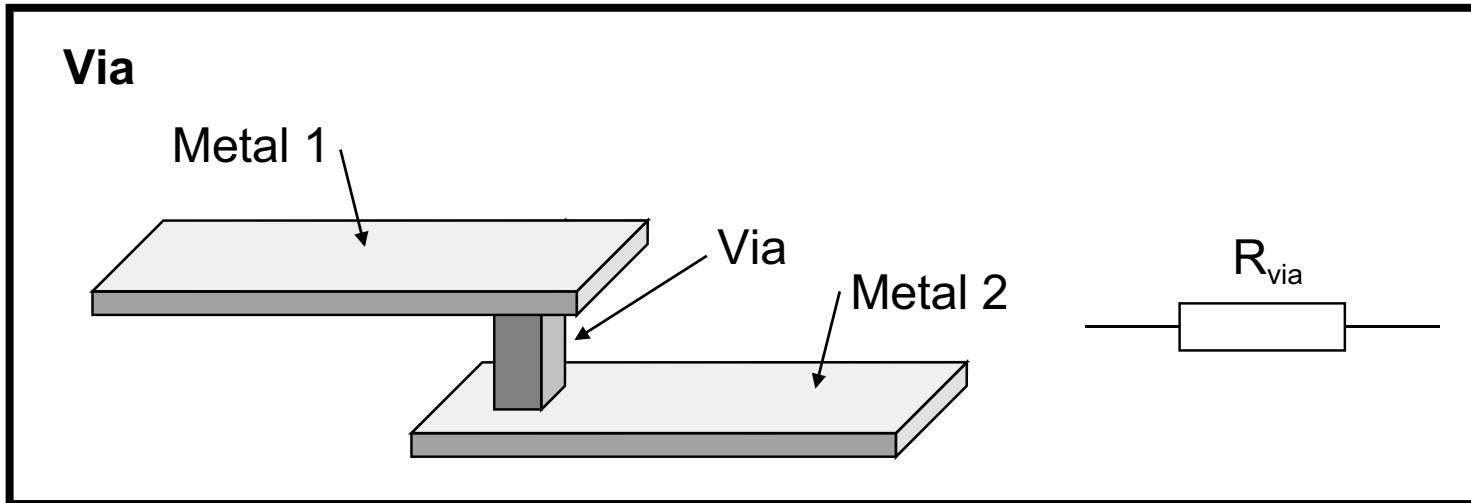
- Via or contact resistance depends on:
    - The contacted materials
    - The contact area

Via/contact	Resistance (Ω)
M1 to n+ or p+	10
M1 to Polysilicon	10
V1, 2, 3 and 4	7

Interconnects

Routing capacitance

Cross coupling capacitance

W

L

L

Fringing field capacitance

Parallel-plate capacitance

Oxide

Substrate

$$C = C_{f0}\, 2\, L + C_{p0}\, W\, L$$

$$C_x = C_{x0}\, L$$
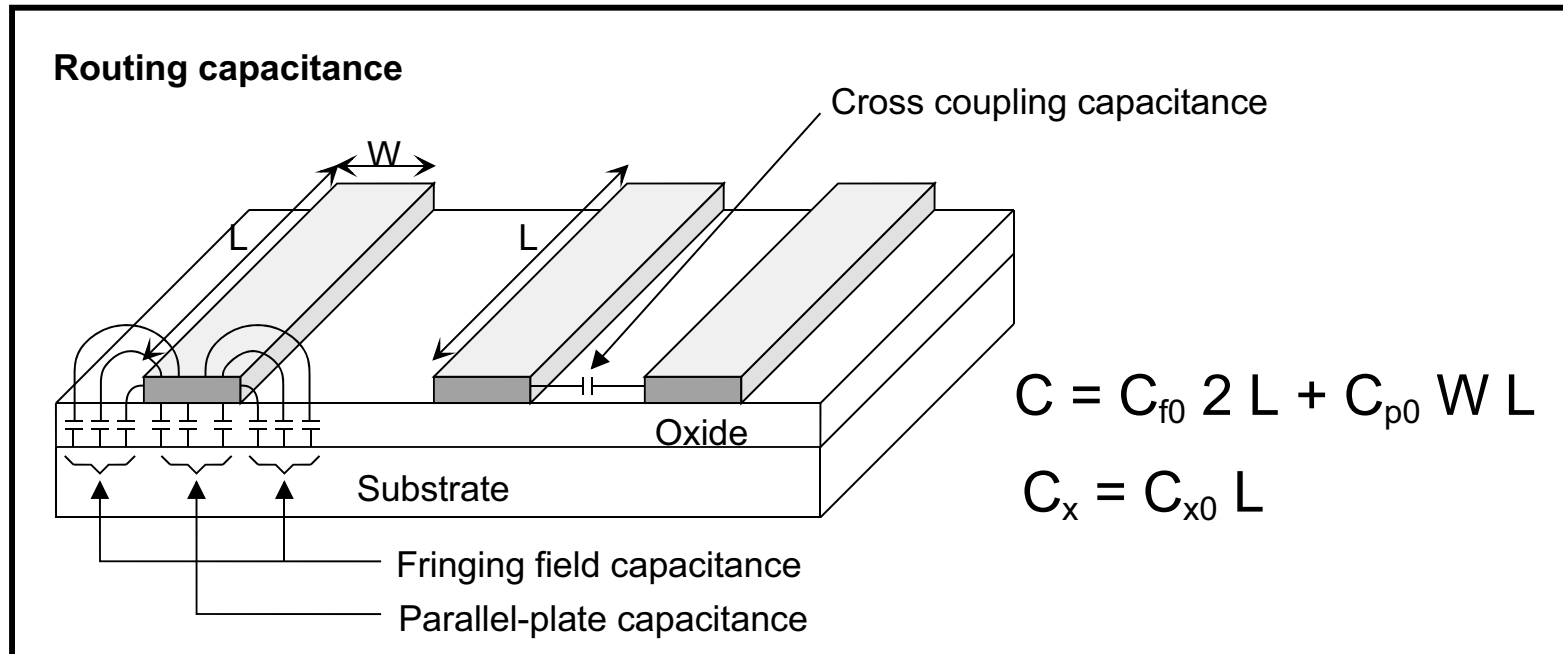
Interconnect layer	Parallel-plate (fF/μm^2)	Fringing (fF/μm)
Polysilicon to sub.	0.058	0.043
Metal 1 to sub.	0.031	0.044
Metal 2 to sub.	0.015	0.035
Metal 3 to sub.	0.010	0.033

Interconnects

Multiple conductor capacitances

M3

M2

M1
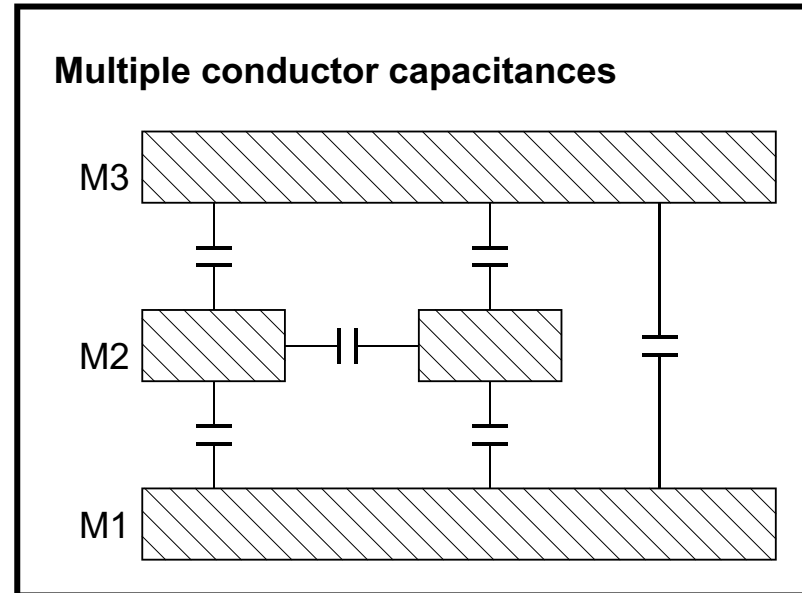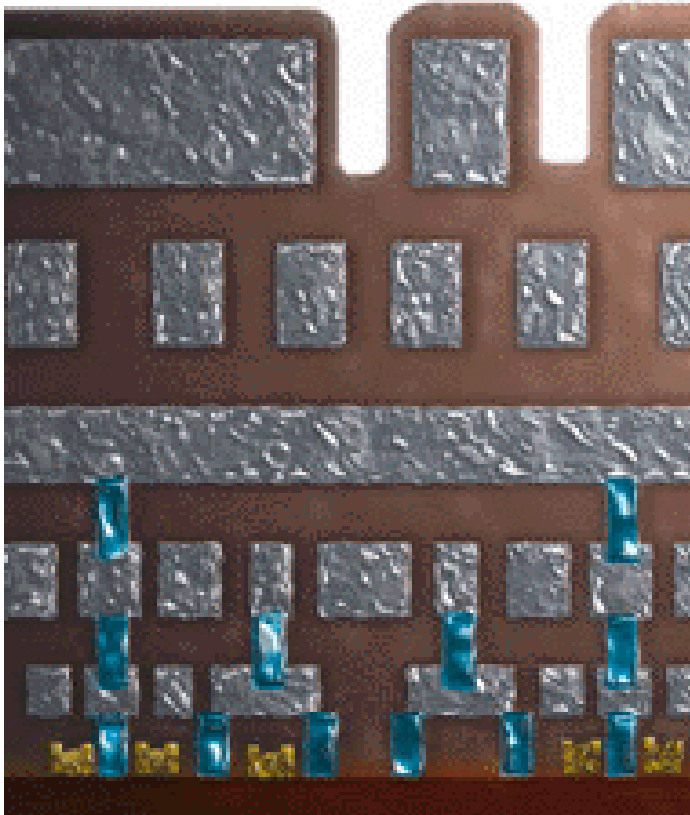
- Three dimensional field simulators are required to accurately compute the capacitance of a multi-wire structure

Interconnects
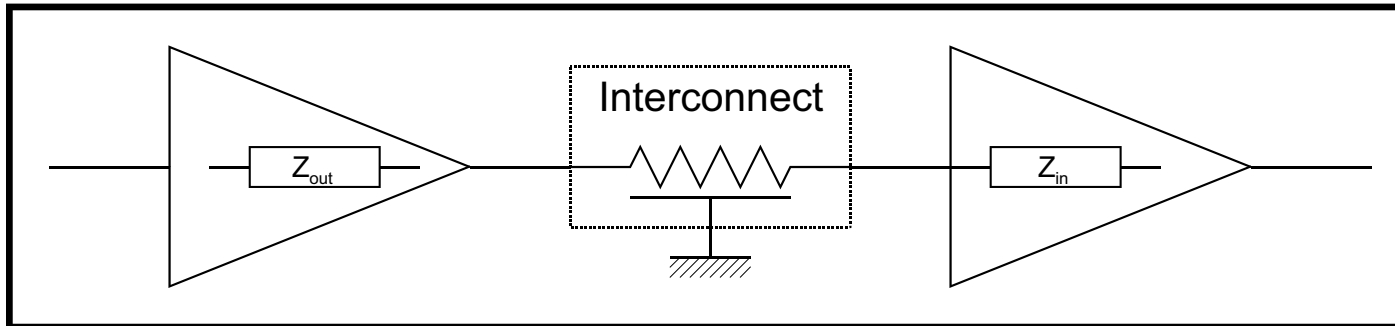
- **Delay depends on:**
  - Impedance of the driving source
  - Distributed resistance/capacitance of the wire
  - Load impedance
- **Distributed RC delay:**
  - Can be dominant in long wires
  - Important in polysilicon wires (relatively high resistance)
  - Important in salicided wires
 - Important in heavily loaded wires

Interconnects

Long line

$$t_d = \frac{1}{2} \cdot R_0 \cdot C_0 \cdot L^2$$

L

R_0

C_0

Delay optimization

$$t_d = \frac{1}{4} R_0 \cdot C_0 \cdot L^2 + t_{buff}$$

L/2

L/2
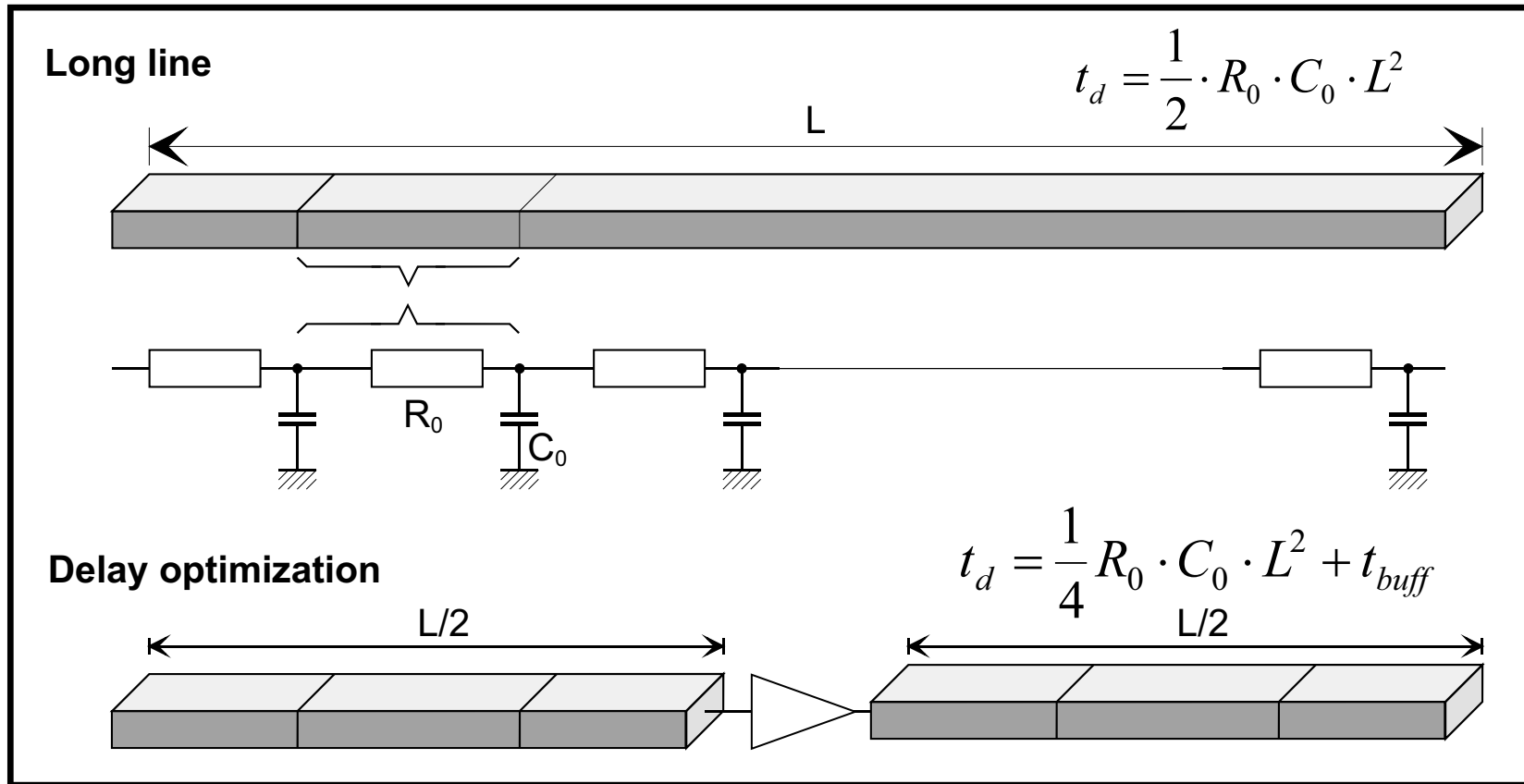
Clock distribution

- Clock signals are "special signals"
- Every data movement in a synchronous system is referenced to the clock signal
- Clock signals:
    - Are typically loaded with high fanout
    - Travel over the longest distances in the IC
    - Operate at the highest frequencies

Clock distribution
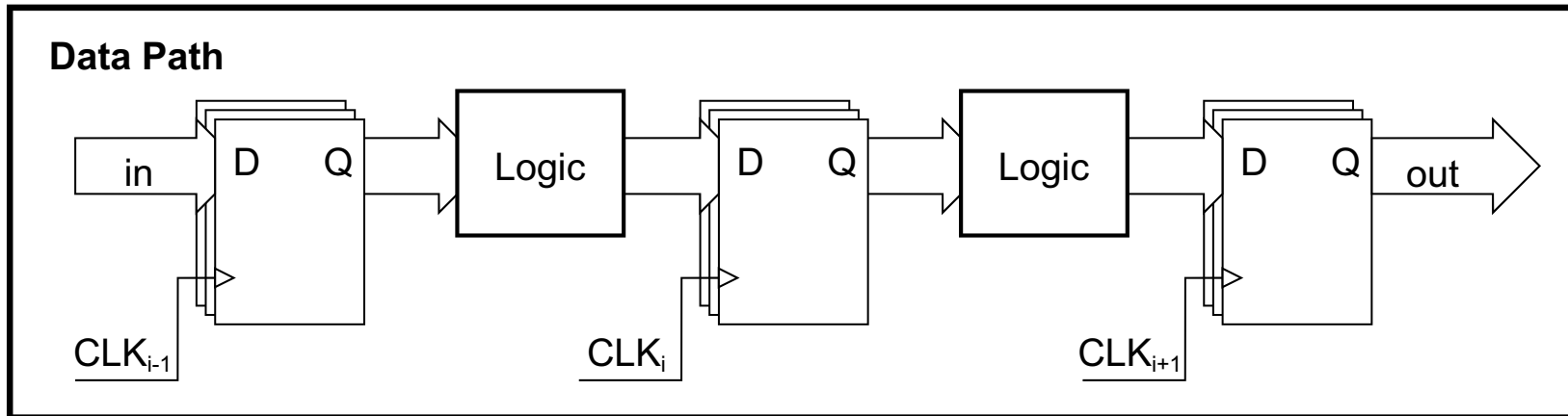
- "Equipotential" clocking:
  - In a synchronous system all clock signals are derived from a single clock source ("clock reference")
  - Ideally: clocking events should occur at all registers <u>simultaneously</u> … = $t(clk_{i-1})$ = $t(clk_i)$ = $t(clk_{i+1})$ = …
  - In practice: clocking events will occur at slightly different instants among the different registers in the data path

Clock distribution
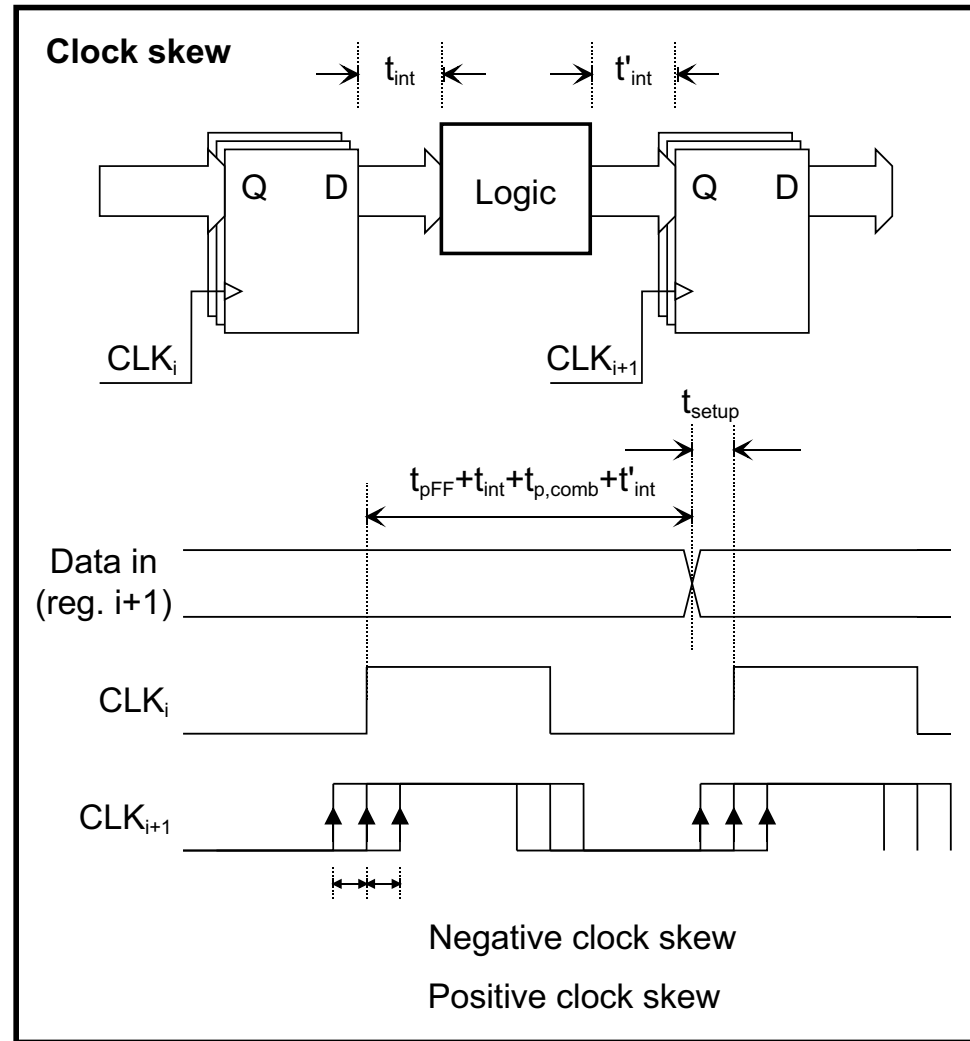
Clock distribution

- Skew: difference between the clocking instants of two "sequential" registers:

$$\text{Skew} = t(CLK_i) - t(CLK_{i+1})$$

- Maximum operation frequency:

$$T_{\min} = \frac{1}{f_{\max}} = t_{dFF} + t_{\text{int}} + t_{p,comb} + t'_{\text{int}} + t_{setup} + t_{skew}$$

- Skew > 0, decreases the operation frequency
- Skew < 0, can be used to compensate a critical data path <u>BUT</u> this results in more positive skew for the next data path!

Clock distribution

- Different clock paths can have different delays due to:
  - Differences in line lengths from clock source to the clocked registers
    - Differences in passive interconnect parameters (line resistance/capacitance, line dimensions, …)
  - Differences in delays in the active buffers within the clock distribution network:
    - Differences in active device parameters (threshold voltages, channel mobility)
- In a well designed and balanced clock distribution network, the distributed clock buffers should be the principal source of clock skew

Clock distribution
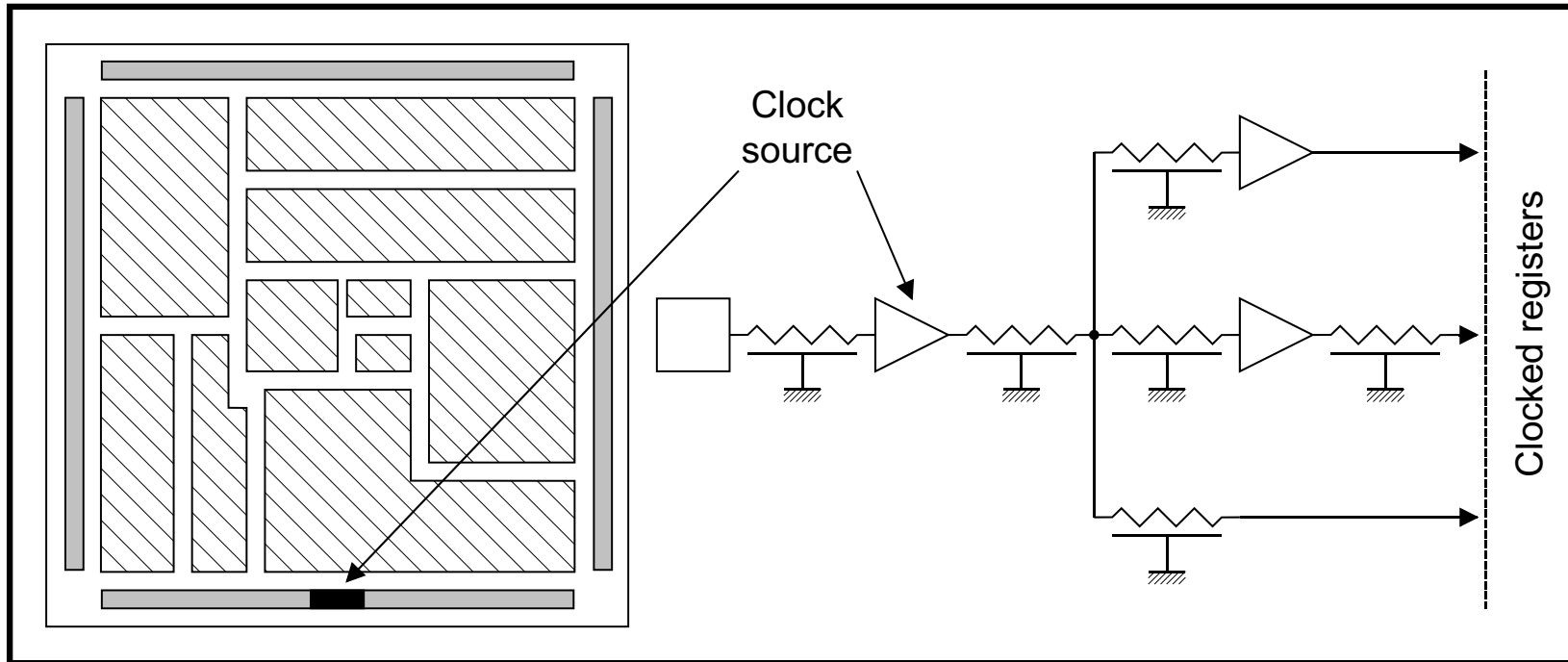
- **Clock buffers:**
  - Amplify the clock signal degraded by the interconnect impedance
  - Isolate the local clock lines from upstream load impedances

Clock distribution

Balanced clock tree

Clock source

Clocked registers

Clock buffer

Clock source