The Abdus Salam
International Centre for Theoretical Physics

United Nations
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2177-24

ICTP Latin-American Basic Course on FPGA Design for Scientific Instrumentation

15 - 31 March 2010

ALICE
Silicon Pixel Trigger

KLUGE Alexander
CERN
Geneva
Switzerland

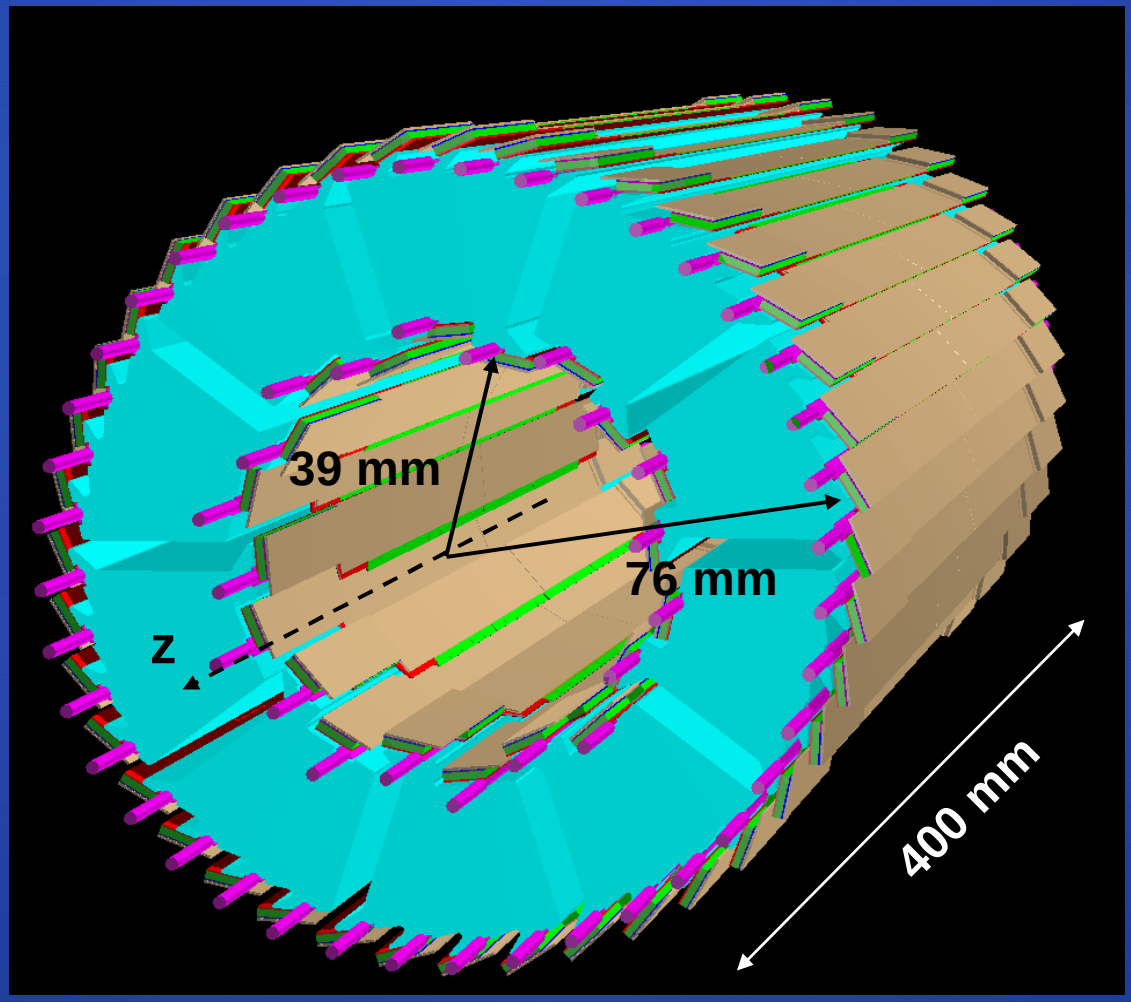
ALICE
Silicon Pixel Trigger

presented by A. Kluge
CERN/PH-ESE
March 17, 2009

Slides by G. Aglieri Rinella[a], A. Kluge[a],

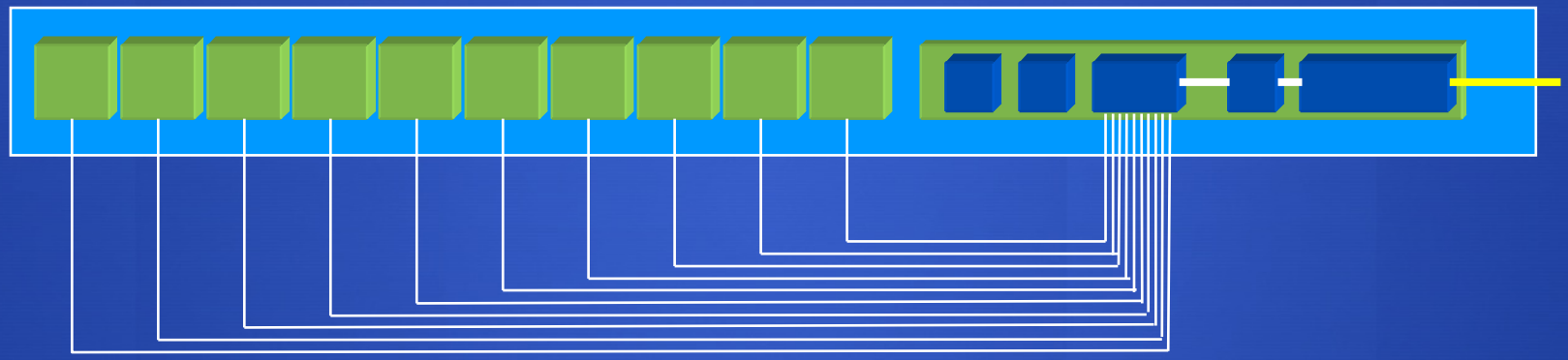
[a] CERN, Geneva Switzerland

ALICE Silicon Pixel Detector



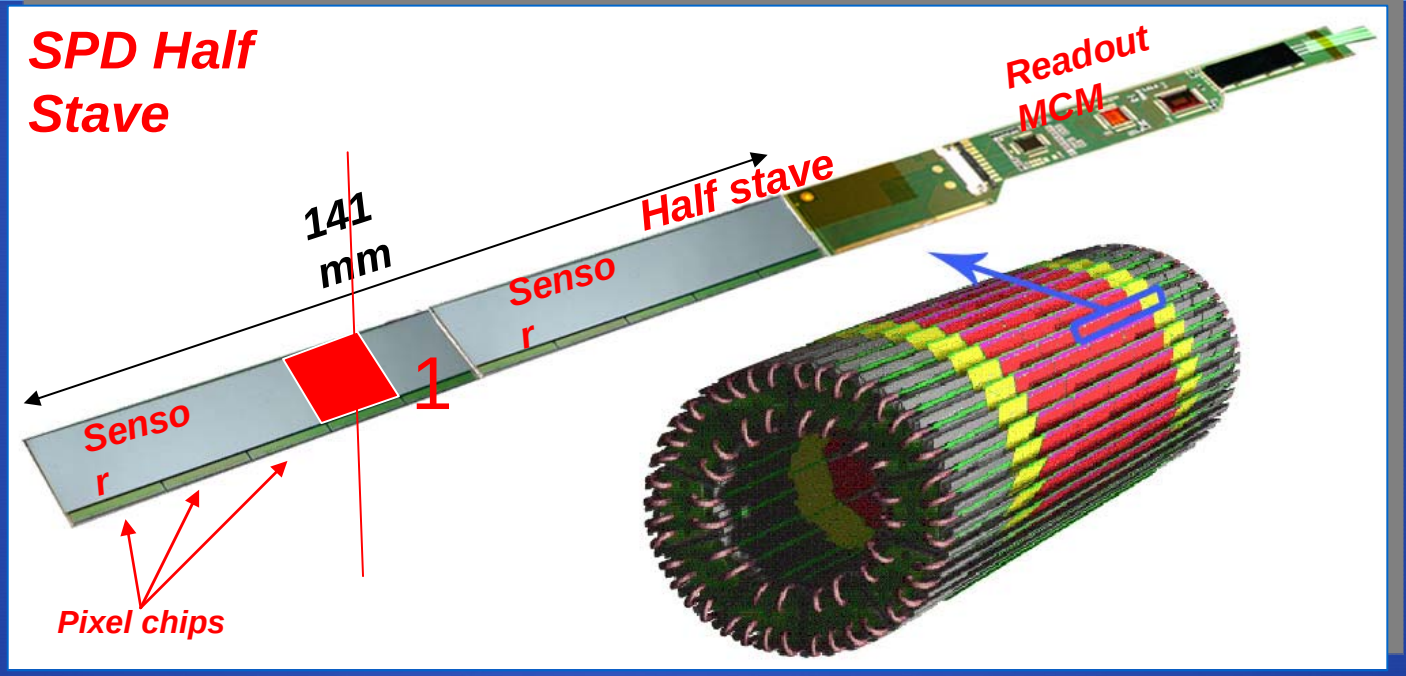
A. Kluge G. Aglieri Rinella

FastOr & Detector module



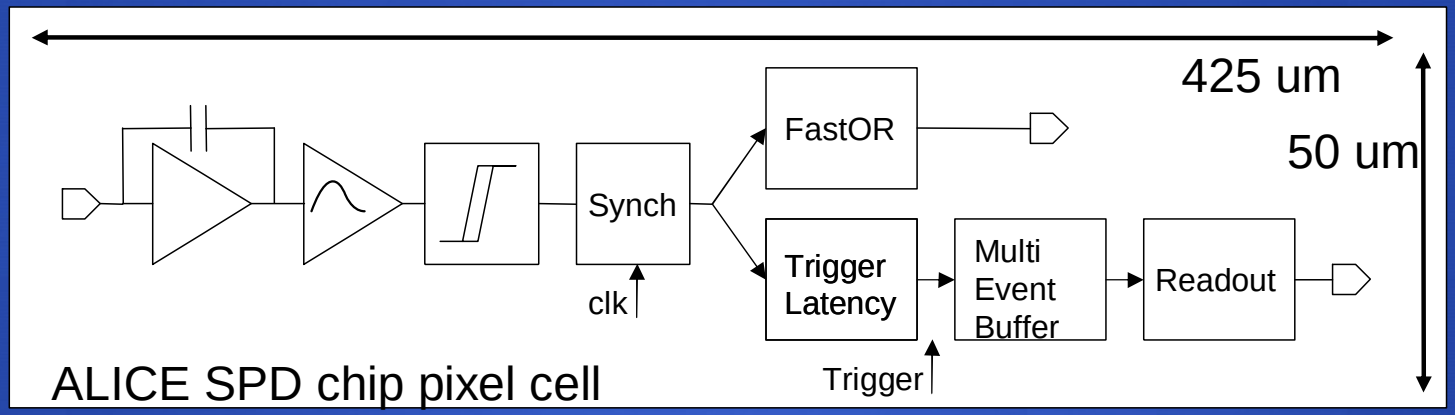
120 x half staves each 10 bit fastOr

Silicon Pixel Trigger

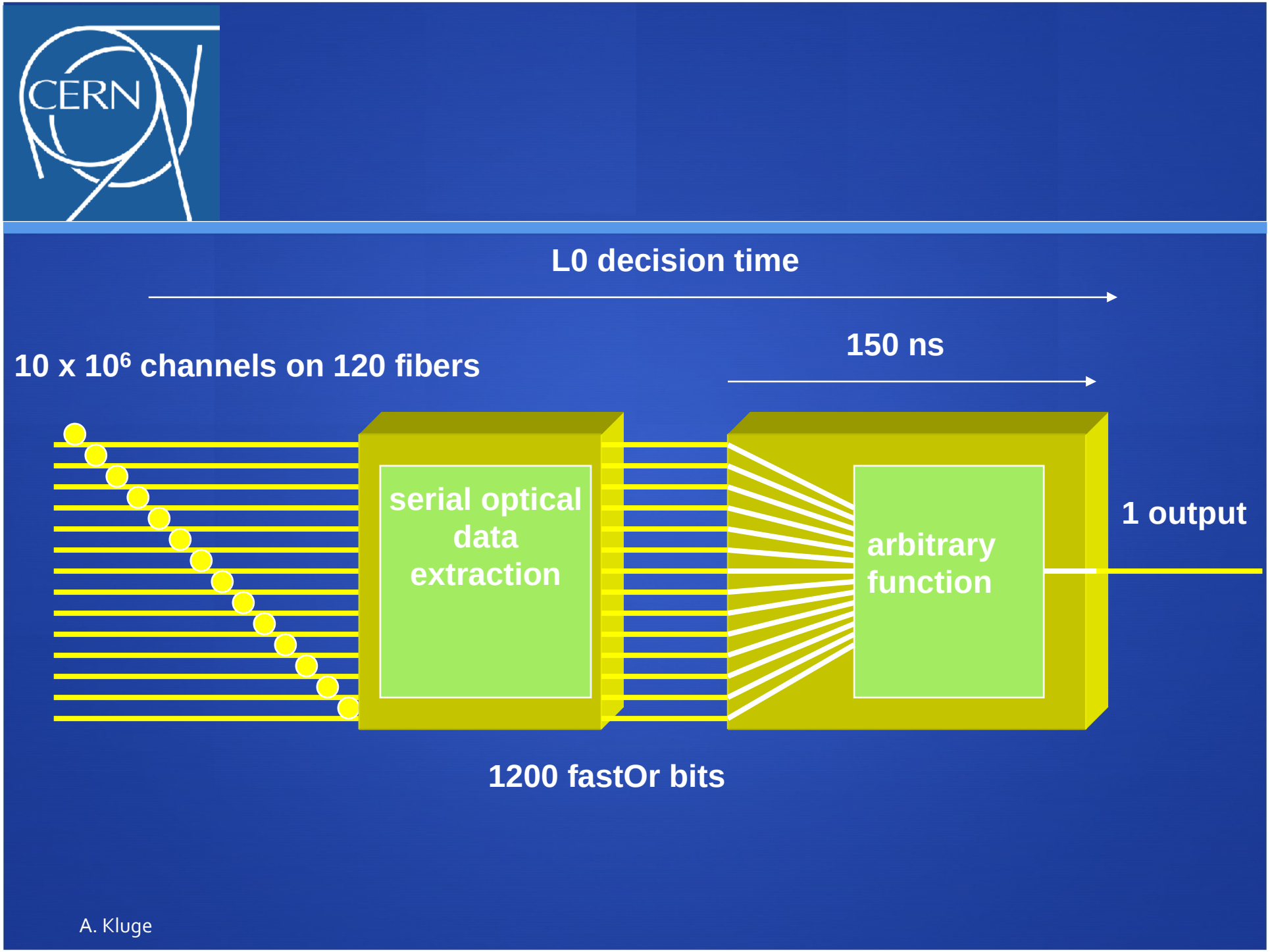


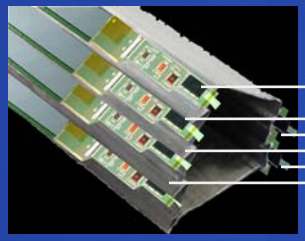
- Front end chip provides prompt FastOR
- Active if at least one pixel in the chip is hit
- Transmitted every 100 ns
- 10 FastOR bits transmitted on each readout fiber -> 120 fibers * 10 * 10 MHz = 12 Gb/s

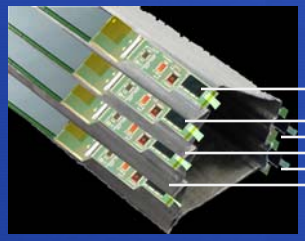
Frontend

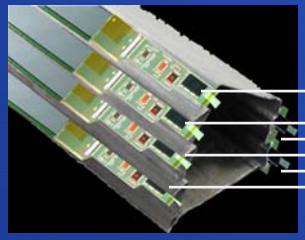


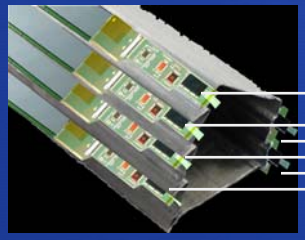
- Dedicated FastOR circuitry follows synchronizer
- Two data streams
- High resolution pixel detector
- Low latency PAD detector
- 1200 pads of 13x14 mm2


L0 decision time
150 ns
10 x 10^6 channels on 120 fibers
serial optical data extraction
arbitrary function
1 output
1200 fastOr bits

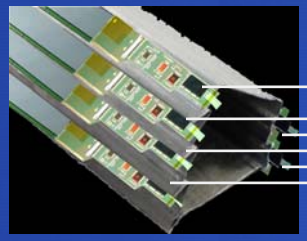
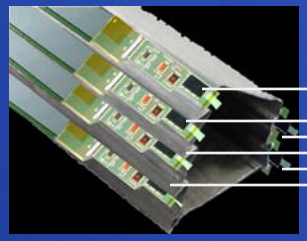
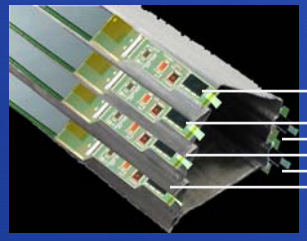
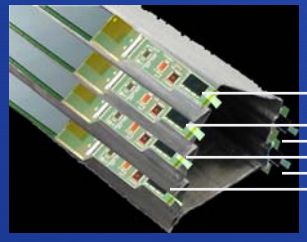








Processor

Data extractor

Data extractor

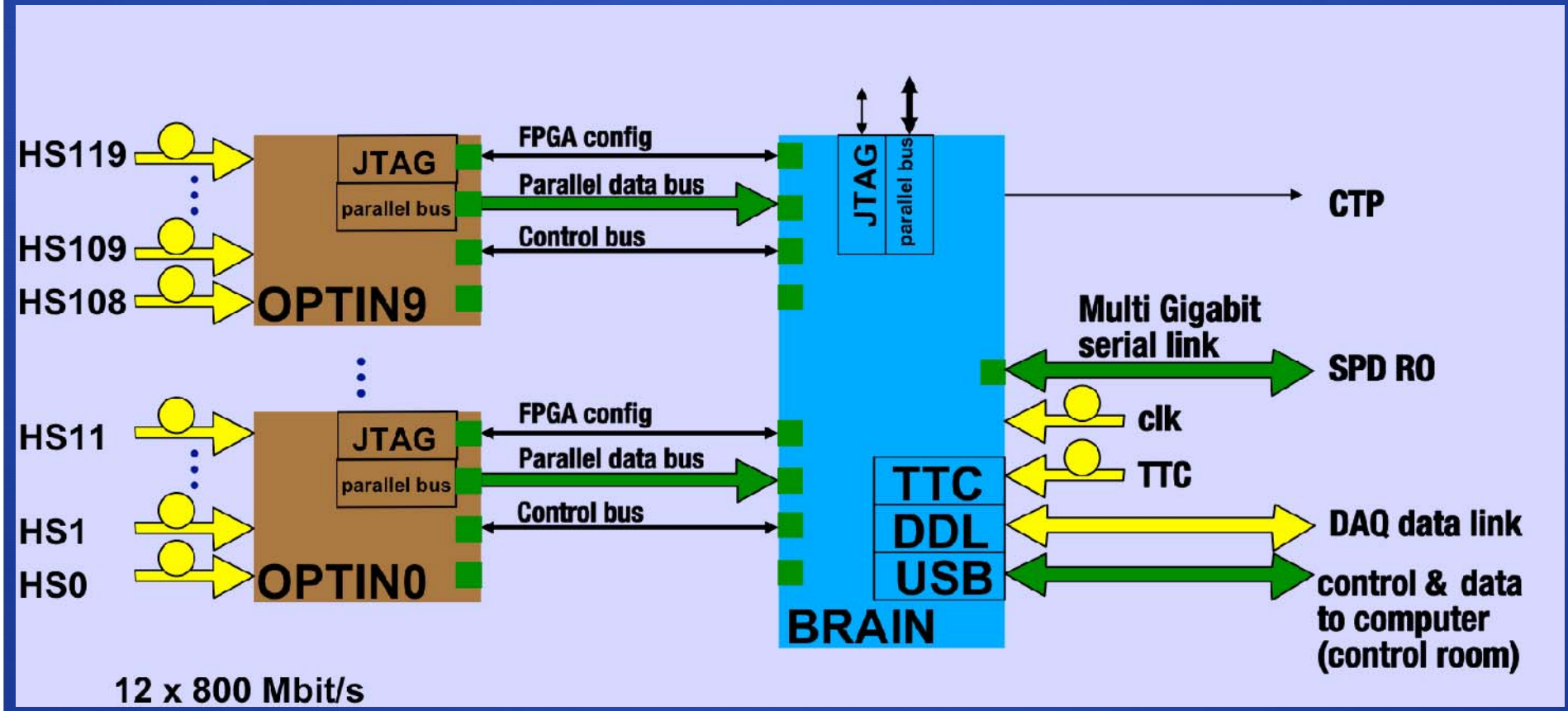
Data extractor

Data extractor

Processor

A. Kluge

Silicon Pixel Trigger block diagram



Algorithms

- Pre-process low latency Fast-OR and generate primitives for the Level 0 trigger decision
  - Proton-proton
  - Minimum bias
  - High multiplicity trigger
  - Topological trigger (jets)
  - Heavy ions
  - Selection of impact parameter
- Algorithms
  - Boolean functions of 1200 bits
    - Look up tables
  - Occupancy (multiplicity)

Pixel Trigger Cosmic Algorithm

- Can be selected from Control Room out of the following
  - TOP_outer *and* BOTTOM_outer
  - OR_OUTER *and* OR_INNER
  - DLAYER (≥2 FOs in the INNER *and* ≥2 FOs in the OUTER)
  - TOP_outer *and* BOTTOM_outer *and* TOP_inner *and* BOTTOM_inner
  - TOP_outer *and* BOTTOM_outer *and* OR_INNER
  - GLOBAL_OR

ALICE Technical Forum.
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Advanced trigger algorithms

- Combinational (boolean AND/OR) functions of 1200 Fast-OR bits
  - Occupancy (multiplicity)
  - Coincidence trigger (topology)
- Not possible: iterative algorithms on data set

Example: vertex trigger

- Pseudo-Tracklet: one chip hit on inner and one on outer layer, in line with region +/-10 cm around vertex
- Chip map for pixel trigger electronics calculated from simulation: (L11,L21), (L12, L22), … , (L1n, L2n)
- FPGA *looks for at least 1 out of 11000* pseudo-tracklets
  - Processing time 12.4 ns (Xilinx ISE)
  - 4% of FPGA resources (Xilinx ISE)
- FPGA *counts* how many out of 11000 tracklets are present
  - ~27 ns processing time (Xilinx ISE)
  - 5% of FPGA resources (Xilinx ISE)

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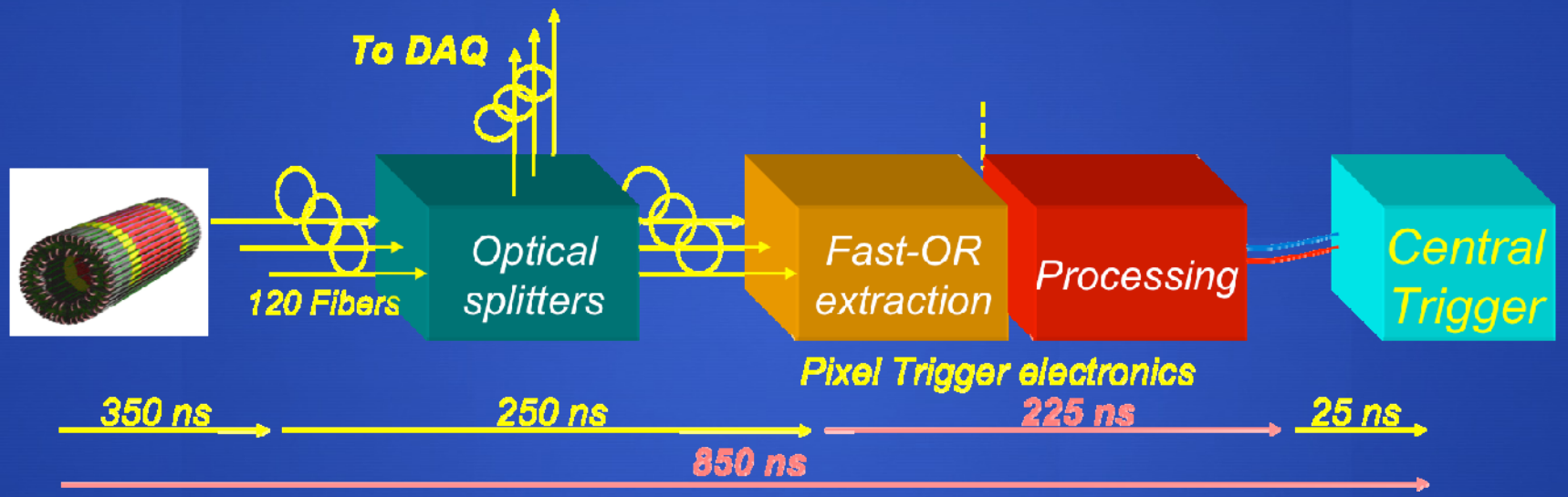
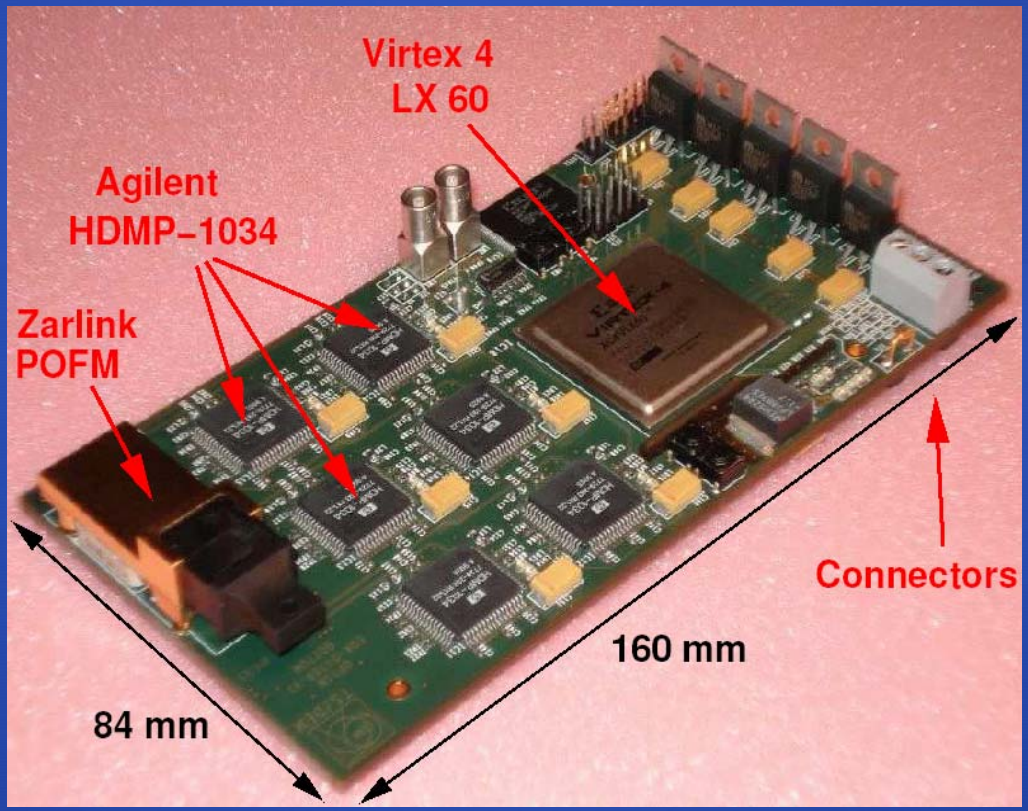
Pixel trigger system



- Extract and synchronize 1200 FastOR bits every 100 ns
- Process algorithm
- User defined and programmable
- Transmit result

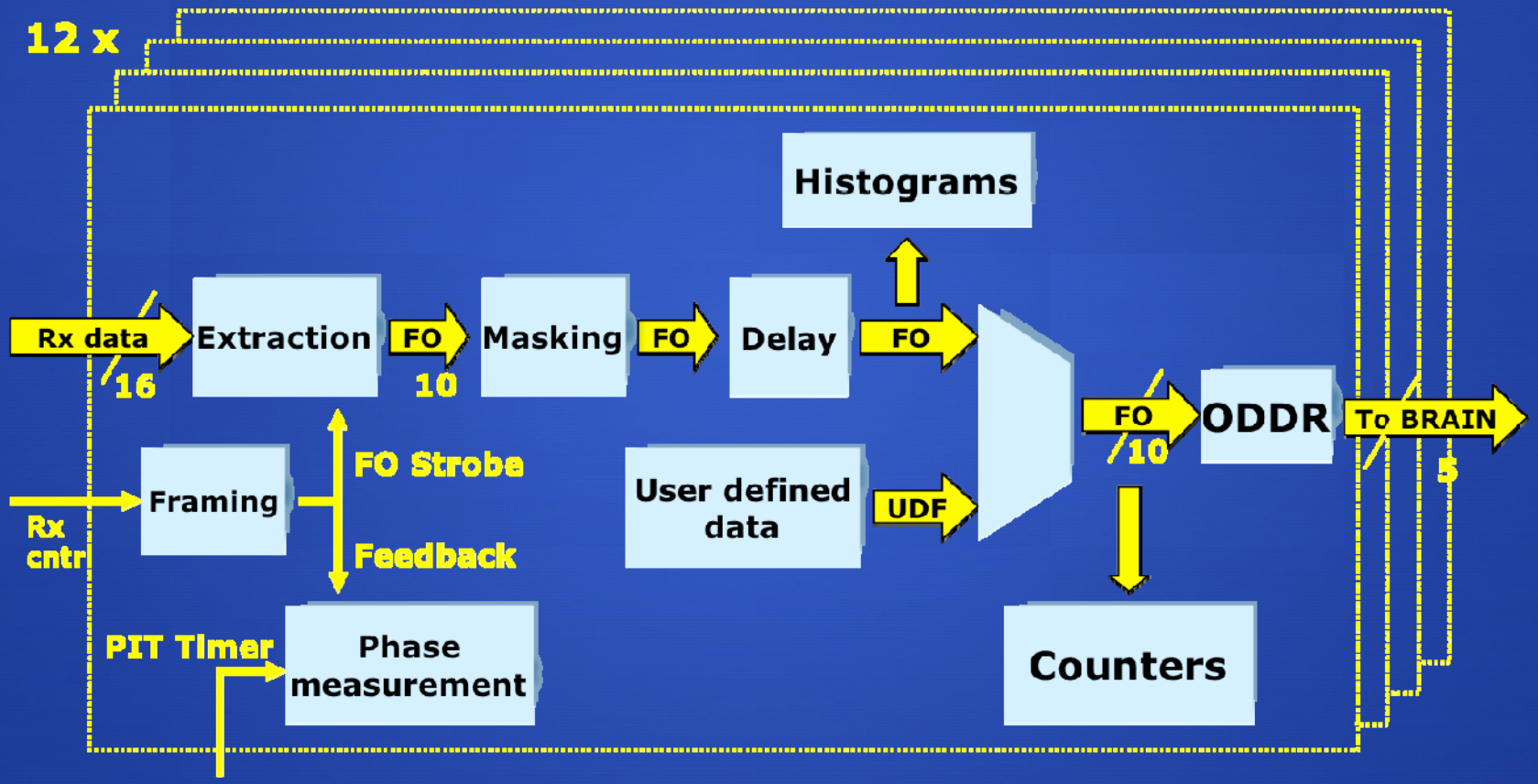
- Overall latency 850 ns
- Bottleneck is deserialization
- Independent from the data readout electronics
- Space constraint (one 9U crate)

OPTIN card



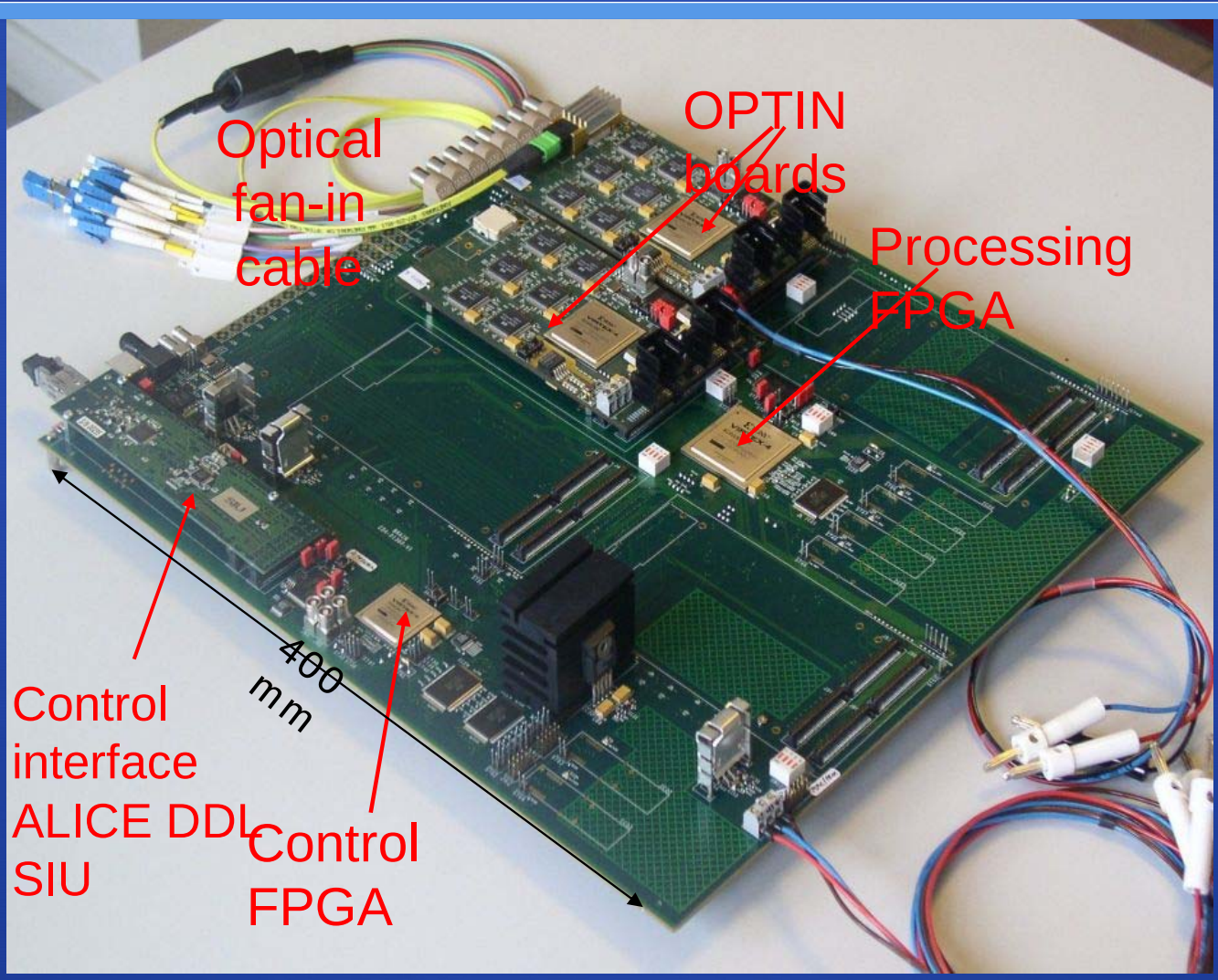
- 12 Channels
- Custom Parallel Optical Receiver Module
- 12 G-Link deserializer ASICs closely packed
- FPGA (60k logic cells)

Optin board channels

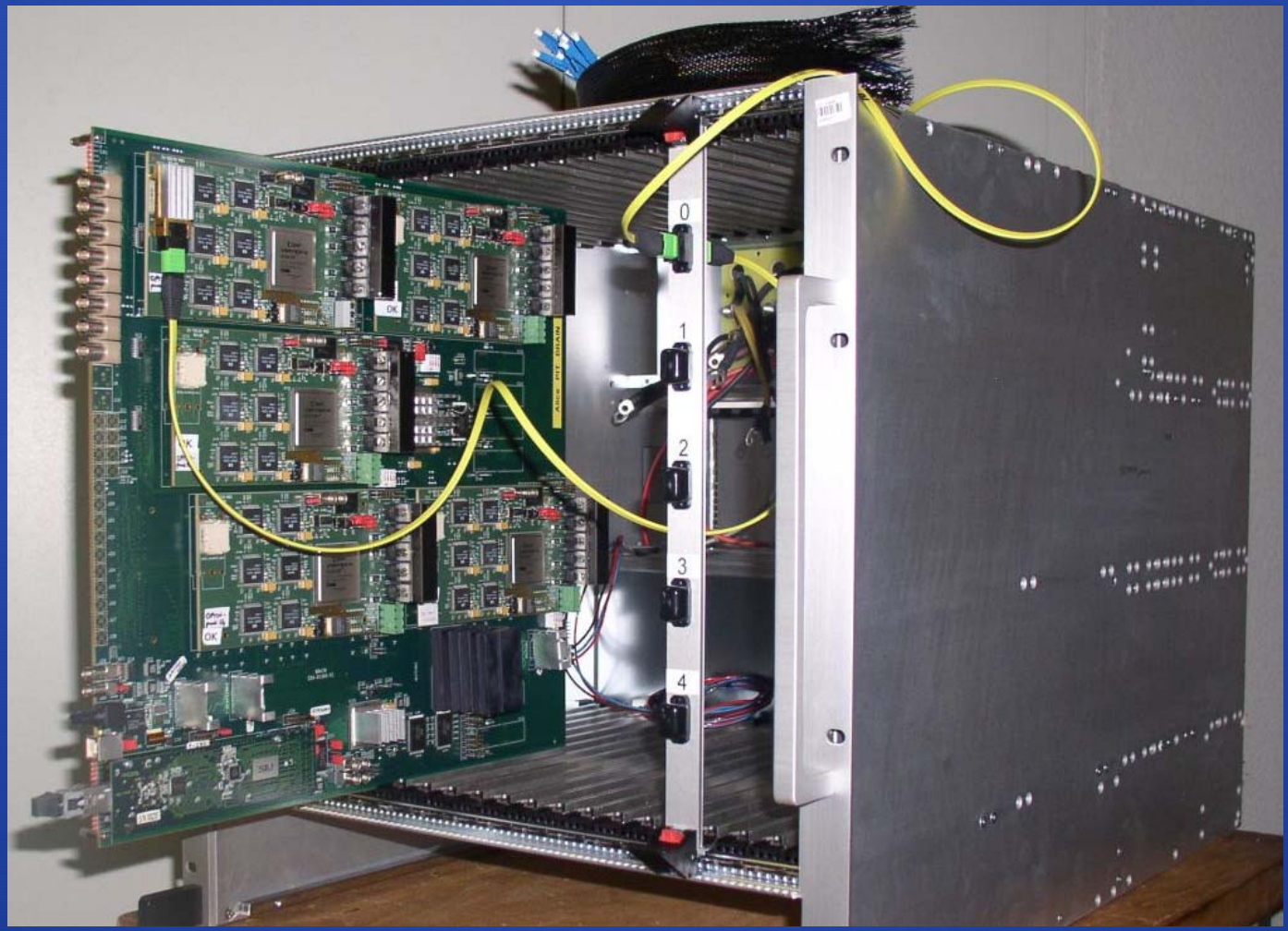


- FastOR extraction, masking, time alignment
- Data quality checks: counters and histograms

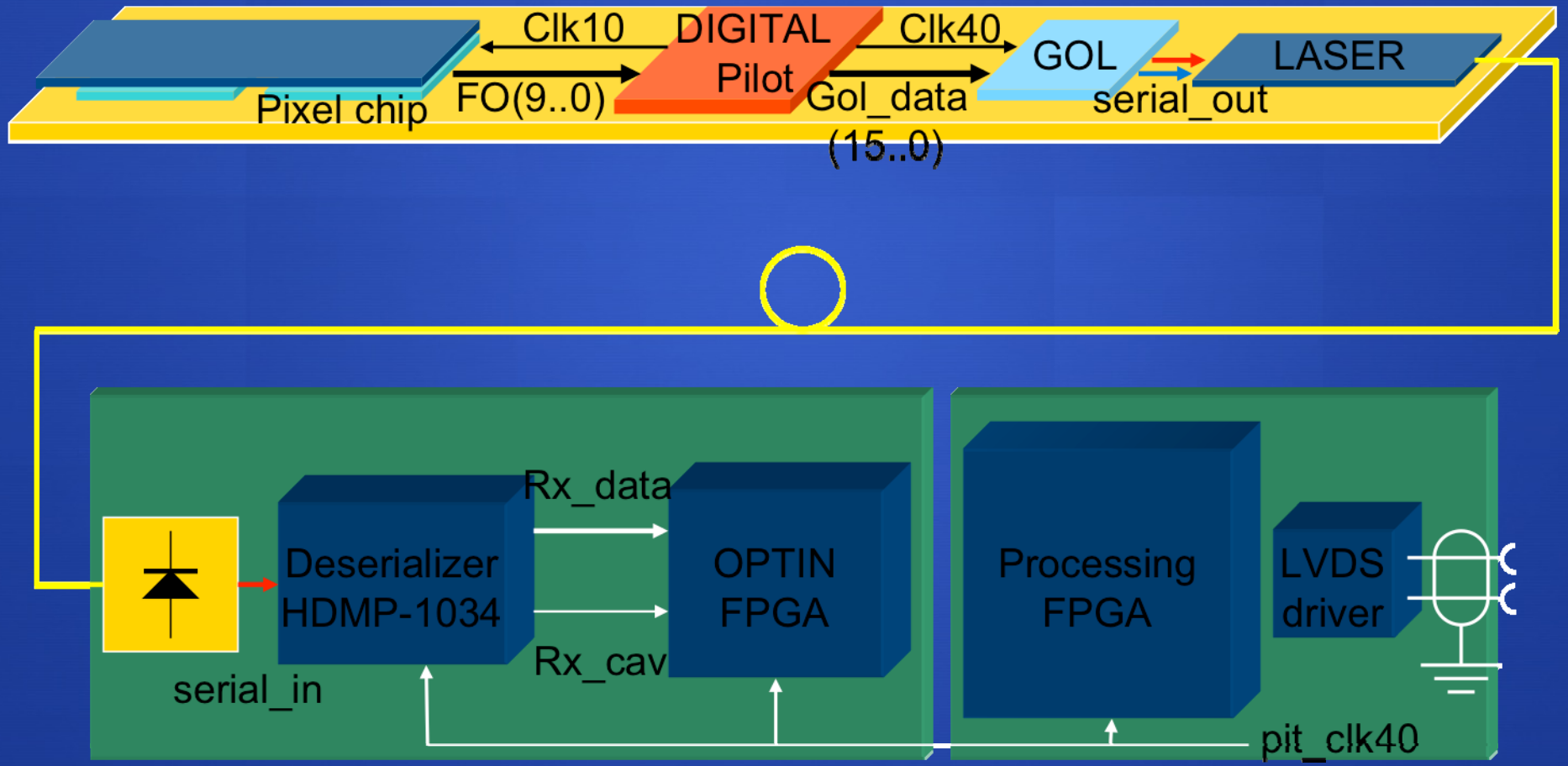
processing board - BRAIN



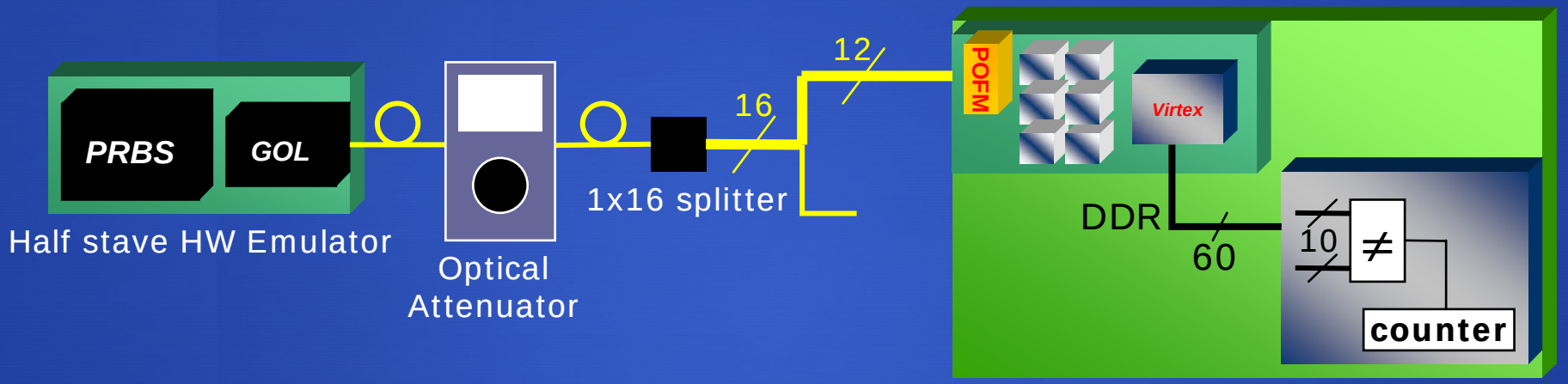
Pixel trigger crate



Full system VHDL simulation



Bit error rate test



	Duration	N_{bits}	Errors	BER (99% c. l.)
Typical	1.5 hrs	$5.7 \cdot 10^{12}$	0	**$< 8.1 \cdot 10^{-13}$**
Max	17.8 hrs	$7.7 \cdot 10^{13}$	0	**$< 6 \cdot 10^{-14}$**

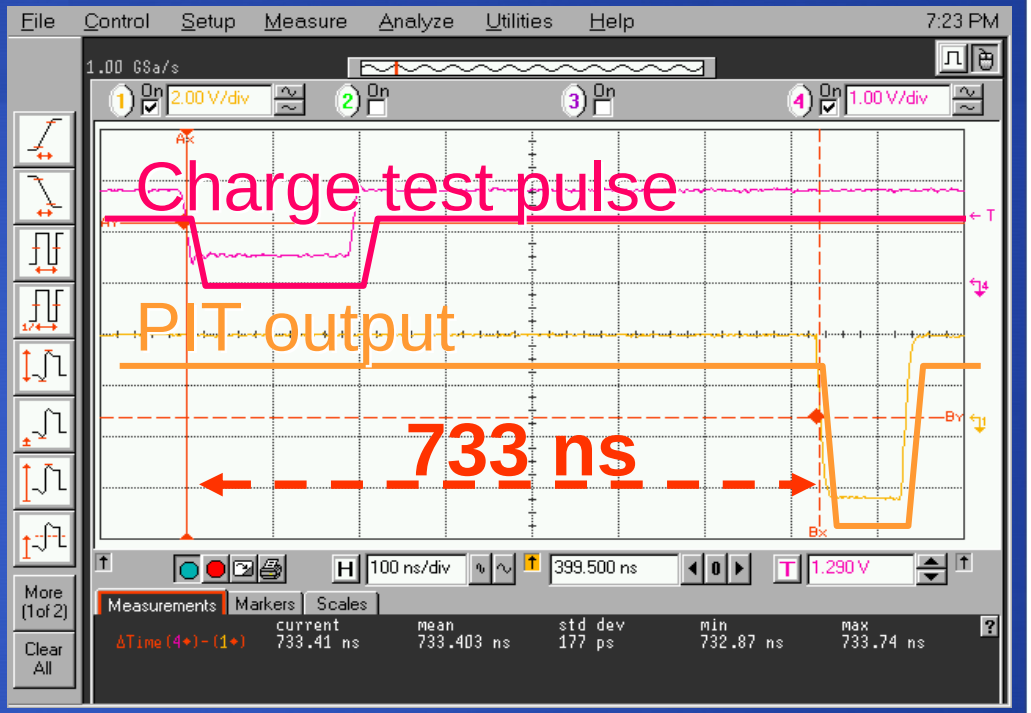
- **Full Fast OR data path Bit Error Rate test**
- **12 channels in parallel, pseudo random data**
- **Optical power: -18.5 dBm, 0.5 dBm margin**

- Remote reconfiguration of the FPGA
- Automatic configuration from database
- Advanced algorithms
- Diagnosis tools (snapshot memory)

Latency

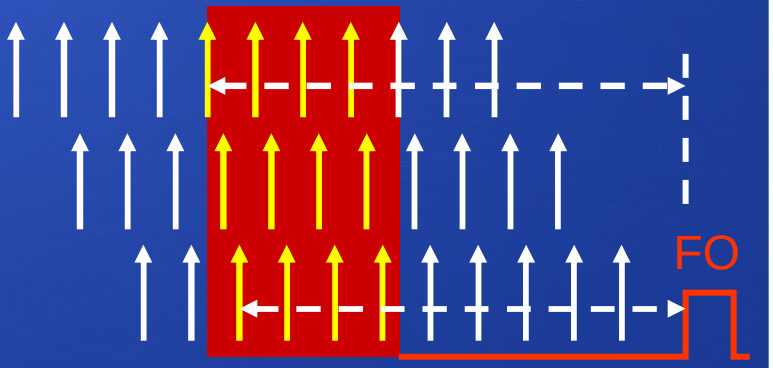
- Measurement in the laboratory

- In ALICE:
  - 733
    + 16 (longer fibers)
    + 25 (wire to CTP)
    =774 ns

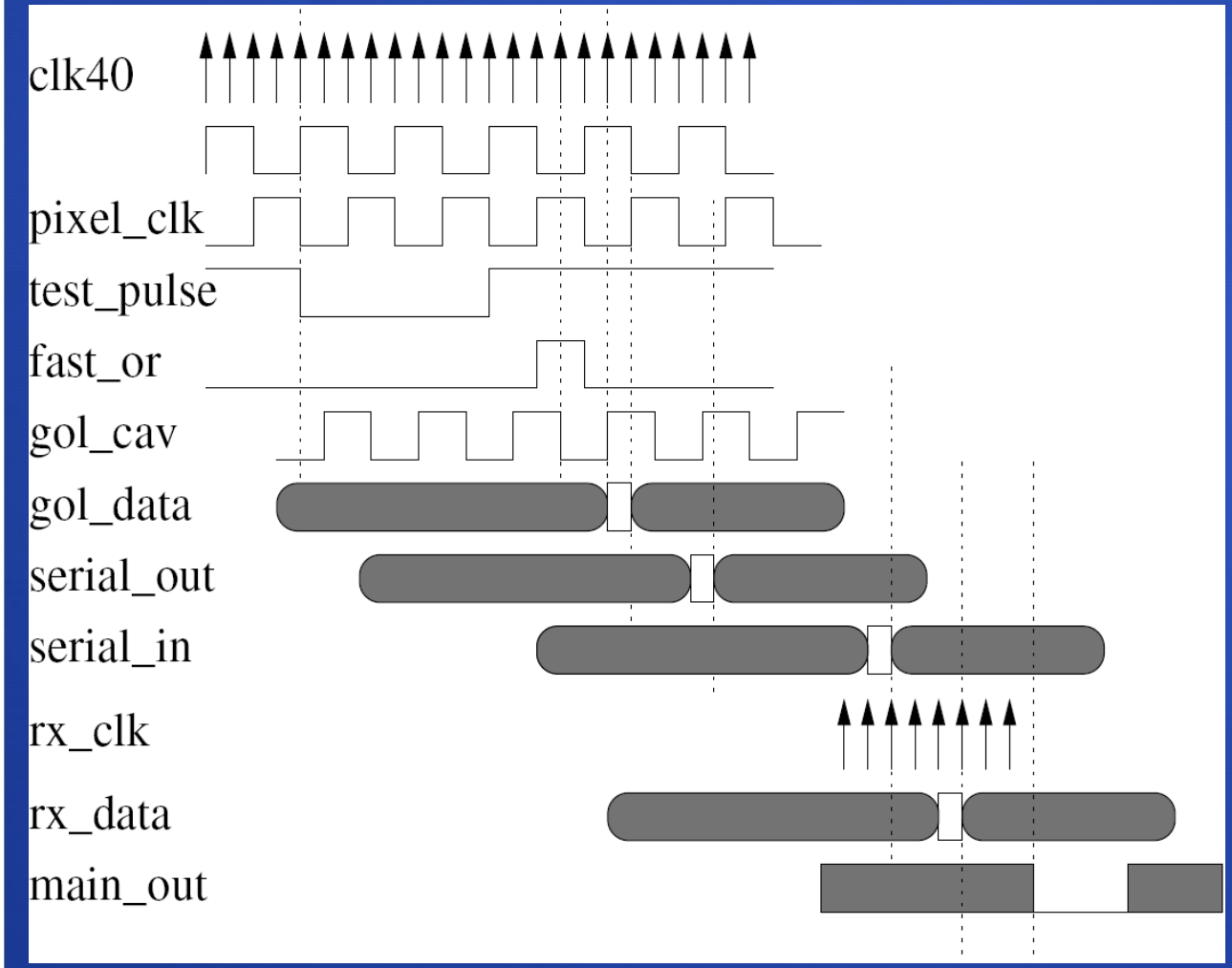


- From Bunch Crossing
  - MIN 724 ns
  - MAX 824 ns

  - Uncertainty of +- 12.5 ns
    - Needs fine clock tuning with beam



Overall latency



Pixel chip	250 +
Digital Pilot	75 +
Clock out-in	25 +
GOL	85 +
Fiber	180 +
Agilent HDMP1034	75 +
Pixel Trigger	75
	-------
	765 ns

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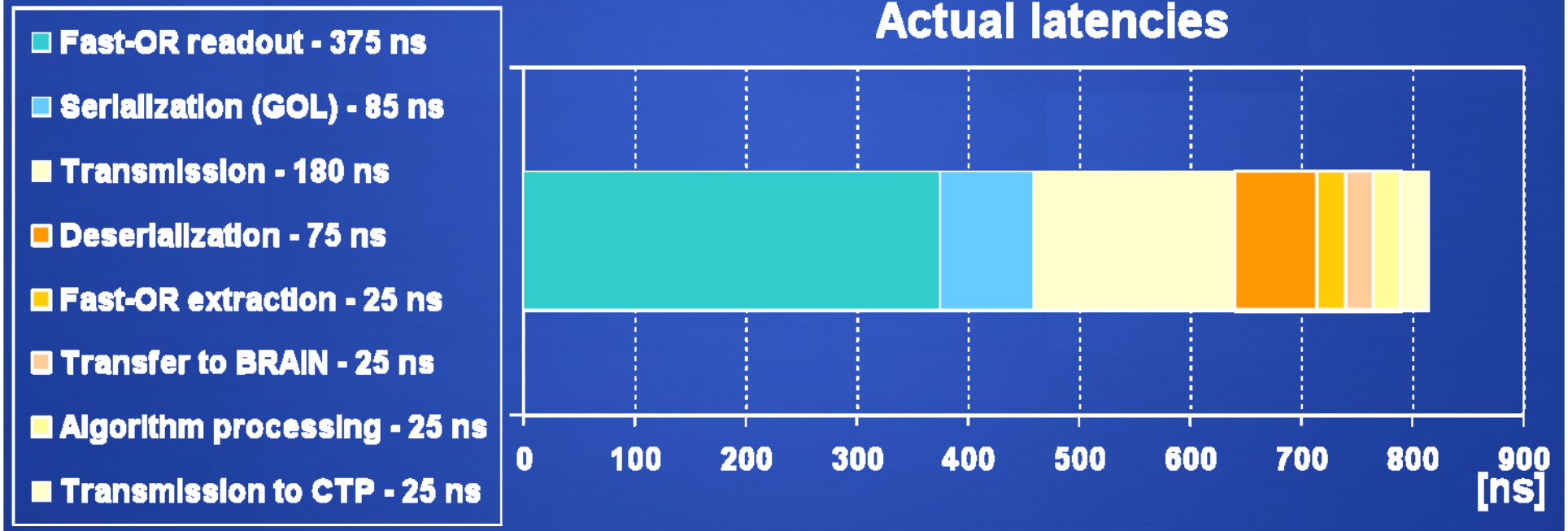
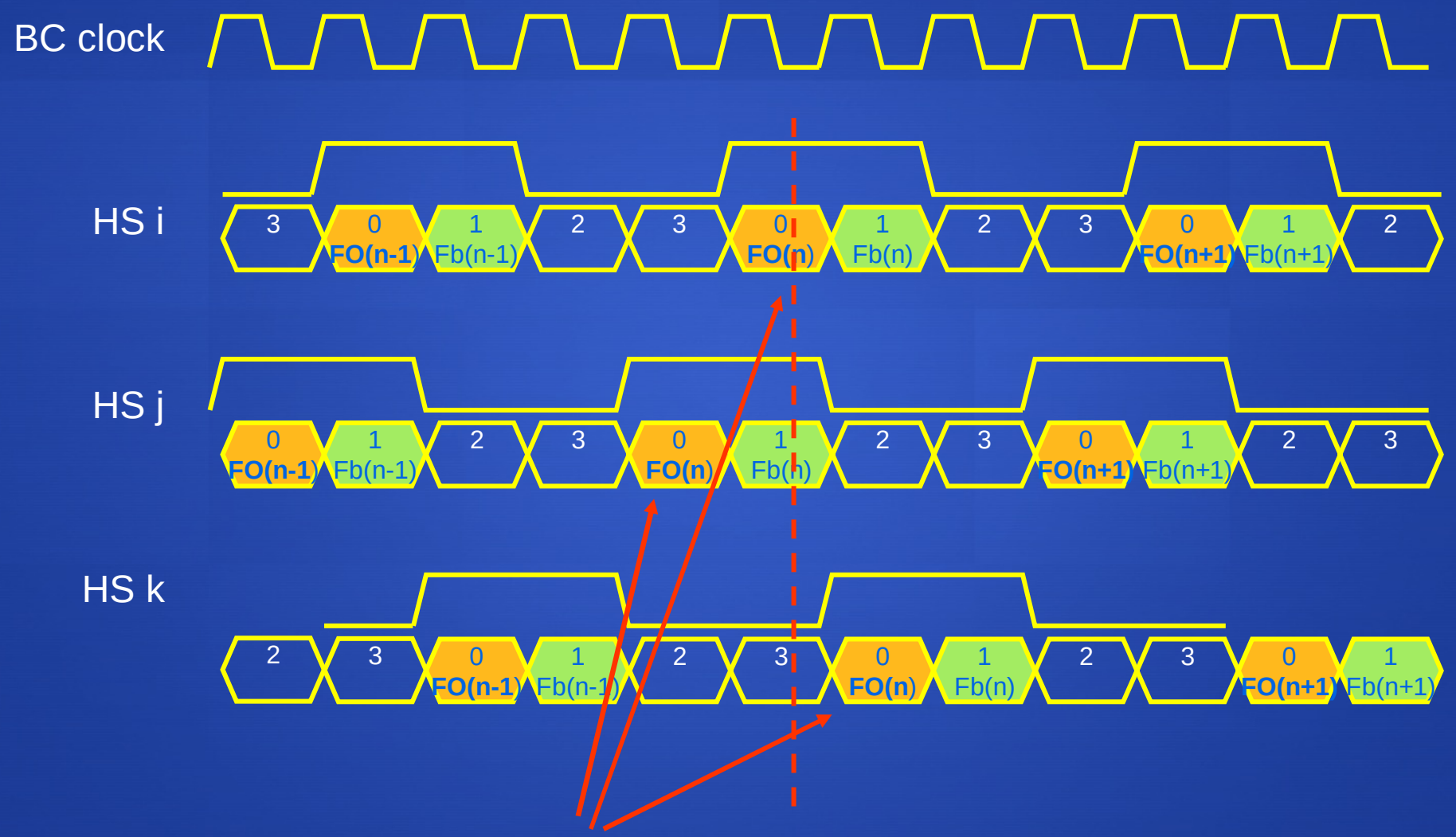
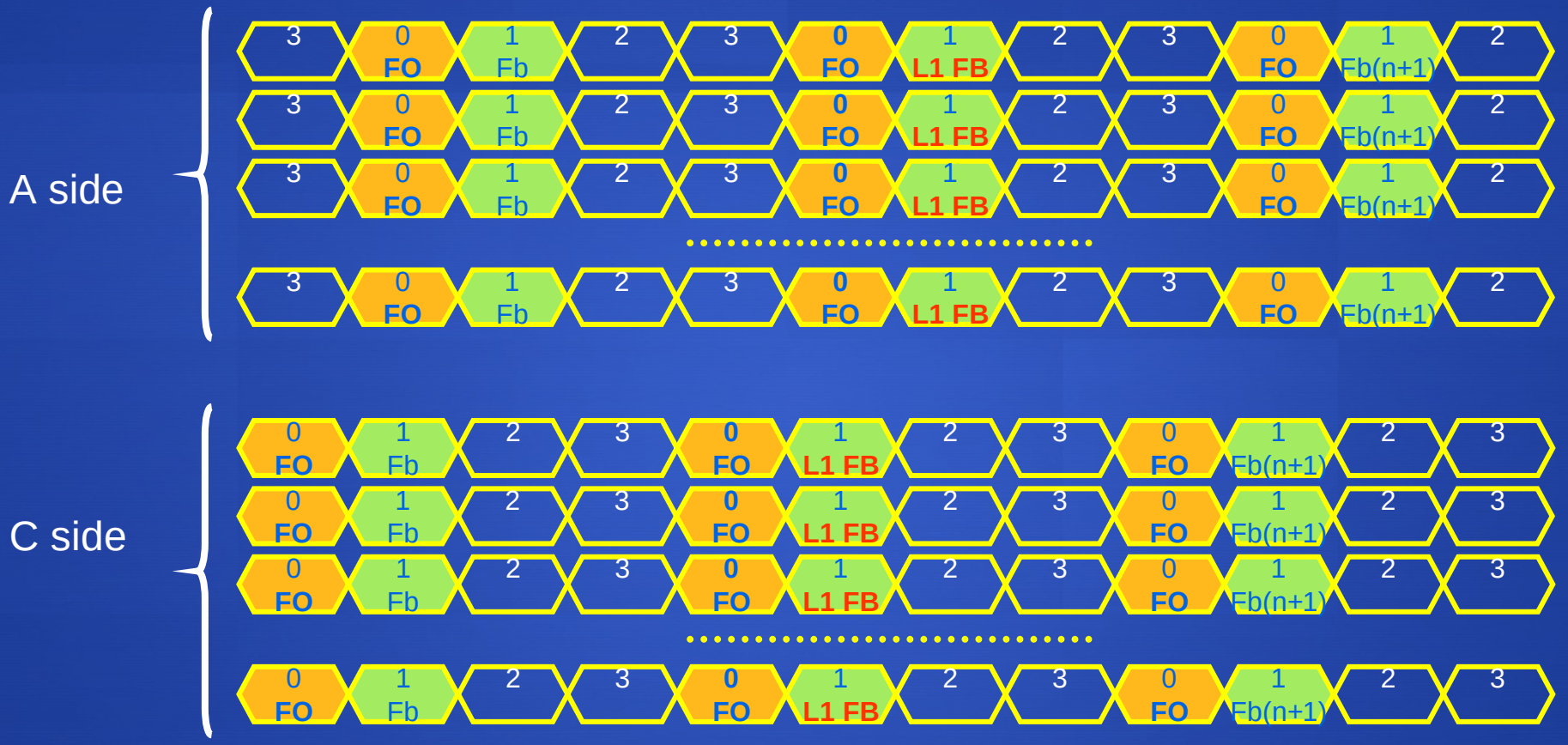
Latency

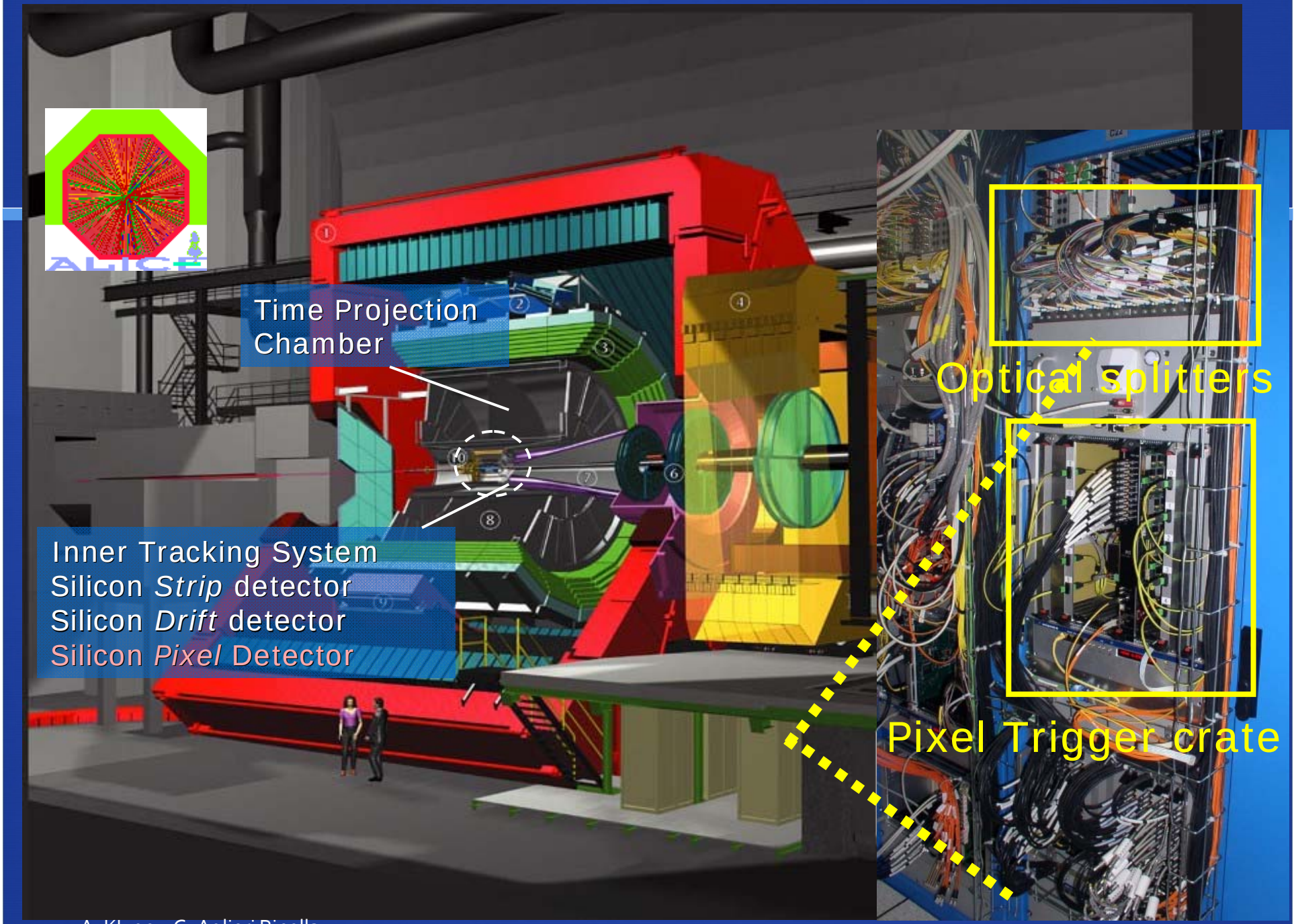

Fast-OR readout - 375 ns
Serialization (GOL) - 85 ns
Transmission - 180 ns
Deserialization - 75 ns
Fast-OR extraction - 25 ns
Transfer to BRAIN - 25 ns
Algorithm processing - 25 ns
Transmission to CTP - 25 ns
Actual latencies
0
100
200
300
400
500
600
700
800
900
[ns]

Non synchronous frames



Frames aligned




Time Projection Chamber
Inner Tracking System
Silicon *Strip* detector
Silicon *Drift* detector
Silicon *Pixel* Detector
Optical splitters
Pixel Trigger crate

Installation in ALICE

TTC

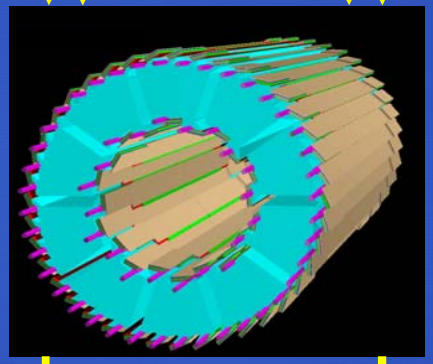
107.6±0.15 m

Clk
Serial

C.R.

60

C
side



A
side

36.6±0.2 m

Data

Optical
splitters

38.5±0.2 m

Central Trigger
Processor

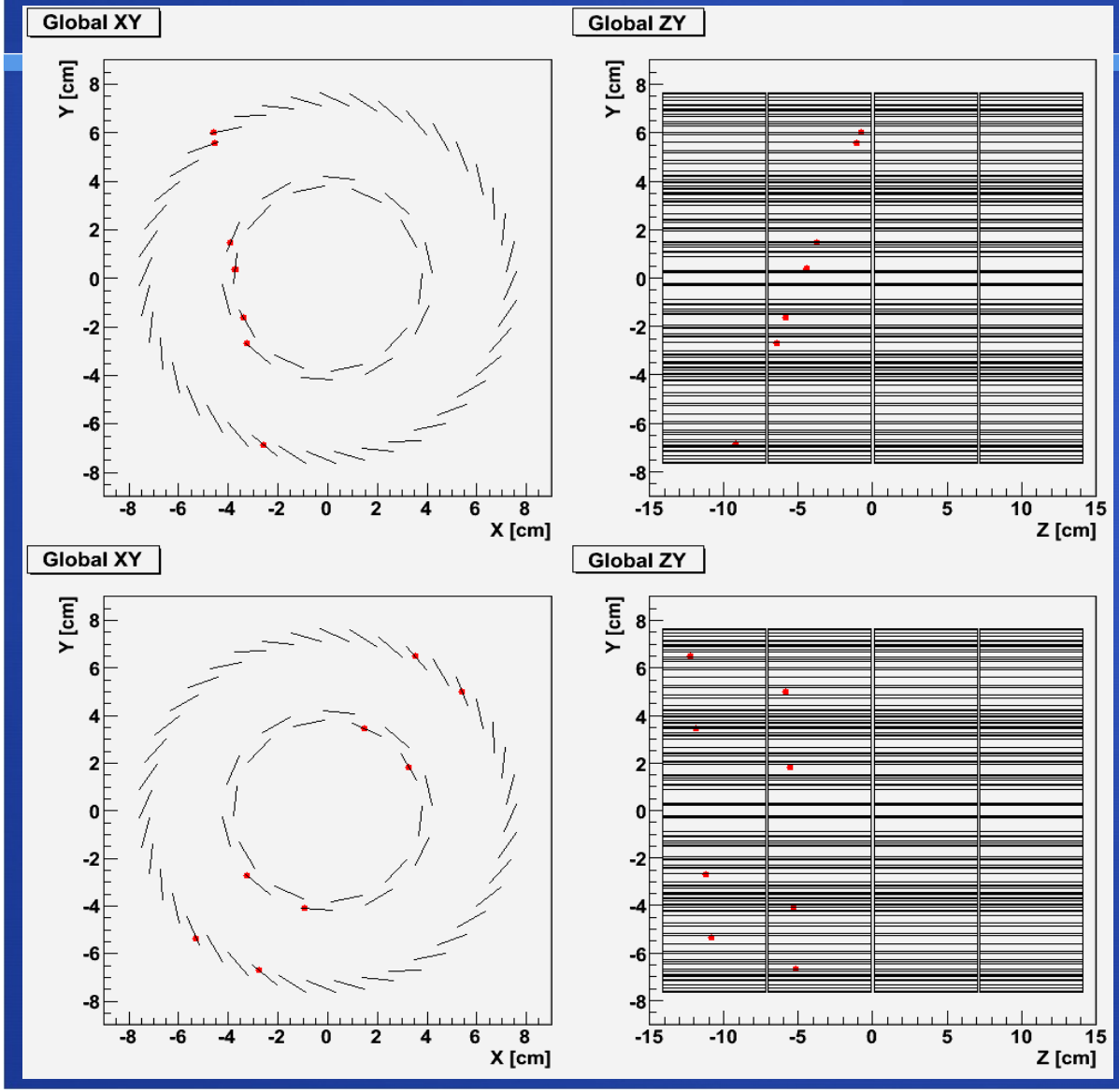
LTU

L0 in

PIT main outputs

TTC

Cosmic ray detection

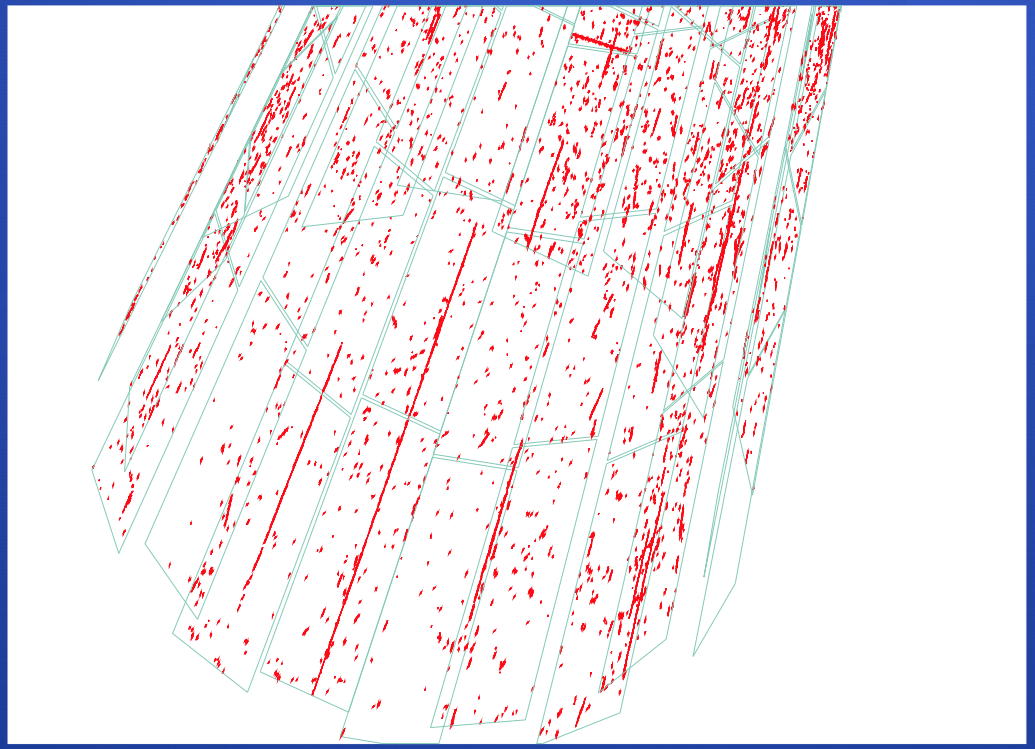


- Pixel Trigger extensively used during ALICE commissioning with cosmic data
- SPD only
- Inner Tracking (SPD+SSD+SDD)
- ITS, TPC, TOF, ECAL

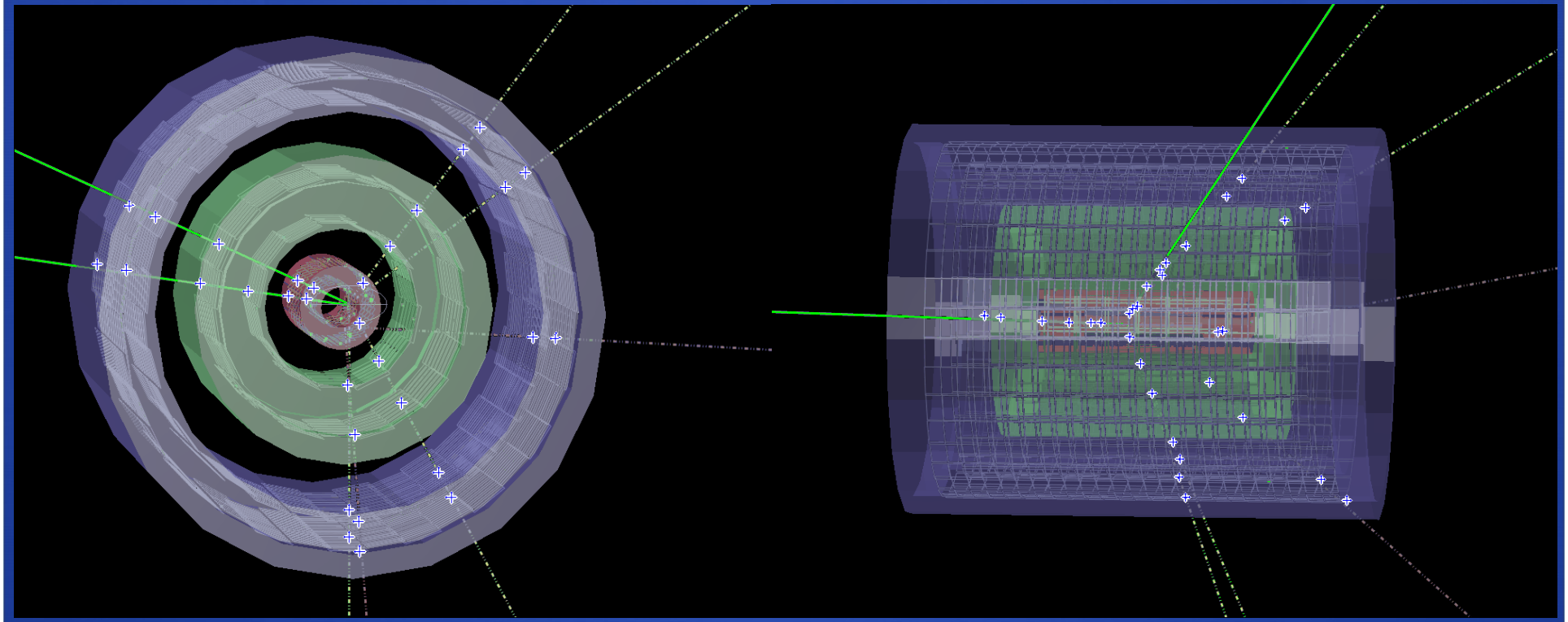
- Alignment data
- 105 events > 3 SPD clusters
- Showers

LHC beam injection test

- August 2008: ALICE SPD was recording data self-triggering via the Pixel Trigger System
- The first "LHC related particles" were detected



Beam events



- Events from LHC circulating beam
  - 11th September 2009

Silicon Pixel Trigger References

- G. Aglieri Rinella et al., "The Level 0 Pixel Trigger system for the ALICE experiment", Journal of Instrumentation JINST 2P01007 and Proceedings of the 12th Workshop on Electronics for LHC and Future Experiments, LECC06, September 2006, Valencia, Spain
- A. Kluge et al., "The ALICE Silicon Pixel Detector", Nuclear Instruments and Methods A, Volume 582, Issue 3, 1 December 2007, Pages 728-73
- ALICE collaboration, "ALICE physics Performance Report", CERN-LHCC-2003-049, J. Phys., G30 (2004) 1517-1763
- J. Conrad et al., "Minimum Bias Triggers in Proton-Proton collisions with the VZERO and Silicon Pixel Detectors", ALICE Internal note, ALICE-INT-2005-025, 19/10/2005