The Abdus Salam
International Centre
for Theoretical Physics

smr2499

International Training Workshop on FPGA Design for Scientific Instrumentation and Computing

11 November – 22 November 2013

Trieste – Italy

LABORATORY EXERCISES I

COMBINATIONAL AND SEQUENTIAL LOGIC DESCRIBED in VHDL

VHDL Description, Synthesis and Simulation

ICTP Multidisciplinary Laboratory
MLAB

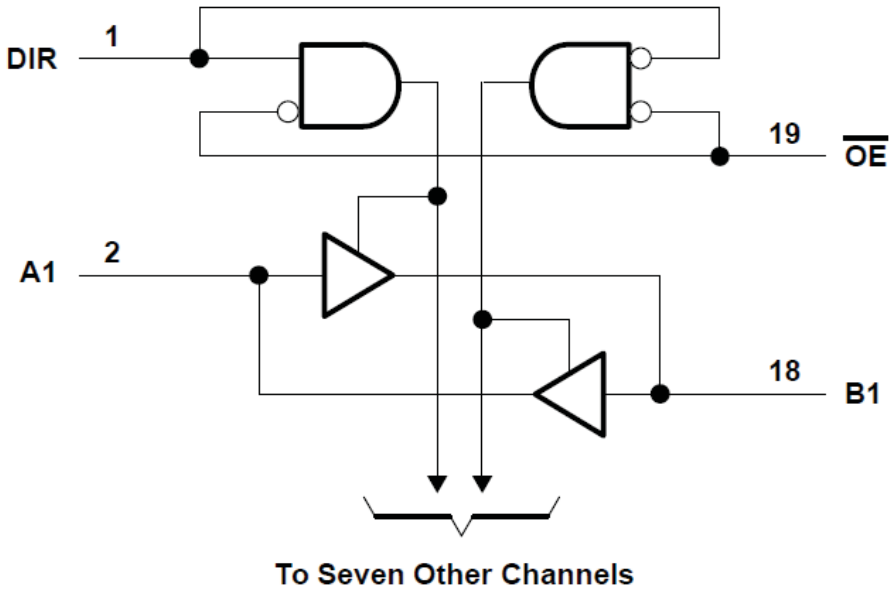
Exercise 1

Design a 3 to 8 decoder using concurrent instructions (*enable:* active high).
Create a *testbench* and simulate your design.

Exercise 2

Design the bidirectional buffer: 74AS245, based on the table and logic circuit shown below:

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



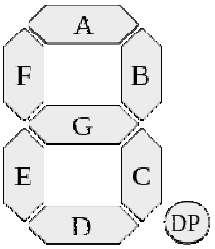
Write a generic code, using parameters, to be easily modified to increase or decrease the number of I/O.
Create a *testbench* and simulate your design.

Exercise 3

Design a hexadecimal to 7-segment decoder with the following I/O:

- Four-bit input
- Active high enable
- Seven outputs indexed from ‘a’ to ‘g’ that correspond to each segment of the *display.* Each segment is active low.

The figure below details the position of each segment in the *display:*



Create a *testbench* and simulate your design.

Exercise 4

Design a Hexadecimal counter (0-F) with the following inputs:

- Clock
- Reset (asynchronous)
- Enable: When enable is high then count else keep last value

Create a *testbench* and simulate your design.

Note: Use ***ieee.numeric_std.all***

Exercise 5

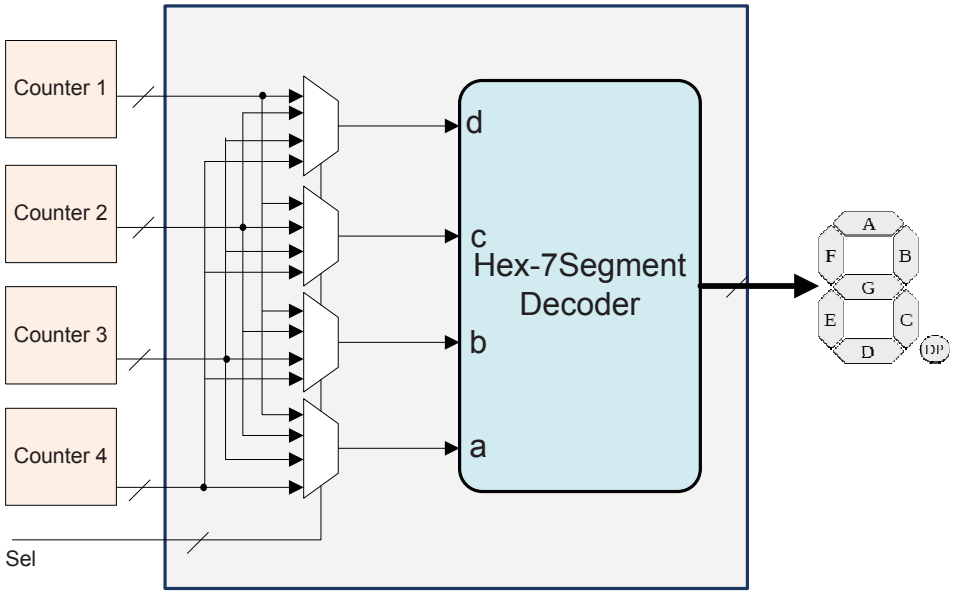
Design an Up/Down BCD counter (0-9) with the following inputs:

- Clock
- Reset (asynchronous)
- Enable: When enable is high then count else keep last value.
- Up_Down

Create a *testbench* and simulate your design.

Exercise 6

Design the system shown below using *component-declaration* and *component-instantiation.*



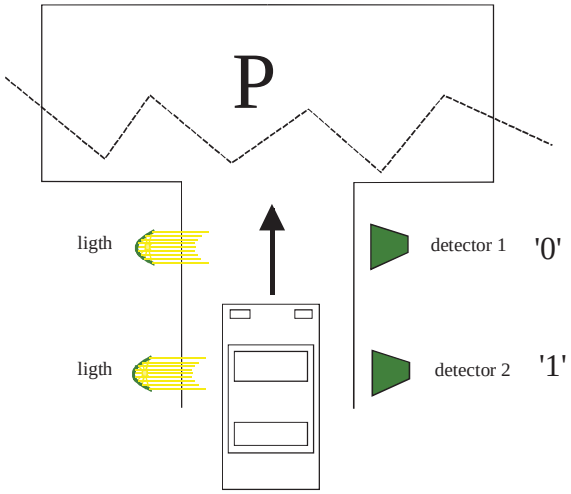
Create a *testbench* and simulate your design.

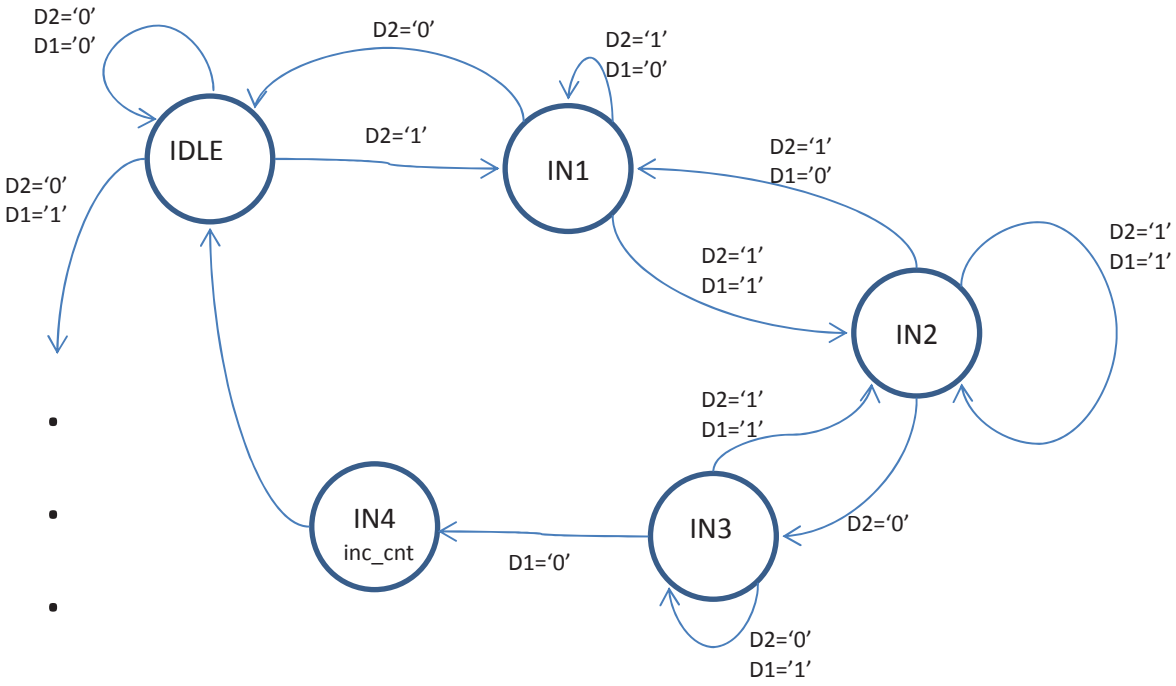
Exercise 7

A parking lot, shown in the figure below, has space for 10 cars. There is only one entrance to the parking lot, consequently one car at a time can enter or exit the parking. There are two light sensors, separated by one meter, in order to detect if the car is entering or leaving the lot. There is a semaphore with signs saying FREE and FULL.

(a) Design and simulate a 'semaphore controller' according to the number of cars at the parking lot (see example below)

(b) The same as previous exercise except that there are an entrance and an exit gate, therefore you have to synchronize the parallel activities using an entrance and an exit semaphore **(optional)**





Example of a car entering to the parking lot