The Abdus Salam
International Centre
for Theoretical Physics

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International Training Workshop on FPGA Design for Scientific Instrumentation and Computing

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LABORATORY EXERCISES III

DIGITAL SIGNAL PROCESSING

with FPGA

ICTP Multidisciplinary Laboratory
MLAB

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Exercise 1

Design, synthesize and implement in the *FPGA Spartan 3E of the Nexys 2 board*, a system that, using the PMOD AD1 and PMOD DA1 hardware modules:

1) Give to the output of the PMOD DA1, an analog signal equivalent to the value set with the eight SW7…SW0 *switches* available in the board
2) Show in the eight *LEDs* of the *board,* the analog input of the PMOD AD1 module
3) Reproduce in the output of the PMOD DA1, the analog input of the PMOD AD1 module
4) Use the switches of the board to set the sampling frequency.
   Decrease the sampling frequency below the *Nyquist* rate, observe the output and explain what you are observing (**optional**).

Exercise 2 – Linear Function

Design, synthesize and implement in the *FPGA Spartan 3E of the Nexys 2 board*, using the PMOD AD1 and PMOD DA1 hardware modules, the following linear function:

$$\mathbf{y(t) = a\ x(t) + b}$$

where **x(t)** is the input signal of the PMOD AD1; **a** and **b** are 8-bit constants.

Set the values of the constants using the *switches* and *buttons* of the board.

Using a signal generator, analyze the behavior of the function for different values of **a** and **b.** Select the input signal and the values of the constants without producing overflow in the output.

Exercise 3 – Average Filter

Design, synthesize and implement in the *FPGA Spartan 3E of the Nexys 2 board*, using the PMOD AD1 and PMOD DA1 hardware modules, the following average filter:

$$\mathbf{y_n = (x_n + x_{n-1} + x_{n-2} + \ldots + x_{n-k-1} + x_{n-k})/\ (k+1)}$$

Set the value of '**k+1**' using the *switches* of the board. Use values of '**k+1**' that are power of 2, with a maximum value of **k** equal to 15.

Using a signal generator, analyze the behavior of the filter for different input signals, frequencies and values of **k.**

Exercise 4 – Differentiator

Design, synthesize and implement in the *FPGA Spartan 3E of the Nexys 2 board*, using the PMOD AD1 and PMOD DA1 hardware modules, a differentiator circuit.

The output of the differentiator is the difference between the last two input samples:

$$y(n) = x(n) - x(n-1)$$

Given that the differentiator is too sensitive to signal noise, it is suggested to implement the following function:

$$y(n) = xa(n) - xa(n-k)$$

Where:

xa(n) is the average value of the **k** last samples **{ x(n),x(n-1),…,x(n-k-1) }**, and

xa(n-k) is the average value of the **k** previous samples **{ x(n-k),x(n-k-1),…,x(n-2k-1) }.**

Set the value of **k** using the *switches* of the board or from the PC. Use values of **k** that are power of 2.

Using a signal generator, analyze the behavior of the differentiator for different input signals, frequencies and values of **k.**

Exercise 5 – Median Filter

A median filter is implemented by ordering the last **k** samples of the signal (with odd k) and selecting as output the median value sample.

Design, synthesize and implement in the *FPGA Spartan 3E of the Nexys 2 board*, using the PMOD AD1 and PMOD DA1 hardware modules, a median filter with **k=5**.

Using a signal generator, analyze the behavior of the filter for different input signals and frequencies**.**