International Training Workshop on FPGA Design for Scientific Instrumentation and Computing

11 – 22 November 2013

Introduction to VLSI Digital Design Technology

Sandro BONACINI
CERN, Geneva
Switzerland
Outline

- Introduction
- Transistors
- The CMOS inverter
- Technology
  - Lithography
  - Physical structure
  - CMOS fabrication sequence
  - Advanced CMOS process
  - Process enhancements
- Scaling
- Gates
- Sequential circuits
- Storage elements
CMOS technology

- An Integrated Circuit is an electronic network fabricated in a single piece of a semiconductor material
- The semiconductor surface is subjected to various processing steps in which impurities and other materials are added with specific geometrical patterns
- The fabrication steps are sequenced to form three-dimensional regions that act as transistors and interconnects that form the switching or amplification network
**Lithography:** process used to transfer patterns to each layer of the IC

Lithography sequence steps:

- **Designer:**
  - Drawing the "layer" patterns on a layout editor

- **Silicon Foundry:**
  - Masks generation from the layer patterns in the design data base
  - Printing: transfer the mask pattern to the wafer surface
  - Process the wafer to physically pattern each layer of the IC

Photolithography for microelectronics:
- Light source
- Mask
- Lens to reduce image
- Die being exposed on wafer

Lithography for paper:
- Plate Cylinder
- Blanket Cylinder
- Impression Cylinder
- Is an indirect printing process. The image is transferred, or offset, from one cylinder to another. A printing plate is generally not exposed to light.
**Lithography**

**Basic sequence**

- **The surface to be patterned is:**
  - spin-coated with photoresist
  - the photoresist is dehydrated in an oven (photo resists: light-sensitive organic polymer)
- **The photoresist is exposed to ultra violet light:**
  - For a positive photoresist exposed areas become soluble and non exposed areas remain hard
- **The soluble photoresist is chemically removed (development).**
  - The patterned photoresist will now serve as an etching mask for the SiO₂
Lithography

- The SiO₂ is etched away leaving the substrate exposed:
  - the patterned resist is used as the etching mask
- Ion Implantation:
  - the substrate is subjected to highly energized donor or acceptor atoms
  - The atoms impinge on the surface and travel below it
  - The patterned silicon SiO₂ serves as an implantation mask
- The doping is further driven into the bulk by a thermal cycle
Lithography

• The lithographic sequence is repeated for each physical layer used to construct the IC. The sequence is always the same:
  - Photoresist application
  - Printing (exposure)
  - Development
  - Etching
Lithography

Patterning a layer above the silicon surface

1. Polysilicon deposition
   Polysilicon
   \( \text{SiO}_2 \)
   Substrate

2. Photoresist coating
   photoresist
   Substrate

3. Exposure
   UV light
   Substrate

4. Photoresist development
   Substrate

5. Polysilicon etching
   Substrate

6. Final polysilicon pattern
   Substrate
Lithography

- **Etching:**
  - Process of removing unprotected material
  - Etching occurs in all directions
  - Horizontal etching causes an undercut
  - “preferential” etching can be used to minimize the undercut

- **Etching techniques:**
  - Wet etching: uses chemicals to remove the unprotected materials
  - Dry or plasma etching: uses ionized gases rendered chemically active by an rf-generated plasma
**Physical structure**

**NMOS physical structure:**
- p-substrate
- n+ source/drain
- gate oxide (SiO₂)
- polysilicon gate
- CVD oxide
- metal 1
- \( L_{\text{eff}} \leq L_{\text{drawn}} \) (lateral doping effects)

**NMOS layout representation:**
- Implicit layers:
  - oxide layers
  - substrate (bulk)
- Drawn layers:
  - n+ regions
  - polysilicon gate
  - oxide contact cuts
  - metal layers
PMOS physical structure:
- p-substrate
- n-well (bulk)
- p+ source/drain
- gate oxide ($\text{SiO}_2$)
- polysilicon gate
- CVD oxide
- metal 1

PMOS layout representation:
- Implicit layers:
  - oxide layers
- Drawn layers:
  - n-well (bulk)
  - n+ regions
  - polysilicon gate
  - oxide contact cuts
  - metal layers
CMOS fabrication sequence

0. **Start:**
   - For an n-well process the starting point is a p-type silicon crystal
   - typically 200 to 300mm in diameter
   - wafer: cut slice less than 1mm thick

1. **Epitaxial growth:**
   - A single p-type single crystal film is grown on the surface of the wafer by:
     - subjecting the wafer to high temperature and a source of dopant material
   - The epi layer is used as the base layer to build the devices
CMOS fabrication sequence

2. N-well Formation:
   - PMOS transistors are fabricated in n-well regions
   - The first mask defines the n-well regions
   - Define the n-well: grow oxide - put resist - mask - expose - strip off resist with solvent - etch oxide with HF
   - N-well’s are formed by ion implantation or deposition and diffusion
   - Lateral diffusion limits the proximity between structures
   - Ion implantation results in shallower wells compatible with today’s fine-line processes

Thermal oxidation:
- \( \text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2 \)
- \( \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \)
2bis. P-well formation:
- In twin-well technologies the p-well has to be created.

3. Active area definition:
- Active area:
  - planar section of the surface where transistors are build
  - defines the gate region (thin oxide)
  - defines the n+ or p+ regions
- A thin layer of $SiO_2$ is grown over the active region and covered with silicon nitride
4. **Isolation:**
- Parasitic (unwanted) FET's exist between unrelated transistors (Field Oxide FET's)
- Source and drains are existing source and drains of wanted devices
- Gates are metal and polysilicon interconnects
- The threshold voltage of FOX FET's are higher than for normal FET's
**CMOS fabrication sequence**

- FOX FET's threshold is made high by:
  - introducing a channel-stop diffusion that raises the impurity concentration in the substrate in areas where transistors are not required
  - making the FOX thick

4 -> **Form Shallow-Trench Isolation (STI)**

- The use of reverse-biased pn junctions to isolate transistors becomes impractical as the transistor sizes decrease
- an anisotropic etch is made in the silicon to a depth of 0.4 to 0.5 um
- CVD dielectric is used to fill the trench
CMOS fabrication sequence

5. Gate oxide growth
- The nitride and stress-relief oxide are removed
- The devices threshold voltage is adjusted by:
  • adding charge at the silicon/oxide interface
- The well controlled gate oxide is grown with thickness tox
- Grow oxide by thermal oxidation
  • SiO₂ has approximately twice the volume of silicon
  • The oxide recedes below the silicon surface by 0.46tox

5b. Channel implant
- Adjust the threshold voltage of devices with a shallow implant in the channel region (stronger doping)
6. **Polysilicon deposition and patterning**
- A layer of polysilicon is deposited over the entire wafer surface
- The polysilicon is then patterned by a lithography sequence
- All the MOSFET gates are defined in a single step
- The polysilicon gate can be doped (n+) while is being deposited to lower its parasitic resistance (important in high speed fine line processes)
- Remove oxide not covered by polysilicon
CMOS fabrication sequence

7. PMOS formation

- Photoresist is patterned to cover all but the p+ regions
- A boron ion beam creates the p+ source and drain regions
- The polysilicon serves as a mask to the underlying channel
  - This is called a self-aligned process
  - It allows precise placement of the source and drain regions
- During this process the gate gets doped with p-type impurities
  - Since the gate had been doped n-type during deposition, the final type (n or p) will depend on which dopant is dominant
- The p+ contact to the p-well is also created
CMOS fabrication sequence

8. NMOS formation
- Photoresist is patterned to define the n+ regions
- Donors (arsenic or phosphorous) are ion-implanted to dope the n+ source and drain regions
- The process is self-aligned
- The gate is n-type doped
- The n+ contact for the n-well is also created
CMOS fabrication sequence

10. Contact cuts

- The surface of the IC is covered by a layer of CVD oxide
  - The oxide is deposited at low temperature (LTO) to avoid that underlying doped regions will undergo diffusive spreading
- Contact cuts are defined by etching SiO₂ down to the surface to be contacted
- These allow metal to contact diffusion and/or polysilicon regions
**CMOS fabrication sequence**

### 11. Metal 1

- The contact cuts are filled with tungsten (low resistivity, good adhesion, uniform deposition)
- A first level of metallization (copper) is applied to the wafer surface and selectively etched to produce the interconnects

Copper has better conductivity than aluminum, but:
- Diffuses quickly into oxides and silicon.
- Oxidizes quickly in air at low temperatures and does not form a protective layer to stop further oxidation.
- Need tantalum or TaN barrier
n-well contact (n+)

n-well

polysilicon

diffusion contacts

substrate contact (p+)

p+ diffusions

n+ diffusions

polysilicon contacts
CMOS fabrication sequence

12. Metal 2
- Another layer of LTO CVD oxide is added
- Via openings are created
- Metal 2 is deposited and patterned
- "Dual damascene": two layers of oxide are made before one single deposition of metal, followed by CMP. Metal fills the vias.
12. Other metal layers
- Thicker top metals for lower resistivity
- The top metal is normally aluminum to allow easy wirebond
13. Over glass and pad openings
- A protective layer is added over the surface:
- The protective layer consists of:
  - A layer of $\text{SiO}_2$
  - Followed by a layer of silicon nitride
- The SiN layer acts as a diffusion barrier against contaminants (passivation)
- A layer of polyimide is often added for additional passivation
- Finally, contact cuts are etched, over the last metal, on the passivation to allow for wire bonding.
Advanced CMOS processes

- Multiple threshold voltages
- source-drain extensions LDD (hot-electron effects)
- Self-aligned silicide (spacers), titanium silicide
- High-k gate dielectric
- Low-k inter-metal dielectric
- Non-uniform channel doping (short-channel effects)
BACKUP SLIDES
Process enhancements

- Twin-well formation
- Copper interconnects
  - Up to 8 metal levels in modern processes
- Stacked contacts and vias
- Chemical Metal Polishing for technologies with several metal levels
- Shallow trench isolation
- Bipolar transistors (BiCMOS)
- Capacitors
- Diodes
- Inductors
- Resistors
- Dual or triple polysilicon (memories)
- Separate n-channel and p-channel implant
CMOS fabrication sequence

9. Annealing
- After the implants are completed a thermal annealing cycle is executed
- This allows the impurities to diffuse further into the bulk
- After thermal annealing, it is important to keep the remaining process steps at as low temperature as possible

![Diagram of CMOS fabrication sequence with n-well, p-type, n+, and p+ regions]
CMOS fabrication sequence

- Silicon oxidation is obtained by:
  - Heating the wafer in a oxidizing atmosphere:
    - Wet oxidation: water vapor, $T = 900$ to $1000^\circ$C (rapid process)
    - Dry oxidation: Pure oxygen, $T = 1200^\circ$C (high temperature required to achieve an acceptable growth rate)
- Oxidation consumes silicon
  - $\text{SiO}_2$ has approximately twice the volume of silicon
  - The FOX is recedes below the silicon surface by $0.46 X_{\text{FOX}}$