



The Abdus Salam
International Centre
for Theoretical Physics



2499-8

**International Training Workshop on FPGA Design for Scientific
Instrumentation and Computing**

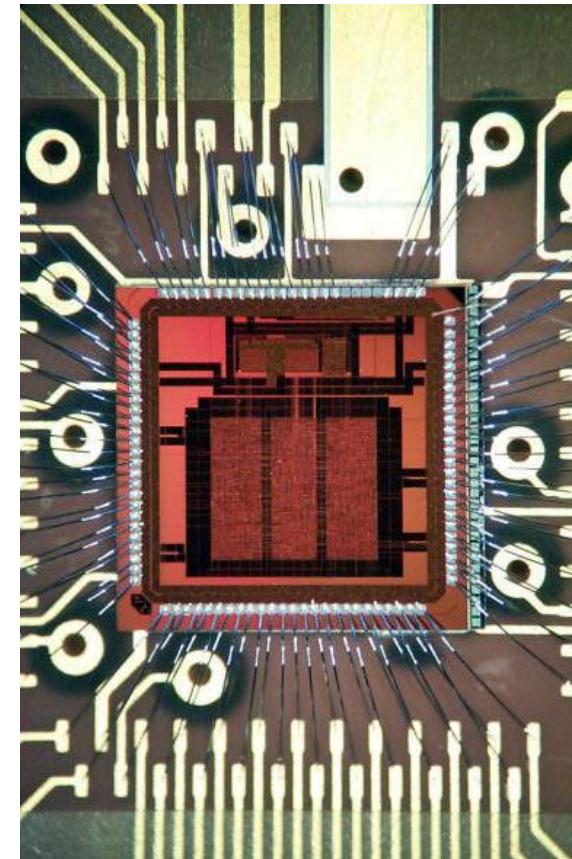
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**Introduction to VLSI Digital Design
Gates**

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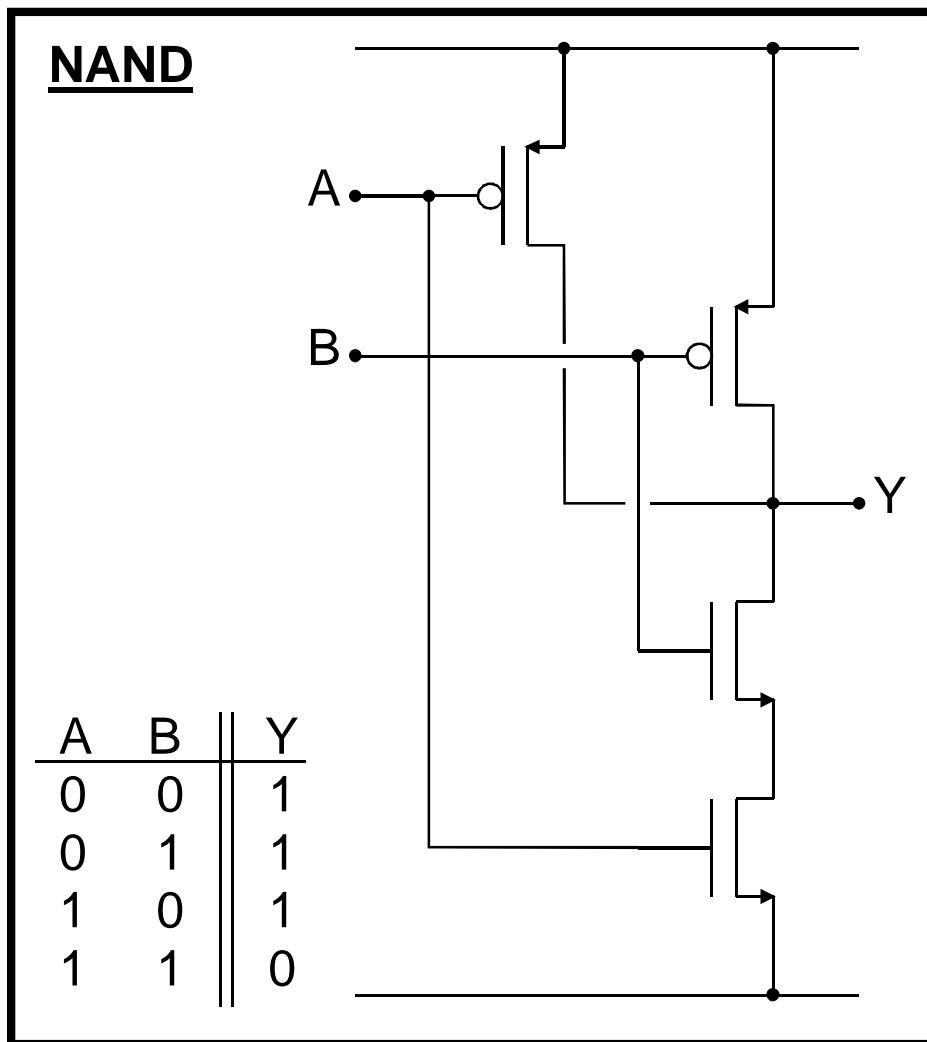
Outline

- Introduction
- Transistors
- The CMOS inverter
- Technology
- Scaling
- Gates
 - The NAND gate
 - "Reading" CMOS gates
 - Designing CMOS gates
- Sequential circuits
- Storage elements
- Phase-Locked Loops
- Example



Many slides are a courtesy of
Paulo Moreira

NAND 2-inputs

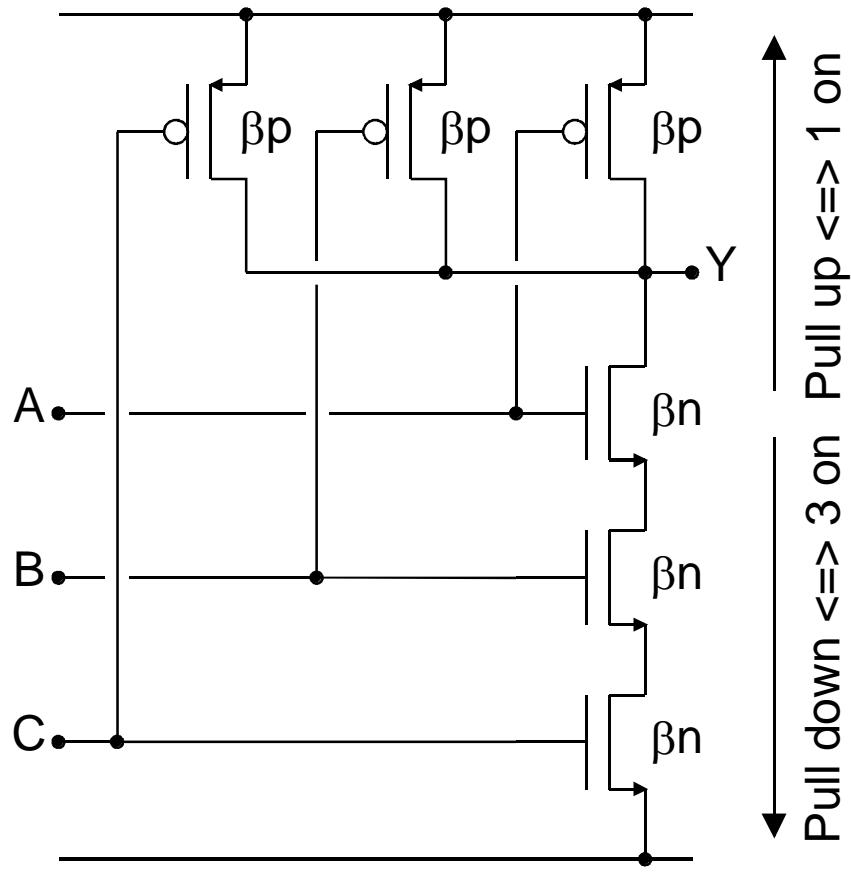


“Gates are inverters in disguise!”

- Pull-down: NMOS in series
 - Need 2 NMOS “on” to pull-down
- Pull-up: PMOS in parallel
 - One PMOS “on” is sufficient to pull-up

NAND 3-inputs

NAND 3 inputs

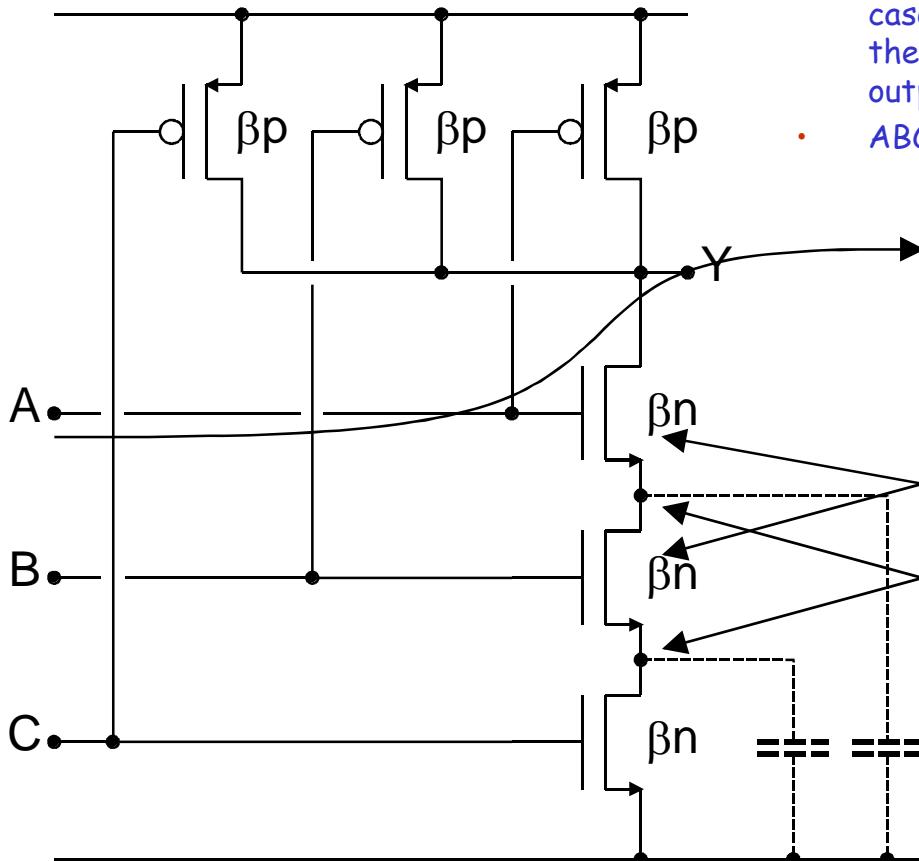


"Delay equivalent" inverter

- Approximates delay
 - Neglects different operating point of NMOSes:
 - V_{gs} , V_{ds} , bulk effect, "memory" of nodes
-
- A simplified model of the inverter's behavior. It consists of a single PMOS transistor (labeled β_p) with its drain connected to VDD and its source connected to the output line. The input signal is connected to the gate of the PMOS transistor. The output is labeled "Pull up <=> 1 on".

NAND 3-inputs

NAND 3 inputs



- The NMOS connected to A is faster to propagate A in the case of a single bit change in the inputs, which brings the output from 1 to 0
- $ABC = 011 \rightarrow 111, \quad Y = 1 \rightarrow 0$

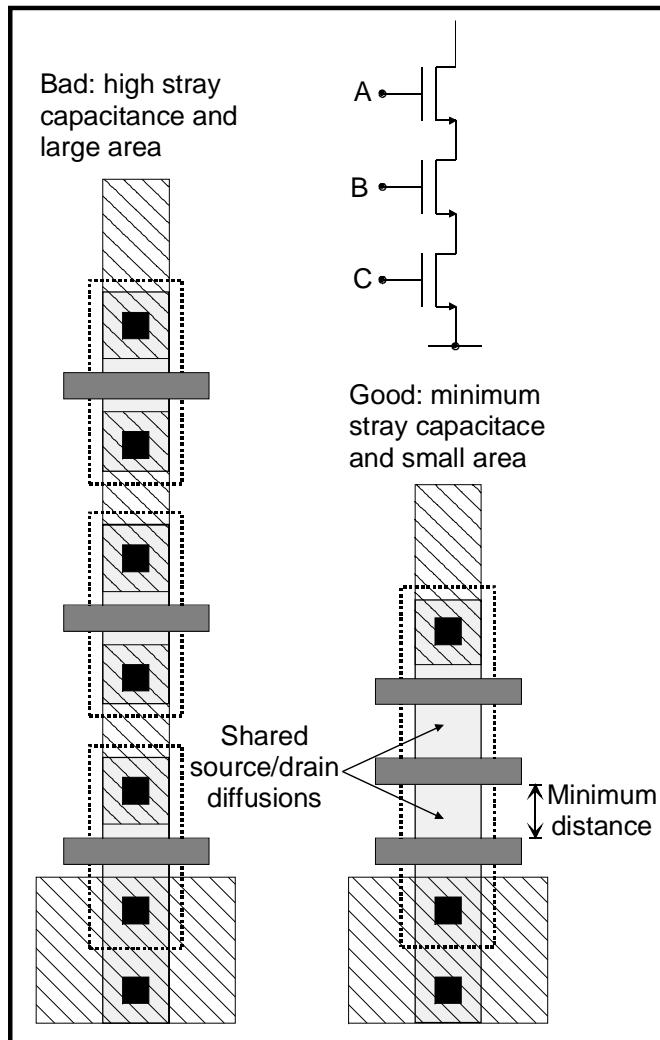
→ Use transistors close to the output for critical signals

Bulk effect

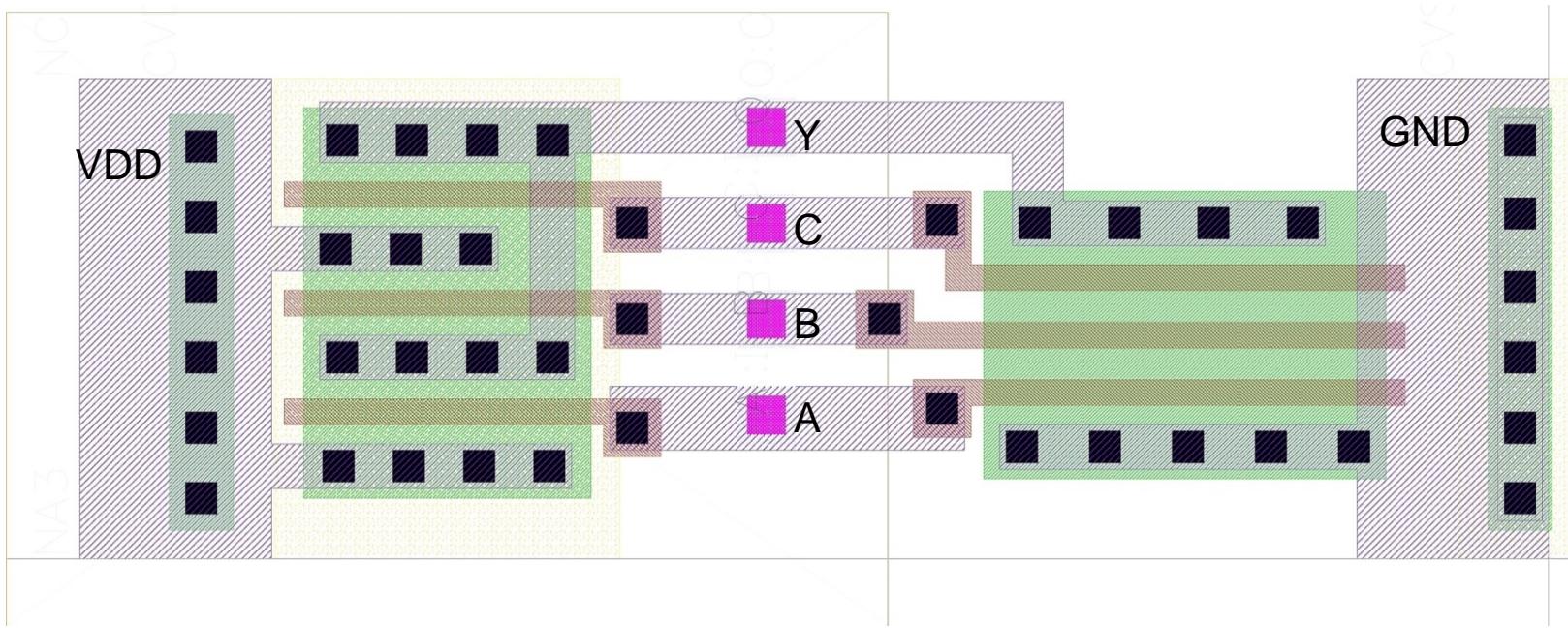
Stray capacitance

- Depending on the timing sequence of the inputs, the capacitors could be at ground, Vdd or an intermediate voltage

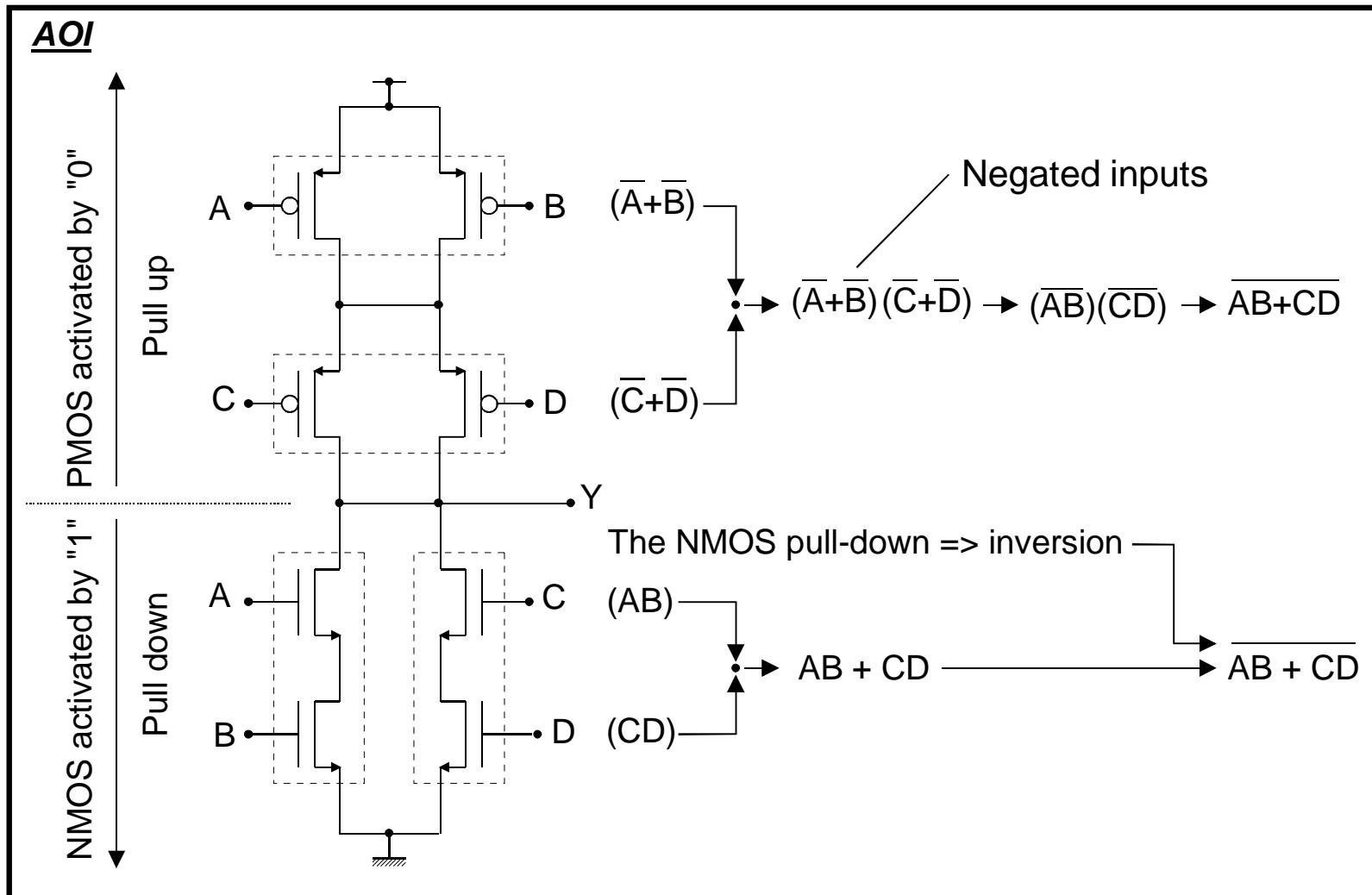
NAND 3-inputs



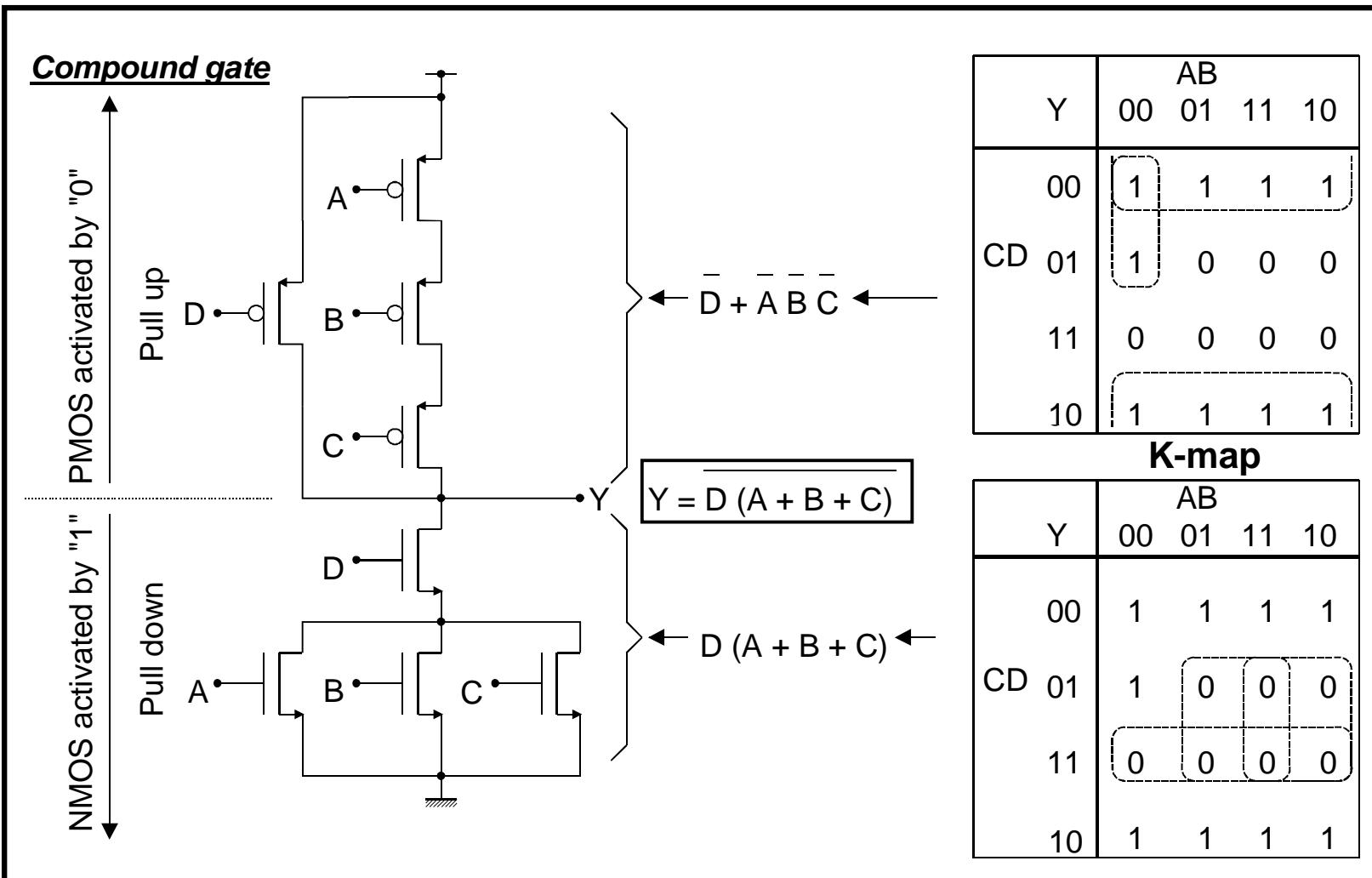
NAND 3-inputs



"Reading" CMOS gates



Designing CMOS gates



Complex CMOS gates

- Can a compound gate be arbitrarily complex?
 - NO, propagation delay is a strong function of fan-in:
$$t_p = a_0 \cdot FO + a_1 \cdot FI + a_2 \cdot (FI)^2$$
 - $FO \Rightarrow$ Fan-out, number of loads connected to the gate:
 - 2 gate capacitances per FO + interconnect
 - $FI \Rightarrow$ Fan-in, Number of inputs in the gate:
 - Quadratic dependency on FI due to "RC" signal path across the channels:
 - The resistance increases with the number of transistors in series
 - » E.g. (FI) R_o series NMOS for a NAND
 - Each drain and source diffusion adds additional parasitic capacitance
 - » E.g. (FI) C_d drain diffusion of PMOS for a NAND
 - » $\rightarrow FI^2 R_o C_d$
 - Avoid large FI gates (Typically $FI \leq 4$)