

2572-11

**Winter College on Optics: Fundamentals of Photonics – Theory,
Devices and Applications**

10 – 21 February 2014

Silicon photonics: Waveguide modulators and detectors

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<http://silicon-photonics.ief.u-psud.fr/>



Silicon photonics: Waveguide modulators and detectors

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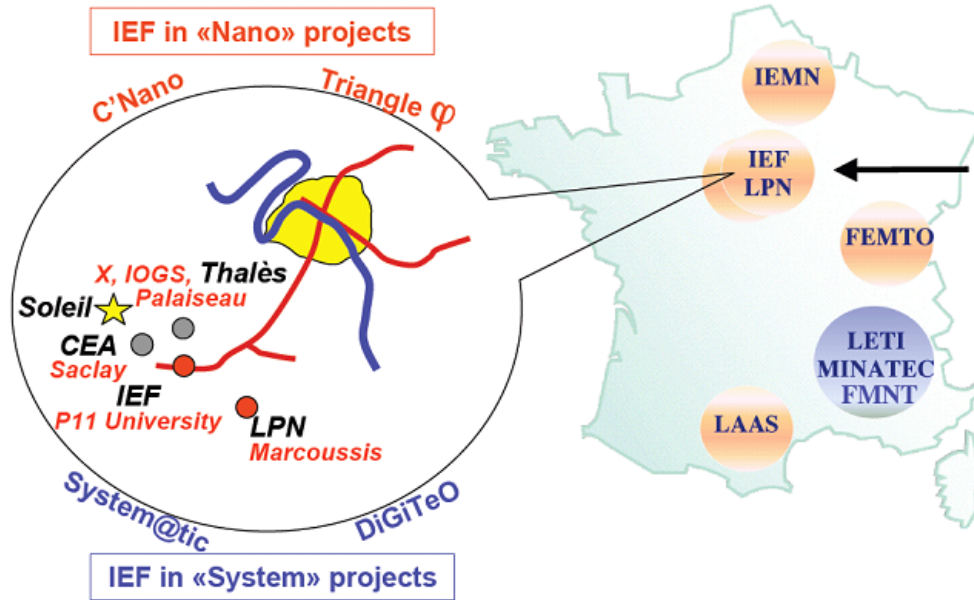
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The Institute for Fundamental Electronics



IEF is a joint research unit between CNRS and University of Paris Sud

- 135** CNRS researchers, professors and lecturers, technical staff
- +100** PhD students, Post-Doc and visitors
- ~ 400** students undergoing training within IEF's ground

Spintronics and Si-based Nano-electronics

Micro-Nano systems and systems

Photonics

**University Technology Center
(CTU) MINERVE**





IEF-MINERVE member of The French Network on
“Basic Technological Research” (RTB)

University Technology Centre (1000 m²):

Photolithography:

- 2-sided UV lithography with wafer bonding
- Deep UV lithography (248 nm)
- 2 e-beams (Raith150 and 100keV nanobeam)
- Laser

Etching:

- Wet etching (KOH, TMAH, ...)
- Dry etching :
 - fluoride gases RIE (2 systems)
 - ICP Si deep etching
 - IBE
 - O₂ plasma etching
 - Chloride gases RIE

...



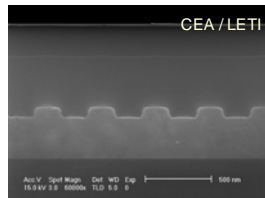


- 4 permanent Researchers
- 2 engineers, technicians
- 16 PhD students
- 2 post-doc
- 2-4 master students / year

Passive devices

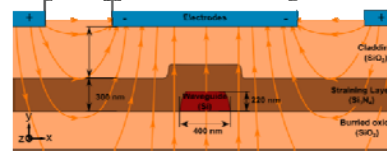
Grating couplers

- Waveguides
- Splitters
- Optical Distribution
- Multi-wavelength circuits



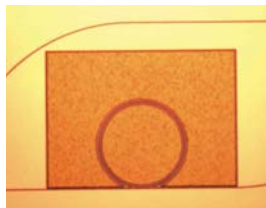
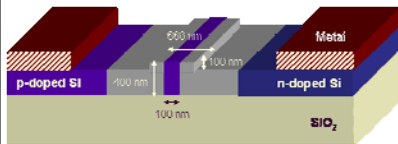
Strained Si photonics

➢ Pockels effect



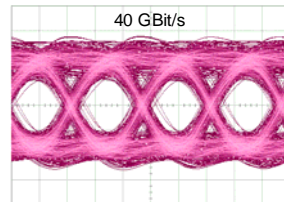
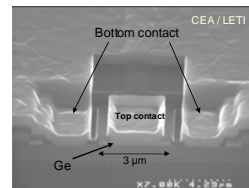
Optical modulators

- All silicon
- NL materials
- Plasmon



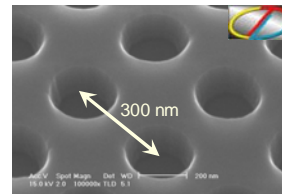
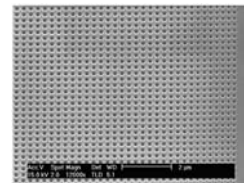
Ge detectors

- Surface illuminated
- Integrated
- APD



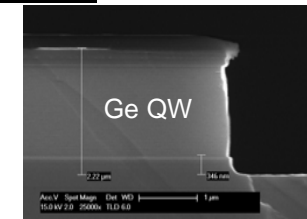
Photonic crystals

- Slow light
- Superprism
- NL enhancement

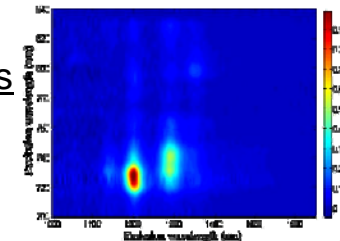


Ge-SiGe QW photonics

- Source
- Modulator
- detector



Carbon nanotubes for photonics





- Motivation (Pavel's and Lorenzo's talks)
- Photodetectors on silicon
 - ✓ Main characteristics
 - ✓ Results
- Optical modulators
 - ✓ Figures of Merit
 - ✓ Modulation in silicon
 - ✓ Results
- Conclusion



FTTH



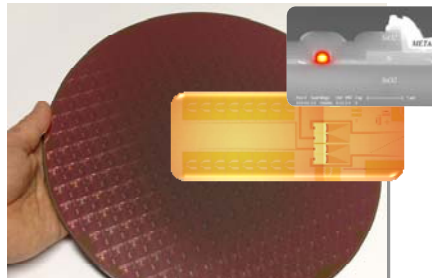
Optical telecommunications



Environment



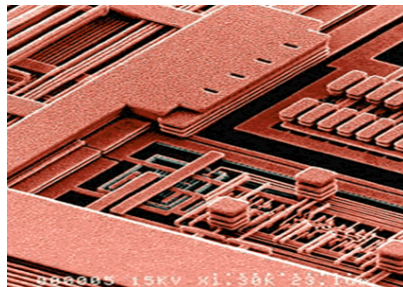
Data centers



Silicon photonics



Chemical/Biological sensors



Interconnects



Free space communications

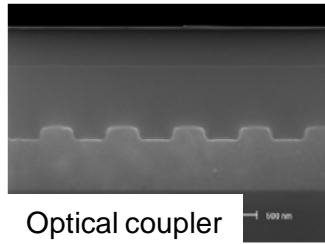


Military

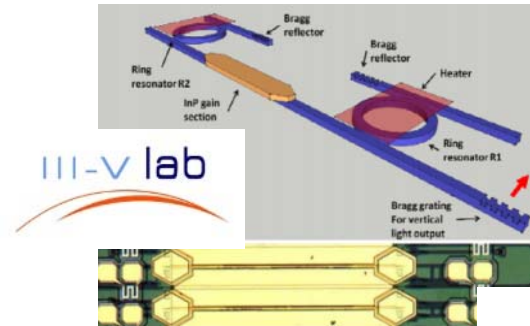


Silicon photonic building blocks

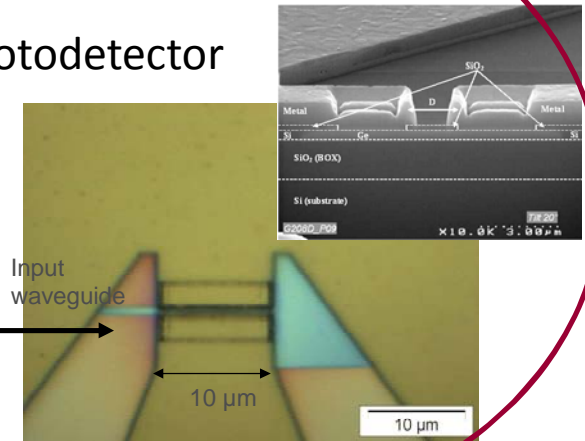
Off-chip III-V laser



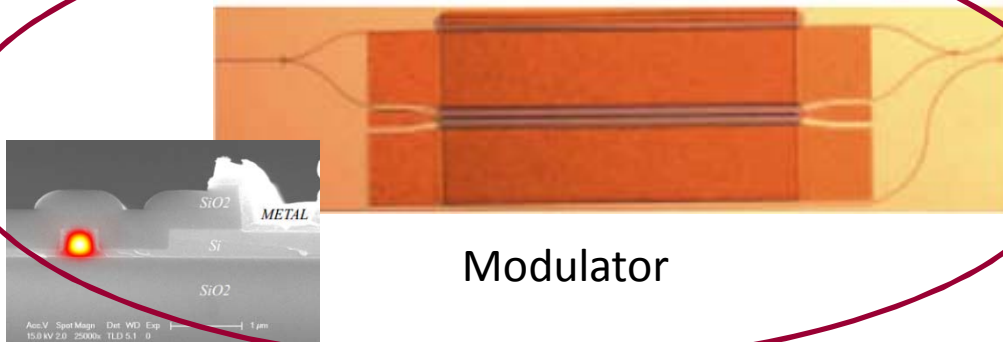
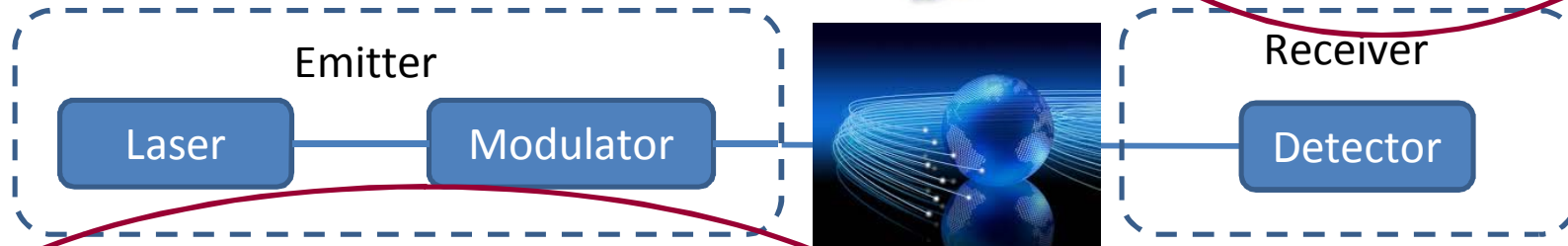
On-chip III-V laser on Si



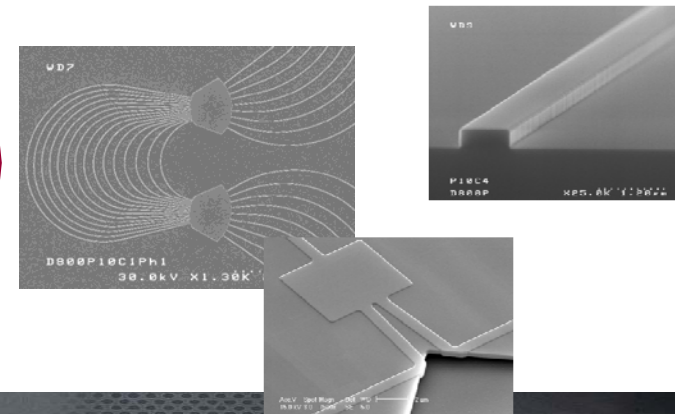
photodetector



Germanium-based laser



Modulator

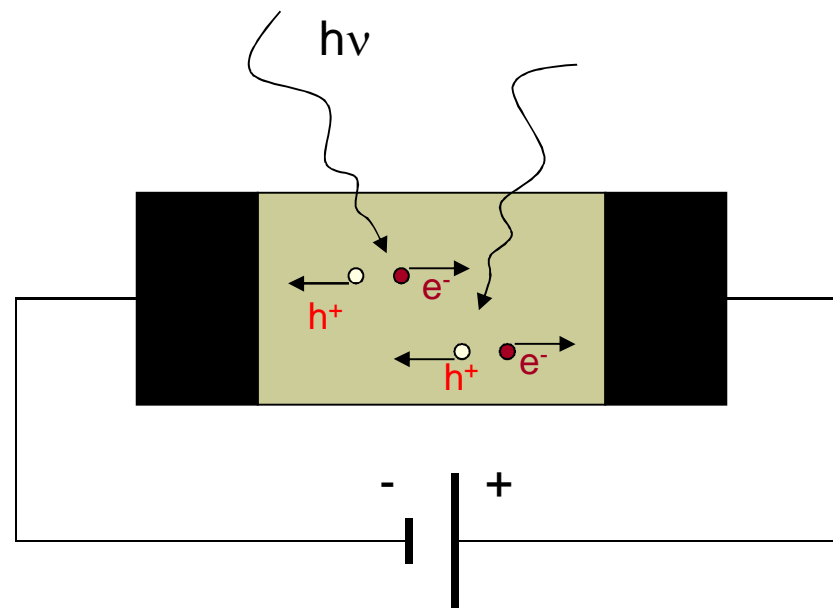




Photodetection



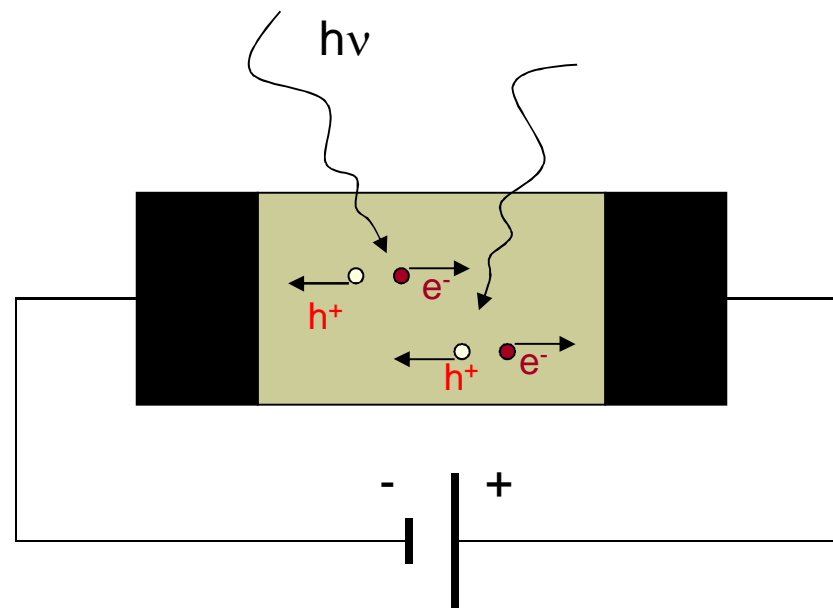
Main characteristic of the material?





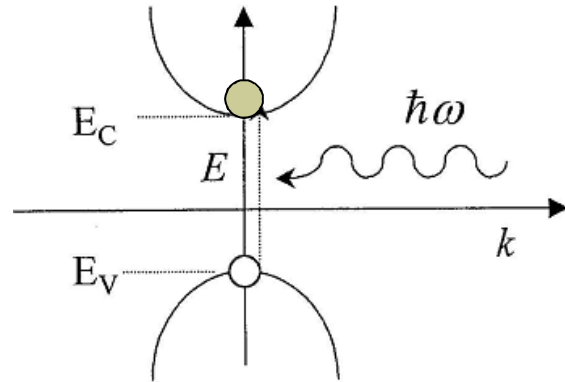
Basic principle

- The absorption of photons generates electron-hole pairs
- Photogenerated carriers are then collected thanks to an external field
 - √ Photocurrent

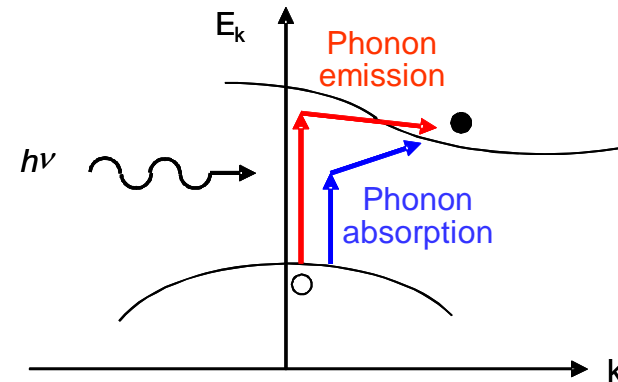




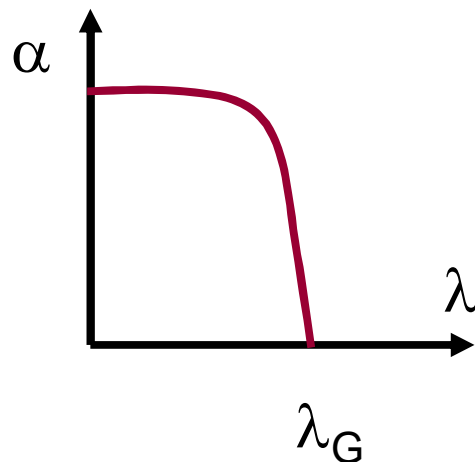
■ Direct gap SC (III-V SC)



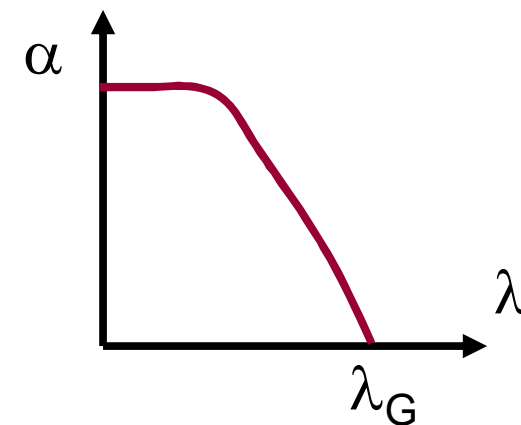
■ Indirect gap SC (IV-IV SC)



✓ absorbed photons generate free electron-hole pairs



$$E_G = hc/\lambda_G$$

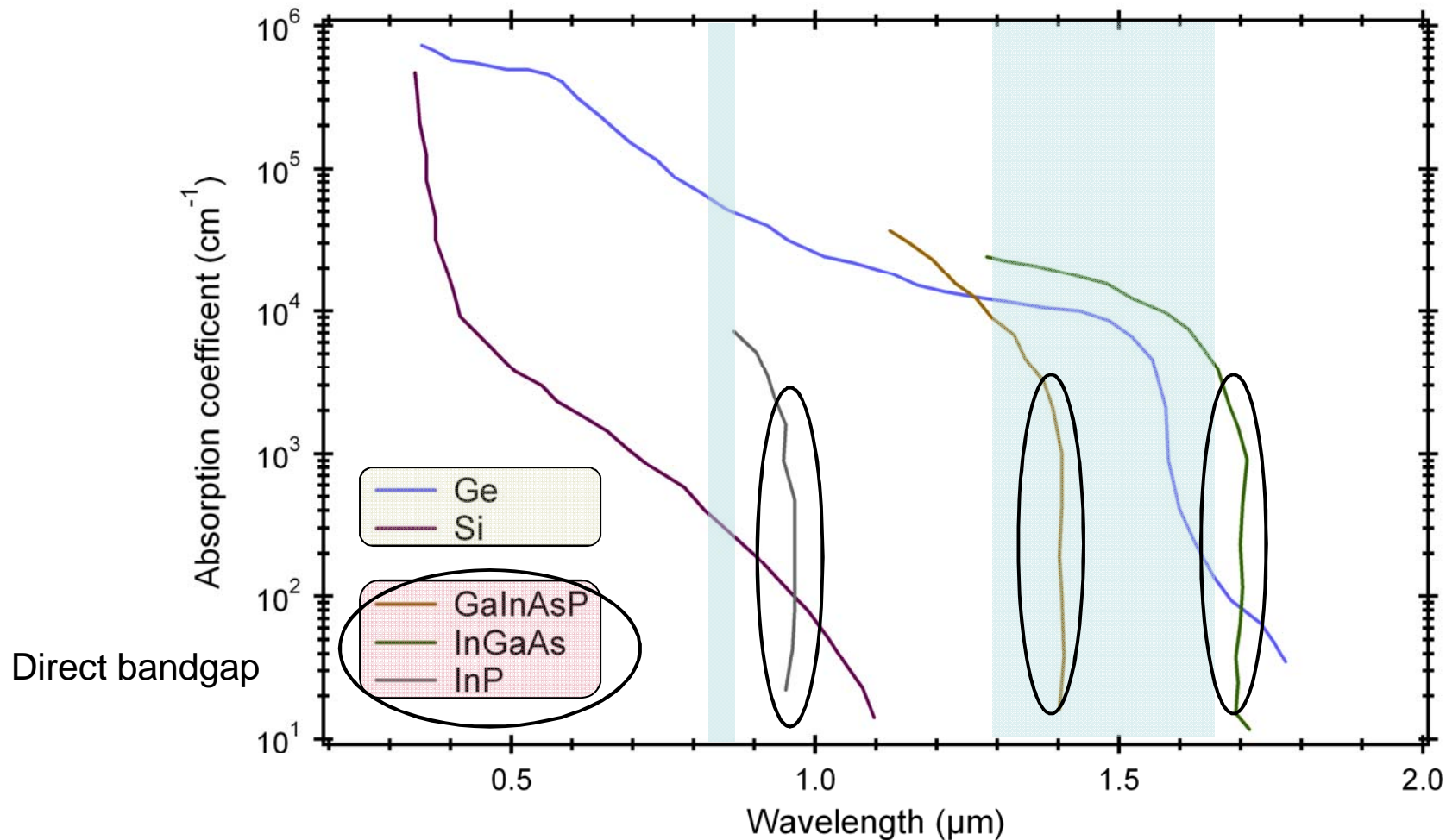




Material choice

■ Wavelength ranges:

- ✓ 1.3 μm – 1.6 μm
- ✓ 0.85 μm

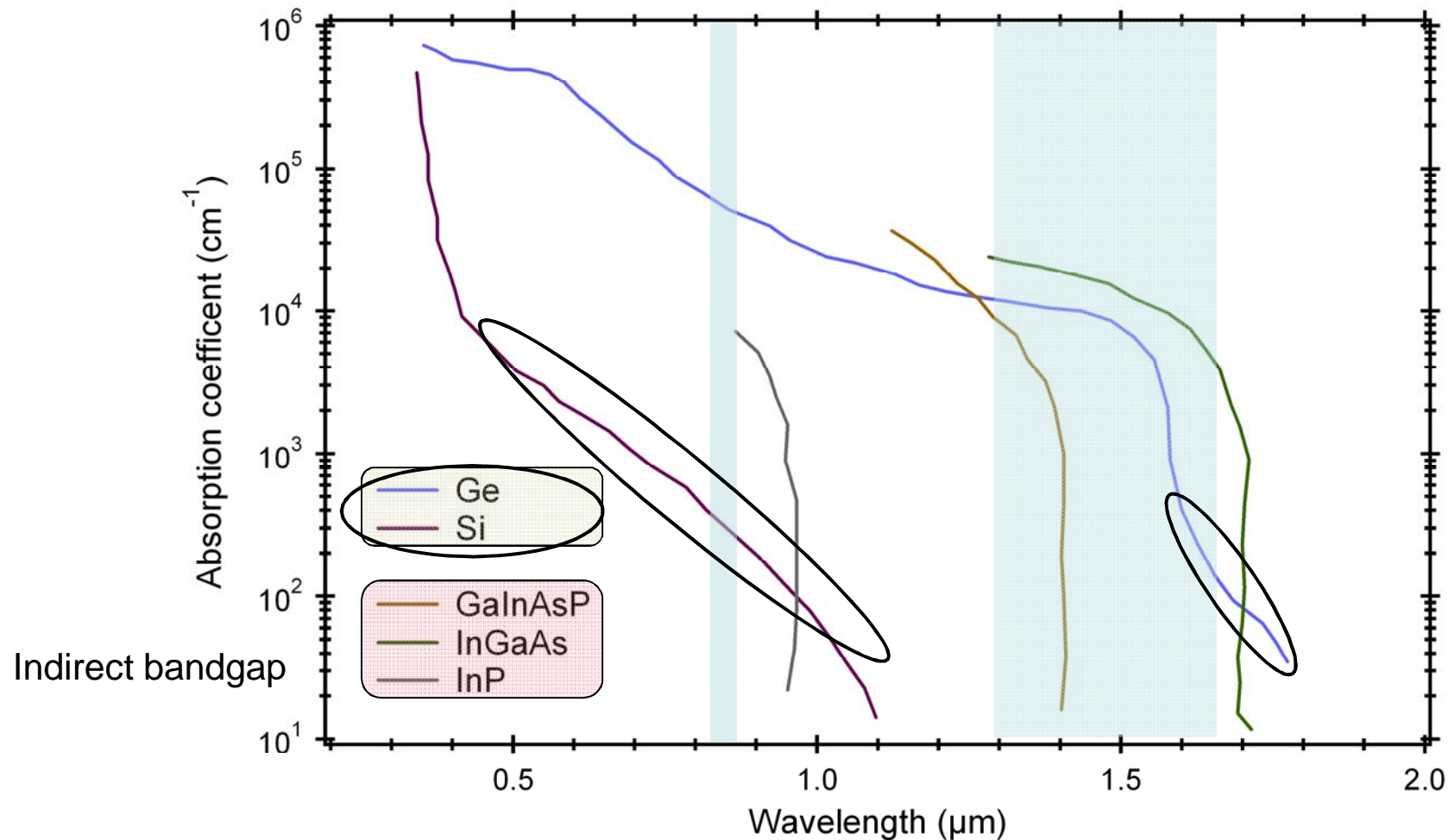




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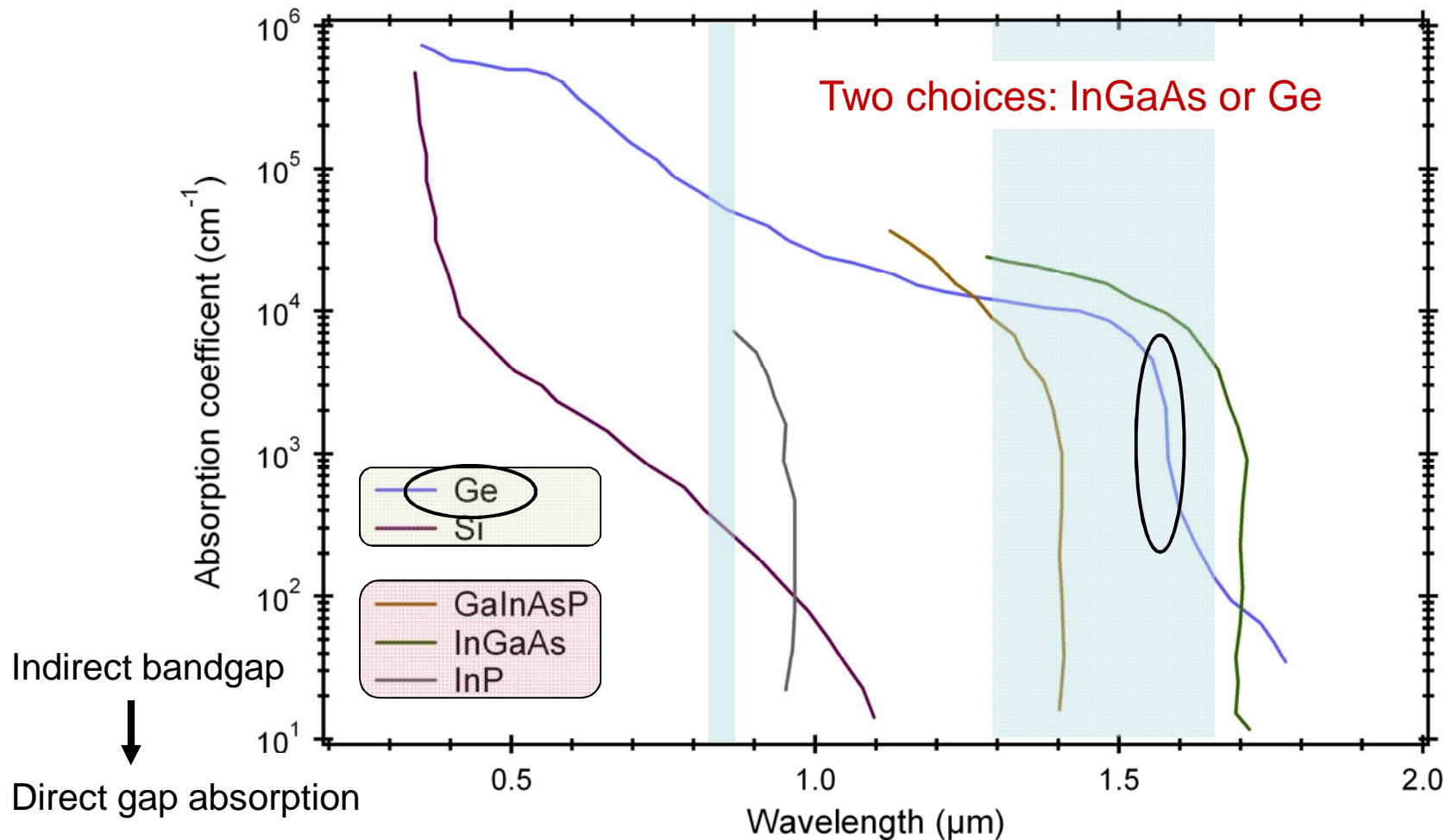




Material choice

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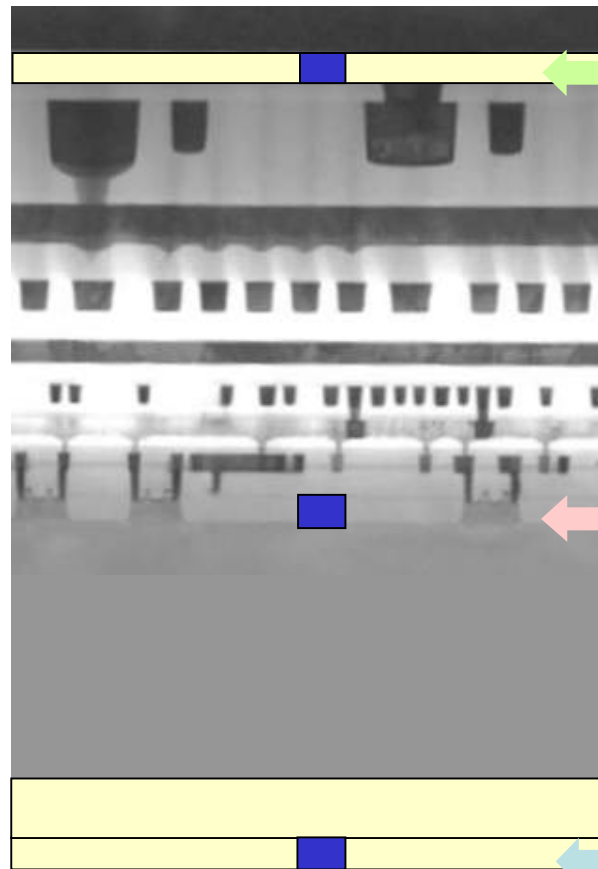


- InGaAs versus Germanium

What is the best material for light detection in near-IR wavelength range ?



Material choice versus electronic photonic integration scheme



BE: Back end FE:Front end

Photonic layer at the last levels of metallizations with back-end fabrication

- 1) Wafer bonding of PIC (high T°C)
- 2) BE fab(<400°C)

- Use of standard FE CMOS technologies
- High integration density (AboveIC)
- Multilevel process capability

Combined front-end fabrication

- Specific FE CMOS technology and library
- Flip-Chip hybridization of InP components
- Moderate integration density
- Efficient connections of EIC and PIC

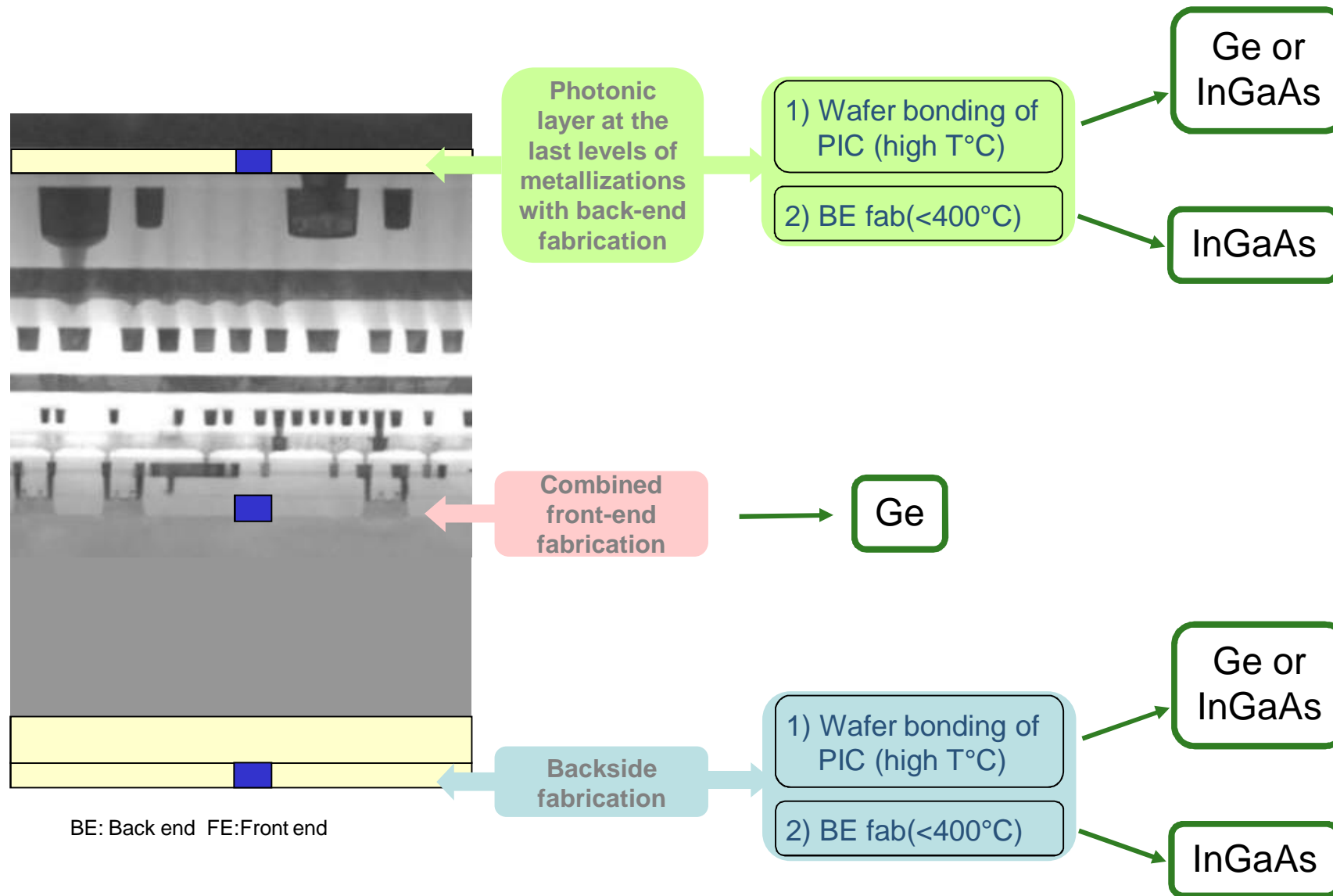
Backside fabrication

- 1) Wafer bonding of PIC (high T°C)
- 2) BE fab(<400°C)

- Through substrate connections
- High integration density



Material choice versus integration scheme

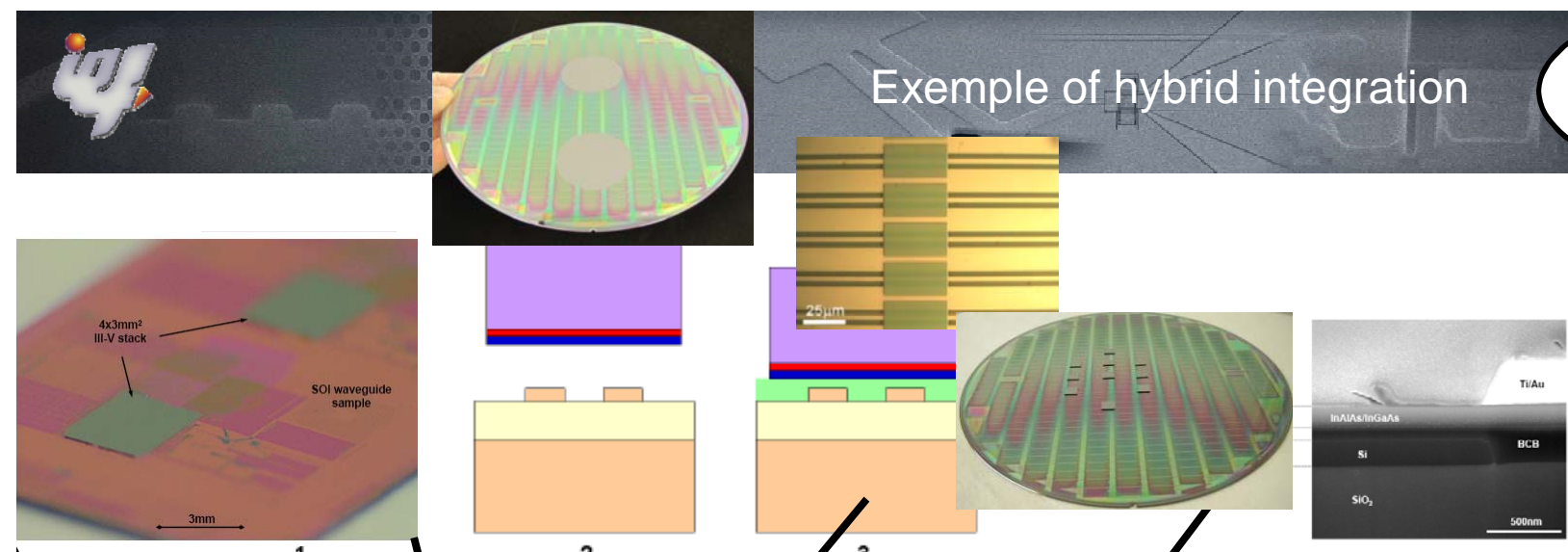




Are III-V materials integrated in silicon platform?

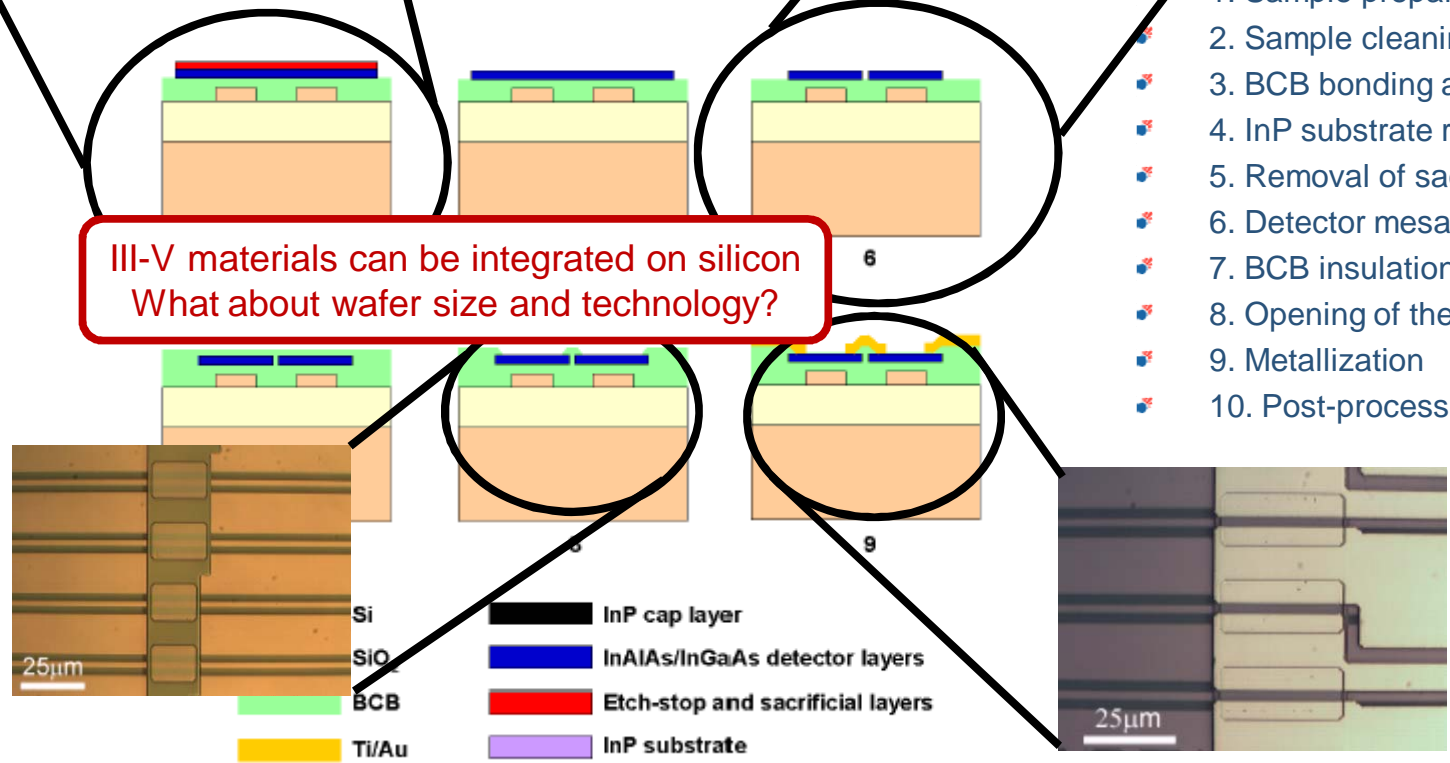
- ✓ Monolithic integration via epitaxial growth
No viable solutions yet
- ✓ Hybrid integration
BCB or molecular bonding

Exemple of hybrid integration



III-V materials can be integrated on silicon
What about wafer size and technology?

1. Sample preparation
2. Sample cleaning + removal of cap layer
3. BCB bonding and curing
4. InP substrate removal
5. Removal of sacrificial layers
6. Detector mesa etching
7. BCB insulation
8. Opening of the contact windows
9. Metallization
10. Post-processing



Si	InP cap layer
SiO ₂	InAlAs/InGaAs detector layers
BCB	Etch-stop and sacrificial layers
Ti/Au	InP substrate



Germanium on silicon: Pros and Cons



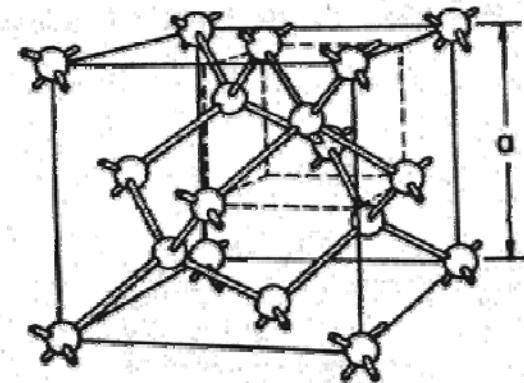
- Absorption coefficient of pure Ge:
 - $\alpha \approx 9000 \text{ cm}^{-1}$ at $\lambda = 1.3 \mu\text{m}$
 - $\Rightarrow L_{\text{ABS}}^{95\%} \approx 3.3 \mu\text{m}$ (!)
 - \Rightarrow Low capacitance devices
 - \Rightarrow High frequency operation
- High carrier mobility



Crystal lattice structure of Silicon and Germanium

- Si and Ge have a diamond lattice structure (two interdigitated FCC lattices)

Properties	Silicon	Germanium
Lattice parameter: a (Å)	5.431	5.658
Atomic density (cm^{-3})	$5,0 \cdot 10^{22}$	$4,42 \cdot 10^{22}$
Atom radius (Å)	0.117	0,122
Lattice structure	Diamond	Diamond



Lattice parameter mismatch: ~4.2 %



Germanium on silicon: Pros and Cons



- Absorption coefficient of pure Ge:

- $\alpha \approx 9000 \text{ cm}^{-1}$ at $\lambda = 1.3 \mu\text{m}$

- $\Rightarrow L_{\text{ABS}}^{95\%} \approx 3.3 \mu\text{m}$ (!)

- \Rightarrow Low capacitance devices

- \Rightarrow High frequency operation

- High carrier mobility

- Lattice misfit with Si of about 4.2%
 \Rightarrow specific growth strategies required (wafer-scale and localized)

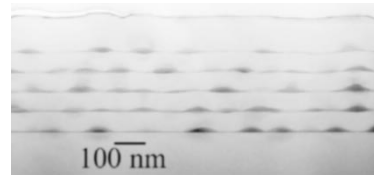
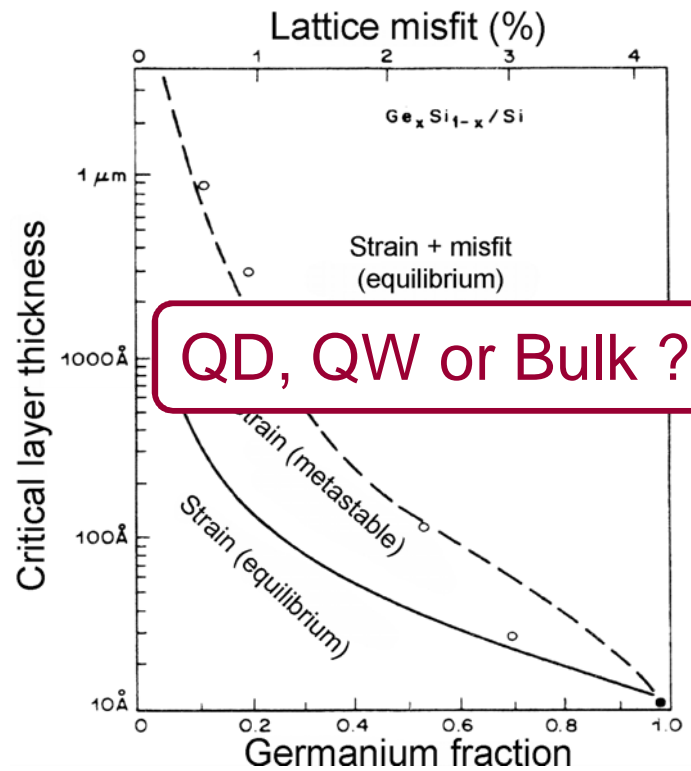
- Low indirect bandgap: $E_G = 0.66 \text{ eV}$
 \Rightarrow high dark current for MSM devices

Can we directly growth Ge on silicon?

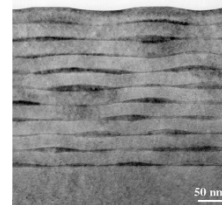


The lattice mismatch

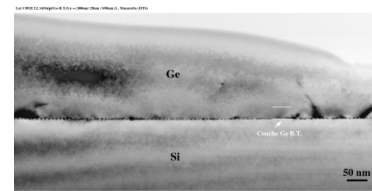
- 4.2% of lattice mismatch between germanium and silicon



Ge quantum dots



$\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ quantum wells



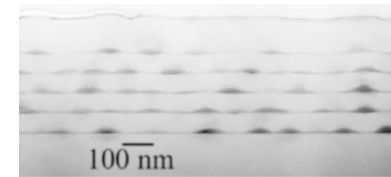
Pure Ge on Si

SiGe on Si



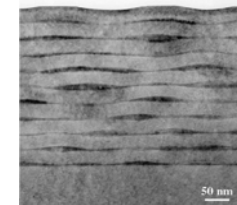
■ Ge quantum dots

√ $\alpha \sim 20 \text{ cm}^{-1}$ (90% absorption length $\sim 1.1 \text{ mm}$)



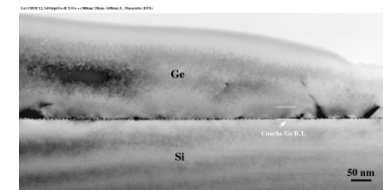
■ $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ quantum wells

√ $\alpha \sim 100\text{-}200 \text{ cm}^{-1}$ (90% absorption length $\sim 230\text{-}110 \mu\text{m}$)



■ Pure Ge on Si

√ $\alpha \sim 7500 \text{ cm}^{-1}$ (90% absorption length $\sim 3 \mu\text{m}$)





- Thick virtual SiGe substrates ($10\mu\text{m}$)
 - √ Need for a new integration scheme – difficult to integrate with SOI waveguides.





- Thick virtual SiGe substrates (10 μ m)
 - √ Need for a new integration scheme – difficult to integrate with SOI waveguides.
- Growth on thin SiGe buffers
 - √ The thickness of the thin SiGe buffer is around 1 μ m
 - Always too thick for integration with SOI





- Thick virtual SiGe substrates ($10\mu\text{m}$)
 - √ Need for a new integration scheme – difficult to integrate with SOI waveguides.
- Growth on thin SiGe buffers
 - √ The thickness of the thin SiGe buffer is around $1\mu\text{m}$
 - Always too thick for integration with SOI
- Direct Ge growth on Si

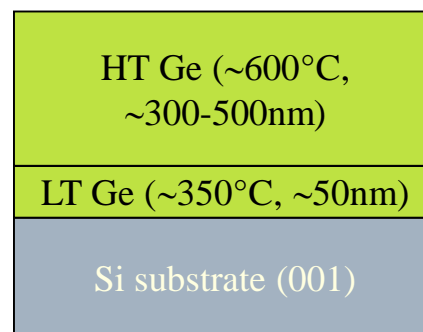




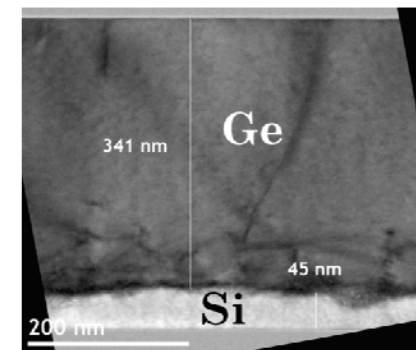
■ Two-step growth process:

- ✓ Direct growth of Ge on Si using a low temperature ($\sim 350^\circ$) CVD process
⇒ thin (a few 10nm) highly-dislocated Ge layer
- ✓ Growth of a thick Ge layer (a few 100nm) at a higher temperature ($\sim 600^\circ$)
⇒ high quality Ge absorbing layer

■ Thermal annealing to reduce the dislocation density



↕
 $\sim 400\text{nm}$
↕



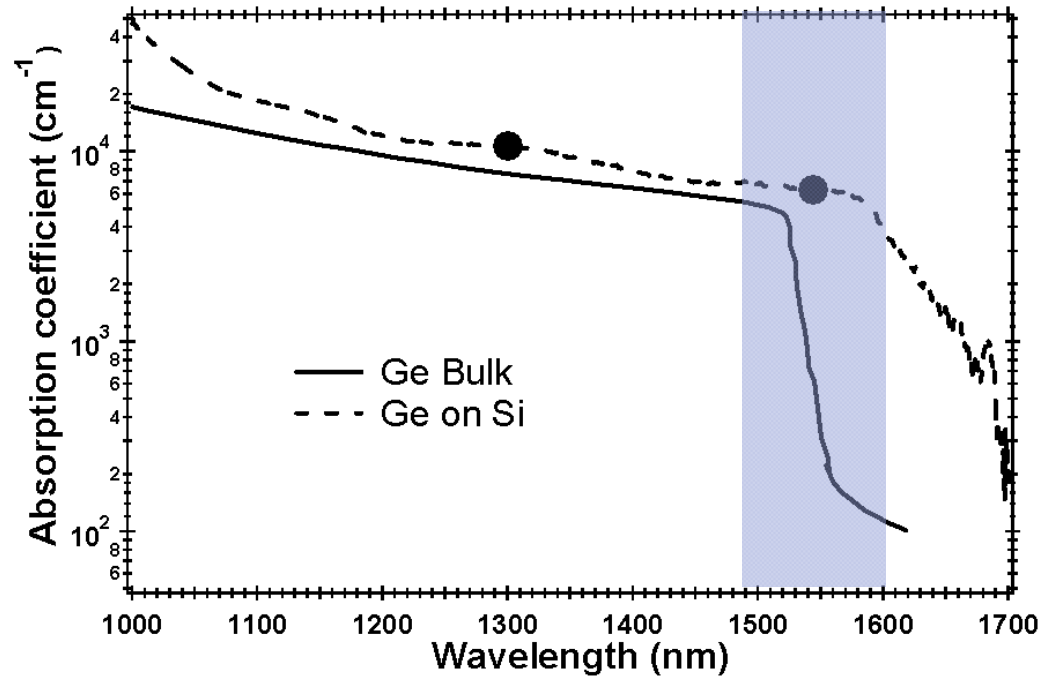


□ Molecular beam epitaxy (MBE)

- Solid sources evaporated \Rightarrow gas sputtering on the wafer
- Ultra-high vacuum required ($P \sim 10^{-10}$ Torr)
- Low thermal budgets ($T < \sim 550^\circ\text{C}$)
- High-control of layer and multi-layer thicknesses ($< \text{nm}$)
- Low growth rates ($< 1 \text{ nm/min}$)

□ Chemical Vapor Deposition (CVD):

- High-control of layer and multi-layer thicknesses ($< \text{nm}$)
- Proper for large wafer-scale fabrication
- A large variety of CVD techniques have been developed, depending on the pressure and heating systems:
 - Ultra-High Vacuum CVD (**UHV-CVD**)
 - Reduced-pressure CVD (**RP-CVD**)
 - Low-energy plasma-enhanced CVD (**LEPE-CVD**)



- The red-shift of the absorption edge is due to the tensile strain-induced bandgap narrowing within the Ge layer, resulting from the difference in the thermal expansion coefficients of Ge and Si

Strong absorption up to 1.6μm



Photodetector characteristics



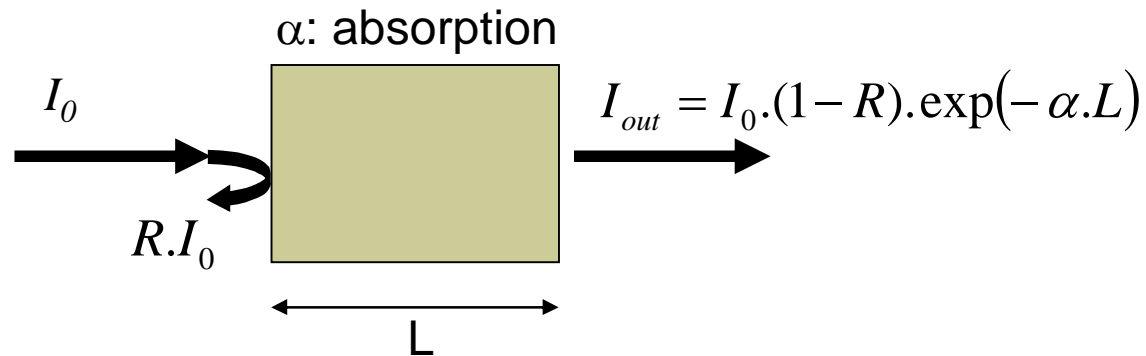
■ Quantum efficiency (η):

- √ Probability of detecting an incident photon by generating an electron/hole pair that contributes to the photocurrent
- √ Ratio of the generated carriers to incident flux of photons (i.e.: ratio of the photocurrent to the incident light power)
- √ The spectral response is governed by the spectral character of the quantum efficiency



Photodetector characteristics: Quantum efficiency (II)

- Quantum efficiency (η) depends on:
 - ✓ Reflectance on the surface
 - ✓ Absorption



The amount of flux that is absorbed in the material

$$I_{abs} = 1 - I_{out} = I_0.(1-R).[1 - \exp(-\alpha.L)]$$

$$\eta = (1-R).[1 - \exp(-\alpha.L)]$$



Photodetector characteristics: Responsivity



- Responsivity (\mathcal{R}) is often more useful to characterize the response of photodetectors

$$\mathcal{R} = \frac{q \cdot \eta}{h \cdot \nu} = \frac{\eta \cdot \lambda (\mu m)}{1.24}$$

- Responsivity is typically linear with wavelength but real photodetectors exhibit a deviation from the ideal behaviour due to photogenerated carrier trapping



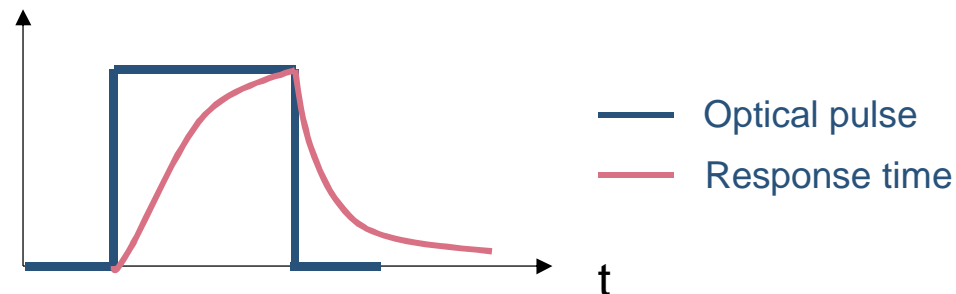
Photodetector characteristics: Response time (I)

■ Response time of the photodetectors:

- ✓ Internal response time
- ✓ External response time

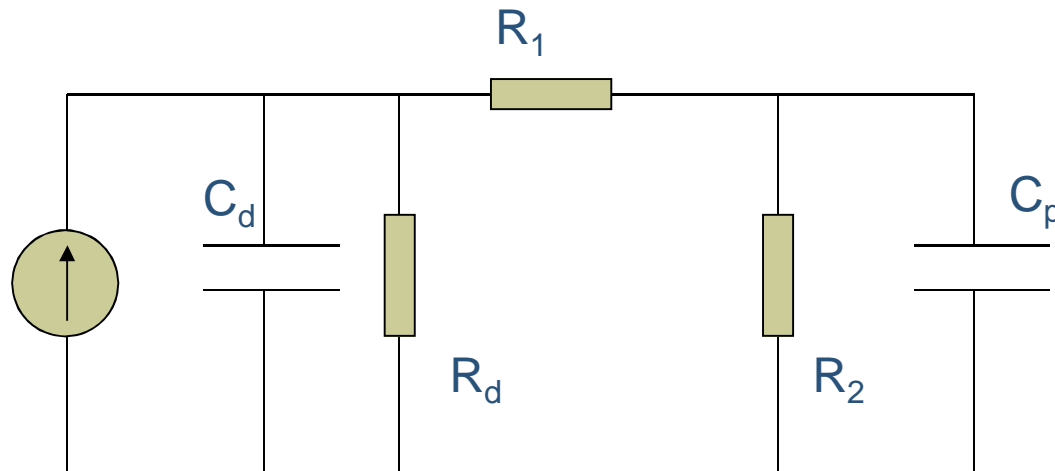
■ Internal response time

- ✓ Transit time of carriers: depends on the velocity of carriers in SC (varies with the doping level and the material)
- ✓ Diffusion time of carriers: diffusion of carrier to be collected. Mainly depends on the structure





■ External response time



typical schematic electrical circuit of the photodiode

C_d : Diode capacitance

C_p : Parasitic capacitance

R_d : Diode resistance

R_1 : contact and substrate resistances

R_2 : charge resistance

$$R_1 \text{ and } R_d \ll R_2$$

$$\text{Response time} = R_2 (C_p + C_d)$$



- “Compatibility” with silicon technology
 - ✓ Silicon-based materials will be better
 - ✓ Large wafer scale technology
 - ✓ Permit electronic integration (Transimpedance amplifier – TIA)
 - ✓ Low cost integration schemes

- Broadband detection (1.3 -1.6 μm)
 - ✓ High absorption coefficient

- Low dark current
 - ✓ Electrical configuration of photodetectors,
 - ✓ Quality of the absorbing layer.



- ❑ High bandwidth (frequency operation > 10 GHz)
 - ✓ Low carrier transit time,
 - ✓ Low RC constant – depend on the considered electrical structure (pin diode, MSM detector).

- ❑ High responsivity
 - ✓ Optimize the light interaction with absorbing layer.

- ❑ Compactness
 - ✓ Strong absorption coefficient



Two approaches



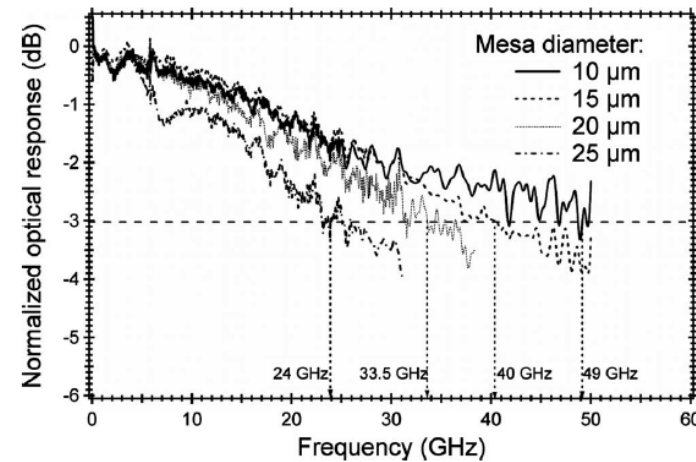
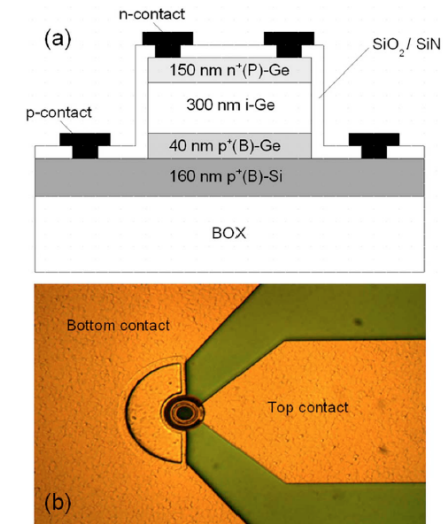
Surface illuminated photodetectors



High bandwidth
"Simple" process



"Low" responsivity



Responsivity ~ 0.1 A/W



Two approaches



Surface illuminated photodetectors



High bandwidth
"Simple" process



"Low" responsivity

photodetectors integrated in waveguide



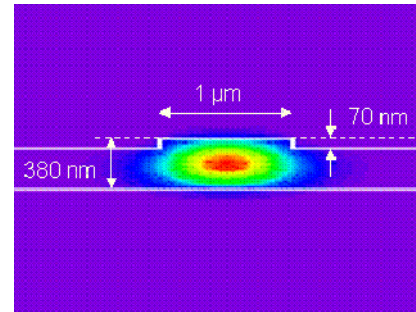
High bandwidth
High responsivity



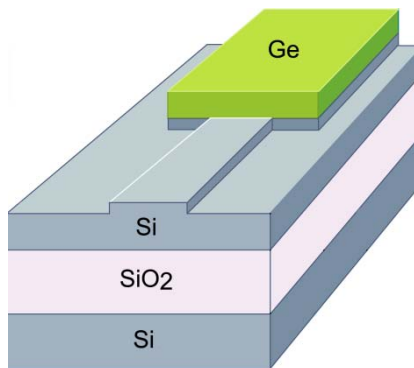
Optical coupling



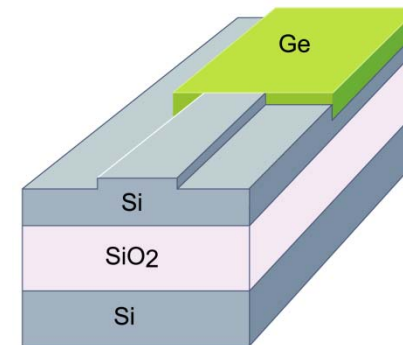
SOI waveguides



Single mode (TE)



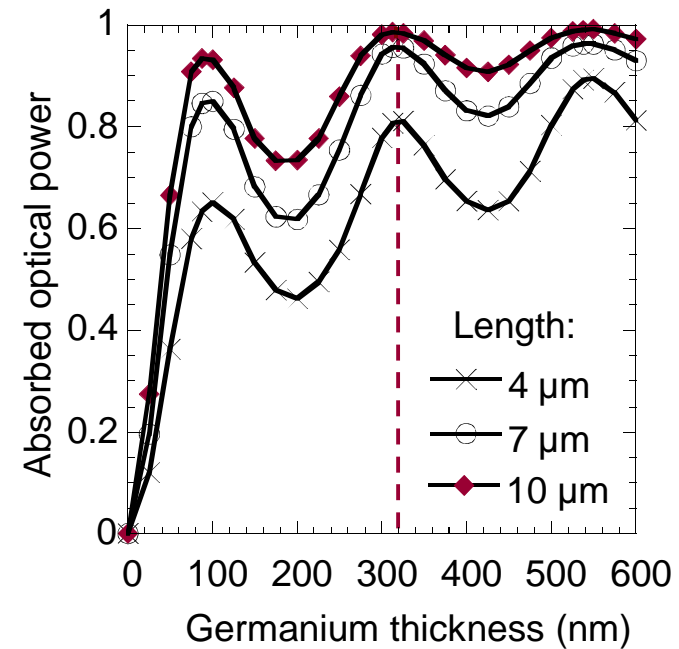
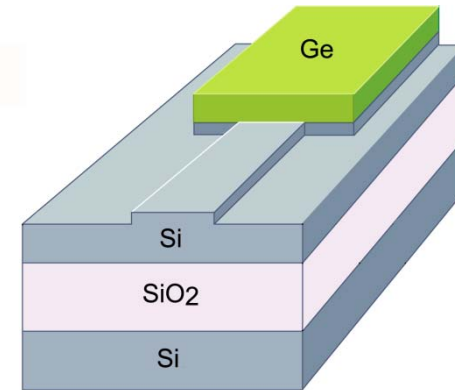
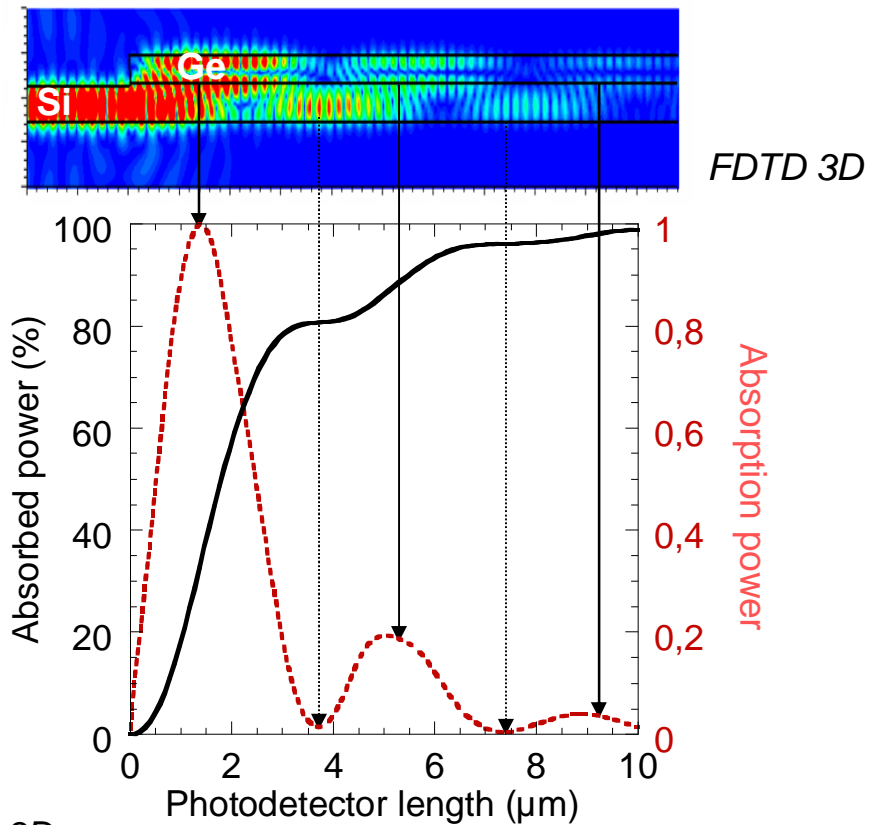
Vertical coupling



Butt coupling



Vertical coupling

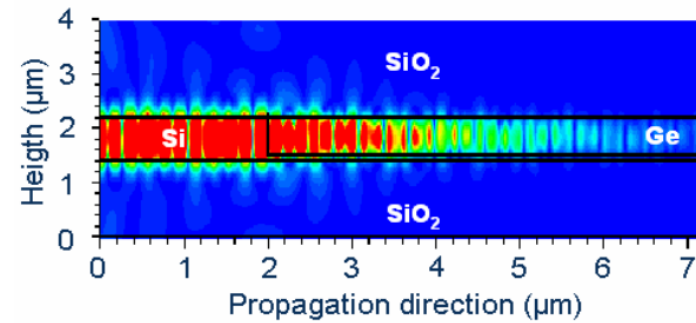
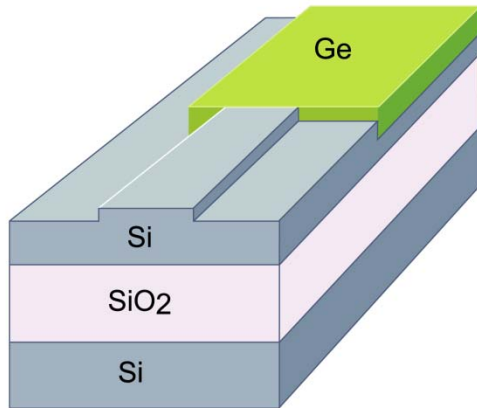


M. ROUVIÈRE, et al., *Optical Engineering*, 44 (2005) 183-187

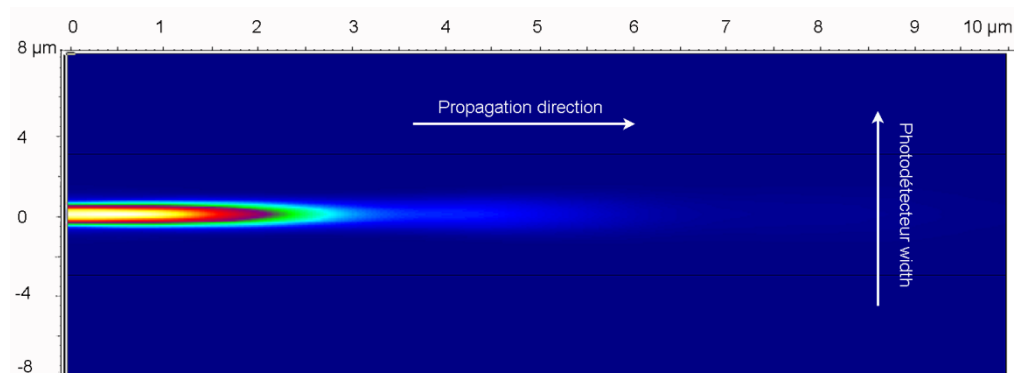
95 % absorption length < 10 μm with 310nm germanium thickness



Butt coupling



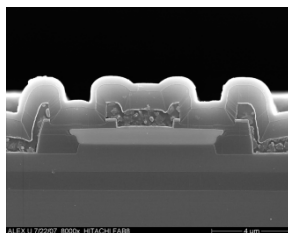
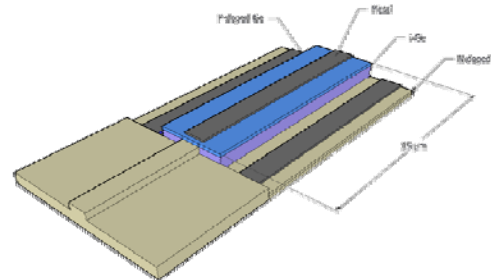
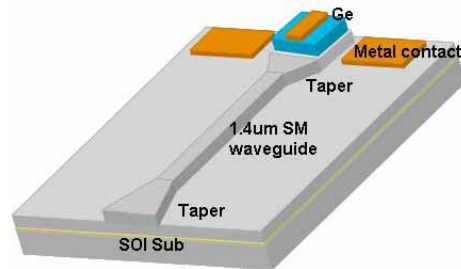
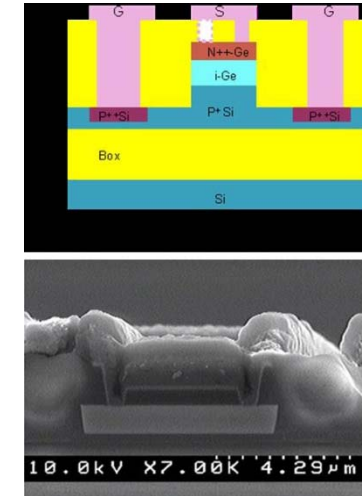
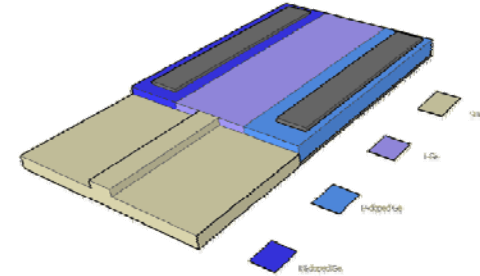
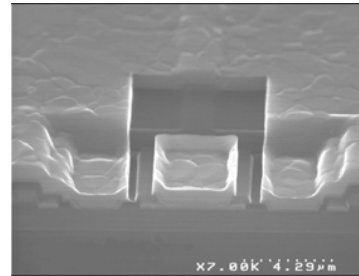
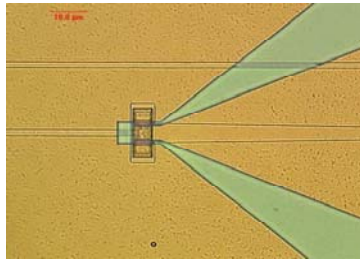
95% absorption length < 4μm



Negligible lateral divergence



Ge Photodetectors



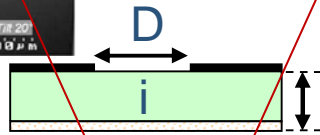
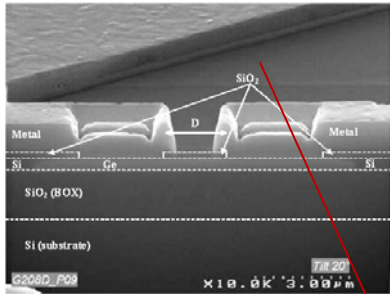
Europe: PSUD-IEF, CEA-Léti, Stuttgart Univ., Roma Univ. ...

Asia: Tokyo Univ., A*Star, Petra, AIST, Chinese Academy of Sciences, ...

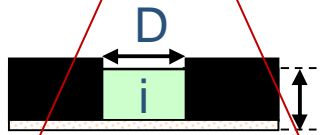
North America: Intel, MIT, IBM, Cornell, Luxtera, Lighthwire, Kortura, Oracle ...



Photodetector: electrical structures

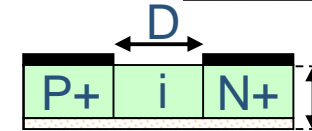
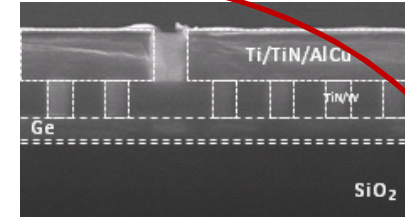


Surface contact MSM

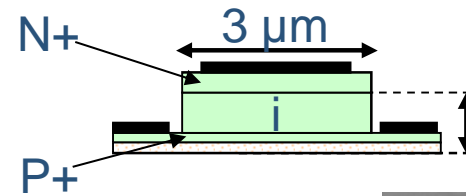


Lateral contact MSM

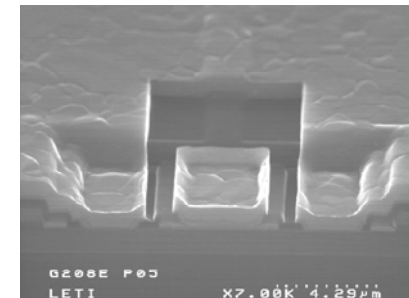
PIN



Lateral PIN



Vertical PIN

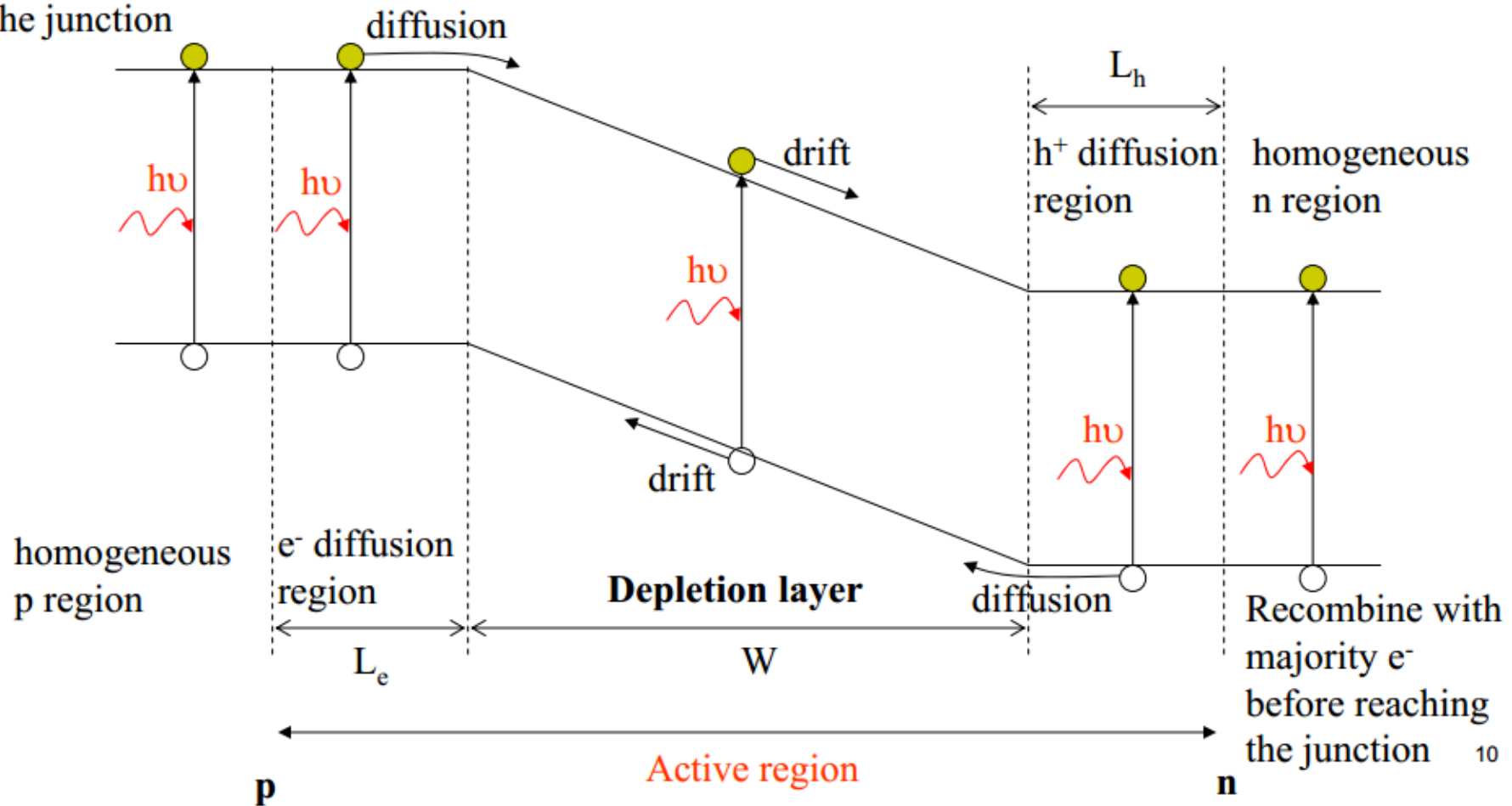




Diode band structure

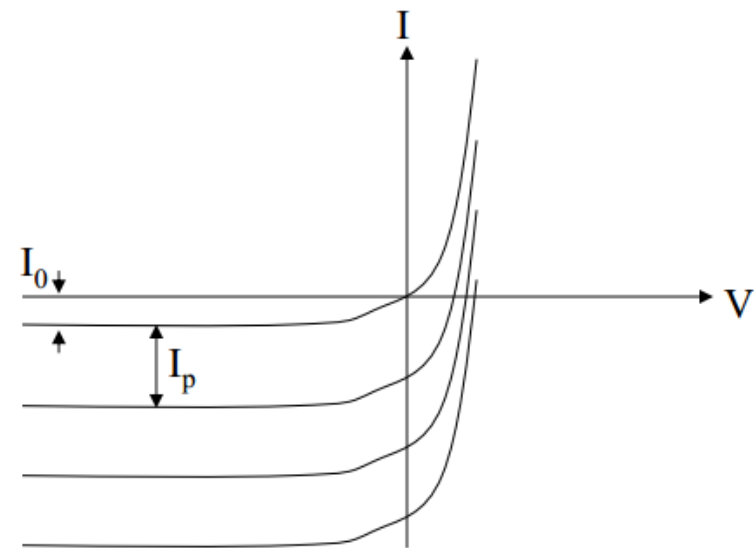
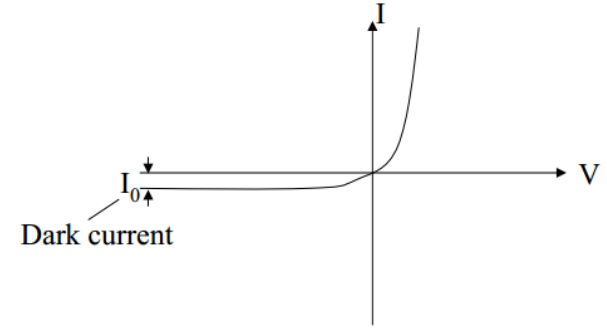
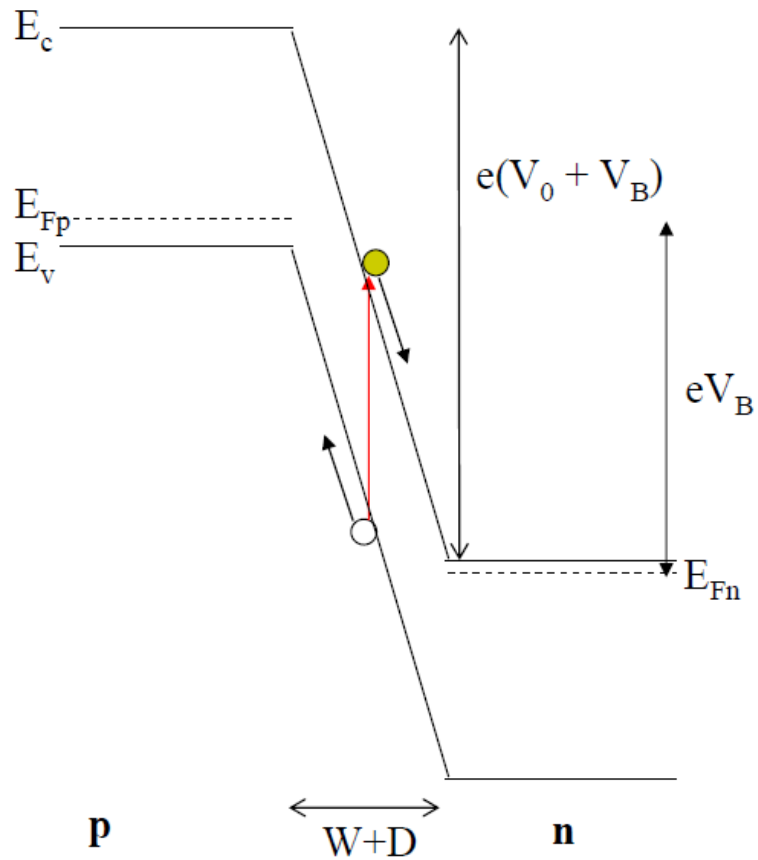


Recombine with majority h^+ before reaching the junction





Diode band structure



Forward or reverse bias ?

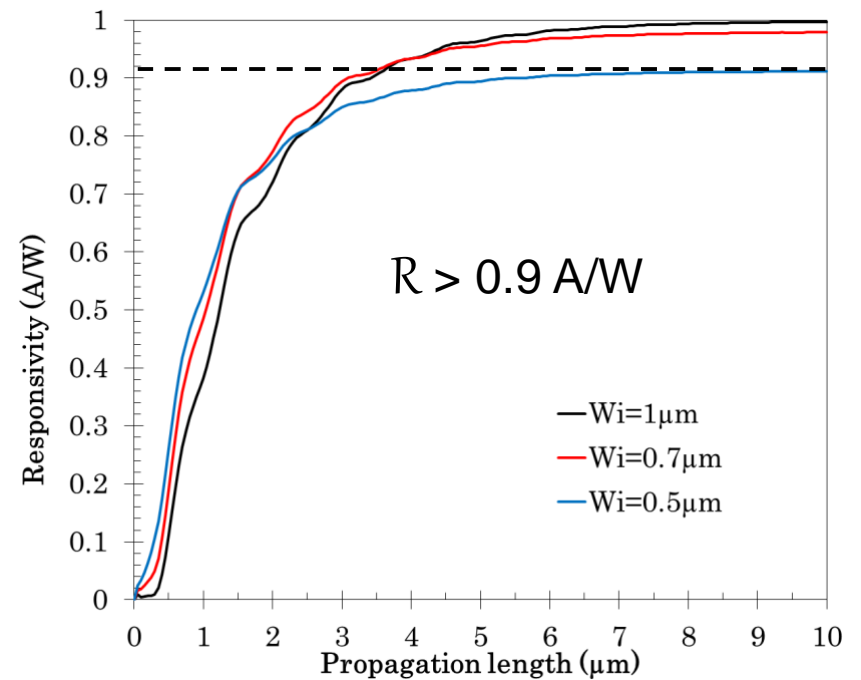
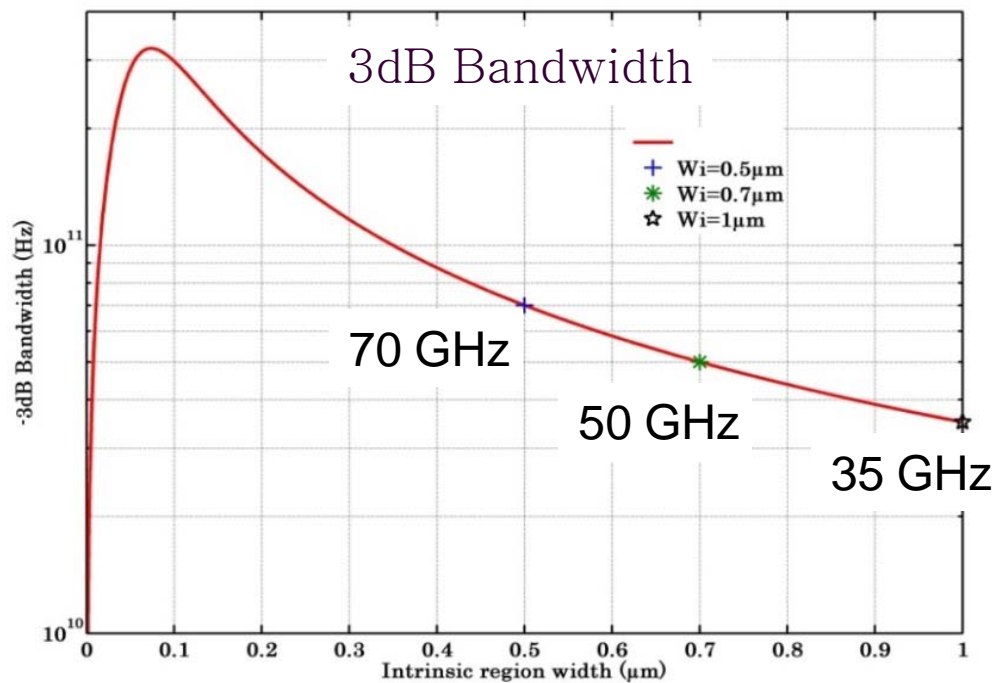
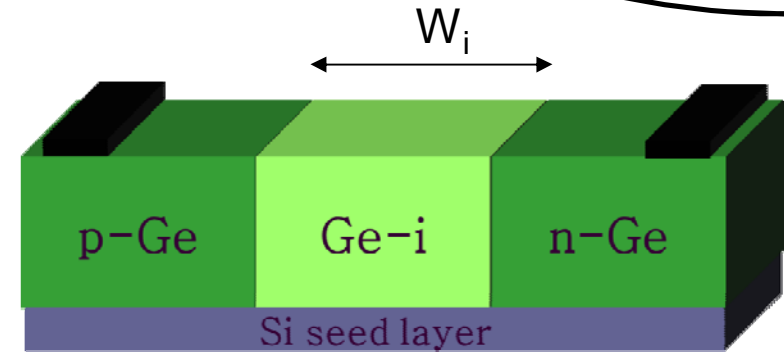


PIN Photodiodes : Design considerations

■ Junction disposition

√ Lateral PIN

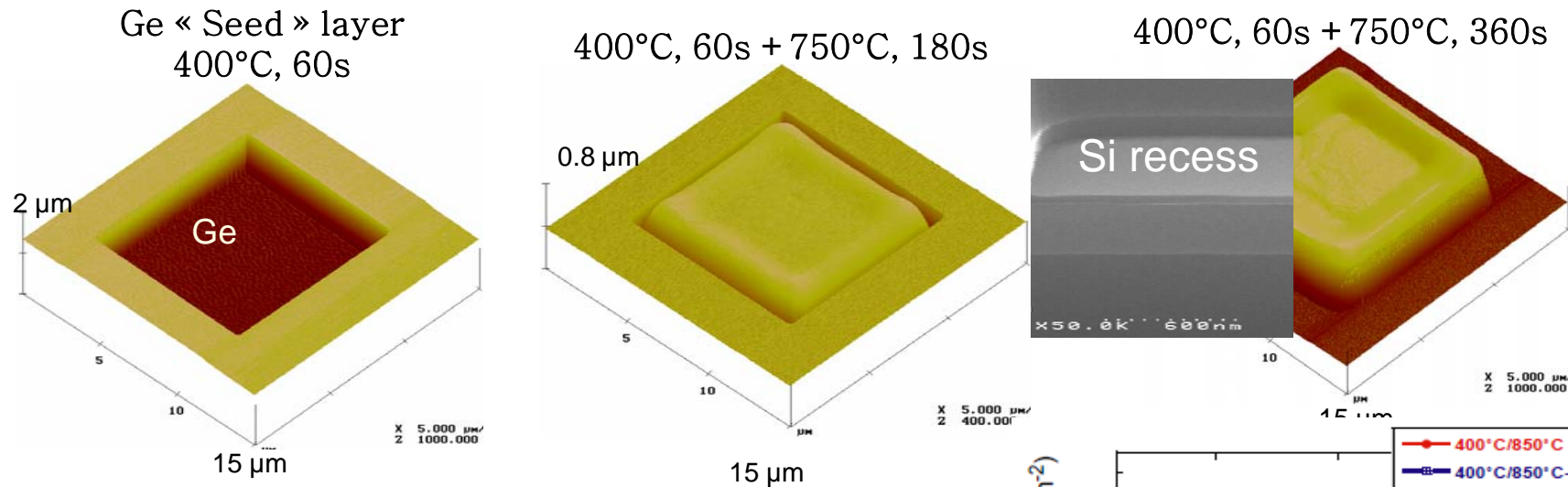
- Contact on Ge: only one etching step
- Definition of intrinsic region by ion implantation





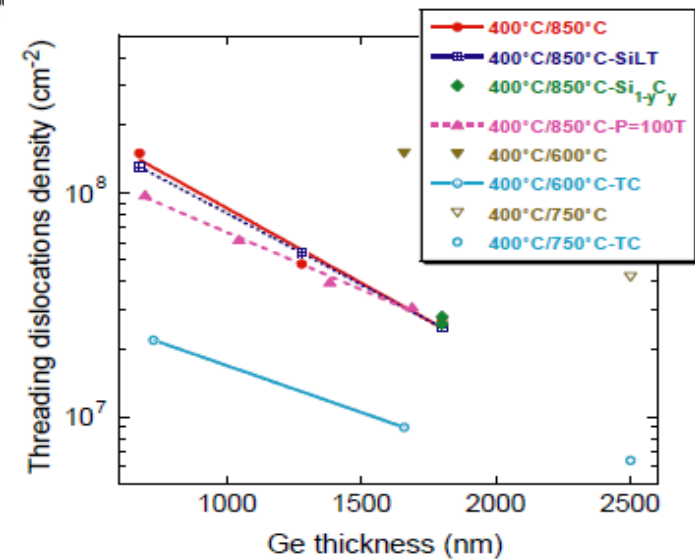
Device Fabrication: Ge Growth

- Two RPCVD steps to overcome lattice mismatch issue



- Overgrowth of Ge

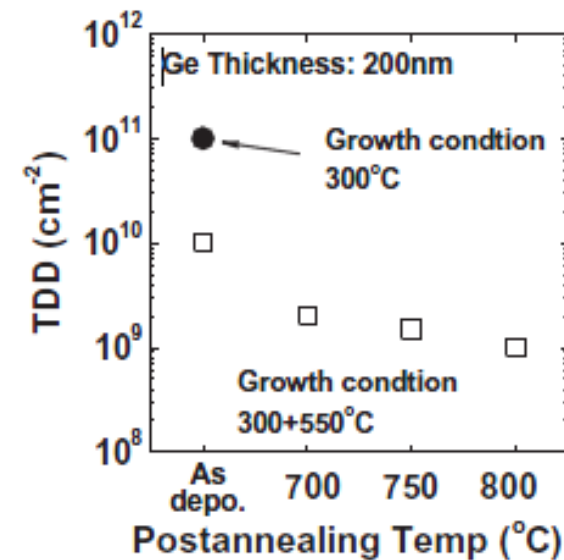
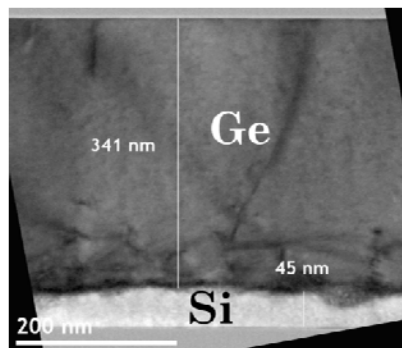
- To avoid faceting inside the cavity
- To reduce Threading Dislocation Density (TDD)



J.M. Hartmann et al., *J. Crystal Growth*, **274**, 90-99 (2005)



- Post epitaxial thermal cycling to further reduce TDD in the Ge layer
- CMP step to remove protruded Ge
- SiO₂ encapsulation
- Ion implantation of Ge
 - √ N-type : Phosphorus
 - √ P-type : Boron
- Rapid Thermal Anneal

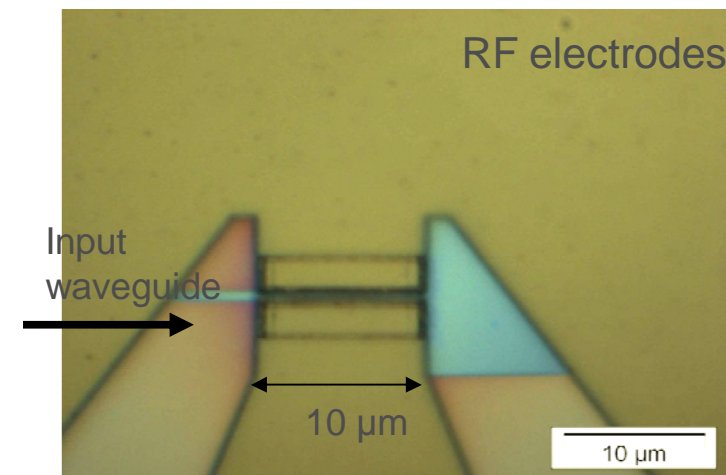
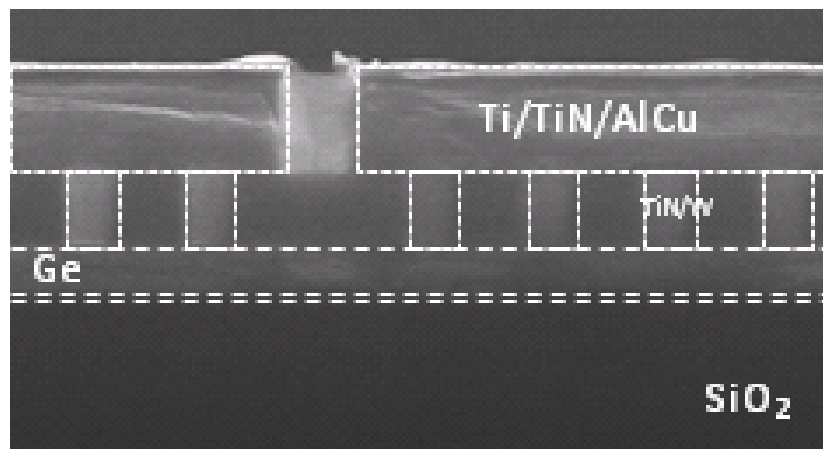
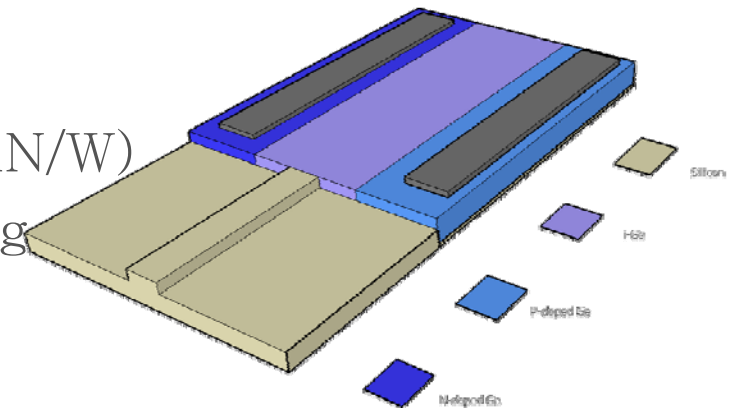


Y. Yamamoto et al., *Solid-State Electronics*, **60-1**, 2–6, (2011).



- Oxide encapsulation
- Planarization
- Contact definition
 - $0.4 \times 0.4 \mu\text{m}$ vias for metal filling (TiN/W)
 - Ti/TiN/AlCu pad defined by etching

Lateral





Results : Dark current and responsivity



Dark current median, mean and best values (373 dies per wafer)

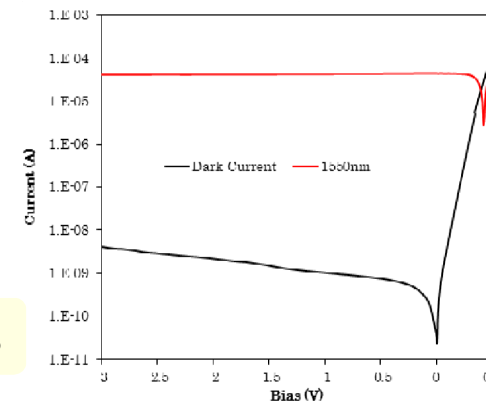
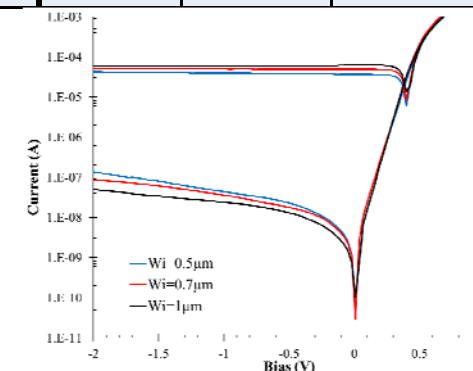
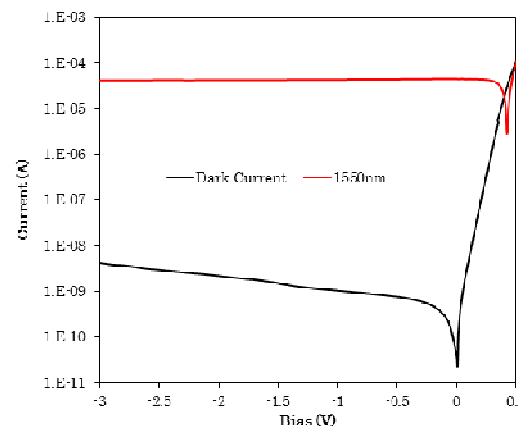
Photodiodes		Wi=0.5μm			Wi=0.7μm			Wi=1μm		
Wafer		1	2	3	1	2	3	1	2	3
@-1V	Median (nA)	85	74	112	66	62	80	68	61	71
	Mean (nA)	433	105	1707	350	83	576	347	110	963
	Best (nA)	32	25	27	18	9.5	9	19	17	6
Yield		99.2%	99.7%	97.8%	100%	100%	99.7%	100%	100%	99.7%

New run: dark current ~1nA @ -1V for $W_i = 0.5\mu\text{m}$

Responsivity @ 1550nm under Zero bias

Wi=0.5μm	0.5A/W
Wi=0.7μm	0.6A/W
Wi=1μm	0.8A/W

Efficient carrier collection at zero bias due to strong built-in electric field



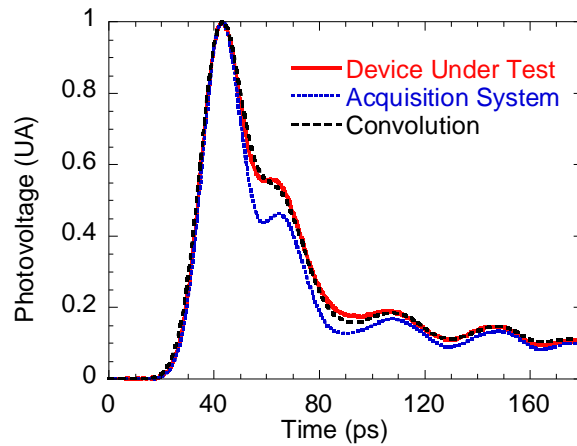
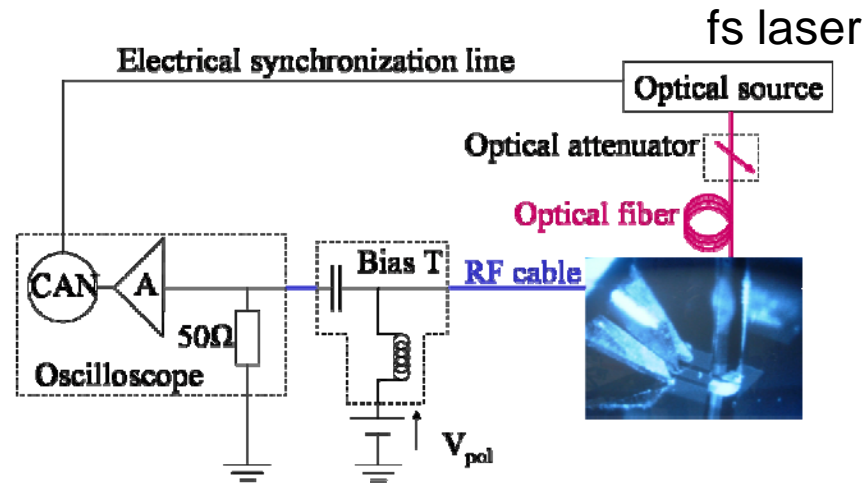
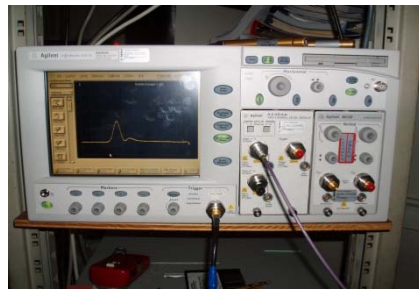
Measured responsivity lower than theoretical values



Characterization methods: Bandwidth (I)



□ Femtosecond pulse experiments



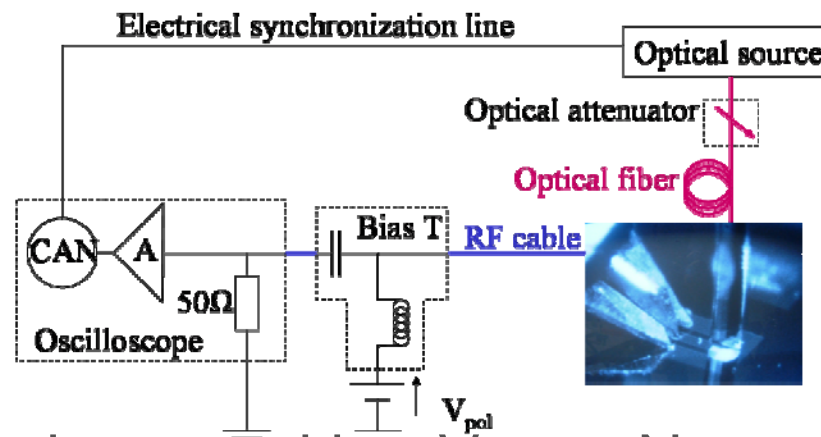
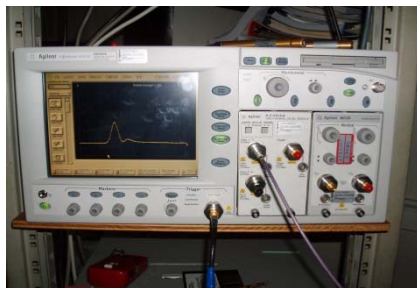
Response time (ps)



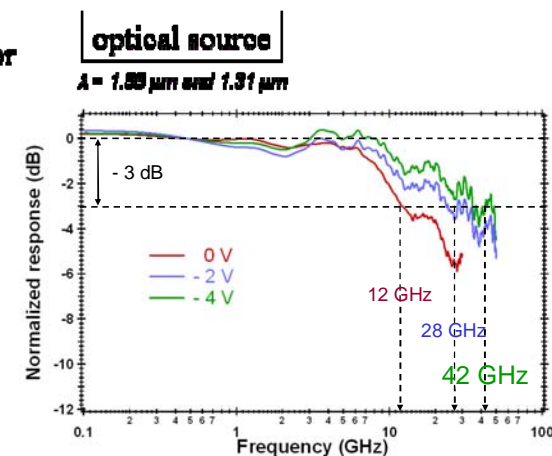
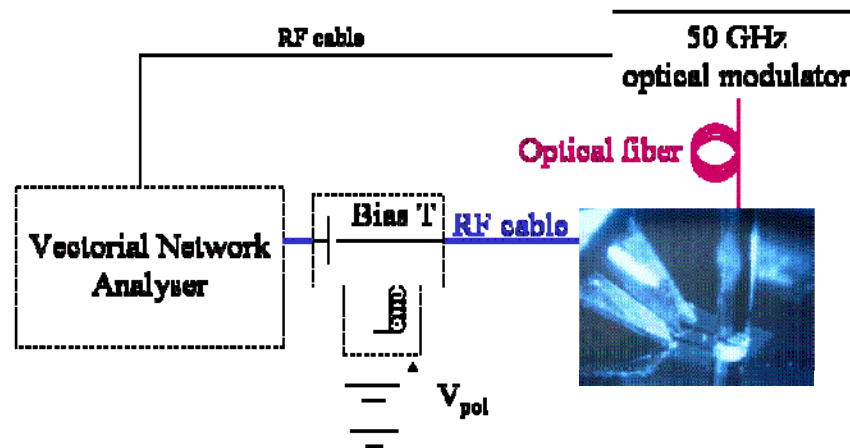
Characterization methods: Bandwidth (I)



□ Femtosecond pulse experiments

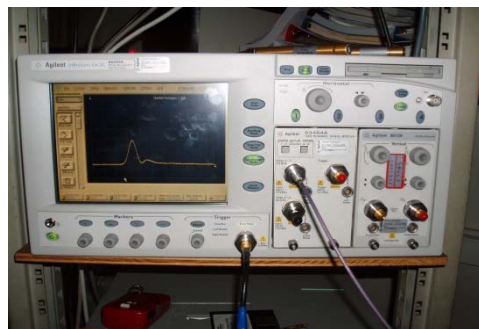
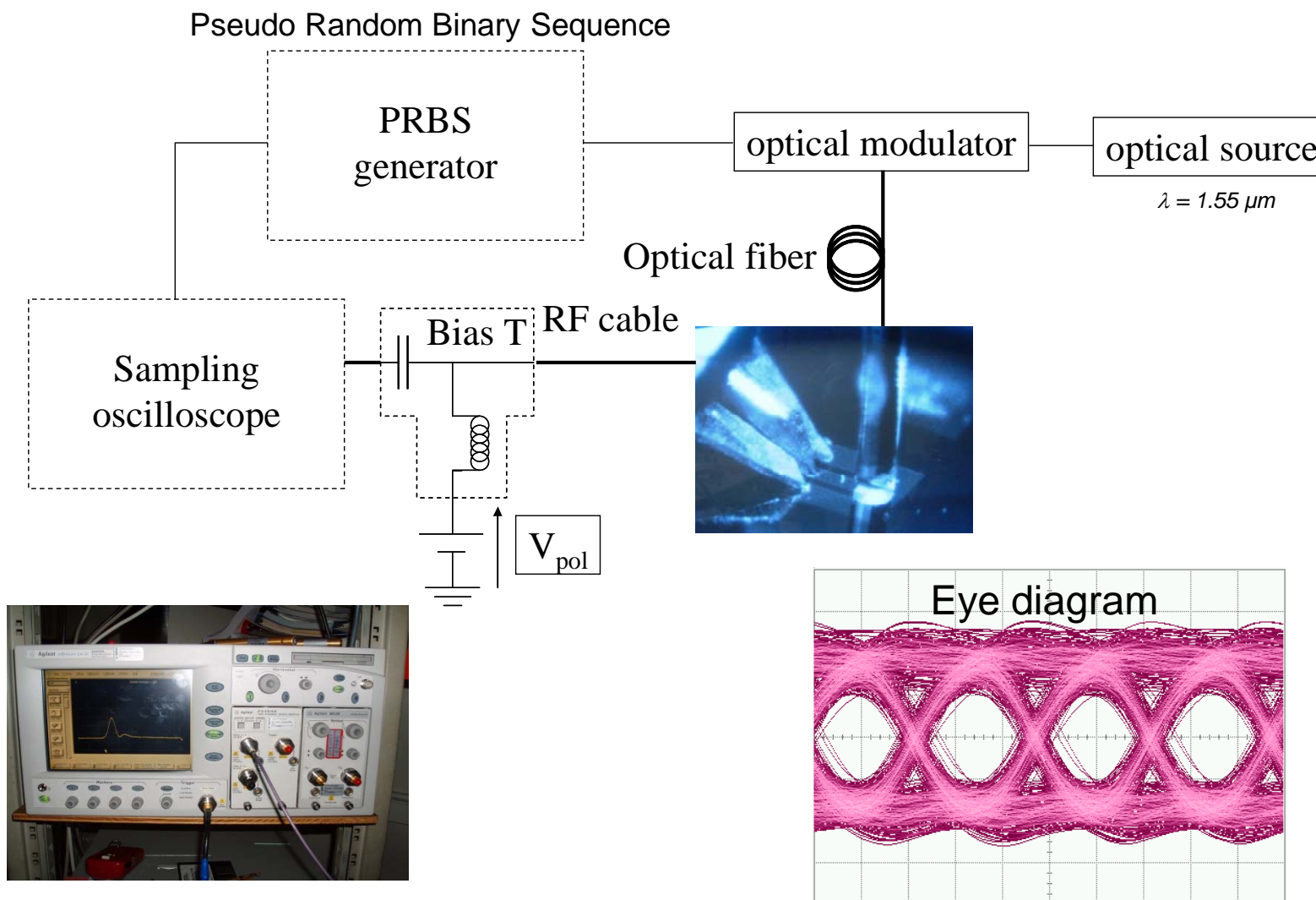


□ Opto-RF experiments with a Vector Network Analyzer





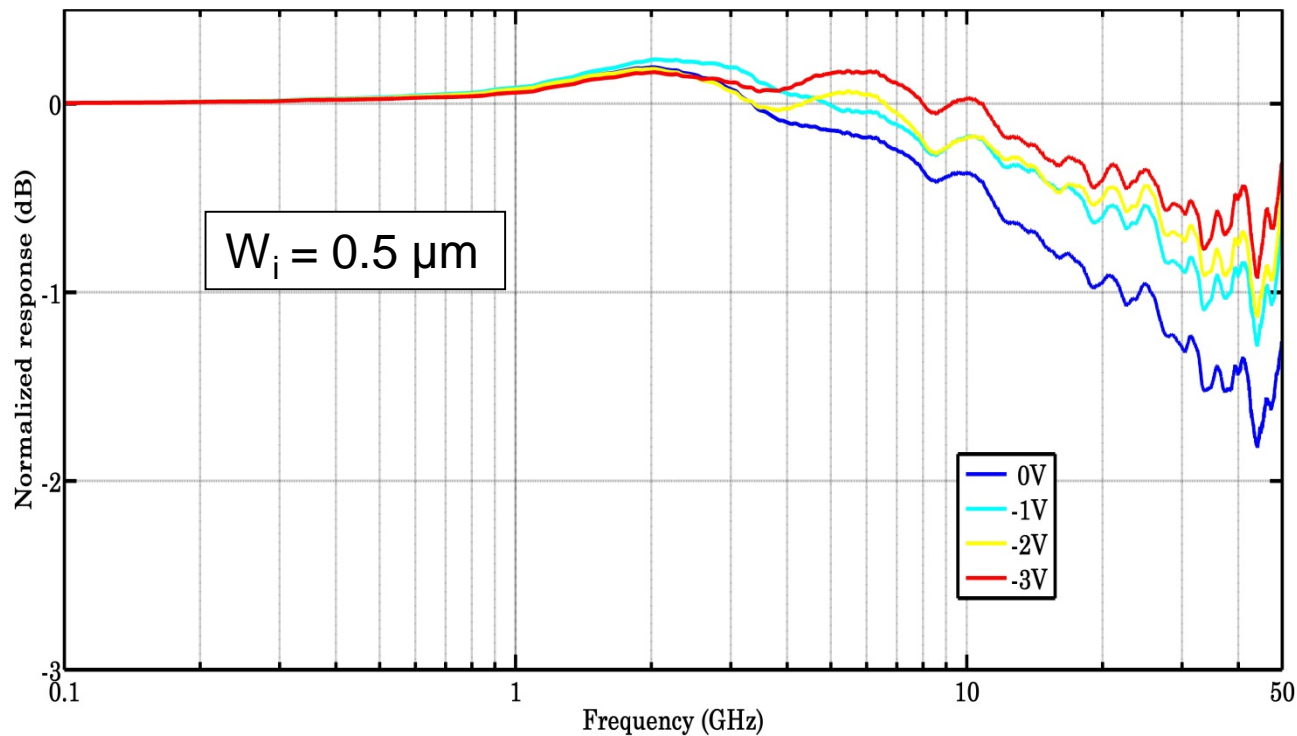
■ Data transmission measurements



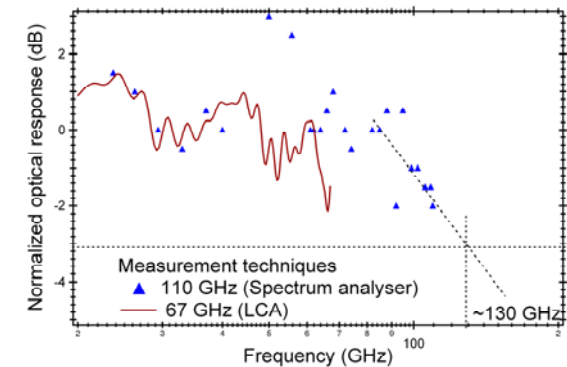


Results : Bandwidth measurement

- Opto-electric frequency response measurement using 50GHz Lightwave Component Analyzer (@1550nm)



-3dB Optical Bandwidth
Over 50GHz
@ 0V



Bandwidth higher than theoretical values



Lower responsivity

	Exp (A/W)	Theo (A/W)
$W_i=0.5\mu\text{m}$	0.5	0.91
$W_i=0.7\mu\text{m}$	0.6	0.96
$W_i=1\mu\text{m}$	0.8	0.99

=> Loss of photo-generated carriers

Higher bandwidth

Measured BW: >130GHz



Theoretical BW: 70GHz

=> Faster carrier collection

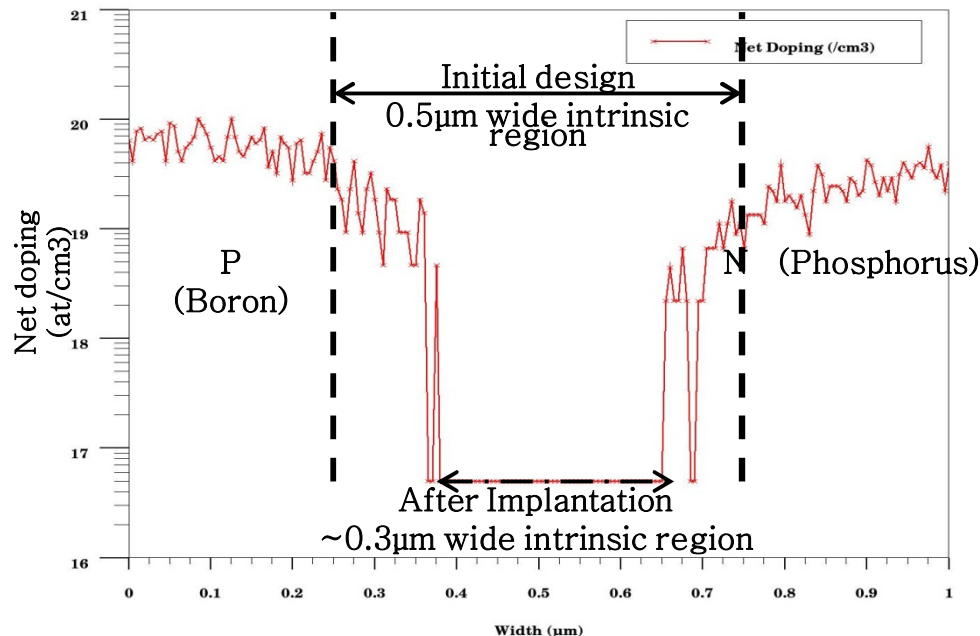
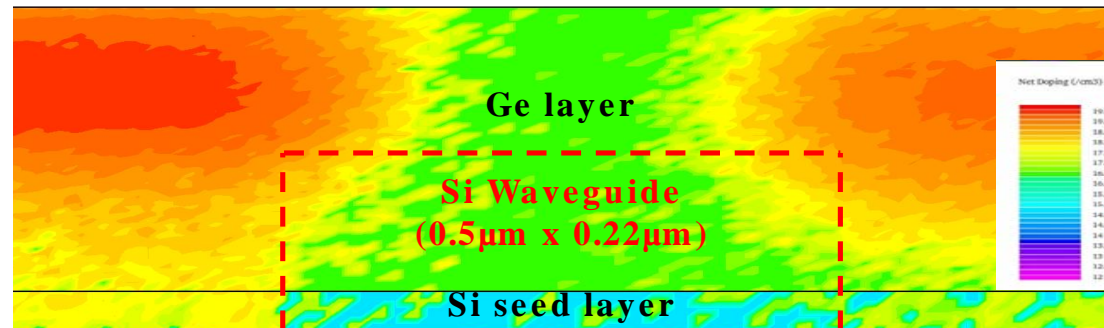
Why are the responsivity lower and the BW higher than theoretical values?

Reduction of the absorption region width



■ Ion implantation

✓ Monte Carlo simulation of ion implantation process



Narrowing of the intrinsic region

→ Absorption inside the doped region

✓ Max responsivity $\sim 0.6 \text{ A/W}$

→ Increase of the electric field strength

✓ Max BW $\sim 120 \text{ GHz}$



Data transmission

Results beyond specifications

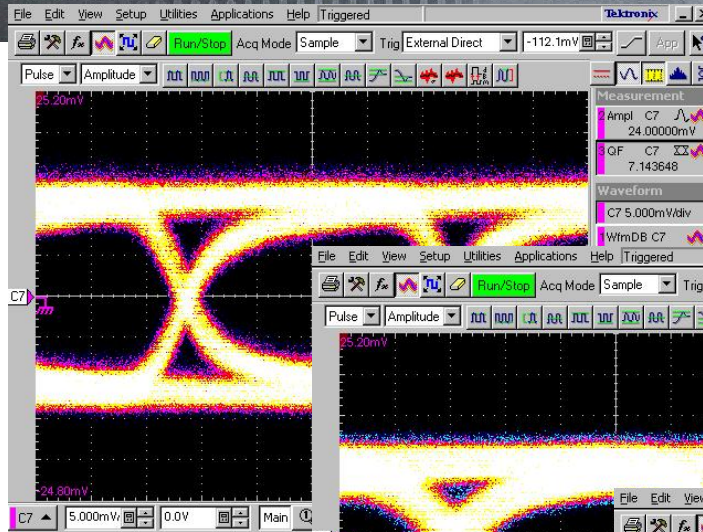
- High responsivity: > 0.5A/W
- High bandwidth: 40Gbit/s
- Low dark current: <1nA @ -1V
- Bias voltage: 0V

Under zero-bias

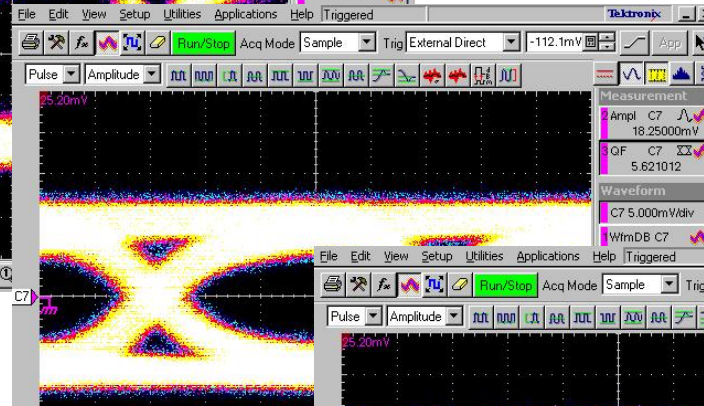


Coll.:

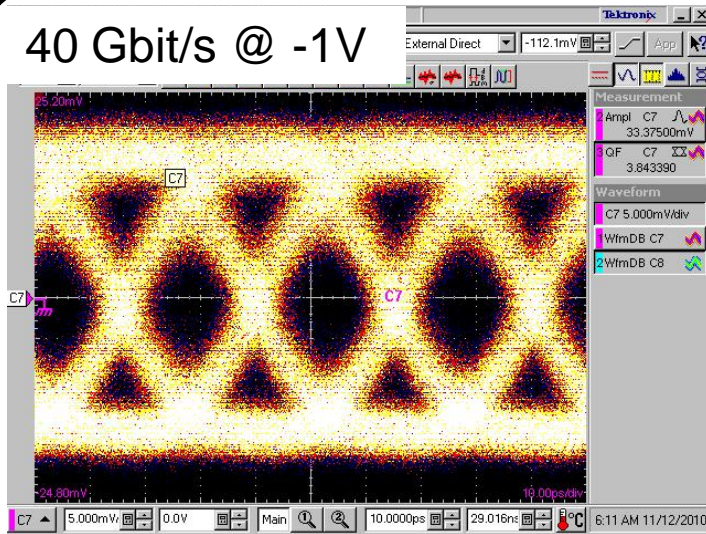
10 Gbit/s



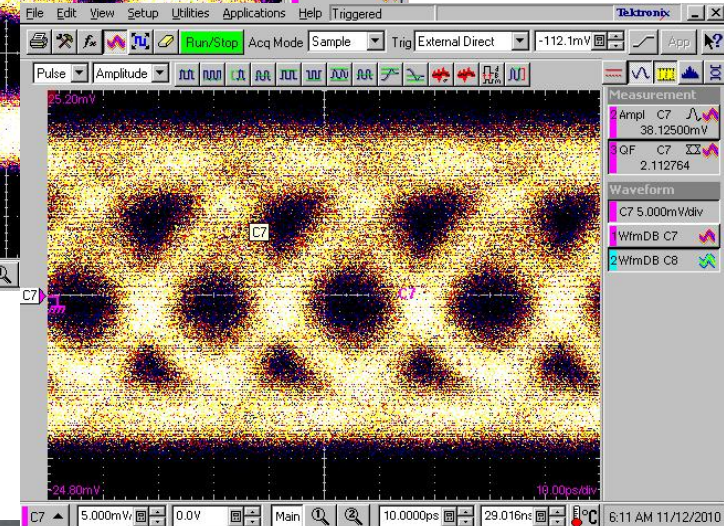
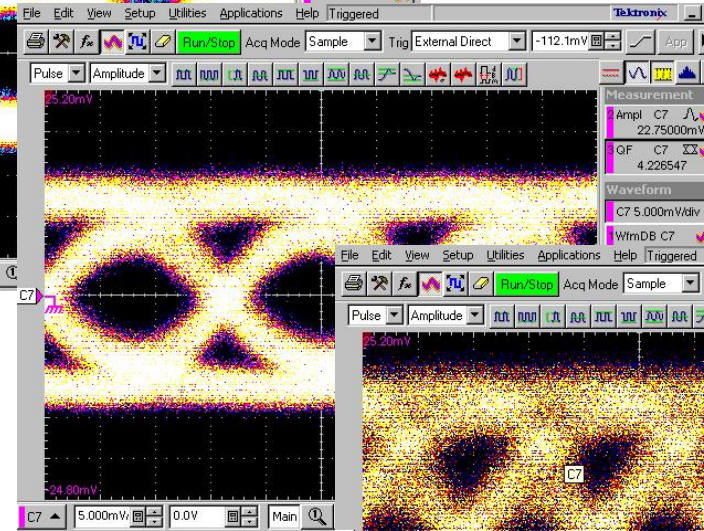
20 Gbit/s



40 Gbit/s @ -1V



40 Gbit/s





How can we increase the receiver bandwidth?

....Towards Tbit/s....

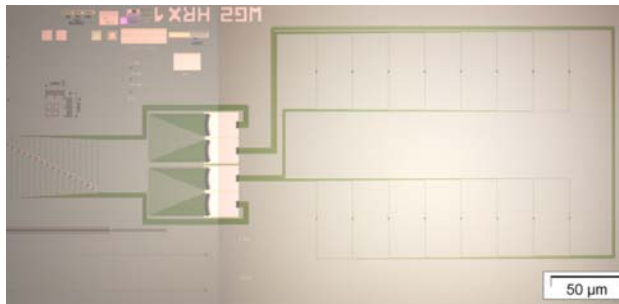


To improve bandwidth of receiver

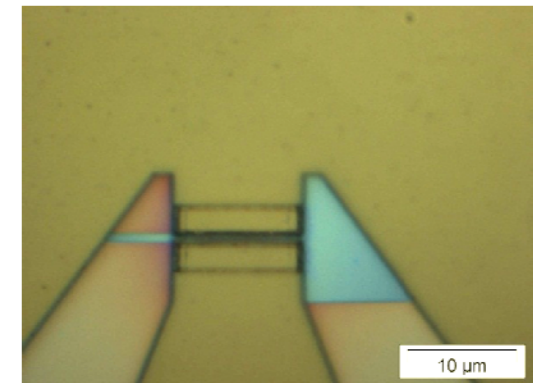
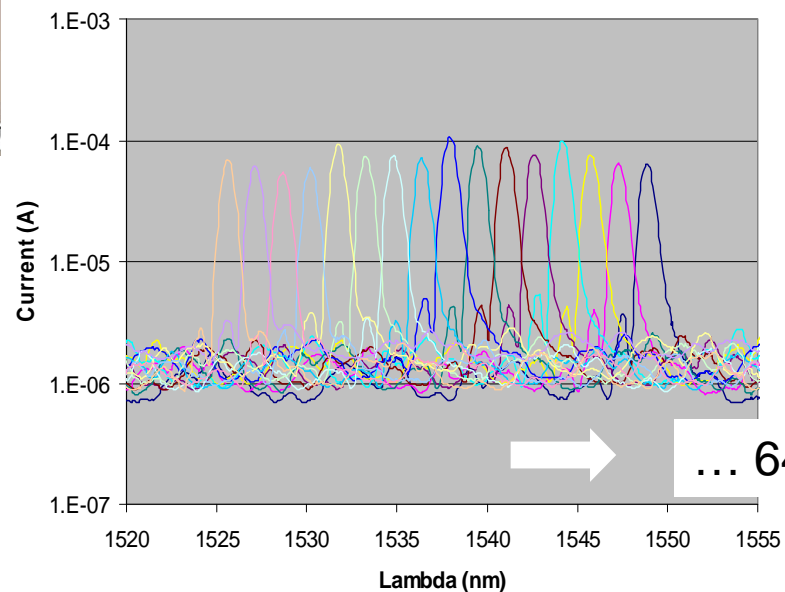
$$\text{Bandwidth} = \text{Parallelism} \times \text{Frequency}$$

■ Need more wavelengths

■ 40Gbit/s detector



2 x 16 channels 200GHz centered at about 1550nm





Conclusion

- Germanium photodetectors are more and more considered as a mature silicon photonics devices.
- The PD characteristics are close to the one of III-V PD.
 - √ Incredible at the beginning.
- The trends
 - √ Development of complex circuits for Tbit/s operation
 - √ Integration with CMOS circuits (TIA)
 - √ Avalanche PD ...
 - new route to reduce the power consumption of the emitter
 - Photon counting – Quantum optics