Silicon photonics: Waveguide modulators and detectors

Laurent Vivien

_Institut d’Electronique Fondamentale_

_CNRS UMR 8622_

_Université Paris Sud, 91405 Orsay Cedex_

_France_
Silicon photonics: Waveguide modulators and detectors

Laurent Vivien
Institut d’Electronique Fondamentale, CNRS UMR 8622, Université Paris Sud, 91405 Orsay Cedex, France
http://silicon-photonics.ief.u-psud.fr/
Silicon photonics:
Waveguide modulators and detectors

L. Vivien, 

Institut d’Electronique Fondamentale, CNRS UMR 8622, Université Paris Sud, 91405 Orsay Cedex, France

http://silicon-photonics.ief.u-psud.fr/

J-M. Fédéli, S, Olivier, Jean Michel Hartmann
CEA-LETI, Minatec 17 rue des Martyrs, 38054 Grenoble cedex 9, France

G. Isella, D. Chrastina, J. Frigerio
L-NESS, Politecnico di Milano, Polo di Como, Via Anzani 42, I-22100 Como, Italy

C. Baudot, F. Boeuf
STMicroelectronics, Silicon Technology Development, Crolles, France

http://silicon-photonics.ief.u-psud.fr/
The Institute for Fundamental Electronics

IEF is a joint research unit between CNRS and University of Paris Sud

135  CNRS researchers, professors and lecturers, technical staff

+100  PhD students, Post-Doc and visitors

~ 400  students undergoing training within IEF’s ground

Spintronics and Si-based Nano-electronics

Micro-Nano systems and systems

Photonics

University Technology Center (CTU) MINERVE

http://silicon-photonics.ief.u-psud.fr/
University Technology Centre (1000 m²):

Photolithography:
- 2-sided UV lithography with wafer bonding
- Deep UV lithography (248 nm)
- 2 e-beams (Raith150 and 100keV nanobeam)
- Laser

Etching:
- Wet etching (KOH, TMAH, …)
- Dry etching:
  - fluoride gases RIE (2 systems)
  - ICP Si deep etching
  - IBE
  - $O_2$ plasma etching
  - Chloride gases RIE

…
Silicon photonics group

- 4 permanent Researchers
- 2 engineers, technicians
- 16 PhD students
- 2 post-doc
- 2-4 master students / year

Passive devices
Grating couplers
- Waveguides
- Splitters
- Optical Distribution
- Multi-wavelength circuits

Optical modulators
- All silicon
- NL materials
- Plasmon

Ge detectors
- Surface illuminated
- Integrated
- APD

Photonic crystals
- Slow light
- Superprism
- NL enhancement

Strained Si photonics
- Pockels effect

Ge-SiGe QW photonics
- Source
- Modulator
- detector

Carbon nanotubes for photonics

http://silicon-photonics.ief.u-psud.fr/
Outline

- Motivation (Pavel’s and Lorenzo’s talks)
- Photodetectors on silicon
  - Main characteristics
  - Results
- Optical modulators
  - Figures of Merit
  - Modulation in silicon
  - Results
- Conclusion
Data centers

Optical telecommunications

FTTH

Environment

Chemical/Biological sensors

Military

Interconnects

Silicon photonics

Free space communications
Silicon photonic building blocks

Off-chip III-V laser

On-chip III-V laser on Si

Photodetector

Germanium-based laser

Emitter

Laser → Modulator → Receiver → Detector

Modulator
Photodetection
Main characteristic of the material?
The absorption of photons generates electron-hole pairs

Photogenerated carriers are then collected thanks to an external field

√ Photocurrent
Absorption mechanisms (II)

- Direct gap SC (III-V SC)
- Indirect gap SC (IV-IV SC)

- absorbed photons *generate* free electron-hole pairs

\[ E_G = \frac{hc}{\lambda_G} \]

http://silicon-photonics.ief.u-psud.fr/
Material choice

- Wavelength ranges:
  - $1.3 \, \mu m - 1.6 \, \mu m$
  - $0.85 \, \mu m$

![Graph showing absorption coefficient vs. wavelength with different materials']
Material choice

- Wavelength ranges:
  - 1.3 µm – 1.6 µm
  - 0.85 µm
Material choice

- Wavelength ranges:
  - $\sqrt{1.3 \, \mu m - 1.6 \, \mu m}$
  - $\sqrt{0.85 \, \mu m}$

Two choices: InGaAs or Ge
InGaAs versus Germanium

What is the best material for light detection in near-IR wavelength range?
Material choice versus electronic photonic integration scheme

1) Wafer bonding of PIC (high T°C)
2) BE fab(<400°C)

Photonic layer at the last levels of metallizations with back-end fabrication

Combined front-end fabrication

• Specific FE CMOS technology and library
• Flip-Chip hybridization of InP components
• Moderate integration density
• Efficient connections of EIC and PIC

Backside fabrication

1) Wafer bonding of PIC (high T°C)
2) BE fab(<400°C)

• Use of standard FE CMOS technologies
• High integration density (AboveIC)
• Multilevel process capability

BE: Back end  FE:Front end

http://silicon-photonics.ief.u-psud.fr/
Material choice versus integration scheme

1) Wafer bonding of PIC (high T°C)
2) BE fab(<400°C)

Ge or InGaAs

InGaAs

Photonic layer at the last levels of metallizations with back-end fabrication

Combined front-end fabrication

Backside fabrication

1) Wafer bonding of PIC (high T°C)
2) BE fab(<400°C)

Ge

Ge or InGaAs

InGaAs

BE: Back end  FE: Front end
Are III-V materials integrated in silicon platform?

- Monolithic integration via epitaxial growth
  No viable solutions yet

- Hybrid integration
  BCB or molecular bonding
Exemple of hybrid integration

1. Sample preparation
2. Sample cleaning + removal of cap layer
3. BCB bonding and curing
4. InP substrate removal
5. Removal of sacrificial layers
6. Detector mesa etching
7. BCB insulation
8. Opening of the contact windows
9. Metallization
10. Post-processing

III-V materials can be integrated on silicon
What about wafer size and technology?
Germanium on silicon: Pros and Cons

- Absorption coefficient of pure Ge:
  - \( \alpha \approx 9000 \text{ cm}^{-1} \) at \( \lambda = 1.3 \mu\text{m} \)
  - \( L_{\text{ABS}}^{95\%} \approx 3.3 \mu\text{m} (!) \)
  - \( \Rightarrow \) Low capacitance devices
  - \( \Rightarrow \) High frequency operation

- High carrier mobility
Si and Ge have a diamond lattice structure (two interdigitated FCC lattices)

<table>
<thead>
<tr>
<th>Properties</th>
<th>Silicon</th>
<th>Germanium</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lattice parameter: a (Å)</td>
<td>5.431</td>
<td>5.658</td>
</tr>
<tr>
<td>Atomic density (cm⁻³)</td>
<td>5.0.10²²</td>
<td>4.42.10²²</td>
</tr>
<tr>
<td>Atom radius (Å)</td>
<td>0.117</td>
<td>0.122</td>
</tr>
<tr>
<td>Lattice structure</td>
<td>Diamond</td>
<td>Diamond</td>
</tr>
</tbody>
</table>

Lattice parameter mismatch: ~4.2 %
Germanium on silicon: Pros and Cons

- Absorption coefficient of pure Ge:
  - $\alpha \approx 9000 \text{ cm}^{-1}$ at $\lambda = 1.3\mu\text{m}$
  - $L_{\text{ABS}}^{95\%} \approx 3.3\mu\text{m}$ (!)
  - Low capacitance devices
  - High frequency operation

- High carrier mobility

- Lattice misfit with Si of about 4.2%
  - $\Rightarrow$ specific growth strategies required (wafer-scale and localized)

- Low indirect bandgap: $E_G = 0.66\text{eV}$
  - $\Rightarrow$ high dark current for MSM devices

Can we directly growth Ge on silicon?
4.2% of lattice mismatch between germanium and silicon

- Ge quantum dots
- Si$_{1-x}$Ge$_x$/Si quantum wells
- Pure Ge on Si

The lattice mismatch

QD, QW or Bulk?
Ge-based structures

- Ge quantum dots
  \[ \alpha \approx 20 \text{cm}^{-1} \] (90% absorption length ~ 1.1mm)

- Si\textsubscript{1-x}Ge\textsubscript{x}/Si quantum wells
  \[ \alpha \approx 100-200 \text{cm}^{-1} \] (90% absorption length ~ 230-110µm)

- Pure Ge on Si
  \[ \alpha \approx 7500 \text{cm}^{-1} \] (90% absorption length ~ 3µm)
Thick virtual SiGe substrates (10µm)

- Need for a new integration scheme – difficult to integrate with SOI waveguides.
Ge growth strategies

- Thick virtual SiGe substrates (10µm)
  - Need for a new integration scheme – difficult to integrate with SOI waveguides.

- Growth on thin SiGe buffers
  - The thickness of the thin SiGe buffer is around 1µm
    - Always too thick for integration with SOI
Ge growth strategies

- Thick virtual SiGe substrates (10µm)
  - √ Need for a new integration scheme – difficult to integrate with SOI waveguides.

- Growth on thin SiGe buffers
  - √ The thickness of the thin SiGe buffer is around 1µm
    - ➢ Always too thick for integration with SOI

- Direct Ge growth on Si
Two-step growth process:

- Direct growth of Ge on Si using a low temperature (~350°) CVD process
  - thin (a few 10nm) highly-dislocated Ge layer
- Growth of a thick Ge layer (a few 100nm) at a higher temperature (~600°)
  - high quality Ge absorbing layer

Thermal annealing to reduce the dislocation density
Epitaxial growth techniques

- **Molecular beam epitaxy (MBE)**
  - Solid sources evaporated ⇒ gas sputtering on the wafer
  - Ultra-high vacuum required (P~10^{-10} Torr)
  - Low thermal budgets (T<~550°C)
  - High-control of layer and multi-layer thicknesses (<nm)
  - Low growth rates (<1 nm/min)

- **Chemical Vapor Deposition (CVD):**
  - High-control of layer and multi-layer thicknesses (<nm)
  - Proper for large wafer-scale fabrication
  - A large variety of CVD techniques have been developed, depending on the pressure and heating systems:
    - Ultra-High Vacuum CVD (UHV-CVD)
    - Reduced-pressure CVD (RP-CVD)
    - Low-energy plasma-enhanced CVD (LEPE-CVD)
Absorption of Ge-on-Si

- The red-shift of the absorption edge is due to the tensile strain-induced bandgap narrowing within the Ge layer, resulting from the difference in the thermal expansion coefficients of Ge and Si.

Strong absorption up to 1.6µm
Photodetector characteristics
Quantum efficiency ($\eta$):

- Probability of detecting an incident photon by generating an electron/hole pair that contributes to the photocurrent
- Ratio of the generated carriers to incident flux of photons (i.e.: ratio of the photocurrent to the incident light power)
- The spectral response is governed by the spectral character of the quantum efficiency
Quantum efficiency ($\eta$) depends on:
- Reflectance on the surface
- Absorption

The amount of flux that is absorbed in the material

$$I_{\text{abs}} = 1 - I_{\text{out}} = I_0 \cdot (1 - R) \cdot [1 - \exp(-\alpha L)]$$

$$\eta = (1 - R) \cdot [1 - \exp(-\alpha L)]$$
Photodetector characteristics: Responsivity

- Responsivity ($\mathcal{R}$) is often more useful to characterize the response of photodetectors

\[
\mathcal{R} = \frac{q \eta}{h \nu} = \frac{\eta \lambda (\mu m)}{1.24}
\]

- Responsivity is typically linear with wavelength but real photodetectors exhibit a deviation from the ideal behaviour due to photogenerated carrier trapping
Photodetector characteristics: Response time (I)

- Response time of the photodetectors:
  - Internal response time
  - External response time

- Internal response time
  - Transit time of carriers: depends on the velocity of carriers in SC (varies with the doping level and the material)
  - Diffusion time of carriers: diffusion of carrier to be collected. Mainly depends on the structure

[Graph showing optical pulse and response time]
Photodetector characteristics: Response time (II)

- **External response time**

  ![Typical schematic electrical circuit of the photodiode]

  - $C_d$: Diode capacitance
  - $C_p$: Parasitic capacitance
  - $R_d$: Diode resistance
  - $R_1$: contact and substrate resistances
  - $R_2$: charge resistance

  $R_1$ and $R_d \ll R_2$

  Response time = $R_2 (C_P + C_d)$
Photodetector specifications (I)

- “Compatibility” with silicon technology
  - Silicon-based materials will be better
  - Large wafer scale technology
  - Permit electronic integration (Transimpedance amplifier – TIA)
  - Low cost integration schemes

- Broadband detection (1.3 -1.6 µm)
  - High absorption coefficient

- Low dark current
  - Electrical configuration of photodetectors,
  - Quality of the absorbing layer.
Photodetector specifications (II)

- **High bandwidth** (frequency operation > 10 GHz)
  - Low carrier transit time,
  - Low RC constant – depend on the considered electrical structure (pin diode, MSM detector).

- **High responsivity**
  - Optimize the light interaction with absorbing layer.

- **Compactness**
  - Strong absorption coefficient
Two approaches

Surface illuminated photodetectors

😊 High bandwidth
“Simple” process

.writeFile
Photodetector integration

Two approaches

Surface illuminated photodetectors
- High bandwidth
- “Simple” process
- “Low” responsivity

Photodetectors integrated in waveguide
- High bandwidth
- High responsivity
- Optical coupling
Integrated photodetectors: optical coupling

SOI waveguides

Single mode (TE)

Vertical coupling

Butt coupling
Vertical coupling

95 % absorption length < 10 µm with 310nm germanium thickness

Butt coupling

95% absorption length < 4µm

Negligible lateral divergence
Europe: PSUD-IEF, CEA-Léti, Stuttgart Univ., Roma Univ. …
Asia: Tokyo Univ., A*Star, Petra, AIST, Chinese Academy of Sciences, …
North America: Intel, MIT, IBM, Cornell, Luxtera, Ligthwire, Kortura, Oracle …
Photodetector: electrical structures

Surface contact MSM

Lateral contact MSM

Lateral PIN

Vertical PIN

PIN

http://silicon-photonics.ief.u-psud.fr/

Laurent Vivien
Diode band structure

Recombine with majority $h^+$ before reaching the junction.

- **homogeneous p region**
- **e^- diffusion region**
- **Depletion layer**
- **p**
- **Active region**
- **n**
- **L_e**
- **W**
- **L_h**
- **h^+ diffusion region**
- **homogeneous n region**

- $h^+$ diffusion region
- Drift
- $e^-$ diffusion region
- $h^+$ diffusion
- Drift
- $e^-$ diffusion region
- $h^+$ diffusion

http://silicon-photonics.ief.u-psud.fr/
Diode band structure

Forward or reverse bias?
Junction disposition

- Lateral PIN
  - Contact on Ge: only one etching step
  - Definition of intrinsic region by ion implantation

3dB Bandwidth

- 70 GHz
- 50 GHz
- 35 GHz

Responsivity (A/W)

- $R > 0.9$ A/W

Propagation length (μm)

- $W_i=1μm$
- $W_i=0.7μm$
- $W_i=0.5μm$
Device Fabrication: Ge Growth

- Two RPCVD steps to overcome lattice mismatch issue

<table>
<thead>
<tr>
<th>Temperature and Duration</th>
<th>Stacking</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>400°C, 60s + 750°C, 180s</td>
<td>Overgrowth of Ge</td>
<td>To avoid faceting inside the cavity, To reduce Threading Dislocation Density (TDD)</td>
</tr>
</tbody>
</table>

Device Fabrication: Ge Growth

- Post epitaxial thermal cycling to further reduce TDD in the Ge layer
- CMP step to remove protruded Ge
- SiO₂ encapsulation
- Ion implantation of Ge
  - N-type: Phosphorus
  - P-type: Boron
- Rapid Thermal Anneal

Device Fabrication: Contact and Metal

- Oxide encapsulation
- Planarization
- Contact definition
  - 0.4x0.4μm vias for metal filling (TiN/W)
  - Ti/TiN/AlCu pad defined by etching

Lateral

Input waveguide

RF electrodes

10 µm
Results: Dark current and responsivity

**Dark current median, mean and best values (373 dies per wafer)**

<table>
<thead>
<tr>
<th>Photodiodes</th>
<th>Wi=0.5µm</th>
<th>Wi=0.7µm</th>
<th>Wi=1µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer</td>
<td>1 2 3</td>
<td>1 2 3</td>
<td>1 2 3</td>
</tr>
<tr>
<td>@-1V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Median (nA)</td>
<td>85 74 112</td>
<td>66 62 80</td>
<td>68 61 71</td>
</tr>
<tr>
<td>Mean (nA)</td>
<td>433 105 1707</td>
<td>350 83 576</td>
<td>347 110 963</td>
</tr>
<tr>
<td>Best (nA)</td>
<td>32 25 27</td>
<td>18 9.5 9</td>
<td>19 17 6</td>
</tr>
<tr>
<td>Yield</td>
<td>99.2% 99.7% 97.8%</td>
<td>100% 100% 99.7%</td>
<td>100% 100% 99.7%</td>
</tr>
</tbody>
</table>

New run: dark current ~1nA @ -1V for $W_i = 0.5µm$

**Responsivity @ 1550nm under Zero bias**

- Wi=0.5µm: 0.5A/W
- Wi=0.7µm: 0.6A/W
- Wi=1µm: 0.8A/W

Efficient carrier collection at zero bias due to strong built-in electric field

Measured responsivity lower than theoretical values
Femtosecond pulse experiments

**Characterization methods:** Bandwidth (I)

- **Bandwidth (I)**
  - Femtosecond pulse experiments

![Diagram of experimental setup](image)

**Graph:**
- **Photovoltage (UA)** vs **Time (ps)**
  - Device Under Test
  - Acquisition System
  - Convolution

**Response time (ps):**
Characterization methods: Bandwidth (I)

- Femtosecond pulse experiments

- Opto-RF experiments with a Vector Network Analyzer
Data transmission measurements

Pseudo Random Binary Sequence

PRBS generator

optical modulator

optical source

\( \lambda = 1.55 \, \mu m \)

Sampling oscilloscope

Bias T

RF cable

\( V_{\text{pol}} \)

Eye diagram

http://silicon-photonics.ief.u-psud.fr/
Results: Bandwidth measurement

- Opto-electric frequency response measurement using 50GHz Lightwave Component Analyzer (\(1550\text{nm}\))

-3dB Optical Bandwidth

Over 50GHz @ 0V

Bandwidth higher than theoretical values
Discussions

Lower responsivity

<table>
<thead>
<tr>
<th>Wi</th>
<th>Exp (A/W)</th>
<th>Theo (A/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5µm</td>
<td>0.5</td>
<td>0.91</td>
</tr>
<tr>
<td>0.7µm</td>
<td>0.6</td>
<td>0.96</td>
</tr>
<tr>
<td>1µm</td>
<td>0.8</td>
<td>0.99</td>
</tr>
</tbody>
</table>

Measured BW: >130GHz
Theoretical BW: 70GHz

Higher bandwidth

Why are the responsivity lower and the BW higher than theoretical values?

=> Loss of photo-generated carriers
=> Faster carrier collection

Reduction of the absorption region width
Discussion: Ion implantation

- Ion implantation
  - √ Monte Carlo simulation of ion implantation process

Narrowing of the intrinsic region

⇒ Absorption inside the doped region
  √ Max responsivity ~0.6A/W

⇒ Increase of the electric field strength
  √ Max BW ~ 120 GHz
Data transmission

10 Gbit/s

20 Gbit/s

40 Gbit/s @ -1V

40 Gbit/s

Under zero-bias

Coll.: TU WIEN

Results beyond specifications

- High responsivity: > 0.5A/W
- High bandwidth: 40Gbit/s
- Low dark current: <1nA @ -1V
- Bias voltage: 0V

http://silicon-photonics.ief.u-psud.fr/
How can we increase the receiver bandwidth?

….Towards Tbit/s…. 
To improve bandwidth of receiver

Bandwidth = Parallelism × Frequency

- Need more wavelengths
- 40 Gbit/s detector

2 x 16 channels 200 GHz centered at about 1550 nm

… 640 Gbit/s and more…
Germanium photodetectors are more and more considered as a mature silicon photonics devices.

The PD characteristics are close to the one of III-V PD.
  √ Incredible at the beginning.

The trends
  √ Development of complex circuits for Tbit/s operation
  √ Integration with CMOS circuits (TIA)
  √ Avalanche PD …
    ➢ new route to reduce the power consumption of the emitter
    ➢ Photon counting – Quantum optics