The Abdus Salam
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2572-9

Winter College on Optics: Fundamentals of Photonics - Theory, Devices and Applications

10 - 21 February 2014

Photonic packaging and integration technologies I

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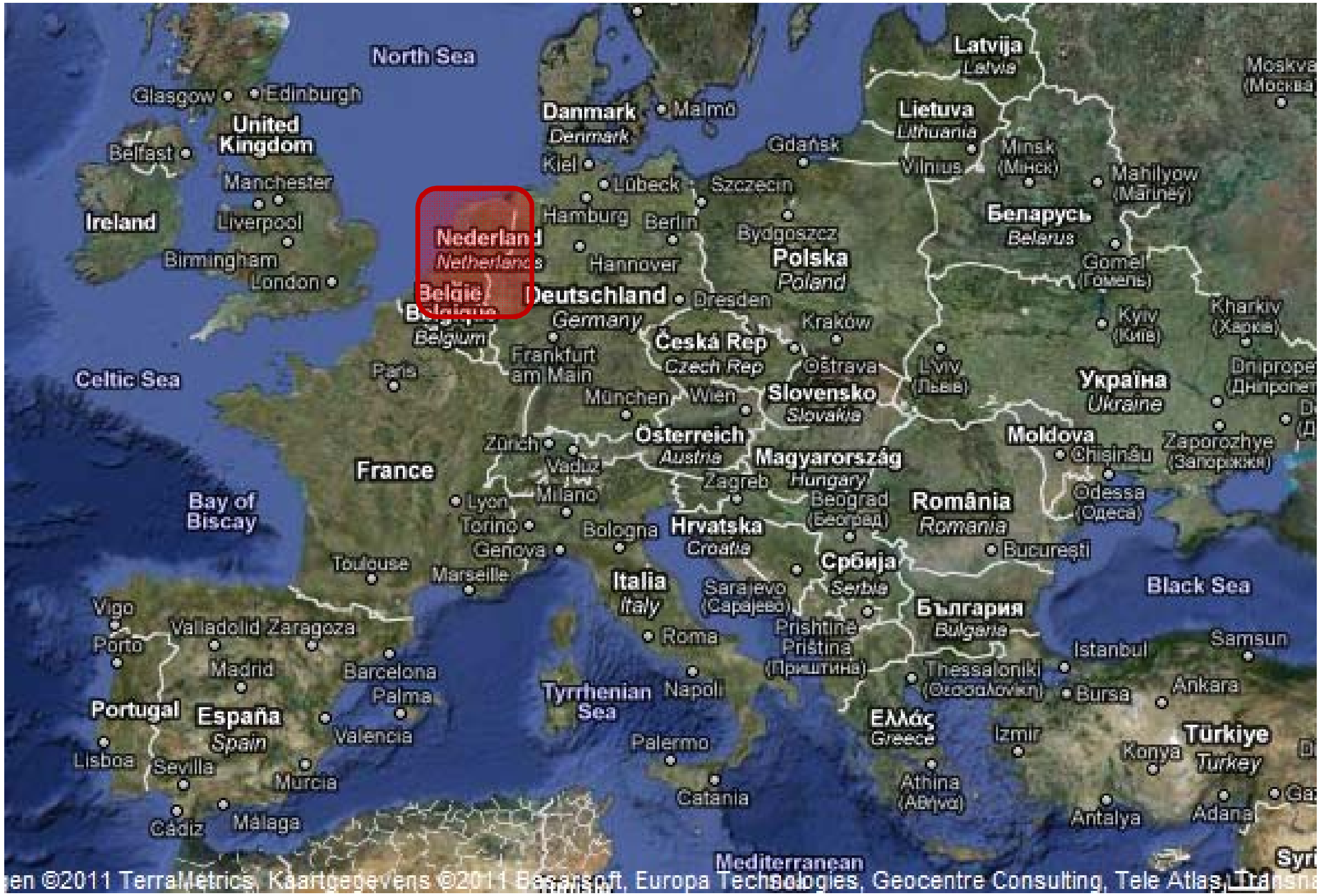
Photonic packaging and integration technologies I

Winter School on Optics

ICTP, Trieste, February 2014

Sonia M. García Blanco, University of Twente

UNIVERSITY OF TWENTE: NETHERLANDS



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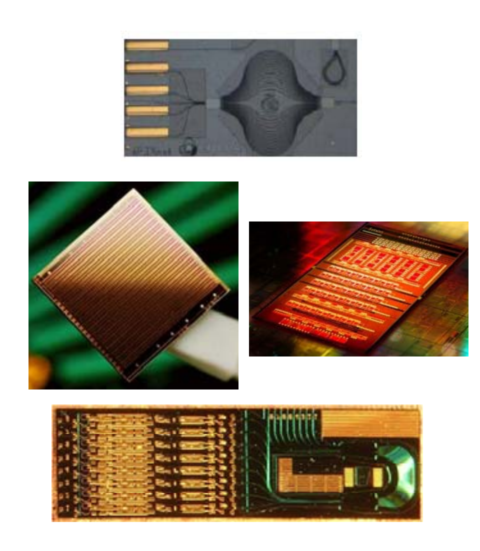
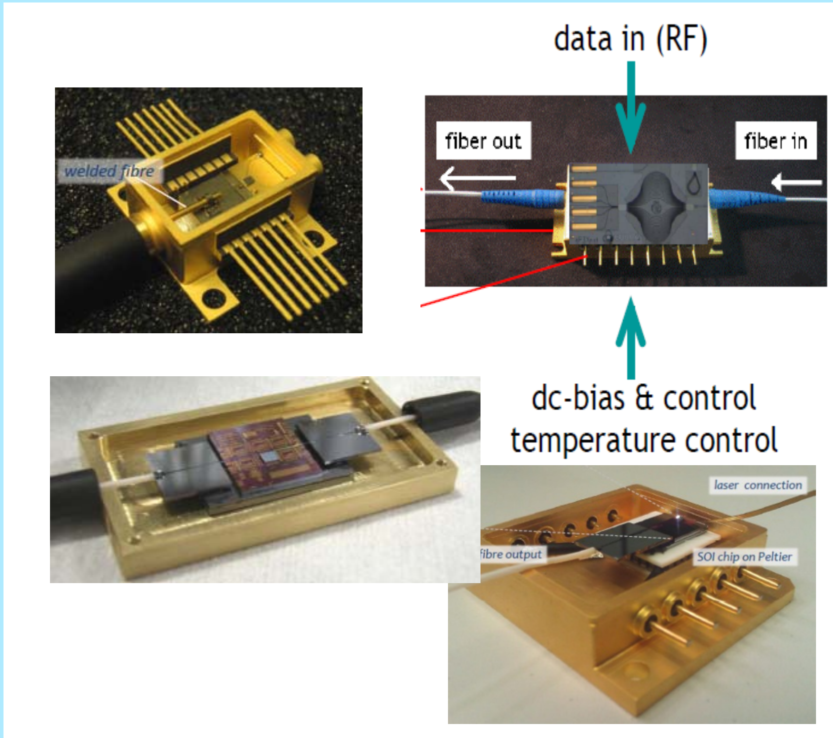
PHOTONIC PACKAGING AND INTEGRATION TECHNOLOGIES

Bare photonic dies



Packaged dies



[Lars Zimmerman, Helios, Silicon Photonics course]
[P. O'Brien, Tyndall National Institute, Cork, Ireland]

PACKAGING GOALS

- Protect devices from environment
- Provide the correct atmosphere for proper functioning (vacuum, nitrogen)
- Interaction of device with environment:
  - Electrical signals
  - Optical signals: transparent window, optical waveguides, fibers
  - Fluidics
  - Pressure, gases, etc
- Increase reliability

- Low cost
- Small size

LECTURE LEARNING GOALS

1. Get an overview of different available packaging and integration technologies

2. Get a “feeling” for the challenges of packaging

3. Acquire a “design-for-packaging” attitude

OUTLINE

1. Packaging of LEDs, detectors and image sensors
2. Packaging of photonic devices
3. Hybrid and heterogeneous integration technologies

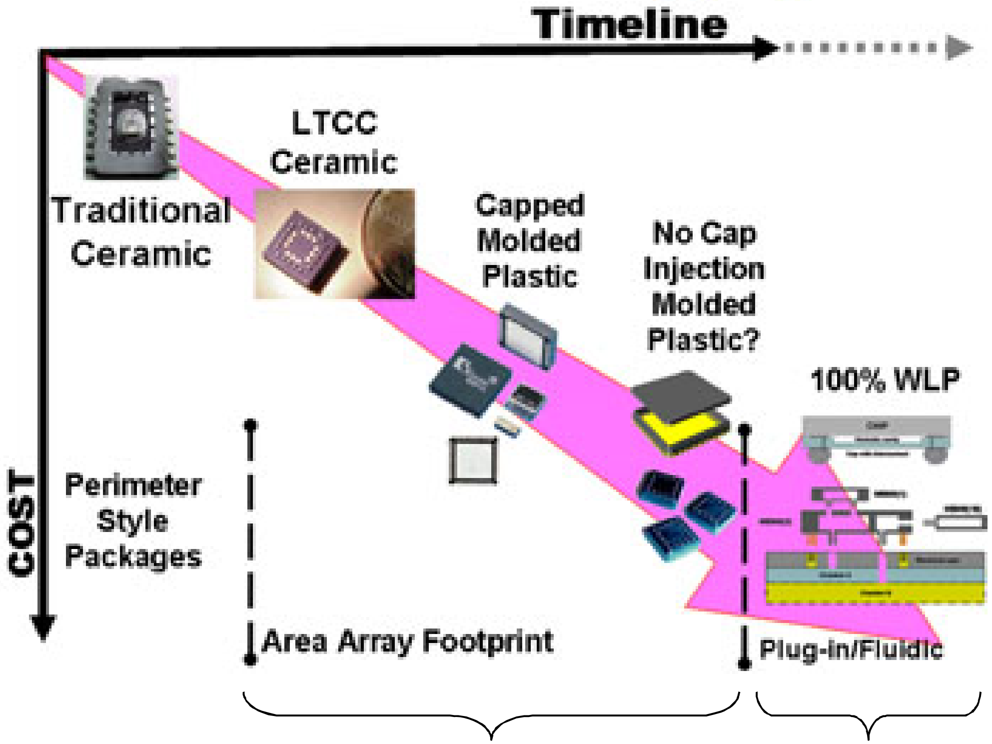
PACKAGING OF LEDs, DETECTORS AND IMAGE SENSORS

- Die-level versus wafer level packaging

- Overview of bonding technologies

- Example: Wafer level packaging of microbolometer detectors

TRENDS ON LED, DETECTOR AND IMAGE SENSOR PACKAGING

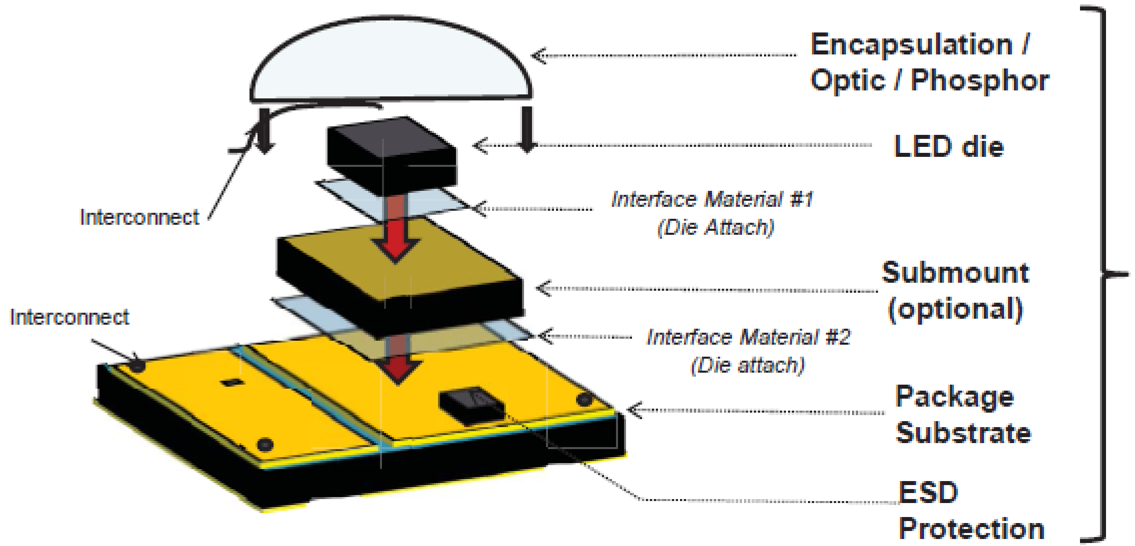


[Image: K. Gilleo]

<u>Level 1</u>: die-level packaging

<u>Level 0</u>: wafer-level packaging

CHIP LEVEL PACKAGING OF LEDs

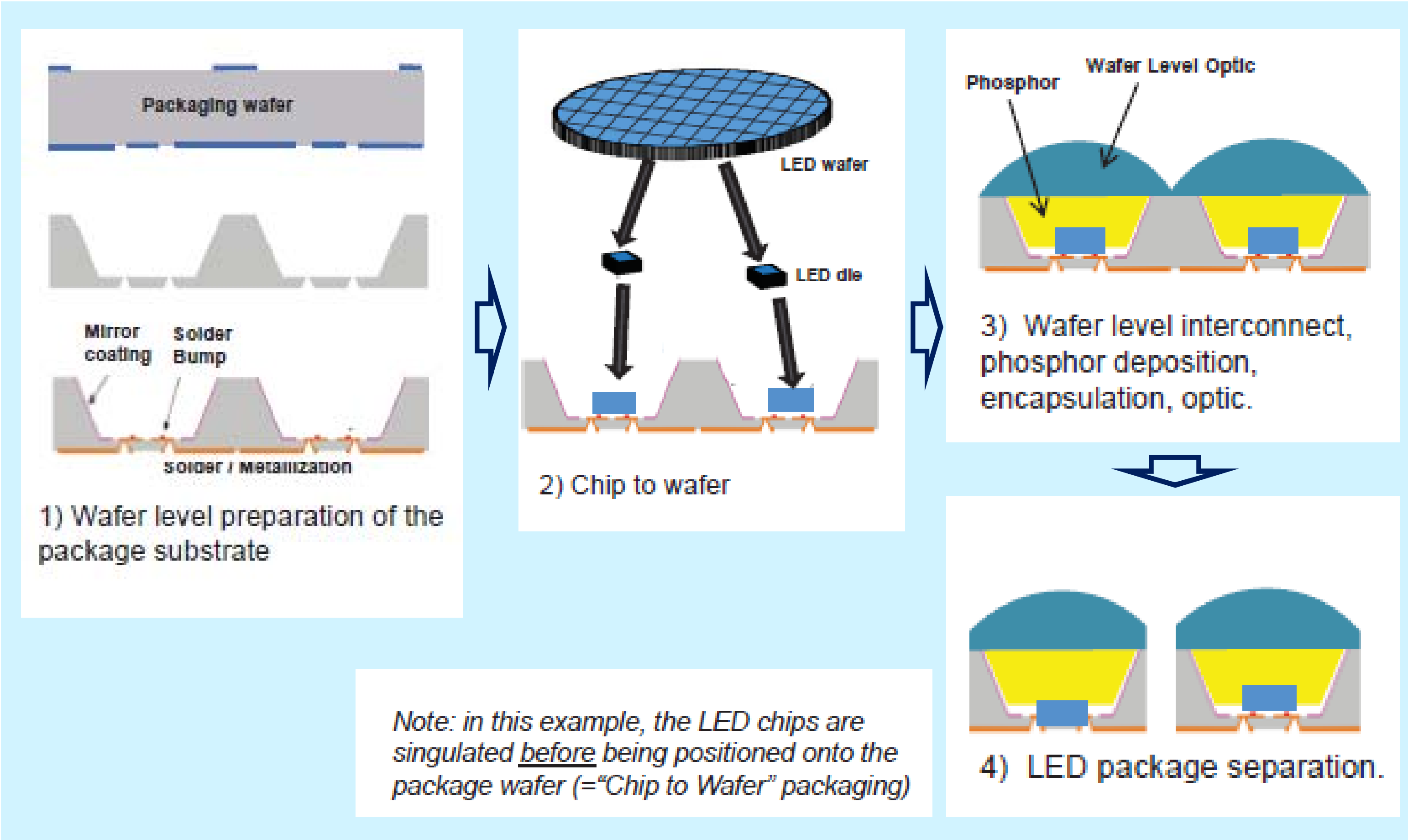


Led Package (picture: Philips Lumileds)

- Many LED dies/wafer
- Several assembly steps per LED die

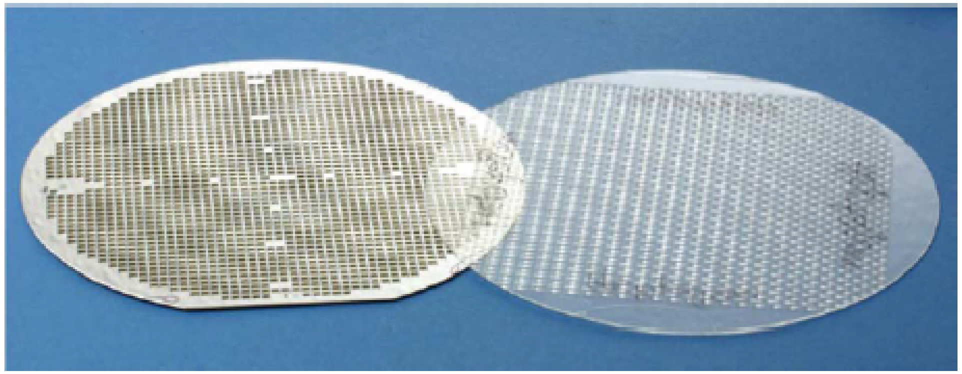
Time + cost

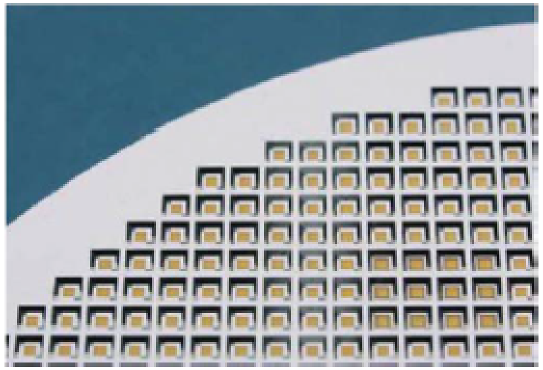
WAFER LEVEL PACKAGING OF LEDs

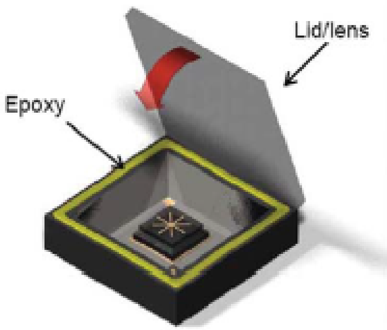


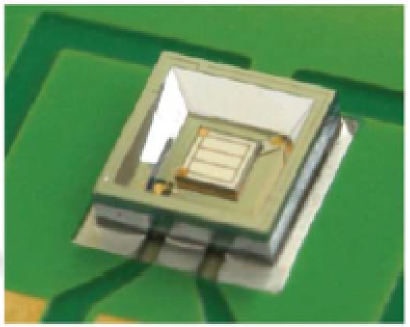
WAFER LEVEL PACKAGING OF LEDs

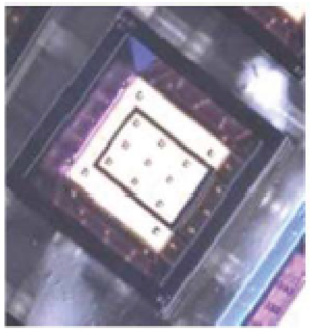
Hymite (technology acquired by Touch Microsystem Technology in 2010)

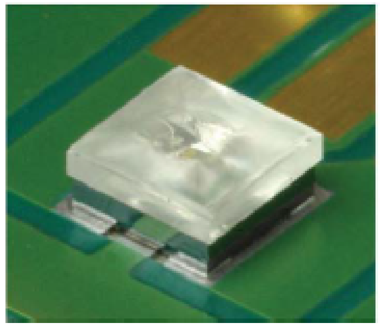








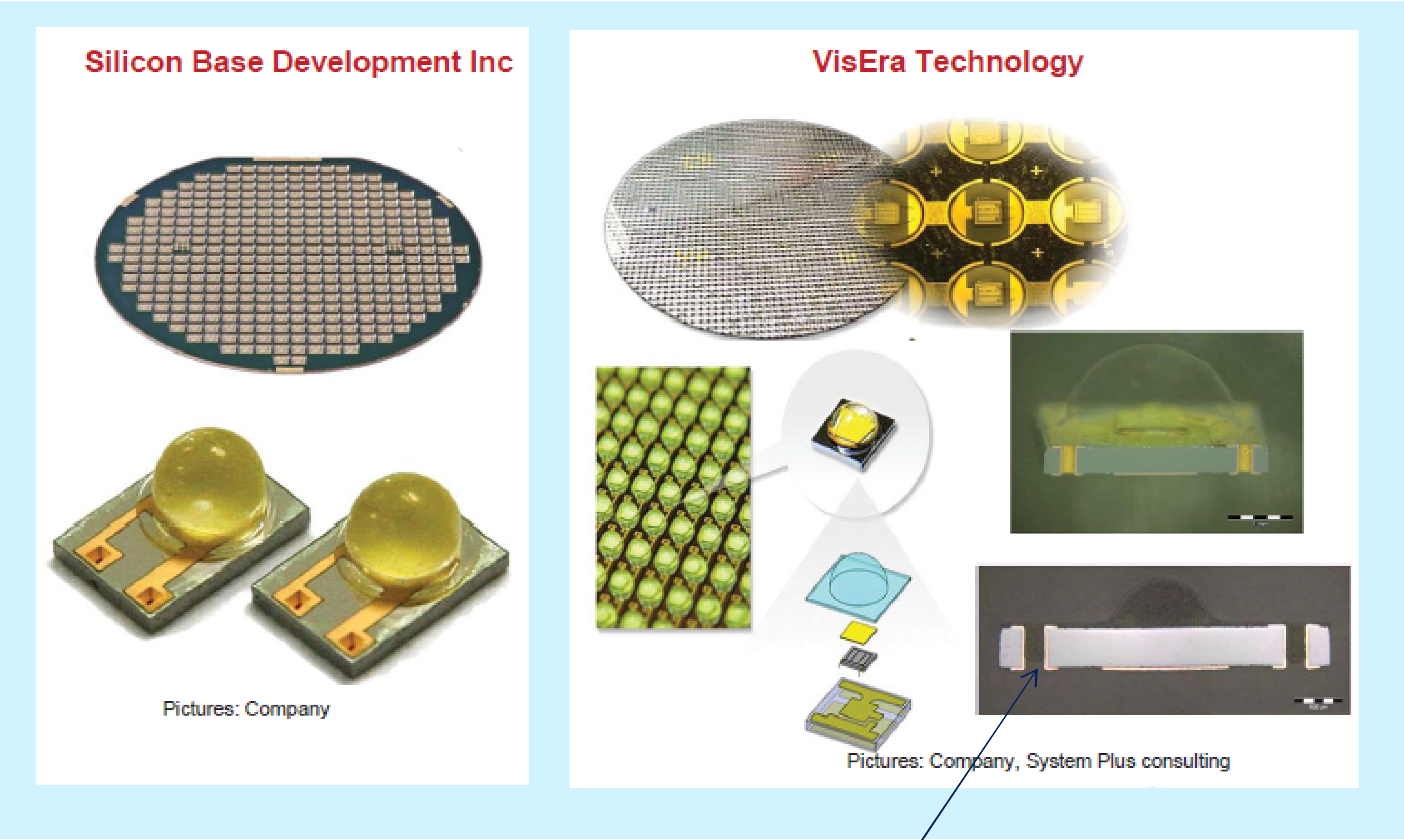




Courtesy of Hymite

[Yole Development, Semicon West 2011]

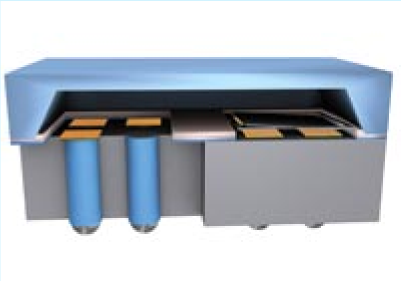
WAFER LEVEL PACKAGING OF LEDs

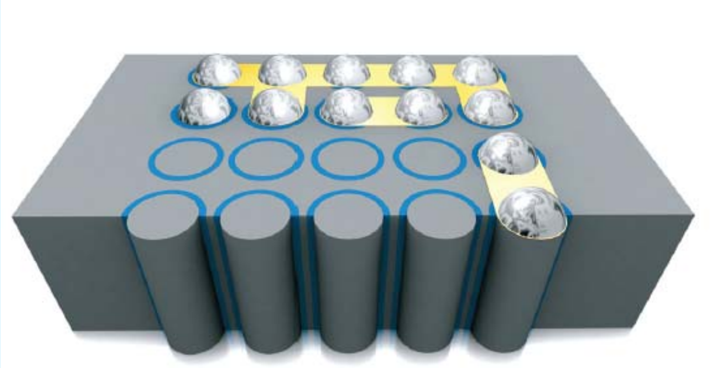


Thru silicon vias (TSV)

TECHNOLOGIES FOR WAFER LEVEL PACKAGING

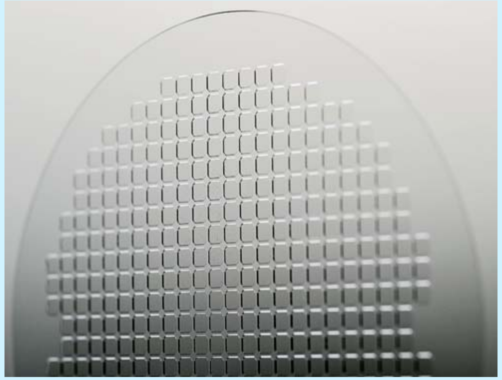
- Thru silicon vias (TSV)





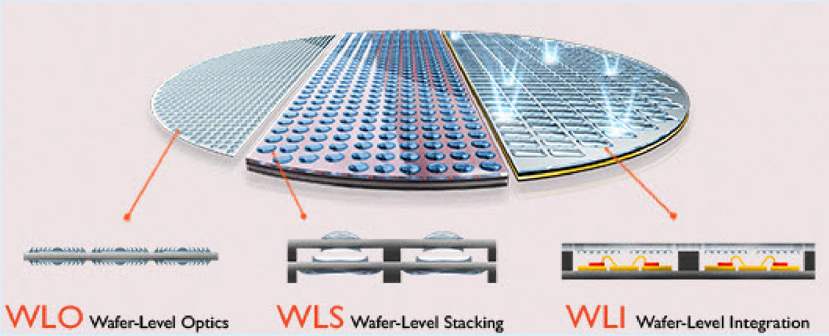
[Silex]

- Packaging wafers



[PlanOptik]

- Wafer level optics



[HeptaGON]

PACKAGING OF LEDs, DETECTORS AND IMAGE SENSORS

- Die-level versus wafer level packaging

- Overview of bonding technologies

- Example: Wafer level packaging of microbolometer detectors

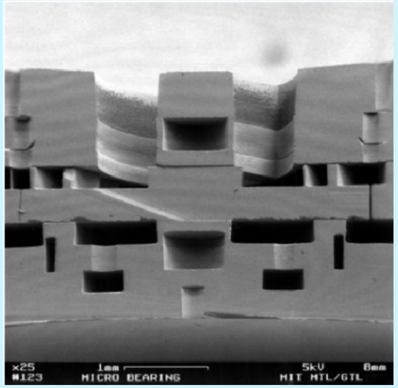
BONDING TECHNIQUES

Technique	Advantages	Disadvantages
Bonding without interlayer	Hermetic	Flat surface required
Direct	Strong bond	High-T
Plasma activated	Low T	Complex equipment
Anodic	Strong bond	High T, high voltage, ionic glass
Metallic interlayer	Hermetic, non flat surface OK	Specific metals required
Eutectic	Strong bond	Flat surface
Thermocompression	More tolerant to flatness	High pressure
Solder	Self-alignment	Solder flow possible
Insulating layer	Non flat surface ok	Vary
Glass frit	hermetic	High T, large bond area
Adhesive	Versatile, low T	Non hermetic

DIRECT BONDING

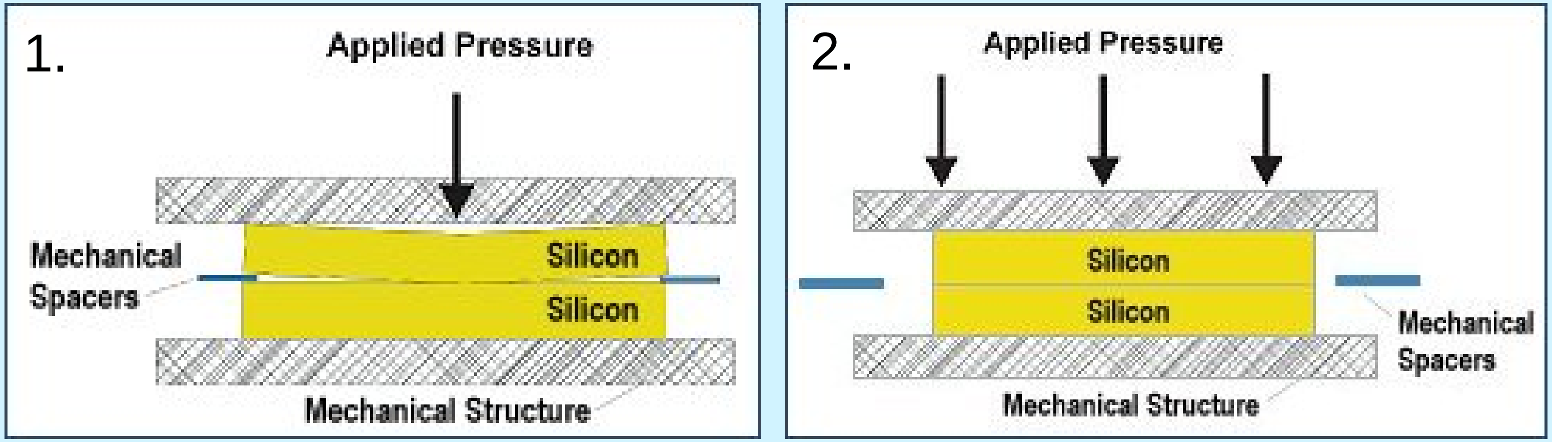
REQUIREMENTS:

- Suitable surface chemistry (hybrophilicity vs hydrophobicity)
- Matching CTEs (otherwise stress-induced cracks)
- Smooth surfaces (<1.5 nm rms)
- Flat wafers (on cm-scale)
- No particles (voids larger than particles!)
- T>500C typically (depending on materials)



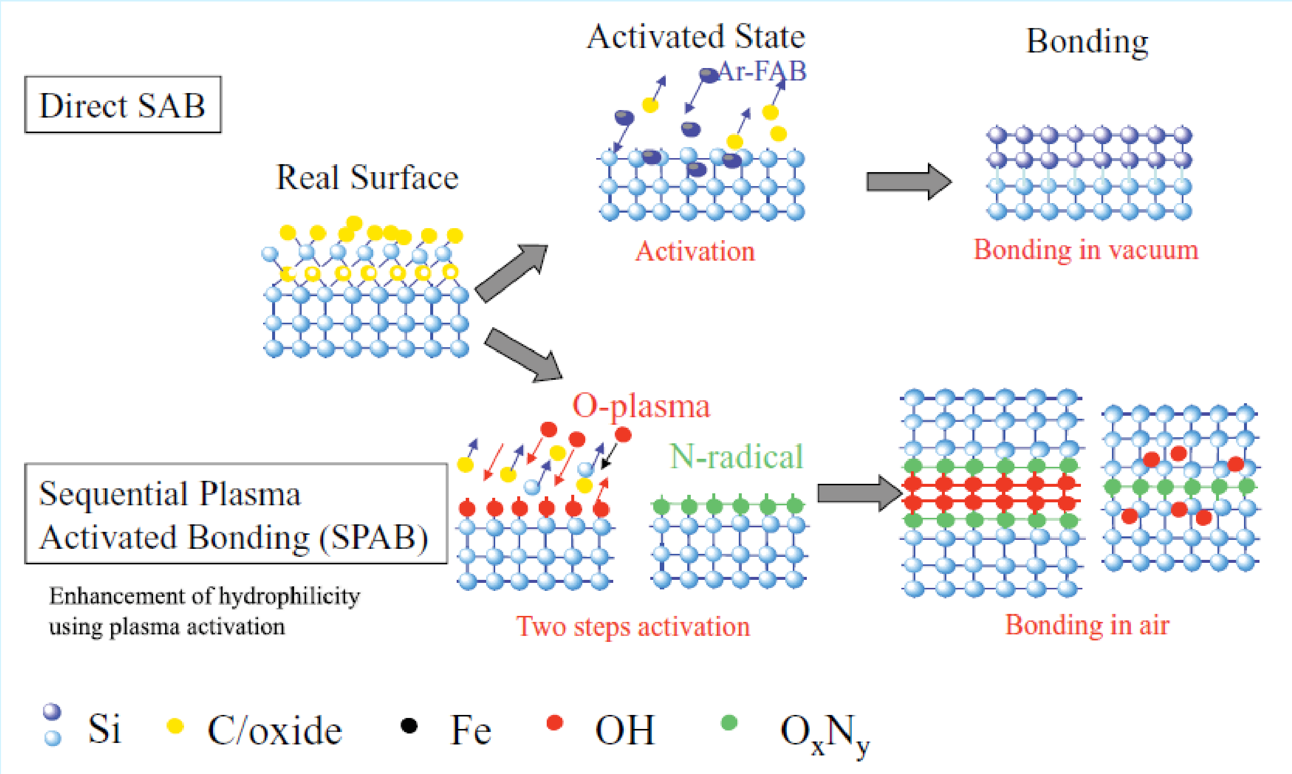
[D. Epstein, MIT]

DIRECT BONDING



[Sami Franssila, Aalto, Finland]

PLASMA ACTIVATED DIRECT BONDING

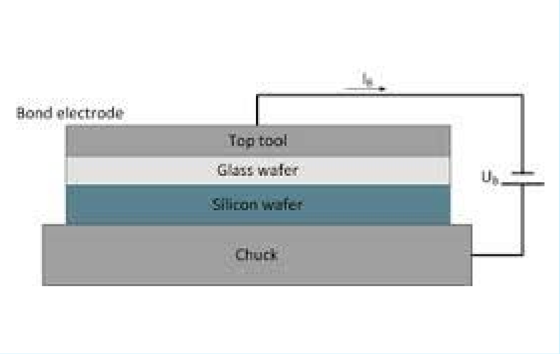


[Howlader et. Al., J. Micro/Nanolith. MEMS MOEMS. 9(4), 041107, 2010]

Anneal Temperature <200 C

ANODIC BONDING

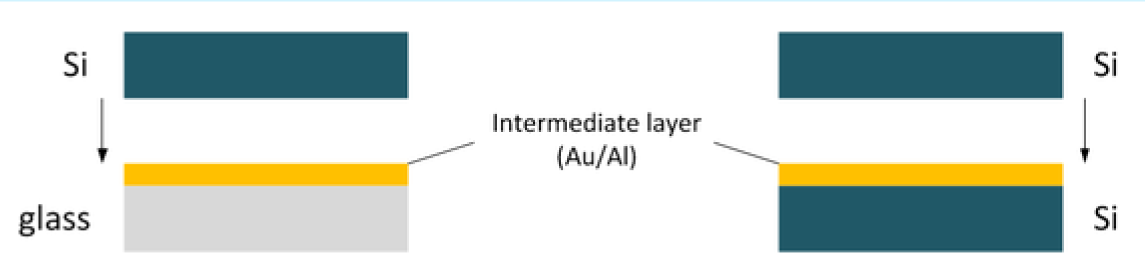
Anodic bonding



- Ion containing glasses: eg., Borofloat 33 or Pyrex 7740
- T >350 C
- V >400 V
- P → not so relevant

[Wikipedia]

EUTECTIC BONDING

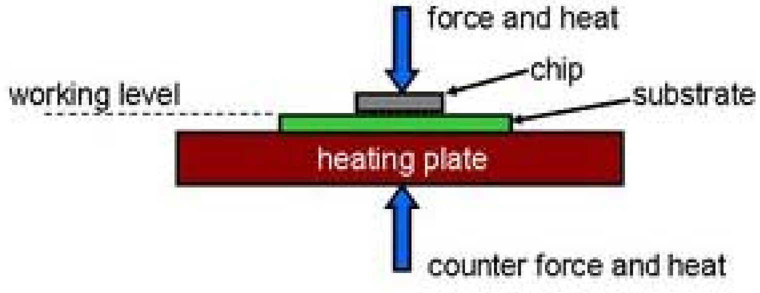


- Tolerant to surface quality and wafer bow
- Low temperature process
- Sensitive to surface oxides

[Wikipedia]

Materials	Composition	Temperature
Au-Sn	80/20 wt%	280 C
Au-Si	97.15/2.85 wt%	370 C
Au-Ge	28/72 wt%	361 C
Al-Si	87.5/12.5 wt%	580 C
Cu-Sn	5/95 wt%	231 C
Au-In	0.6/99.4 wt%	156 C

METAL THERMOCOMPRESSION BONDING



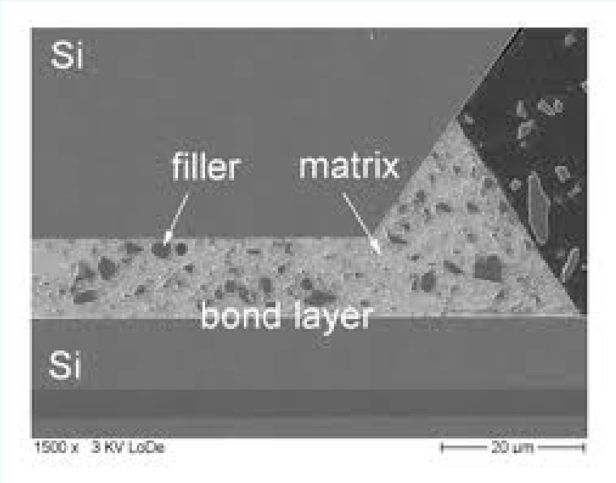
PROCESS:
- Metal between chip and substrate
- T
- Pressure

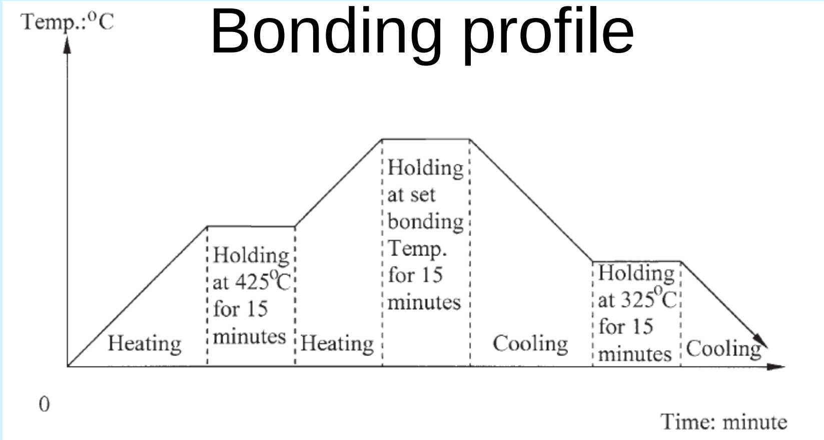
BONDING MECHANISM:
- Breaking of surface oxides
- Interface formation
- Grain growth

Metal	Temperature	Applied Force Range†	Time	Atmo-sphere
Al	400-450°C	>70KN	20-45 min	Vac or H_2/N_2
Au	300-450°C	>40KN	20-45 min	Vac or H_2/N_2
Cu	380-450°C	>30KN	20-60 min	Vac or H_2/N_2

[Suss Microtec]

GLASS FRIT BONDING





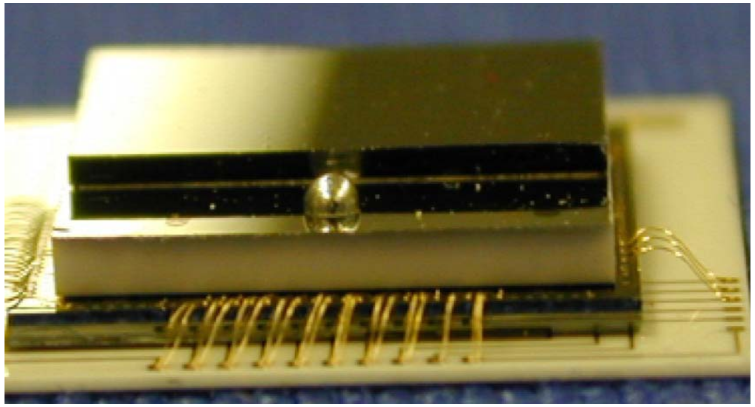
<u>Characteristics</u>:

- T >400 C
- Tolerant to particles
- Tolerant to surface quality
- Possible voids
- Possible outgassing

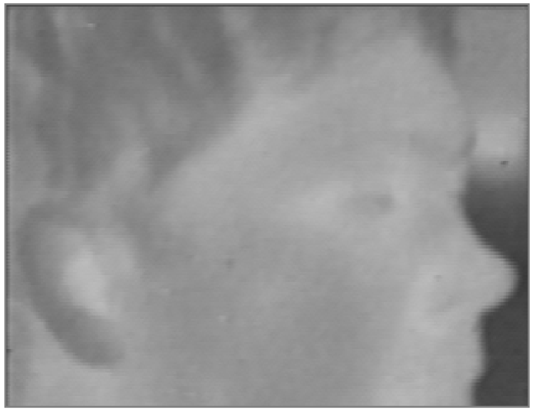
[Sun et. al, J. Eletron. Mat, 2004]

EXAMPLE OF WAFER-LEVEL PACKAGING

INO's μ-package:

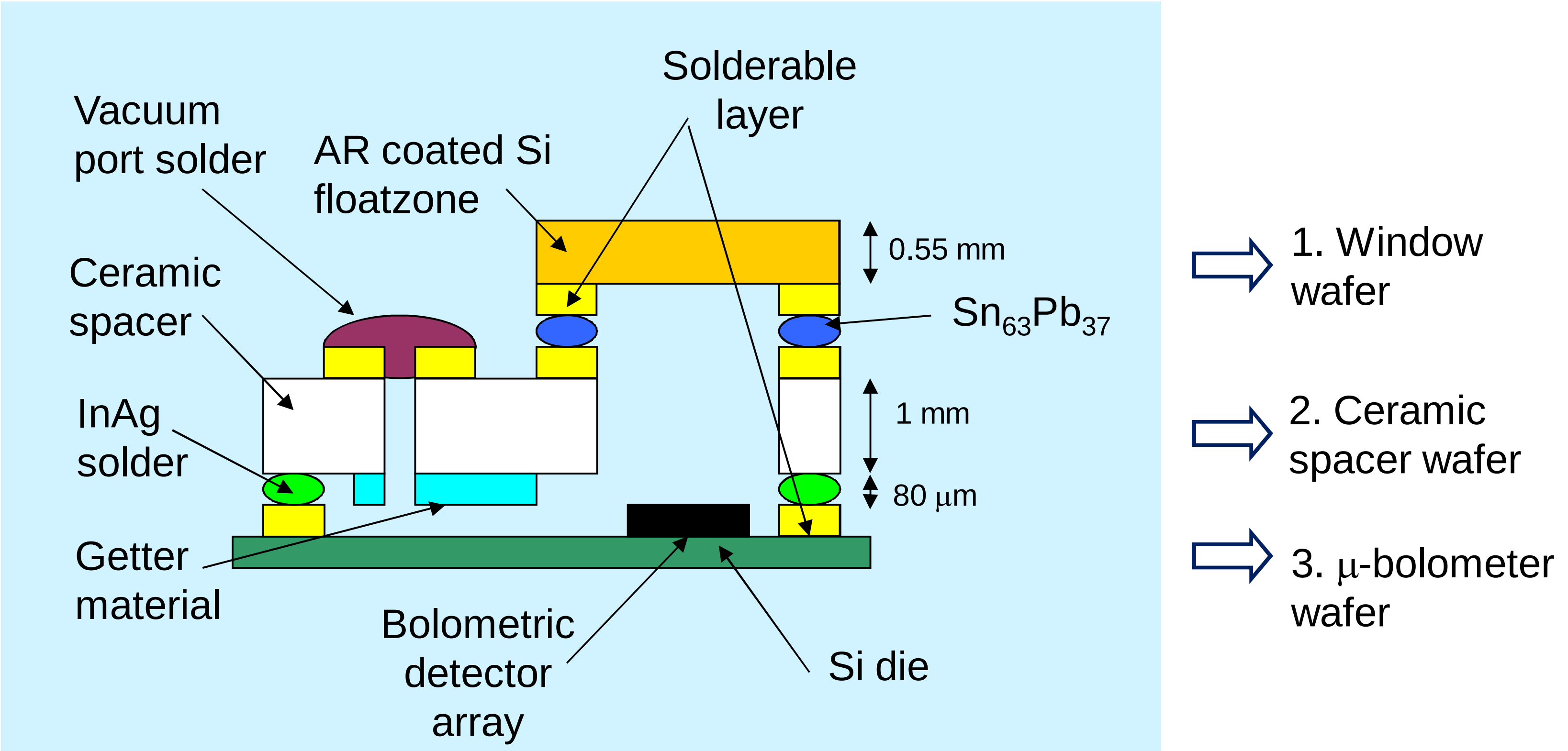


160x120 pixel FPA 130 mK:



	μ-pack
Footprint (mmxmm)	10.5 x 9.7
Volume	60 μL
Weight (g)	0.53

CONCEPT OF LOW-T MICROPACKAGE

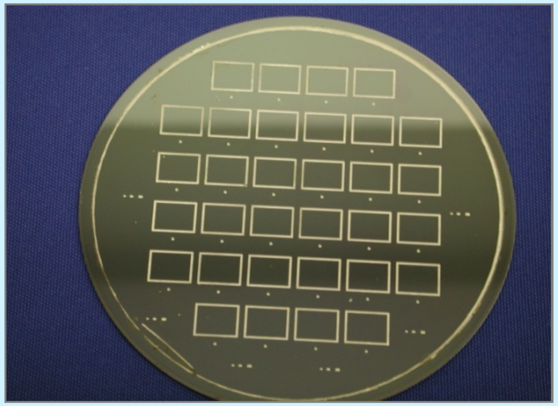


Each level microfabricated at the wafer level

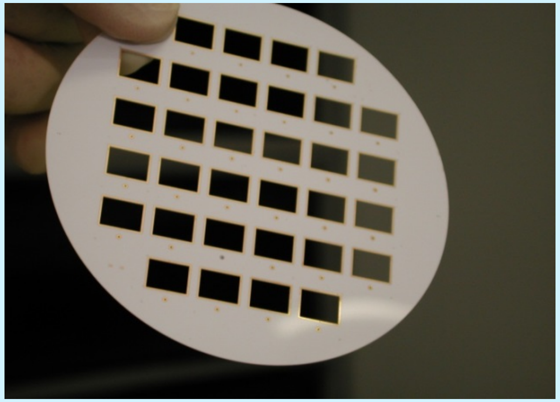
[S. García-Blanco et. al., « Hybrid wafer-level vacuum hermetic micropackaging technology for MOEMS-MEMS », Proc. SPIE 720602, 2009]

CONCEPT OF LOW-T MICROPACKAGE

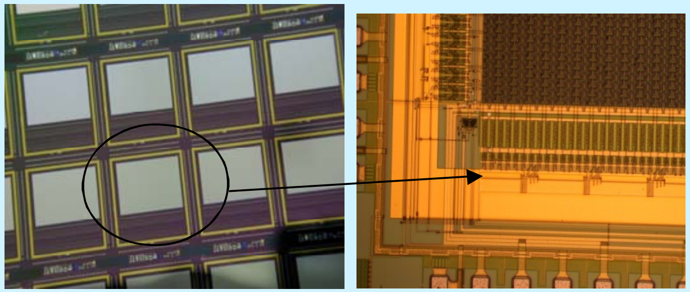
1. IR window wafer



2. Ceramic spacer wafer



3. Microbolometer wafer

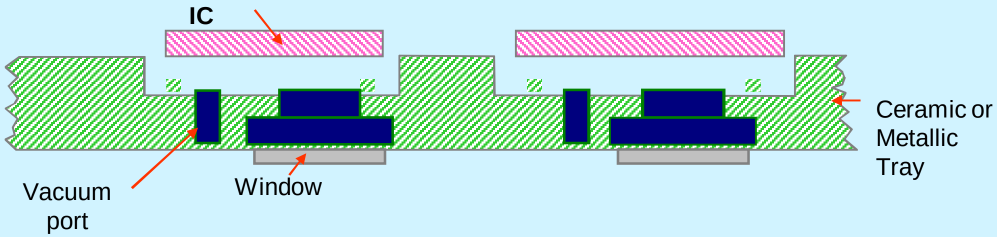


Batch
microfabrication
technologies

Low cost devices

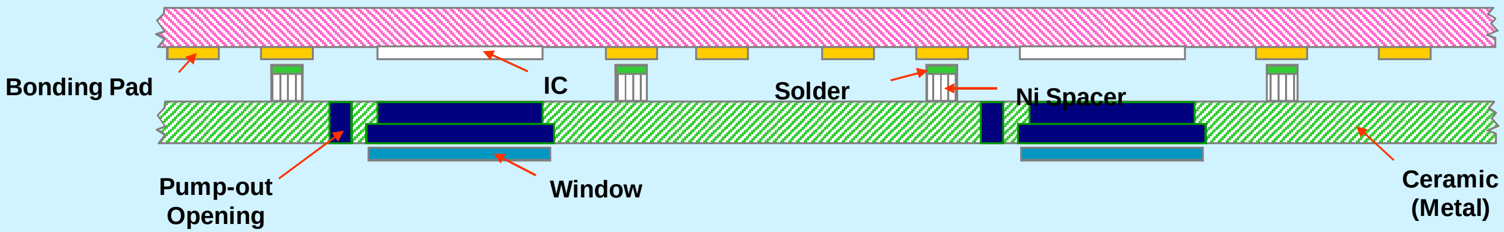
CONCEPT OF LOW-T MICROPACKAGE

1. Die and window to carrier wafer



Cost reduction by:
- Assembly of only known-good dies
- Minimize costly IR-coated window material
- Assembly done with low cost instrumentation

2. Wafer-to-wafer bonding



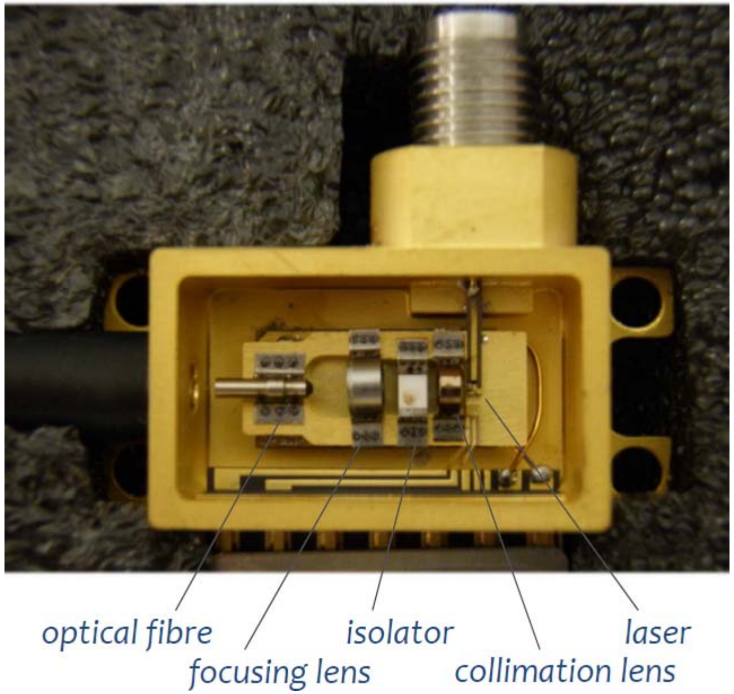
OUTLINE

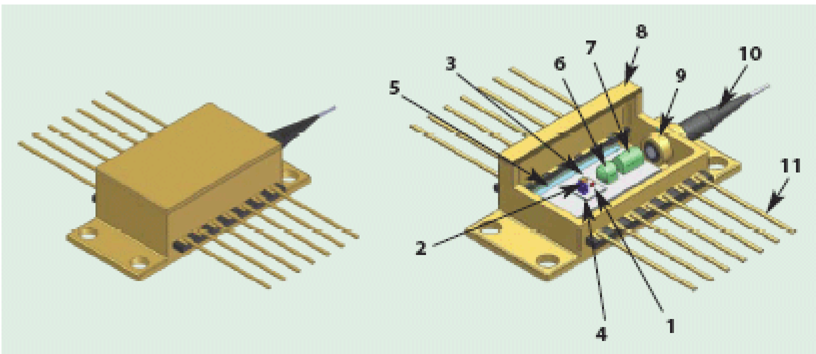
1. Packaging of LEDs, detectors and image sensors
2. Packaging of photonic devices
3. Hybrid and heterogeneous integration technologies

PACKAGING OF PHOTONIC DEVICES

1. Two examples of packaging of photonic modules
   - Laser diode in butterfly package
   - Transmitter optical subassembly (TOSA)
2. "Fiber-to-the-chip" assembly strategies
   - Ferrule welding
   - Fiber array butt coupling (active vs passive alignment)
   - Grating couplers

PACKAGING OF PHOTONIC MODULES



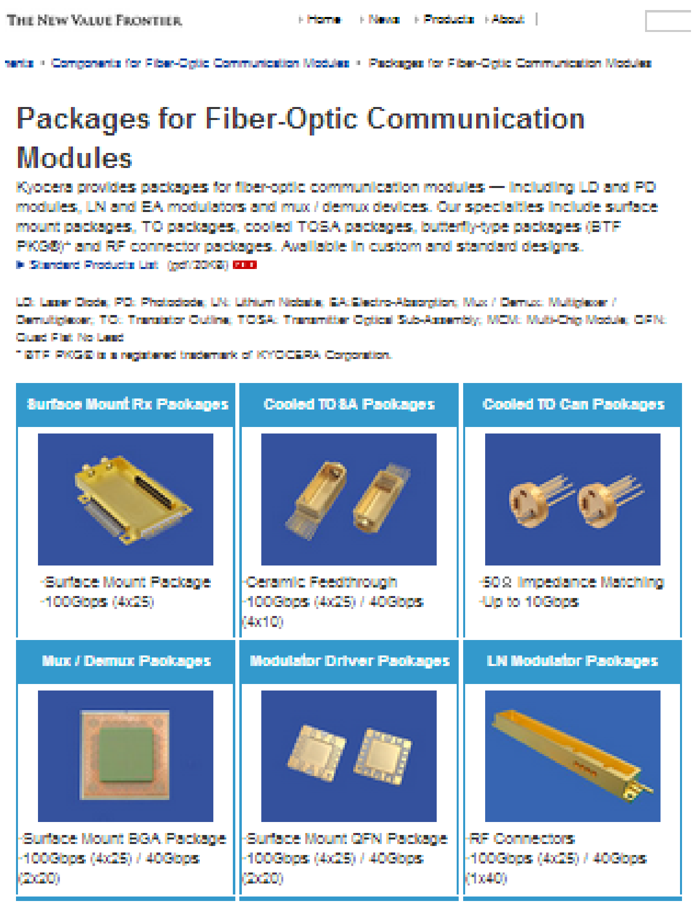


Laser diode module package:

- Butterfly package
- Laser chip
- Thermistor
- Thermoelectric cooler
- Focusing lens
- Isolator
- Optical fiber
- Electrical leads

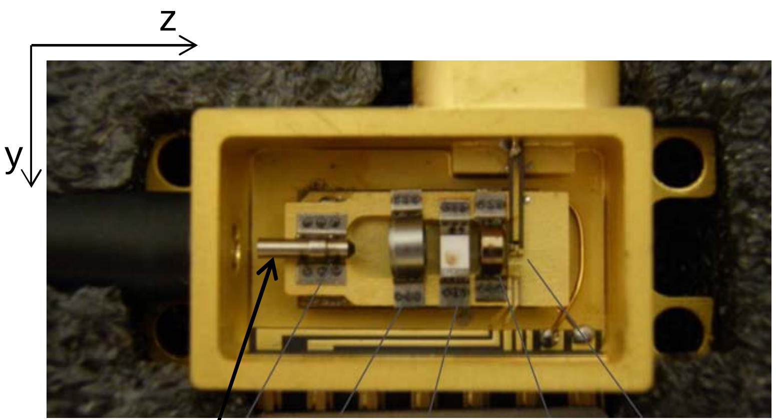
[Peter O'Brian, Tyndall]

EXAMPLES OF PACKAGES

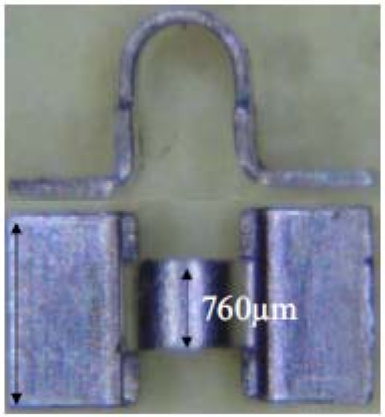


[Kyocera]

EXAMPLE 1: LASER DIODE MODULE

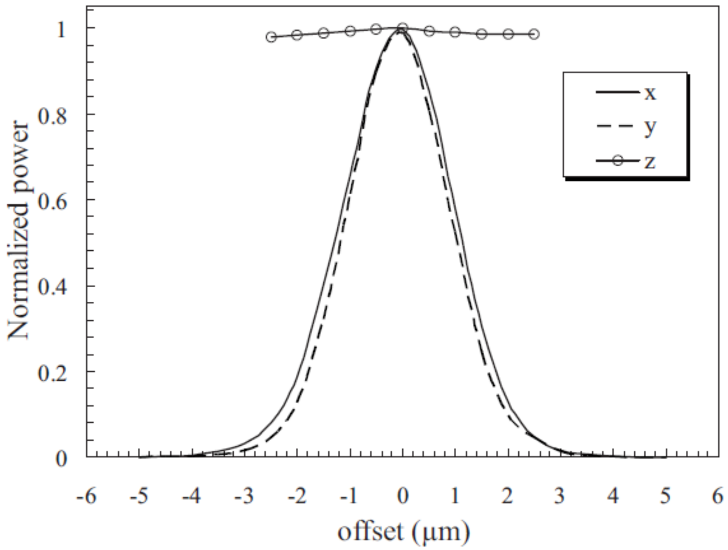


Welded fiber ferrule



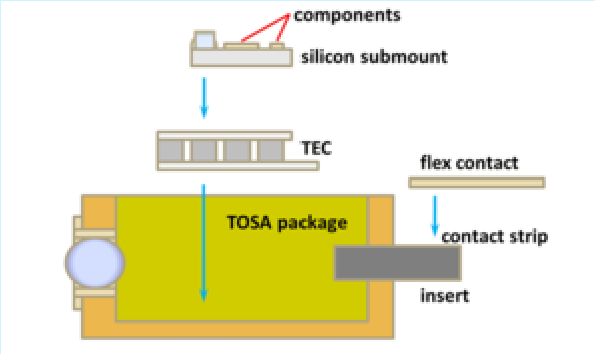
Ni weld clip
(Ni 99%+ Fe 0.4%+Cu 0.25% +etc)

Sensitivity to alignment errors:



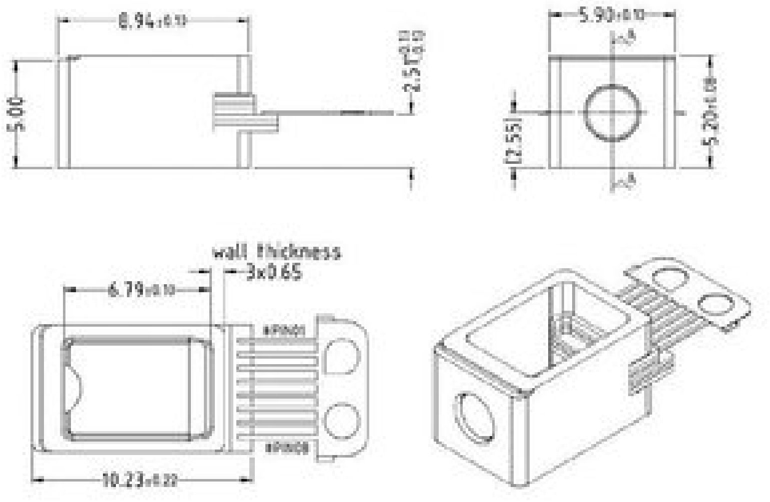
EXAMPLE 2: ASSEMBLY OF A TRANSMITTER OPTICAL SUBASSEMBLY (TOSA) PACKAGE

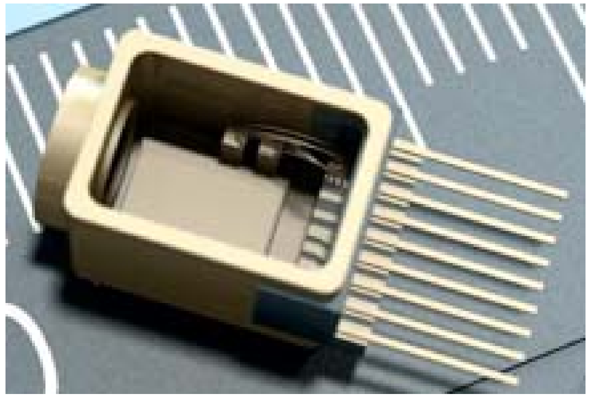
1. Components and lens attachment (adhesive) on silicon submount



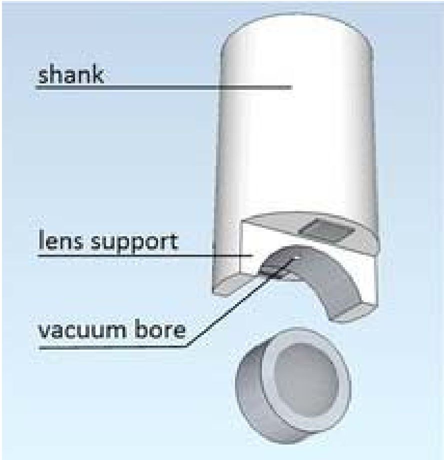
TOSA PACKAGE

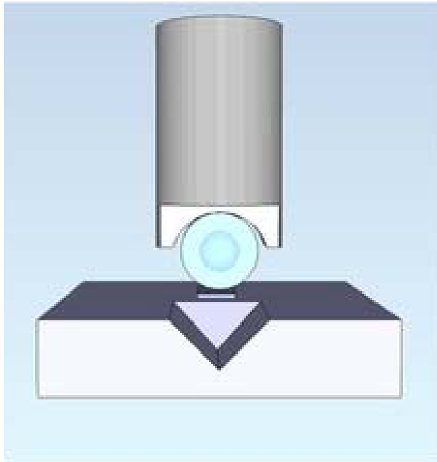
TOSA package from TEC Microsystems

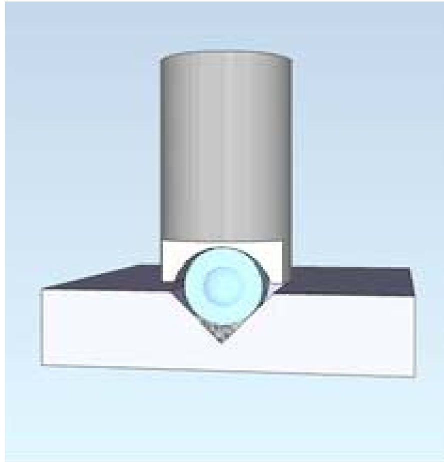


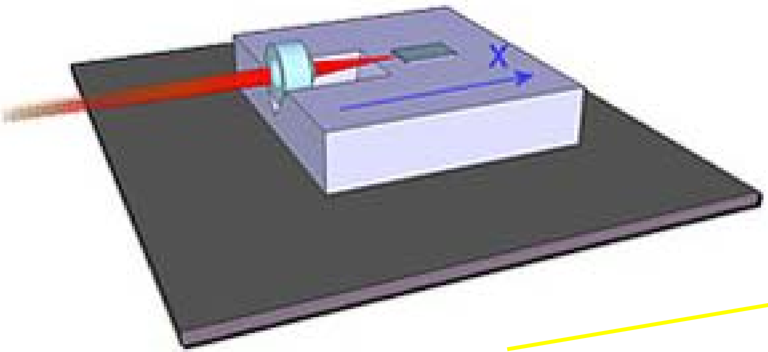


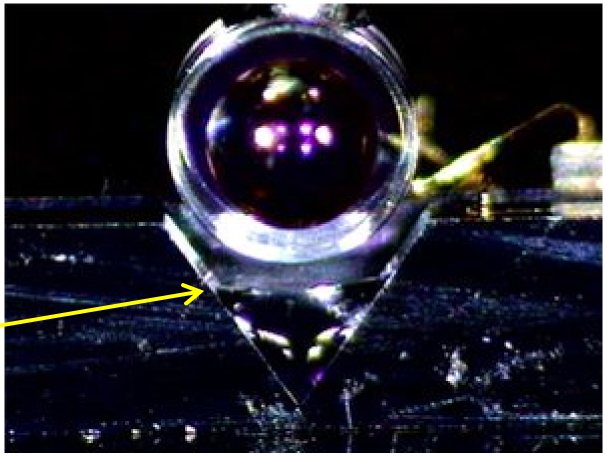
LENS PLACEMENT







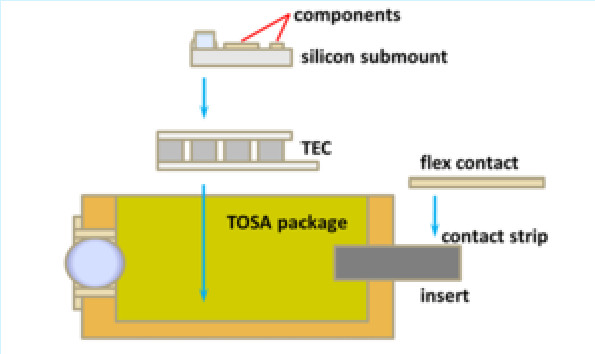




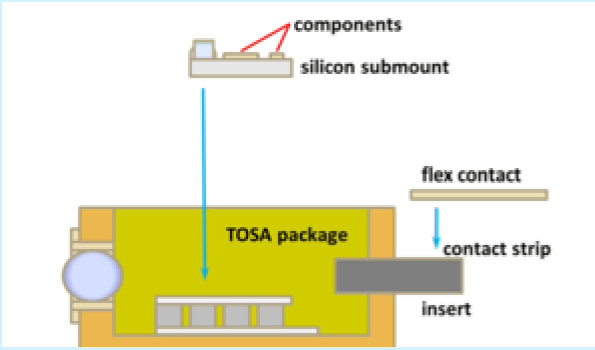
Adhesive in V-groove

EXAMPLE 2: ASSEMBLY OF A TRANSMITTER OPTICAL SUBASSEMBLY (TOSA) PACKAGE

1. Components and lens attachment (adhesive) on silicon submount



2. TEC assembly into package (fluxless, lead-free solder)



3. Silicon submount onto TEC (fluxless, lead-free solder)

PACKAGING OF PHOTONIC DEVICES

1. Two examples of packaging of photonic modules
   - Laser diode in butterfly package
   - Transmitter optical subassembly (TOSA)
2. Fiber-to-the-chip assembly strategies
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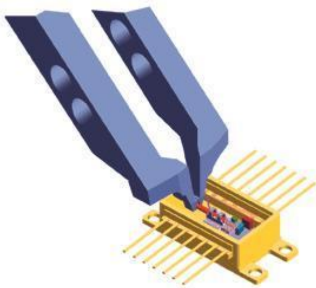
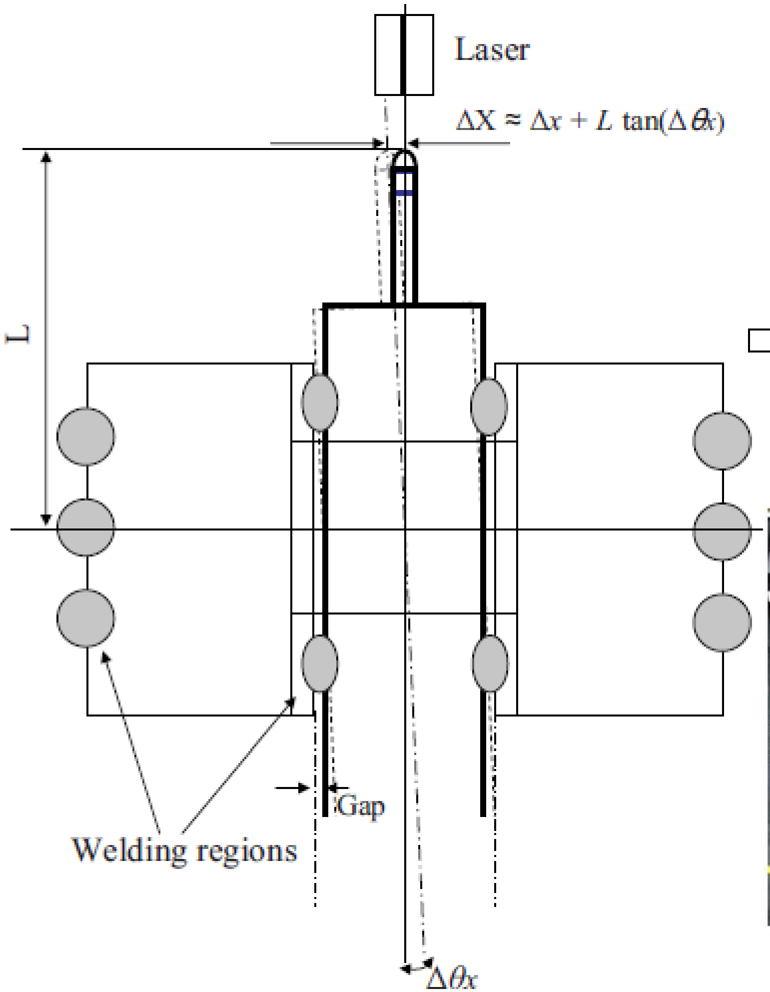
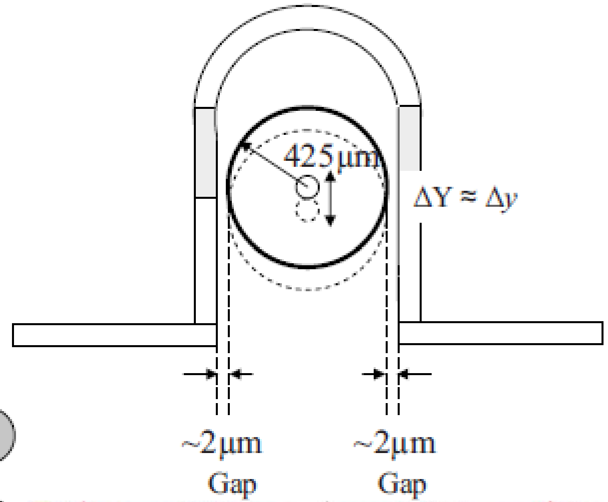
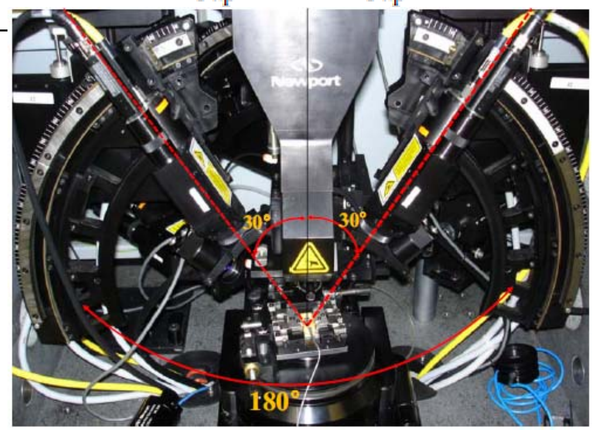
FIBER WELDING

1. #1. Initial shift
2. #2. Front welding
3. #3. Rear welding
4. #4. Gripper release
5. #5. Mechanical adjustment (ΔX)
6. #6. Laser hammering (ΔY)





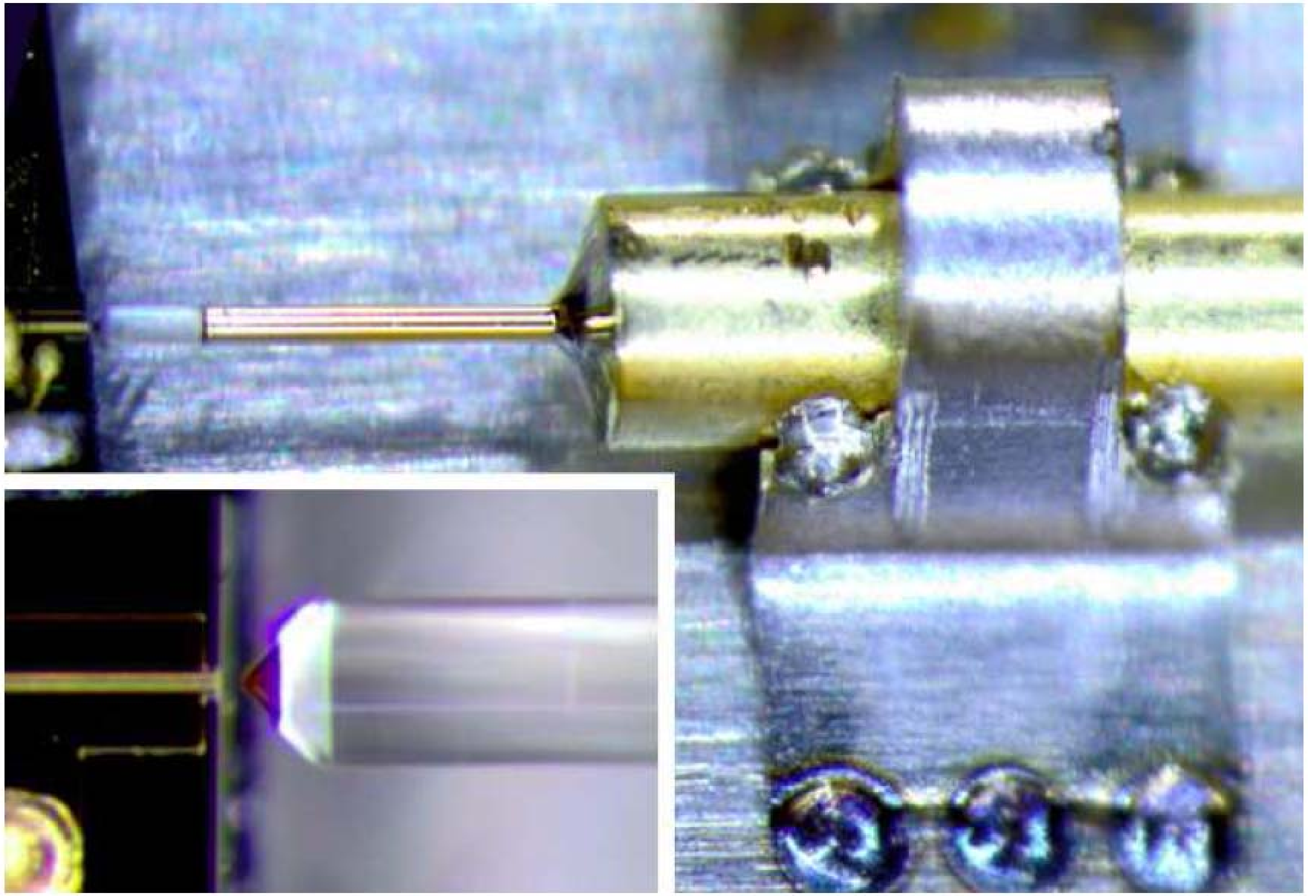




Nd:YAG laser welding station. Newport

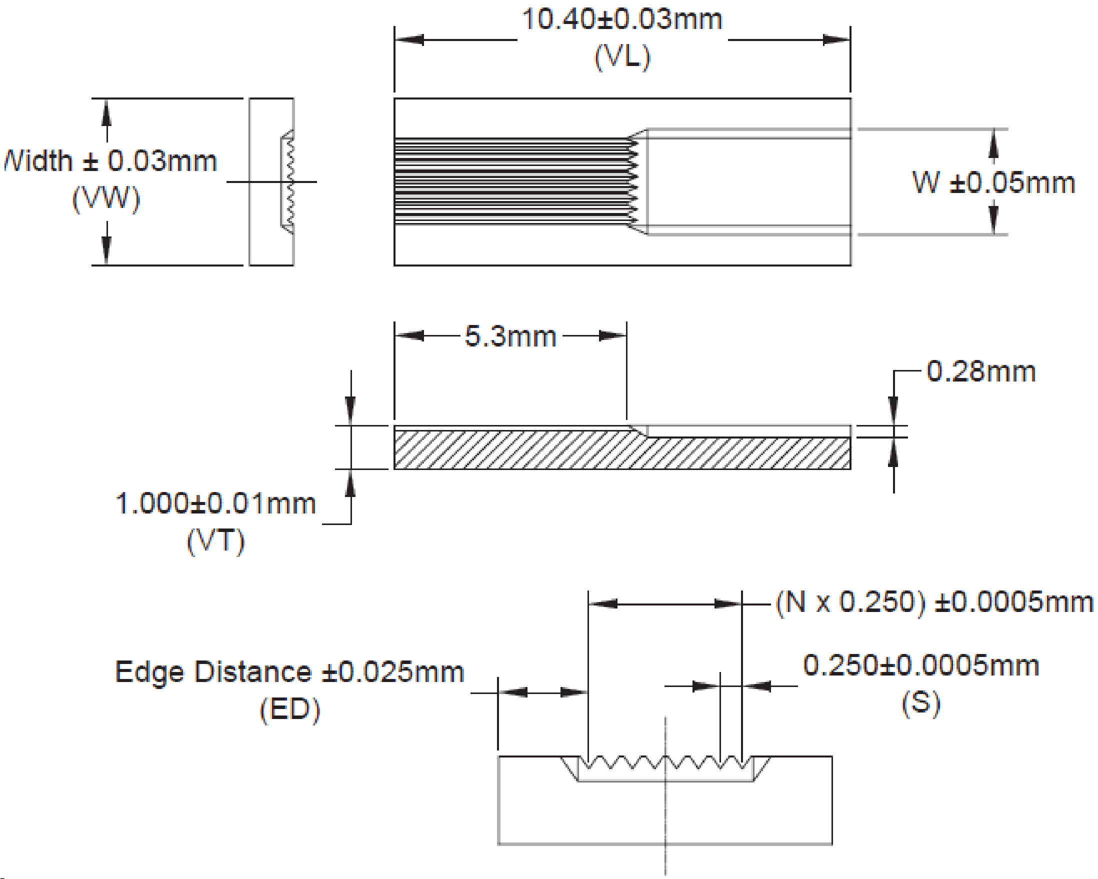
<u>Attention</u>: Post-weld shift!

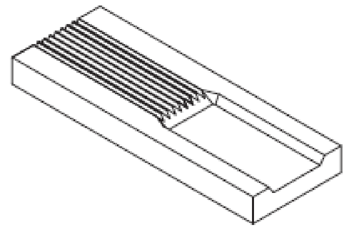
FIBER WELDING

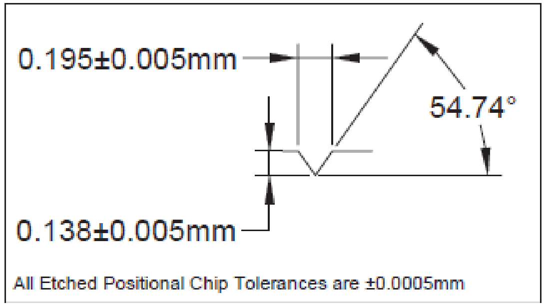


FIBER PIGTAILING: FIBER GROOVE ARRAYS

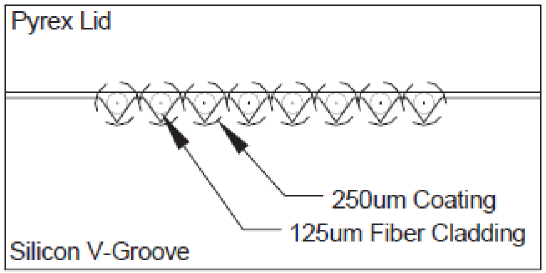
1X12 V-groove array OZ Optics:





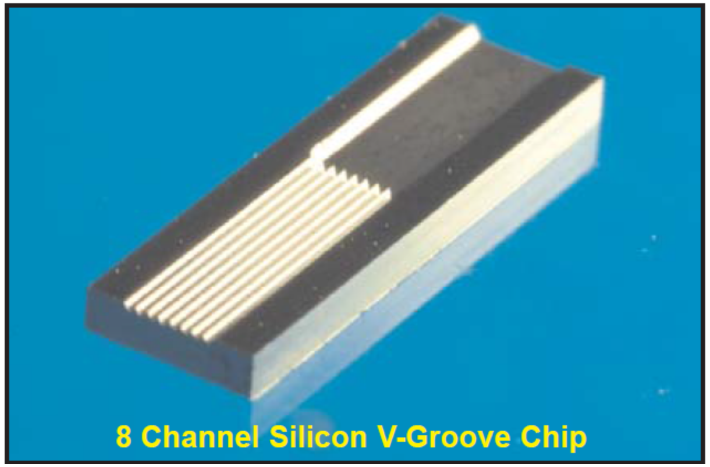


V-Groove Detail



Assembled V-Groove, Showing Fiber Layout

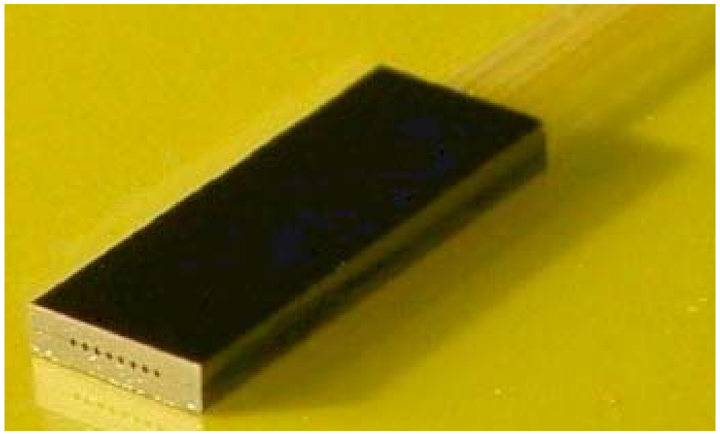
FIBER PIGTAILING: FIBER GROOVE ARRAYS

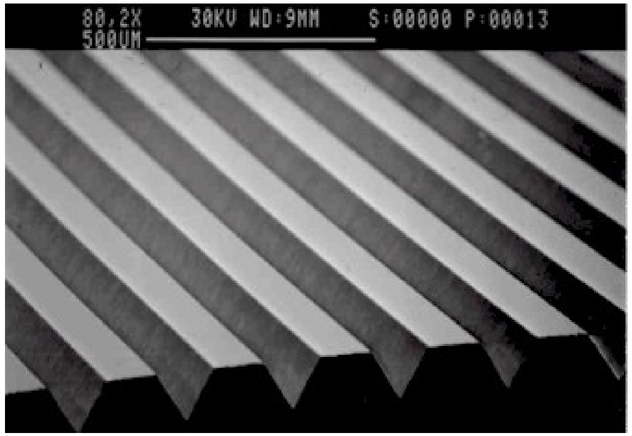


Accurate Silicon Spacer Chips for an Optical-Fiber Cable Connector

By C. M. SCHROEDER

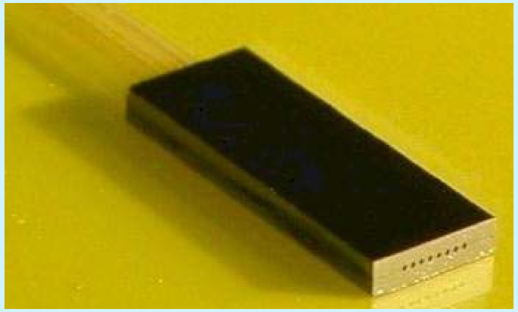
(Manuscript submitted July 1, 1977)

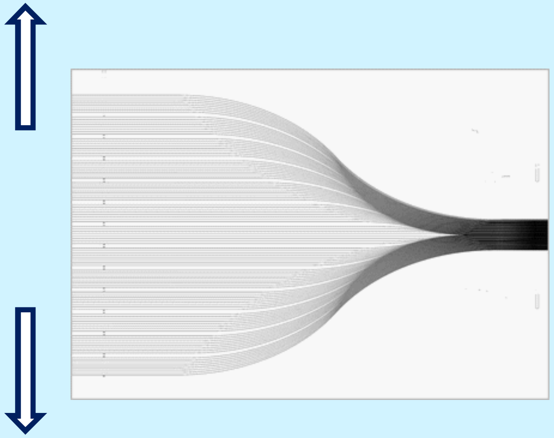




[O/E Land Inc]

ACTIVE ALIGNMENT





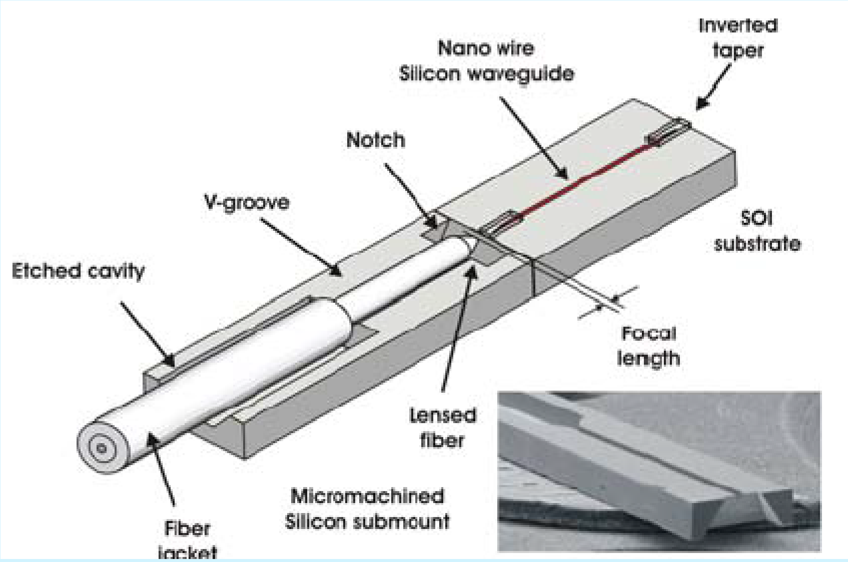
PROCEDURE:

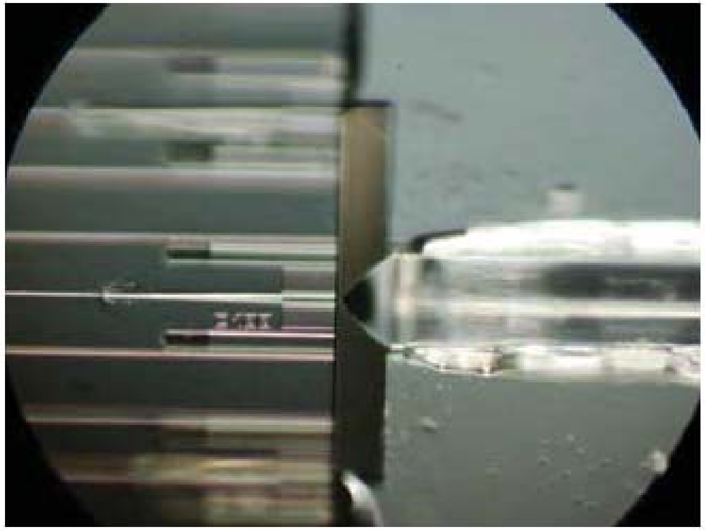
- Move fibre array vs chip in 6-axes to maximize coupling of light
- Glue in place with typically UV curable epoxy

CONSIDERATIONS:

- Time consuming, costly procedure
- Mode mismatch between fibre and waveguides → Low coupling efficiency
- Pitch mismatch between fibre array and photonic chip → Loss of real-state

PASSIVE ALIGNMENT: SILICON MICROBENCH TECHNOLOY

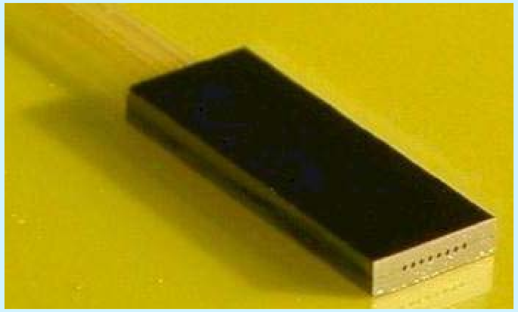


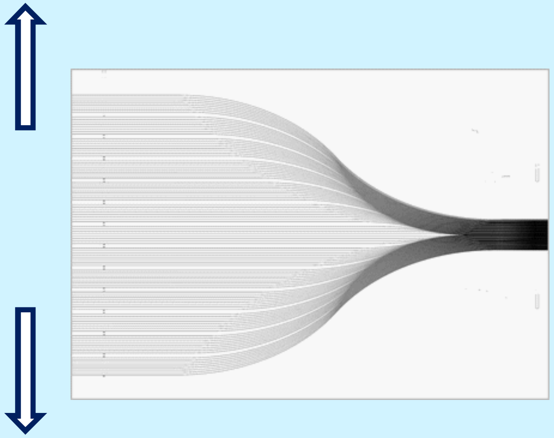


[Group IV photonics, 2011]

- Etched V-grooves lithographically aligned to photonic device
- Extra notch for glue relief
- Alignment errors limit the overall performance

ACTIVE ALIGNMENT





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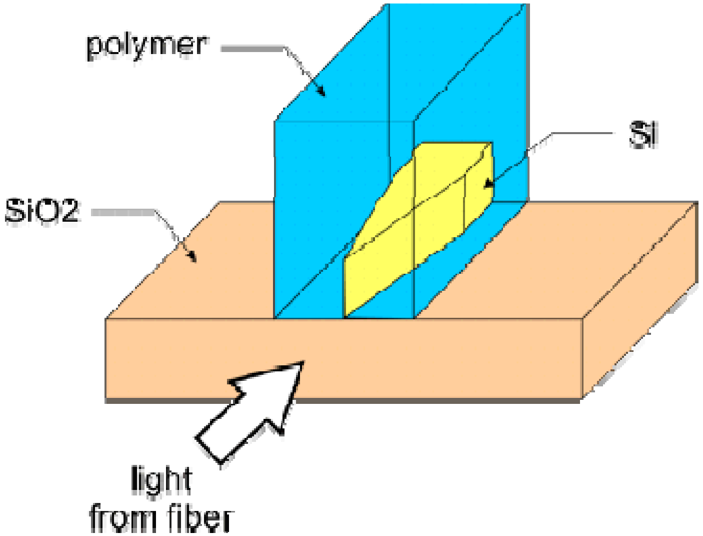
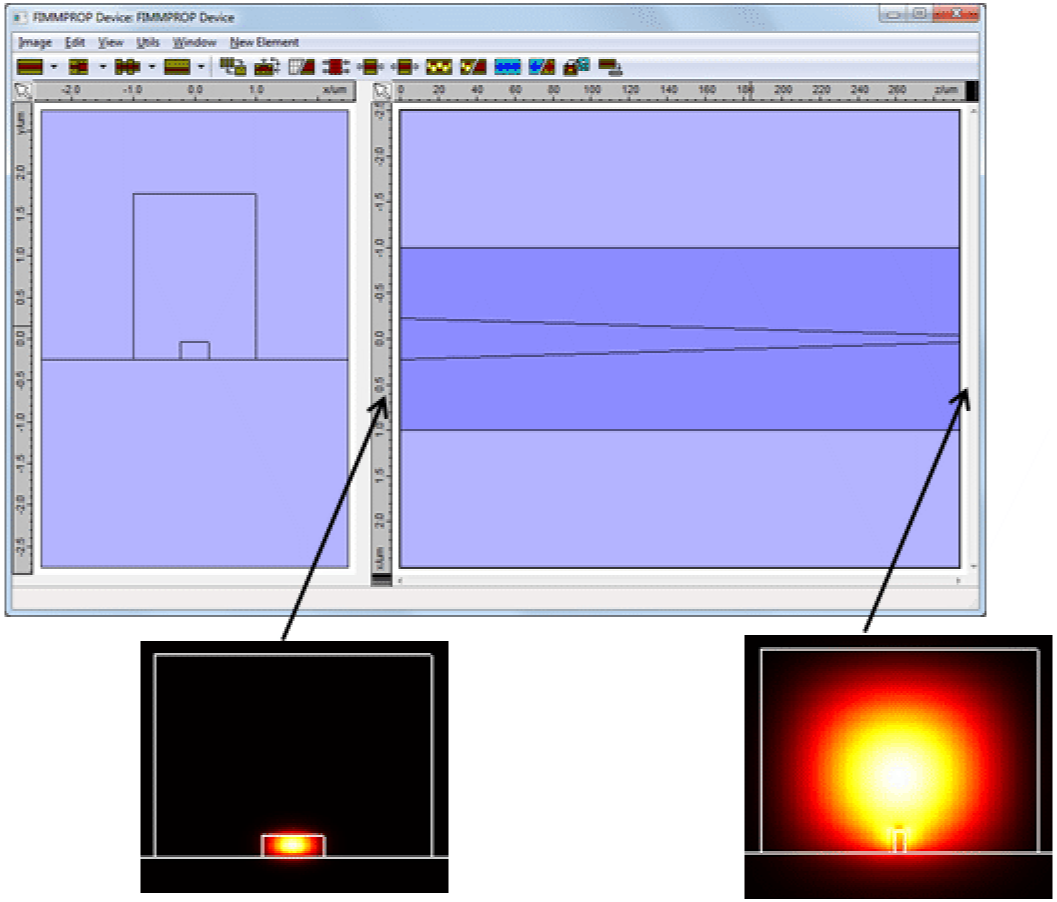
MODE SIZE CONVERTERS



Si layer thickness	220nm
Silicon layer width	450nm to 75nm
Refractive index of polymer	1.58
Total size of the polymer layer	2um by 2um
Thickness of silica substrate	2.5um
Taper length	Varied between 10um and 300um
Wavelength	1.5um

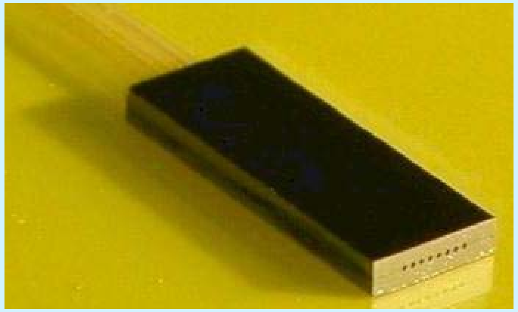
[FiMMProp]

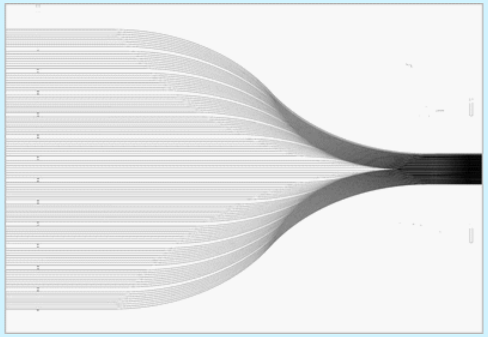
MODE SIZE CONVERTERS



[FiMMProp]

ACTIVE ALIGNMENT





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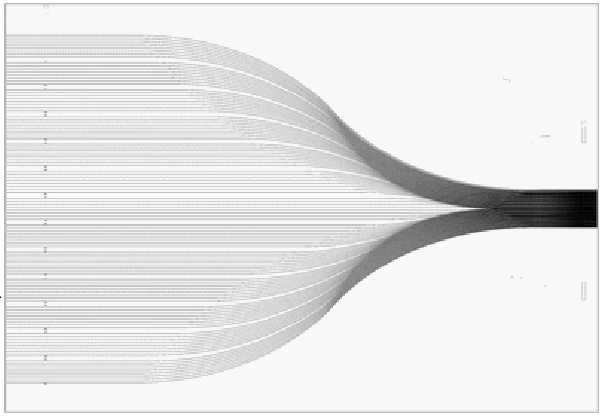
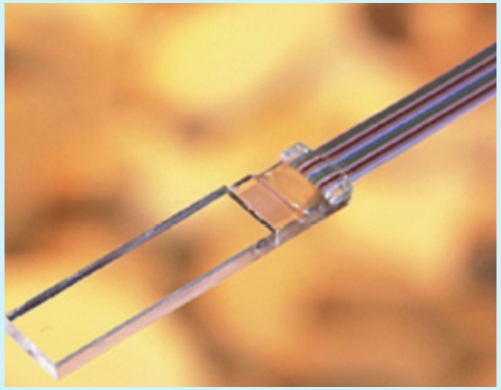
INTRODUCTION OF DIFFERENT INTERPOSERS

Match to fibre pitch

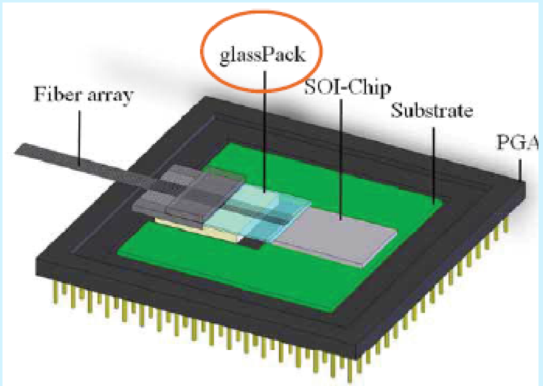


Match to photonic waveguides

Two examples of ion-exchange waveguides in glass interposer:



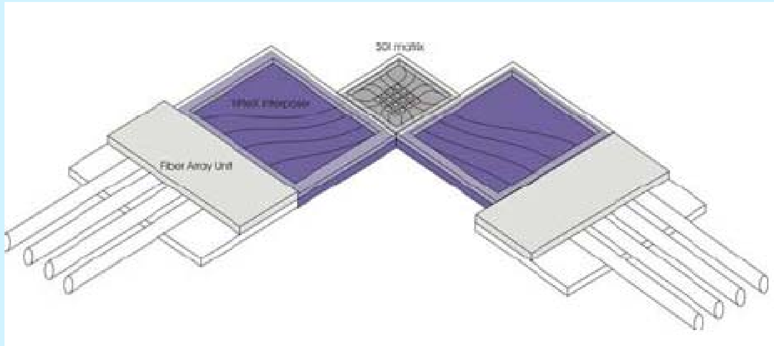
[Teem photonics]



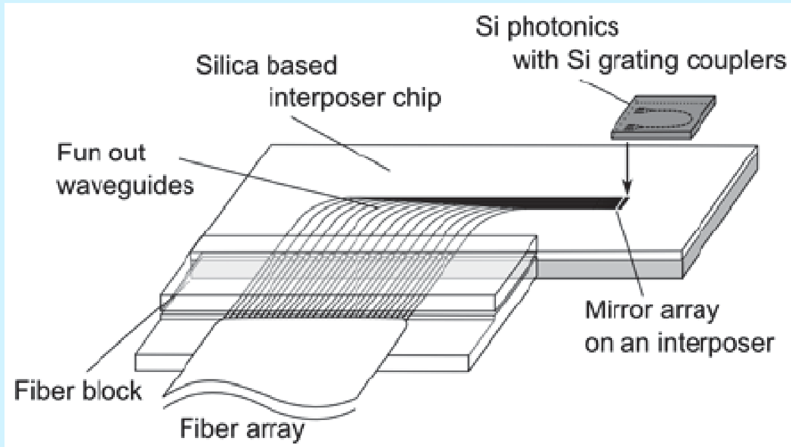
[Fraunhofer IZM, glassPack]

INTRODUCTION OF DIFFERENT INTERPOSERS

Interposer in TripleX (Si_3N_4/SiO_2 based waveguide technology from LioniX):



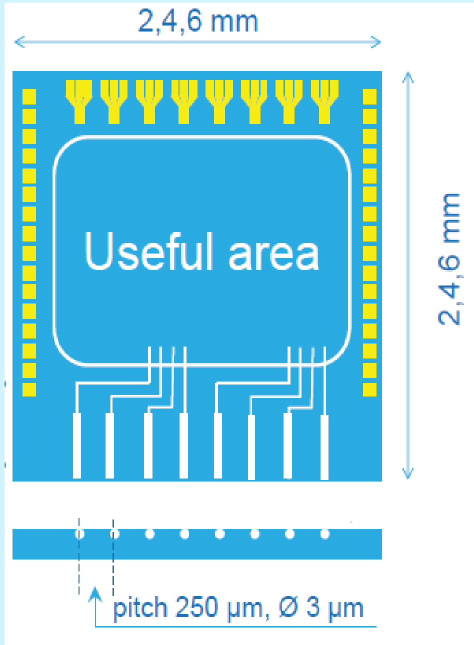
[C. Stamatiadis et. al., Optical Network Design and Modelling (ONDM), 2011]

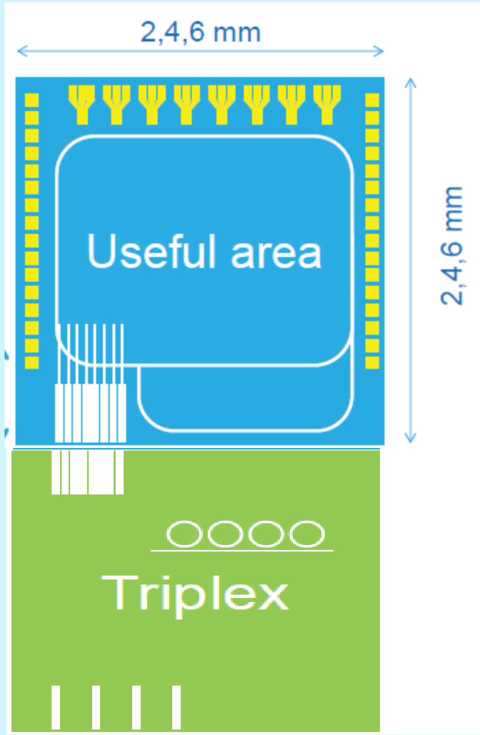


[K. Watanabe et. al., CLEO Europe 2009]

INTRODUCTION OF DIFFERENT INTERPOSERS

InP with TripleX interposer:

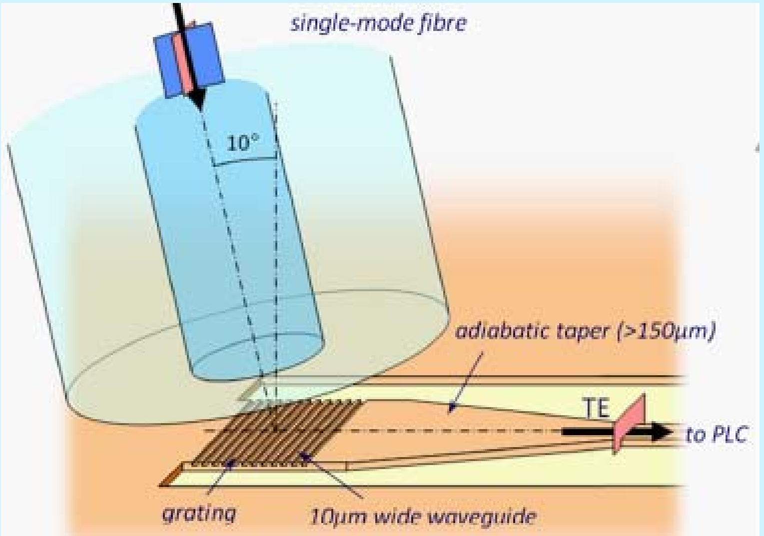




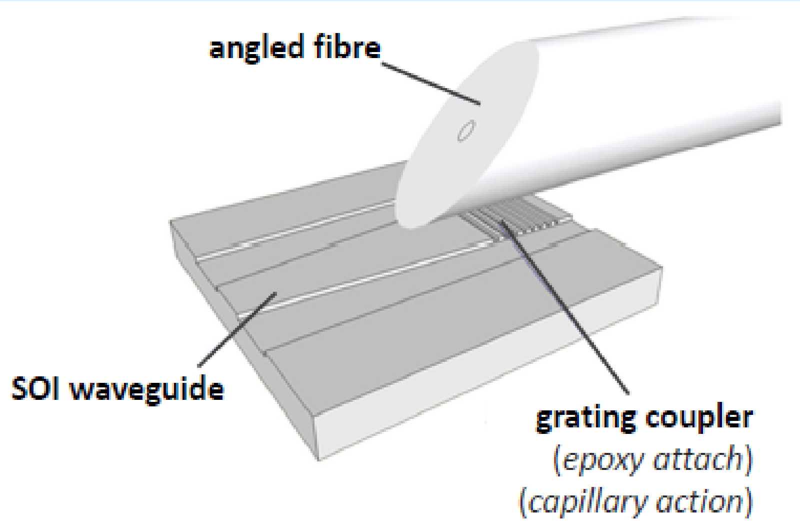
[M. Smit, Packaging requirements, Paradigm project]

GRATING COUPLING

gPack (IZM, Epixfab):



Angled fibre (Tyndall, Epixfab):

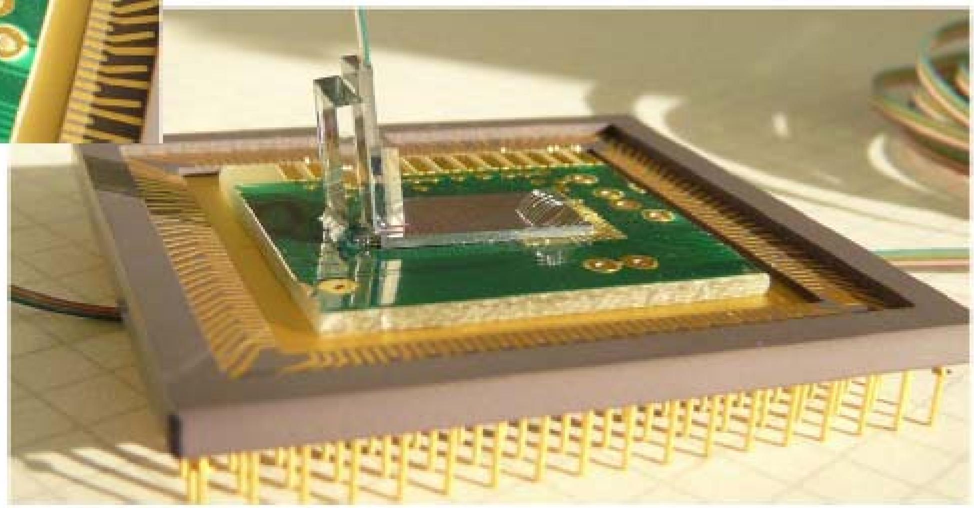


[P. O'Brien, ECOC 2012]

gPACK (IZM, Epixfab)

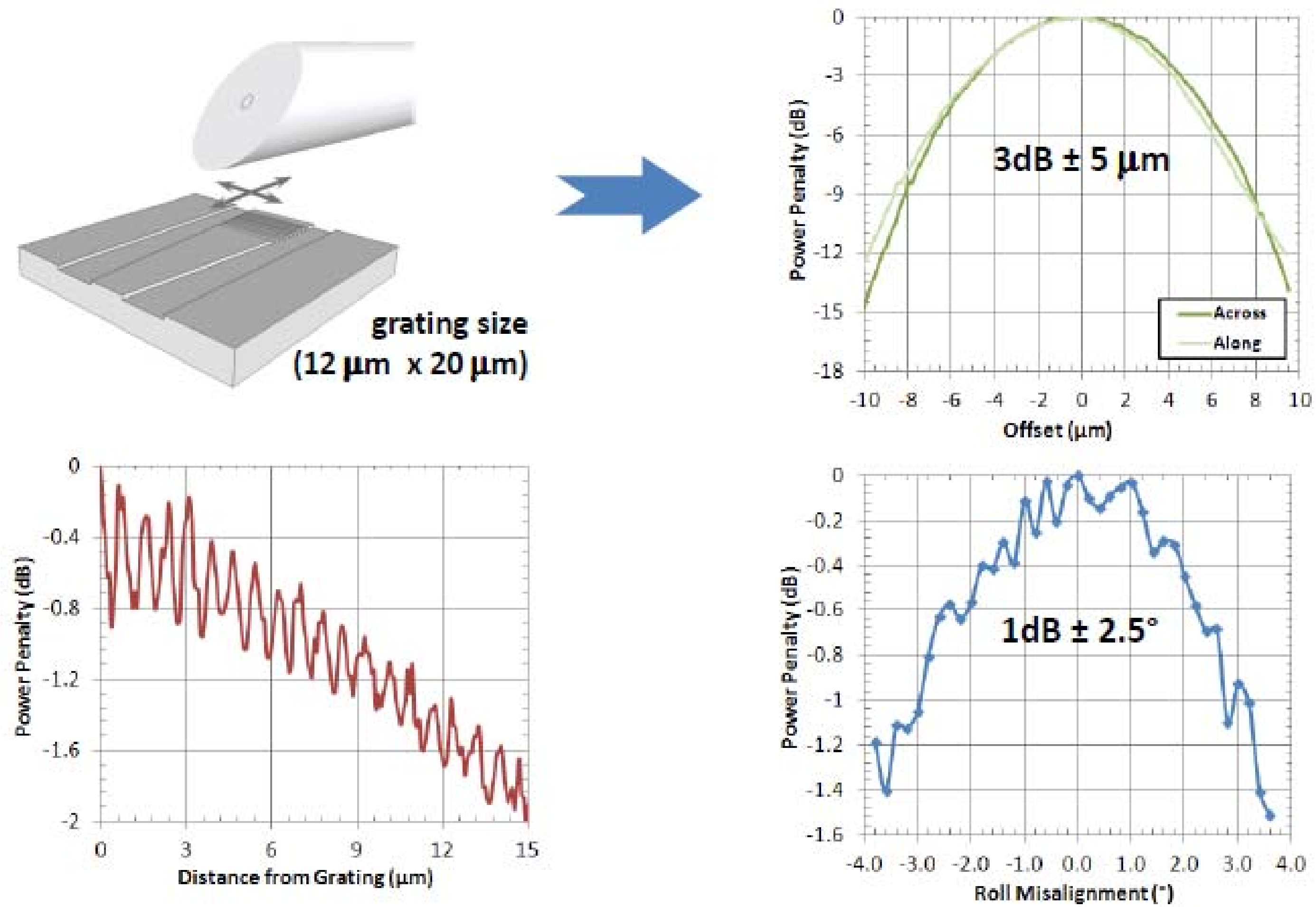
gPack

- up to 26 fibers
- up to 60 DC connections
- non-hermetic

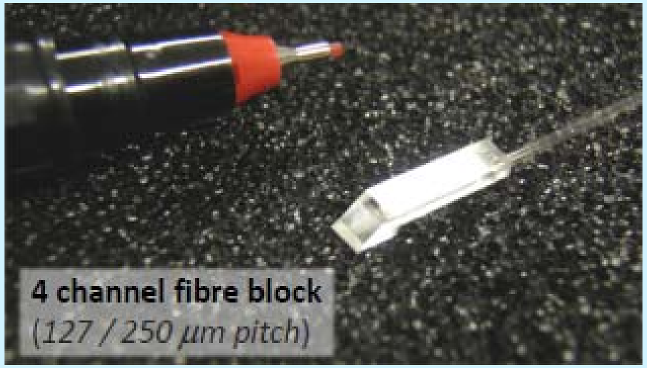


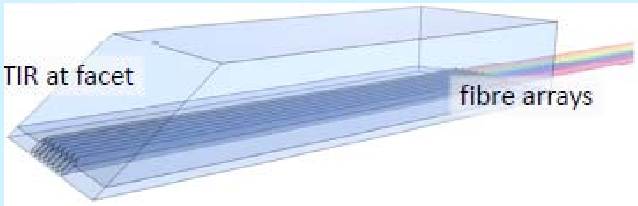
Fraunhofer
IZM

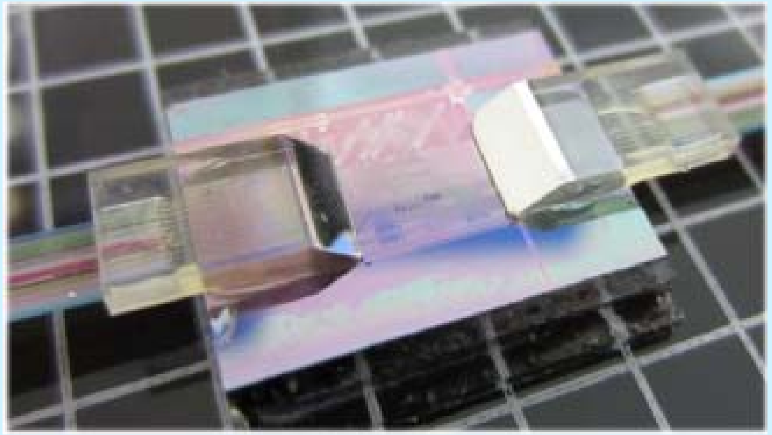
ANGLED FIBER (Tyndall, EPIXFAB)



ANGLED FIBER (Tyndall, EPIXFAB)





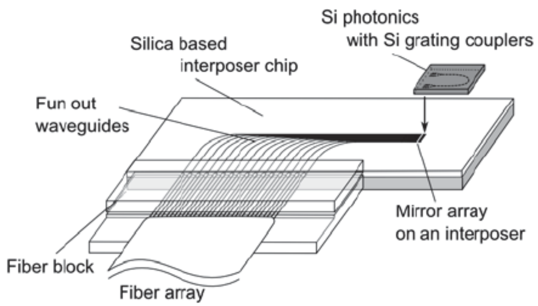


[P. O'Brien, ECOC 2012]

<u>However</u>:

Still size and pitch problem!

→ Use of interposer



[K. Watanabe et. al., CLEO Europe 2009]

OUTLINE

- Packaging of LEDs, detectors and image sensors
- Packaging of photonic devices
- Hybrid and heterogeneous integration technologies

LECTURE LEARNING GOALS

1. Get an overview of different available packaging and integration technologies

2. Get a “feeling” for the challenges of packaging

3. Acquire a “design-for-packaging” attitude