Some FPGA SoC Applications and Trends in Advanced System On Chip

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Outline of Presentation
(1) SoC Applications

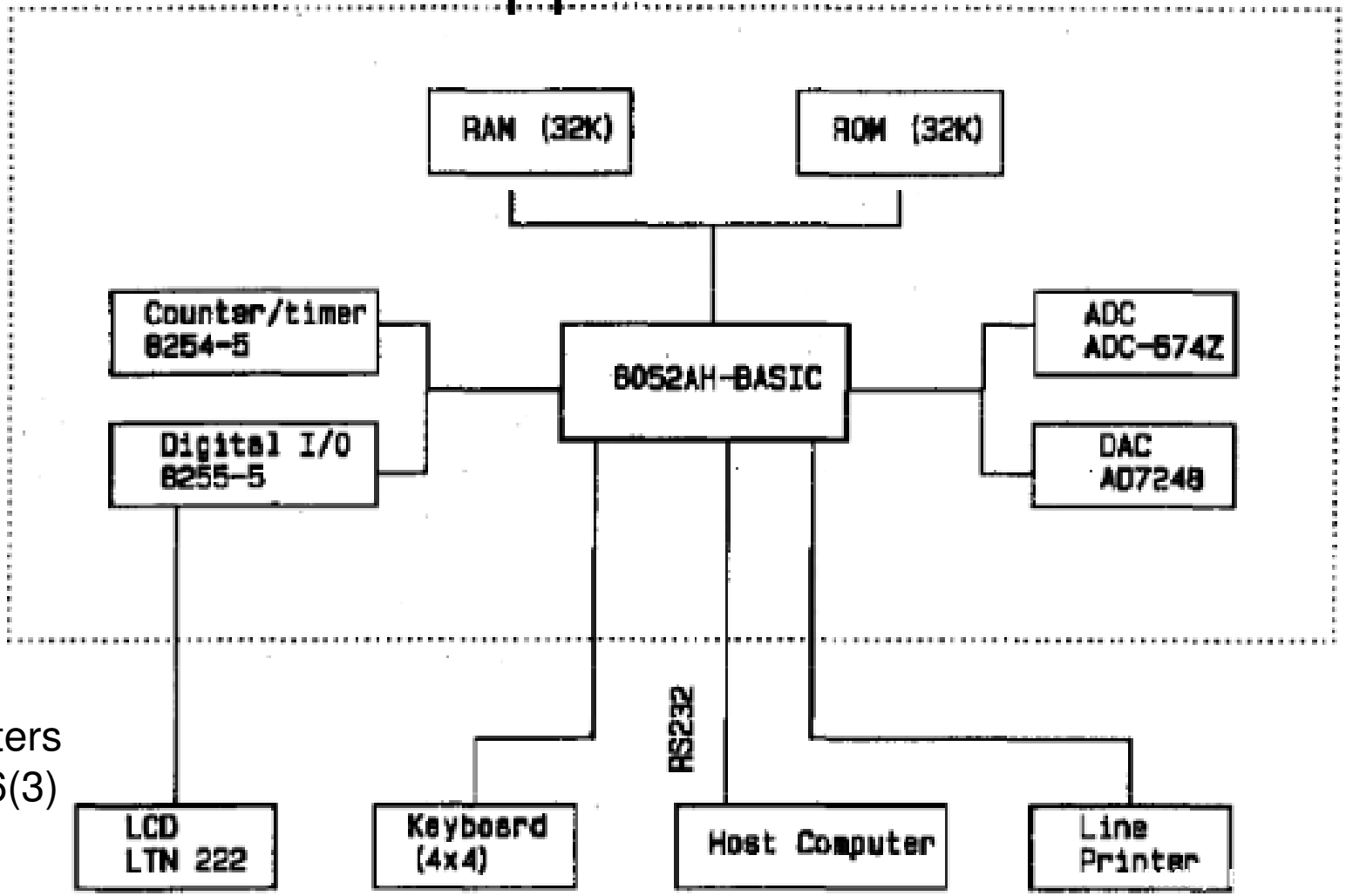
- Context
- Why FPGA Technology?
- The Options?
- Two Case Studies
- Summary
- Short stretch break
  - 5 minutes

Outline of Presentation
(2) SoC Trends

- What is a SoC?
- Future Trend Drivers
- 3D Chip Stacking
- Current SoC tools
- Conclusions

Scope – Instrumentation

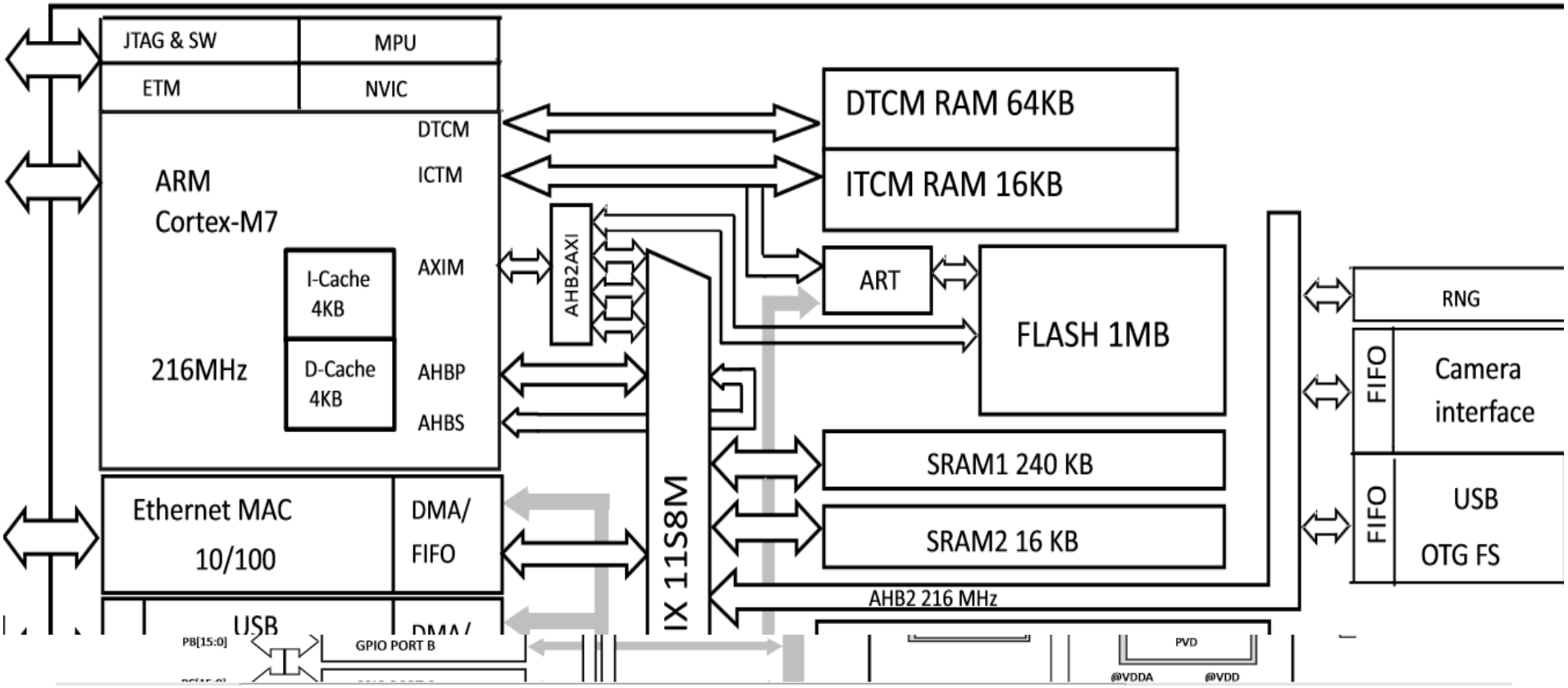
- The “traditional” approach



Source: Computers & Chemistry, 16(3) July 1992

Scope – Instrumentation

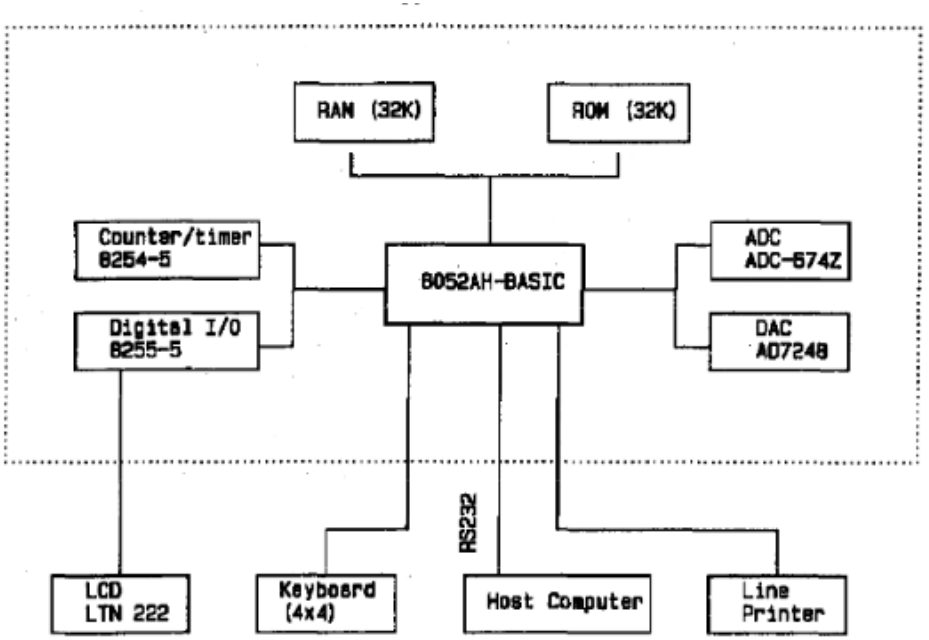
- How much has really changed?



Source: STMICRO ARM® Cortex®-M7 core datasheet

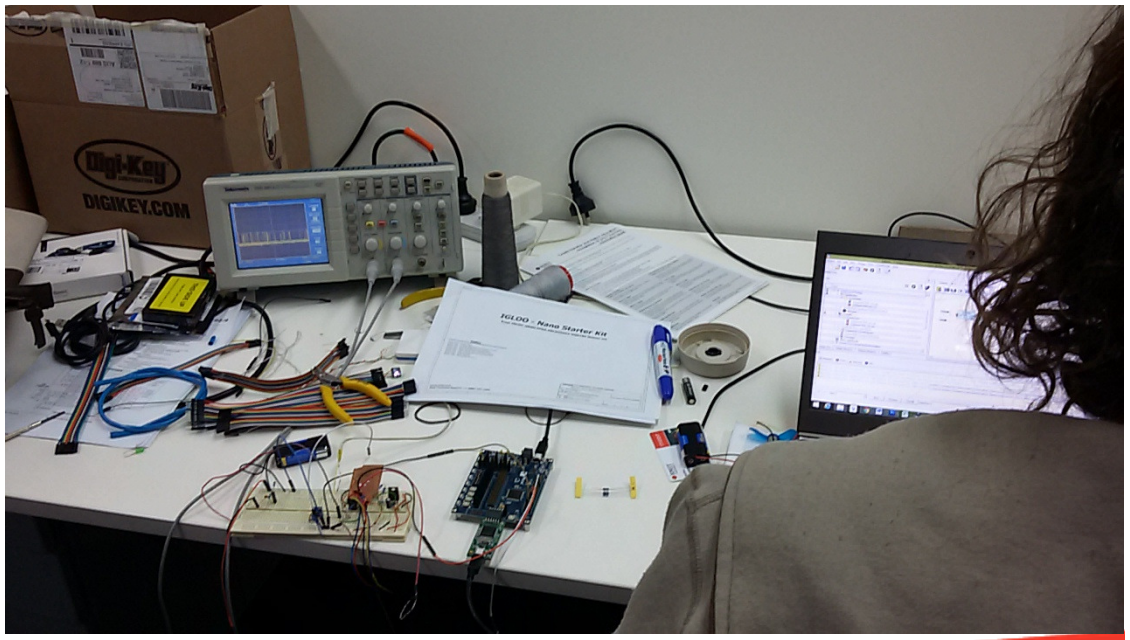
Context – the problem

- Data acquisition & storage
- Local control
- Local processing
  - Filtering
  - Formatting
- Data transfer
  - Protocols
  - Error detection/correction



Embedded Sensors – the challenges

- Sensor Complexity
- Noise
- Flexibility
- Size
- **Power**

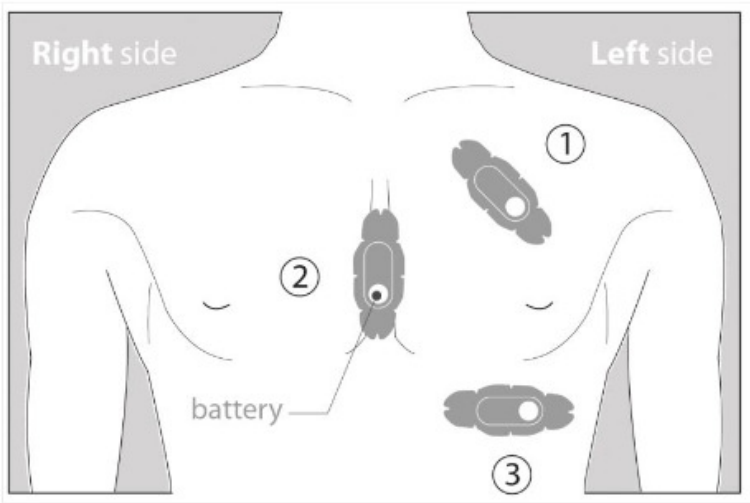


Embedded Sensors– the issues

The Issues	Some solutions
Sensor Complexity e.g., physiological monitoring	High sensitivity ADC, variable resolution, sensor control and timing
Noise – e.g., common mode interference	Digital interfaces - $\Sigma\Delta$ ADC systems
Flexibility – e.g. multiple protocols	In-field and post manufacture programmability,
Size personal interfaces	Beyond SMD, SOIC, SOT Flexible substrates, implanted electronics
Power	Flash-based devices (e.g., IGLOO)

Why FPGA Technology?

- Performance
  - exploiting hardware parallelism
  - can do more per clock cycle
- Time to Market
  - flexibility and rapid prototyping capabilities
- Cost
  - low NRE compared to ASIC
  - (But) higher compared to microprocessor
- Power
  - Parallel operation with lower clock rates can reduce power
  - Ability to “sleep” when inactive



http://www.vitalconnect.com/upload/Documents/AutomatedPrediction_2014_IEEE_published.pdf

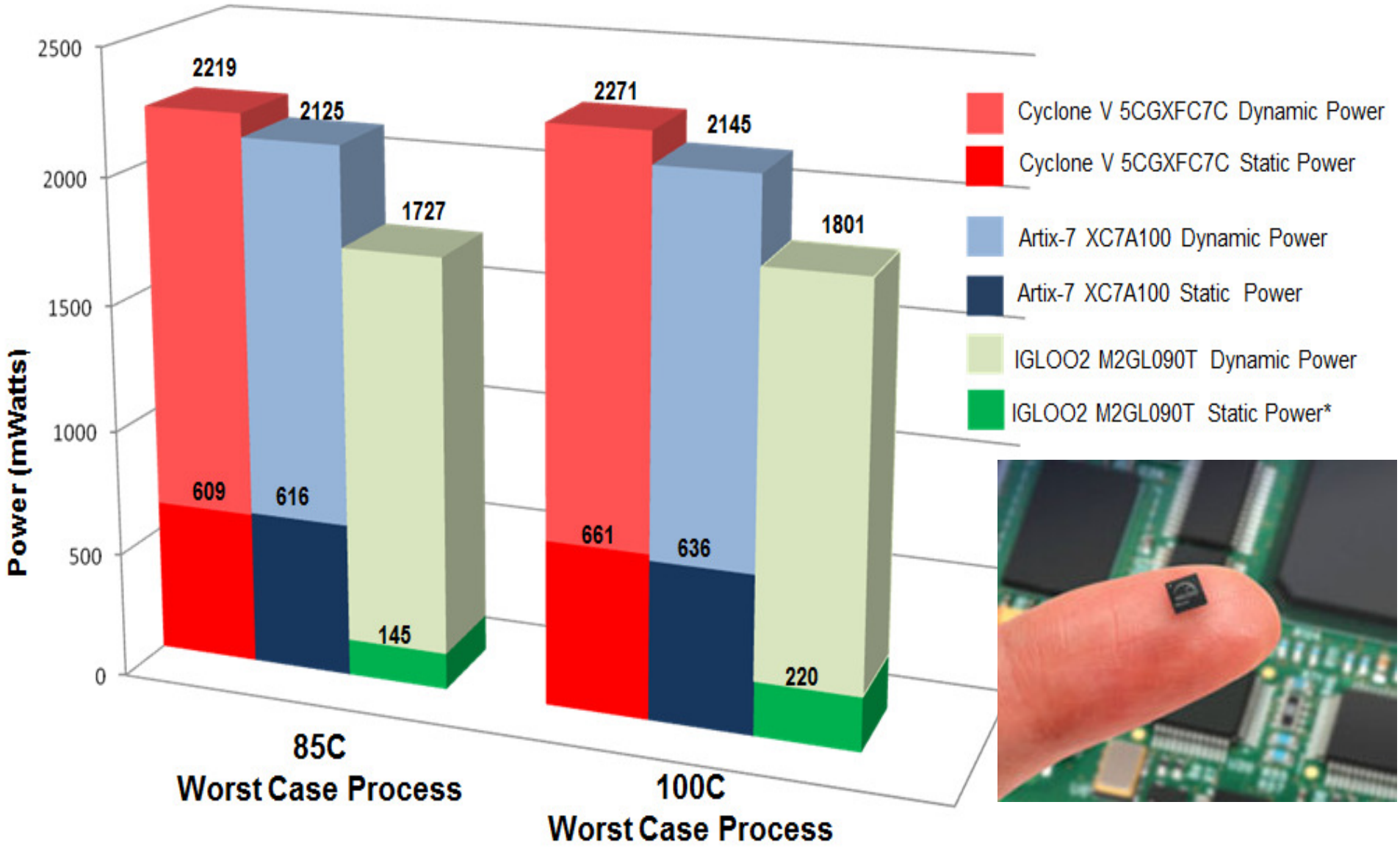
The Options?

- The "usual suspects"
  - Xilinx, Altera
  - tend to be focusing on high performance & DSP processing

Louis Renault – Casablanca 1942

- Smaller players – e.g. MicroSemi starting to offer system on chip
  - Low power
  - Integrated functions (e.g. analog)

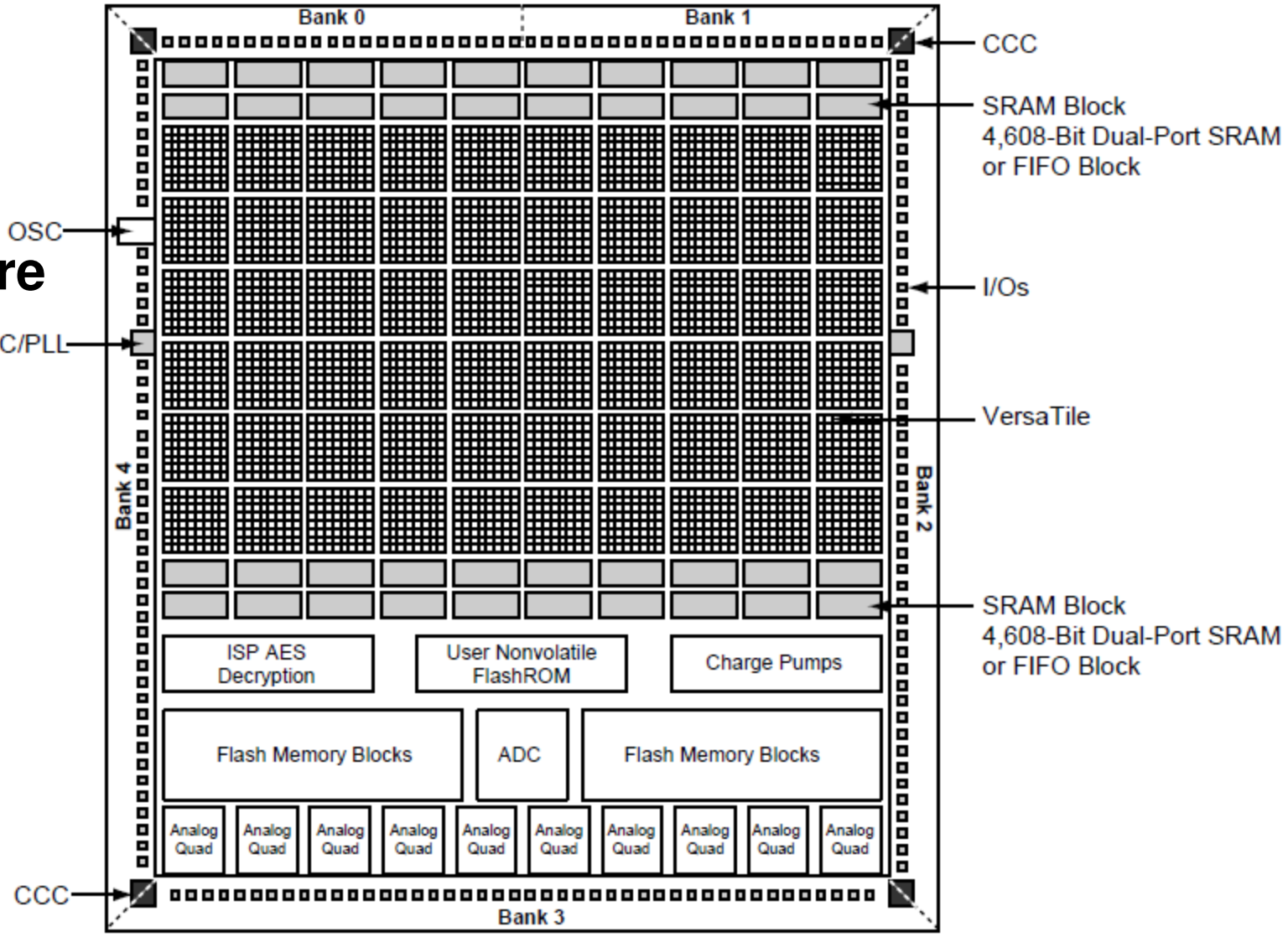
SoC – Power Considerations



Small SoC Features

MicroSemi
Fusion ®

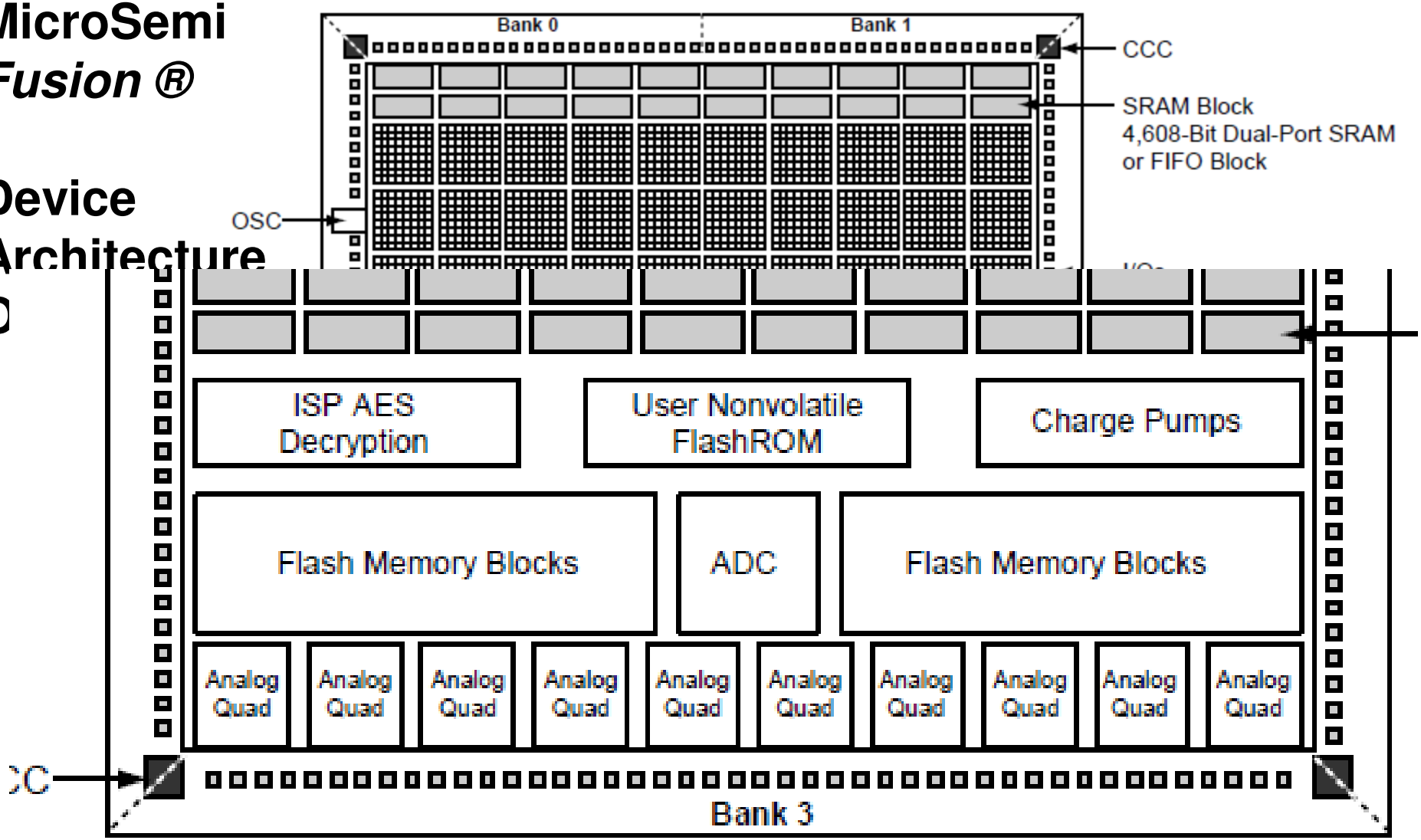
Device Architecture Overview



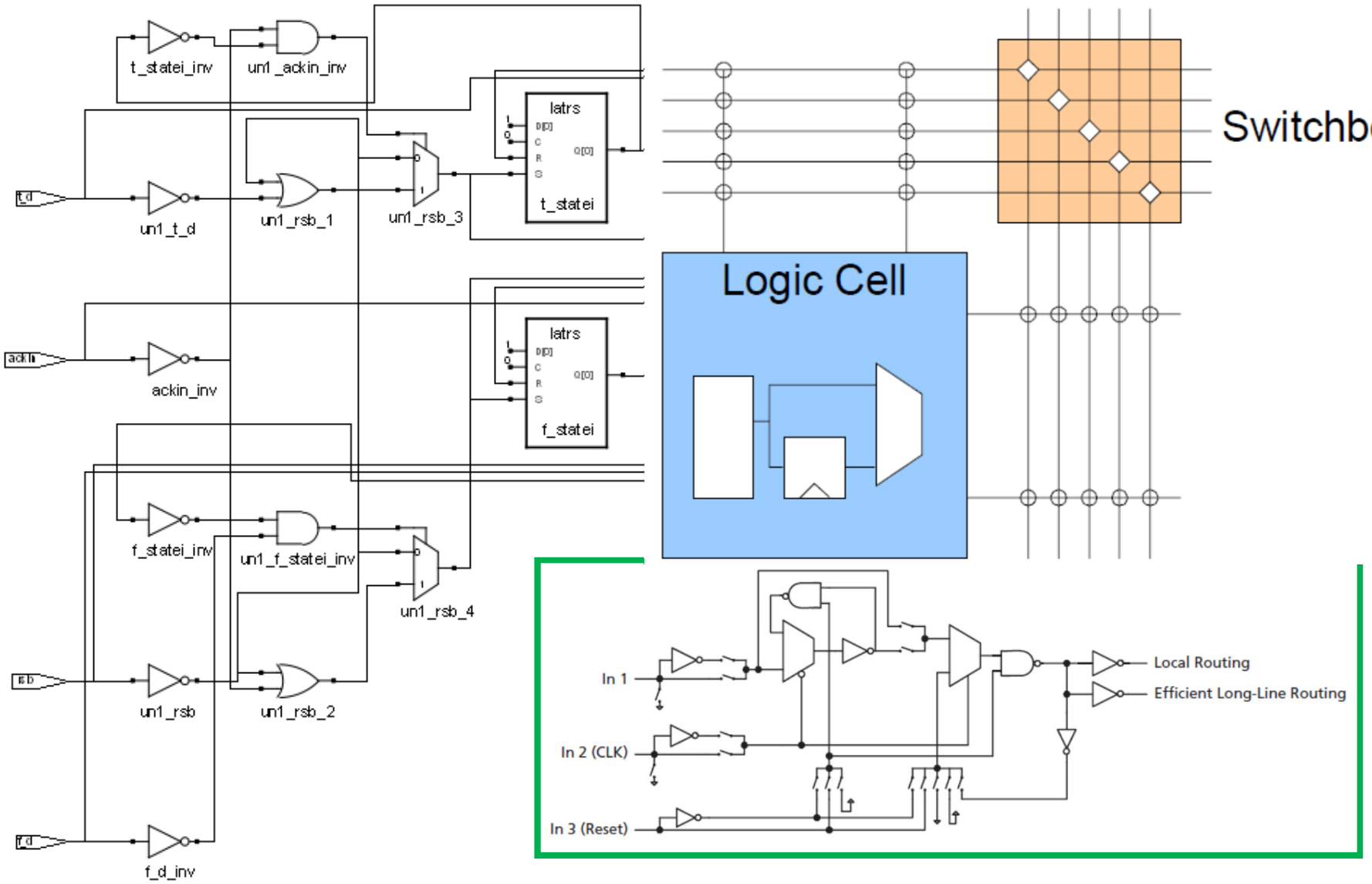
Small SoC Features

MicroSemi
Fusion ®

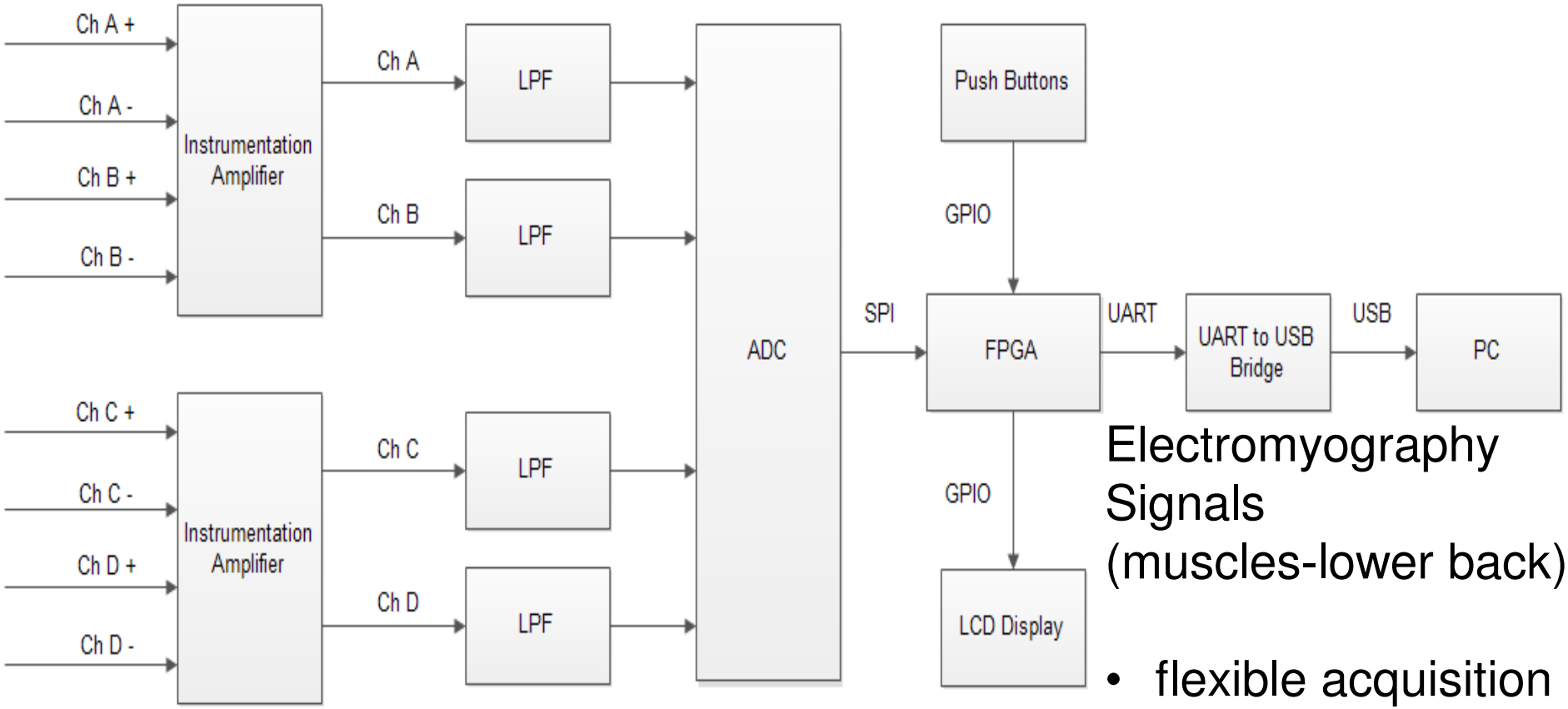
Device
Architecture
O



Example: “Igloo Nano”



Case Study 1 – EMG Monitor



Electromyography Signals (muscles-lower back)

- flexible acquisition
- multiple filters
- signal processing
- interface protocols

Case Study 1 – EMG Monitor

- flexible acquisition
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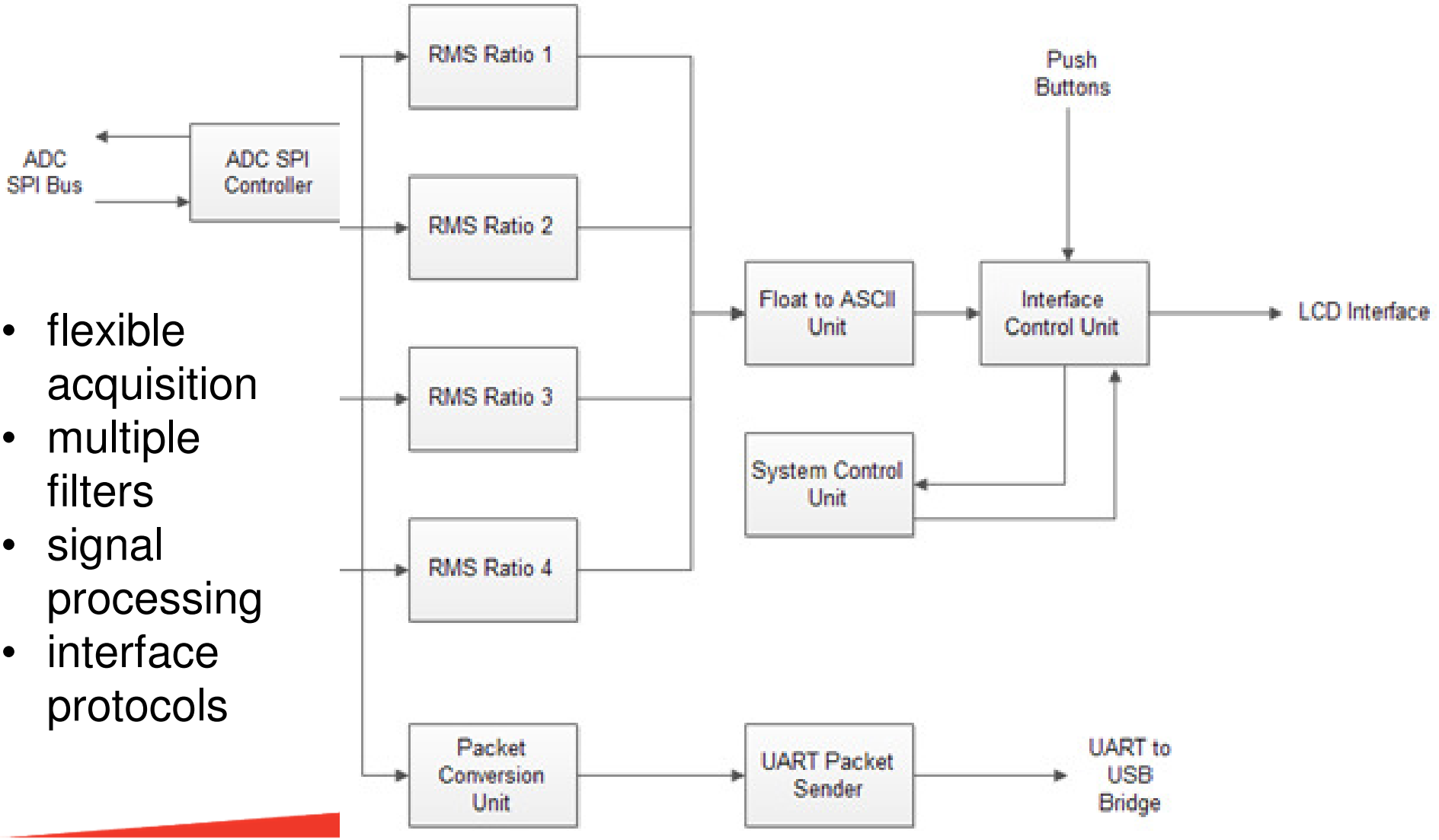
- interface protocols



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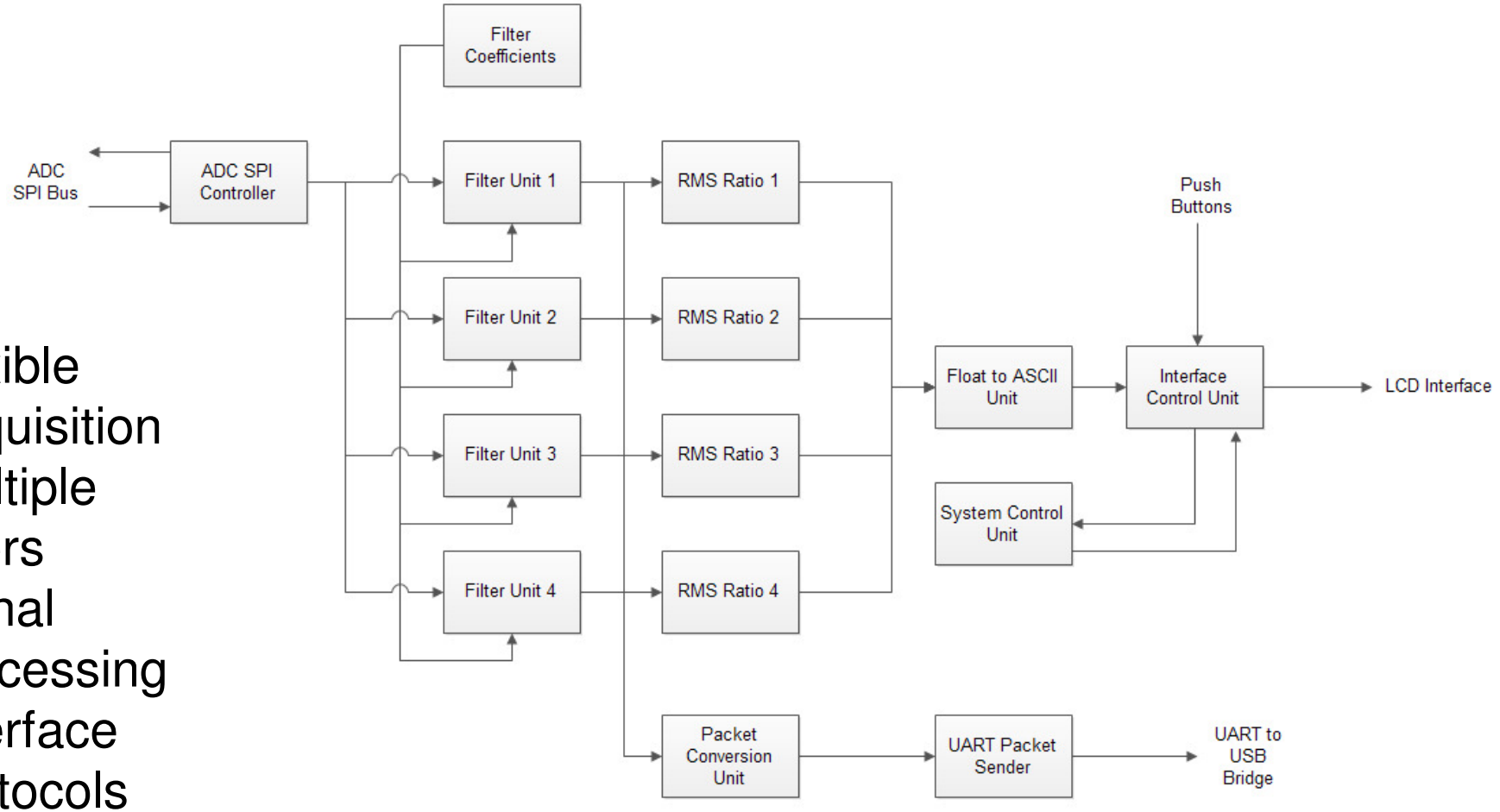

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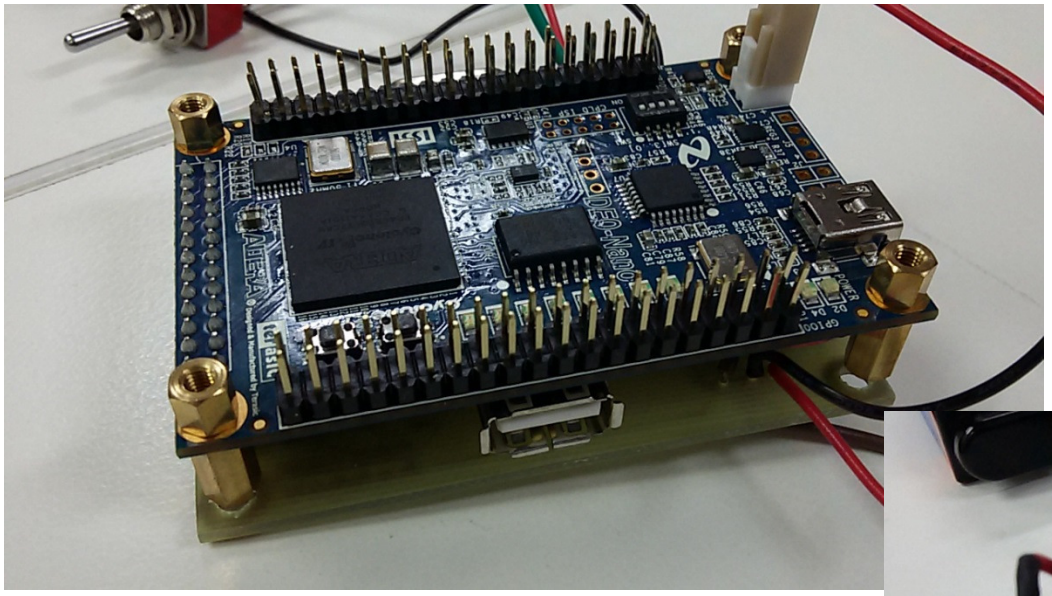
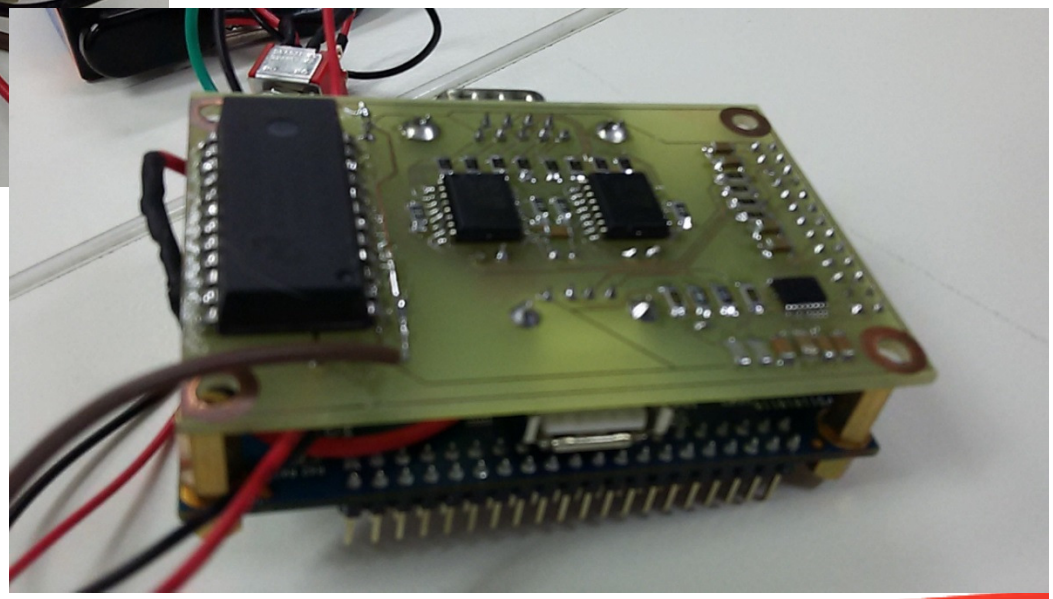
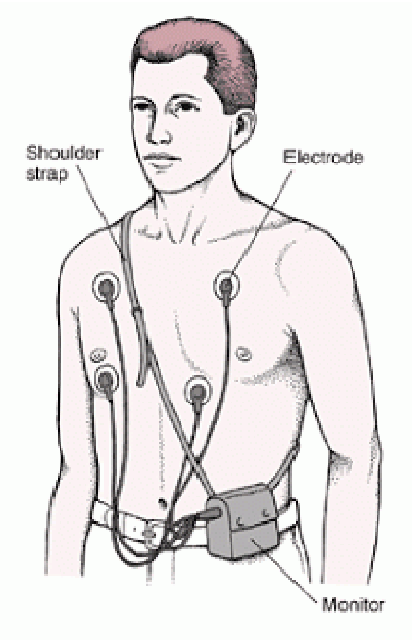
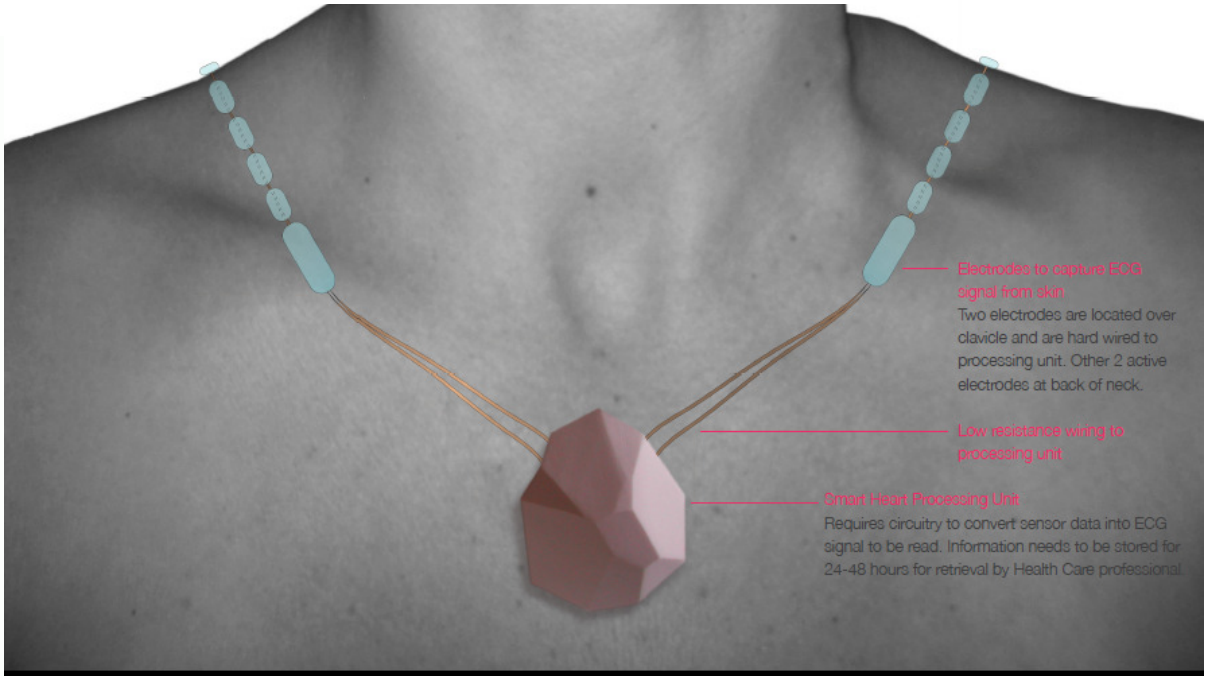




Case Study 2 – "Smart Heart" - miniaturization

- Continuous monitoring for people at risk of cardiac event
- Necklace stores 24-48 hours of ECG data for download and analysis by healthcare professional
- Wearable device that is comfortable and aesthetically desirable



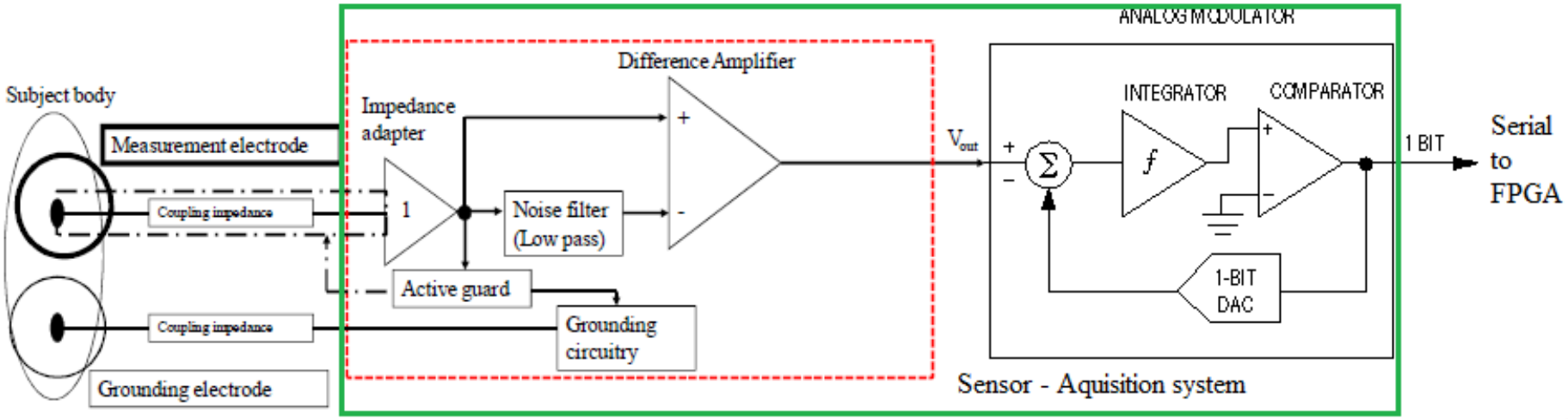


Case Study - Smart Heart

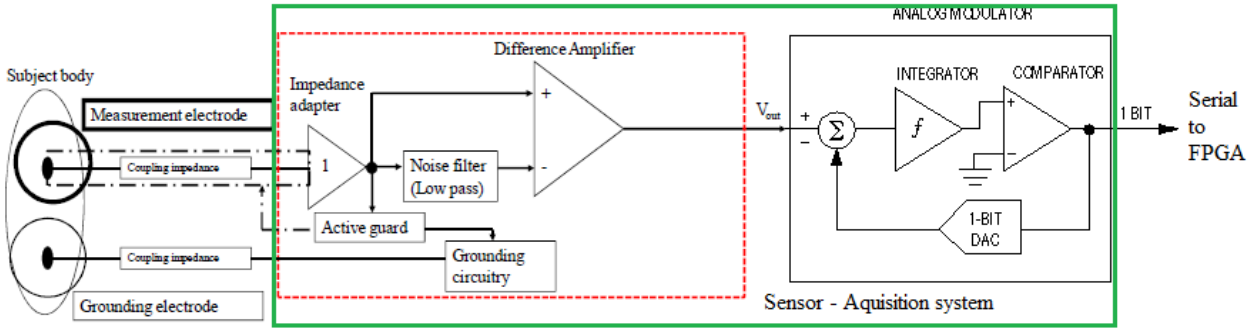
- Initially intended to record low noise high resolution ECG signal
- Applicable to a number of different low signal body sensors (ECG, temp, etc.)
- low powered – ideally, support monitoring of ECG signal over several days
- Compact, non-invasive implementation, compatible with woven and other fabric holters.

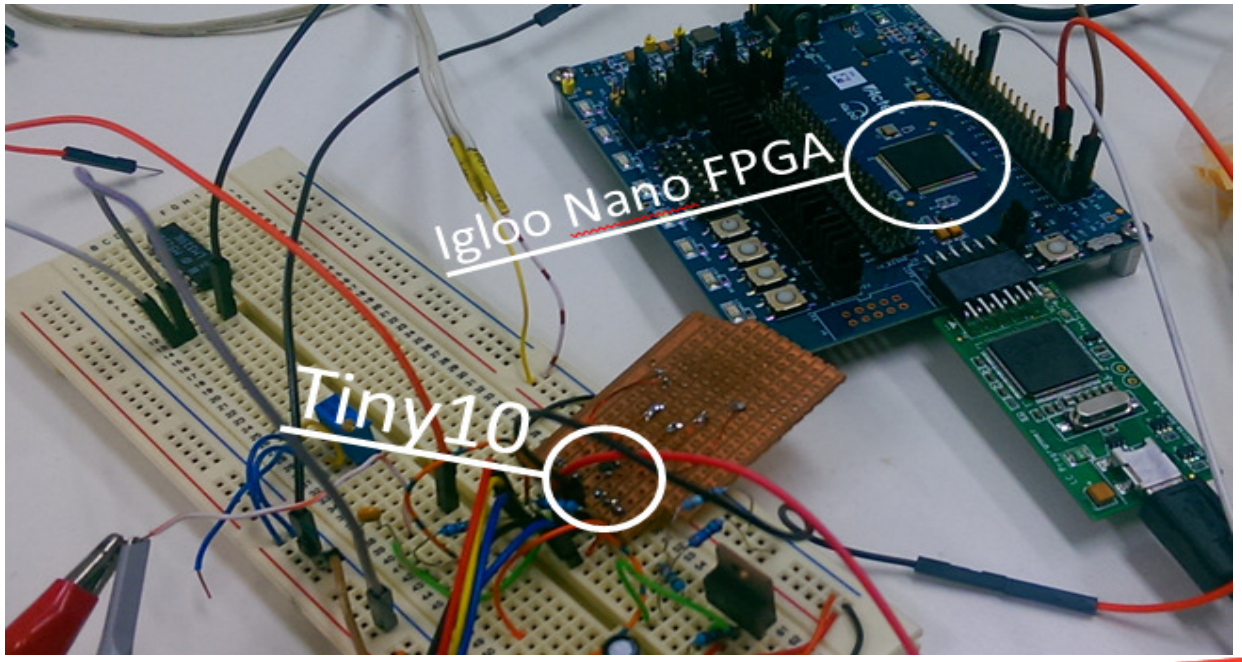
Case Study – "Smart Heart"

- Front-end microprocessor (ATTiny)
- Backend FPGA
  - Multi-channel signal processing
  - Protocol assembly

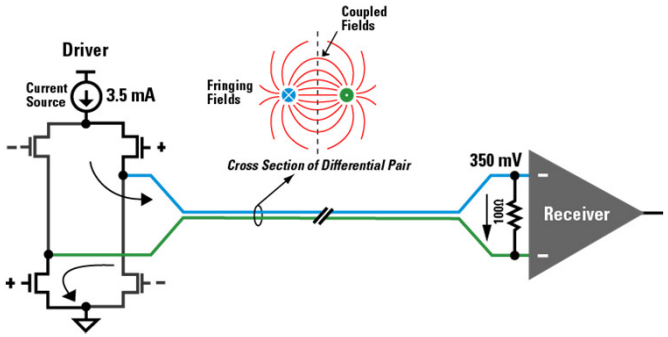


Case Study – “Smart Heart”

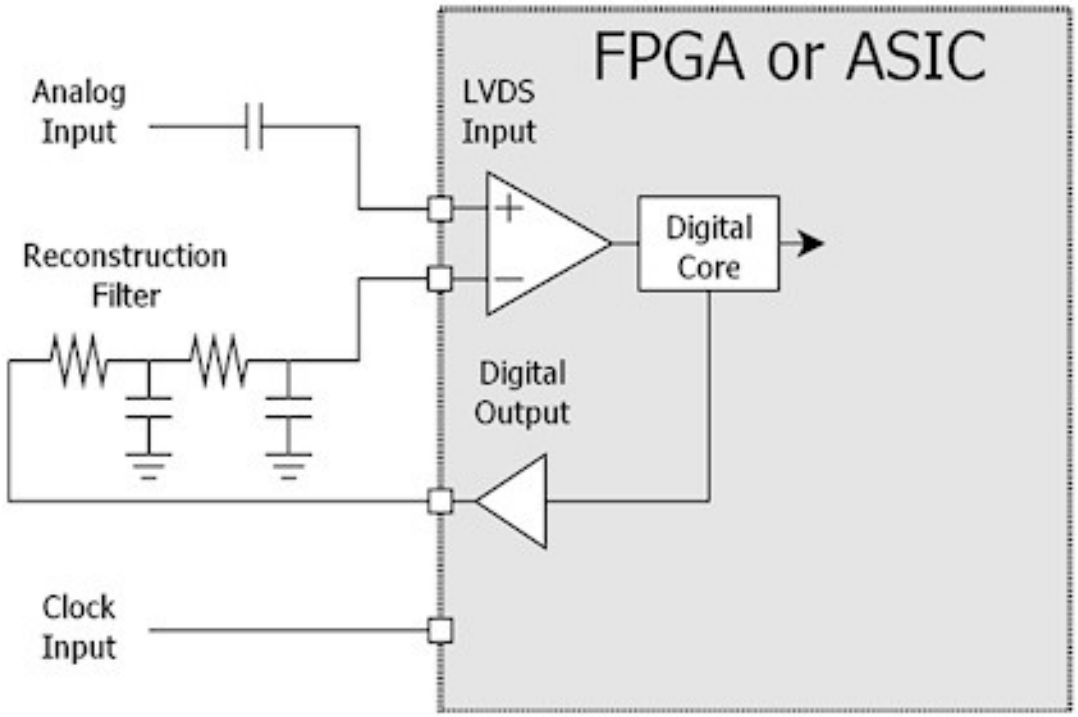




An Aside: Interface "Tricks"



http://en.wikipedia.org/wiki/Low-voltage_differential_signaling



- "All-Digital" ADC
  - e.g. 11 bits resolution 20 kHz bandwidth
  - 14 bits over 500 Hz (≅ 61µV with 1V reference)
    - http://www.stellamar.com/products.shtml#adc

Another Aside: Effect of Description on Performance

- Case study – two description styles
  1. Merged synchronous-combinational
  2. Separate synchronous-combinational
- Identical functional outcome
  - 15% lower delay along critical paths

```
always @(posedge System_Clock) begin
 //Counter_Preload, Restart_Counter, Cycle_Counter
      case(trigger)
      2'b00: begin //continue, nothing found
         Restart_Counter <= 1'b0;
         Counter_Preload <= Counter_Preload;
      end
      2'b01: begin //edge found inc/dec counter preload
                           Restart_Counter <= 1'b1;
//always queue counter to edge.
                           Cycle_Counter <= 1'b0;
      if(!Cycle_Counter) begin
// edge found but counter unfinished.
         if (Counter_Preload > Pre_Low)
            Counter_Preload <= Counter_Preload - 1;
         else
            Counter_Preload <= Counter_Preload;
         end else begin
            if (Counter_Preload < Pre_High)
               Counter_Preload <= Counter_Preload + 1;
            else
               Counter_Preload <= Counter_Preload;
         end
   end
```

```
2'b10: begin
//counterOVF
//inc count start counter again
   Cycle_Counter <= Cycle_Counter + 1;
   Restart_Counter <= 1'b1;
 Counter_Preload <= Counter_Preload;
end
2'b11: begin
//countinue, clocks synced
      Restart_Counter <= 1'b1;
      Counter_Preload <=
Counter_Preload;
  end
Endcase
```

Timing Result:

37MHz

```
    wire [9:0] SDMCountInc;
    wire [9:0] SDMCountDec;
    wire [9:0] preloadSEL;
    wire [9:0] counterPreLoadIn;
    wire resetCycleCountIn;

    always @(posedge System_Clock) begin
            Counter_Preload <= counterPreLoadIn;
            ResetCycleCounter <= resetCycleCountIn;
    end

    assign preloadLow = (Counter_Preload < Pre_Low);
    assign preloadHigh = (Counter_Preload > Pre_High);
    assign SDMCountDec = (preloadLow)? Pre_Low :Counter_Preload - 1;
    assign SDMCountInc = (preloadHigh)? Pre_High :Counter_Preload + 1;
    assign preloadSEL = (!Cycle_Counter)? SDMCountDec: (Cycle_Counter == 1)? SDMCountInc:
preloadSEL;
    assign counterPreLoadIn = (edgeFound_assessPreload)? preloadSEL:counterPreLoadIn;
    assign resetCycleCountIn = (edgeFound_assessPreload)? 1'b1: 1'b0;
```

Clocked components

Combinational components

Timing Result: 43MHz

Summary

- Meeting Performance, Time to Market and Cost targets has tended to mean a micro-processor implementation, BUT…
- FPGA devices are becoming small, low power and mixed signal
- As long as hardware parallelism is available then performance can be many times better than DSP
- Added bonus of flexibility
- Still have to be careful about description style

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Some FPGA Applications and Trends in Advanced System On Chip

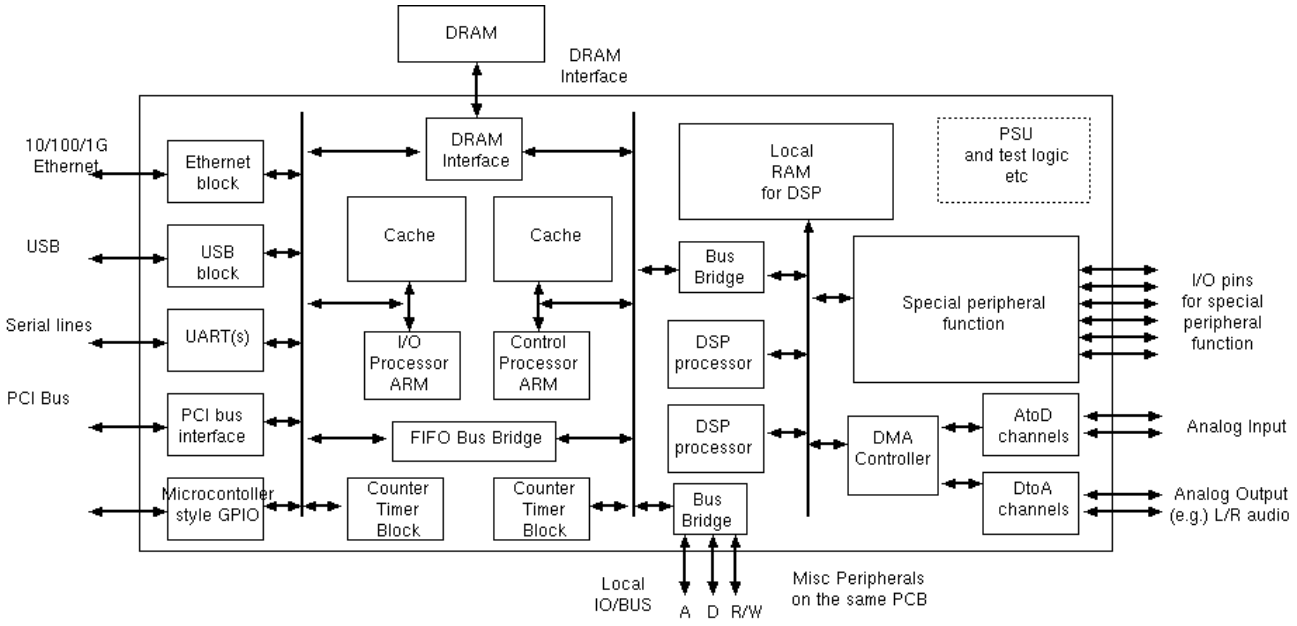
Take a short break (5 minutes)

Outline of Presentation
(2) SoC Trends

- What is a SoC?
- Future Trend Drivers
- Current SoC tools
- 3D Chip stacking
- Conclusions

Scope

- Recent SoC trends
- 3D Hardware Trends
- Design abstractions for SoC models



Definition:
A "system" includes a microprocessor, memory and peripherals.

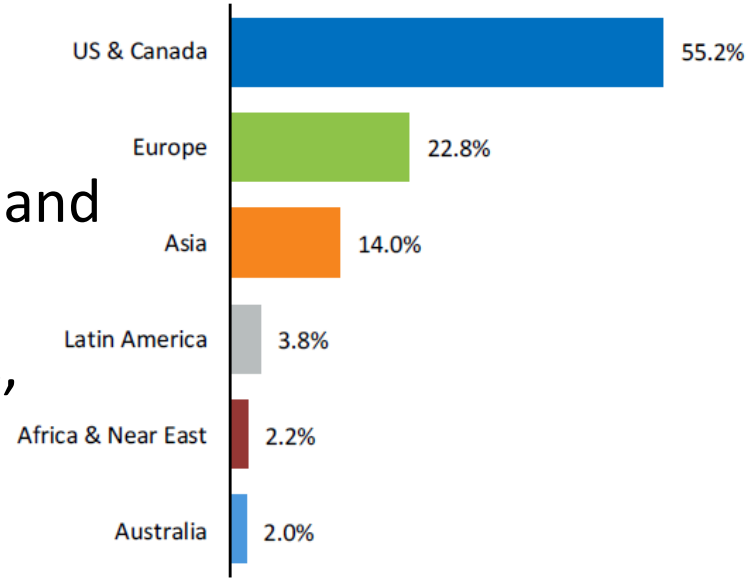
Caveat

- “It's tough to make predictions, especially about the future.”

  Yogi Berra (b. 1925),
  former American Major League Baseball catcher, outfielder, and manager.

Trends: UBM Tech®
2014 Embedded Market Study

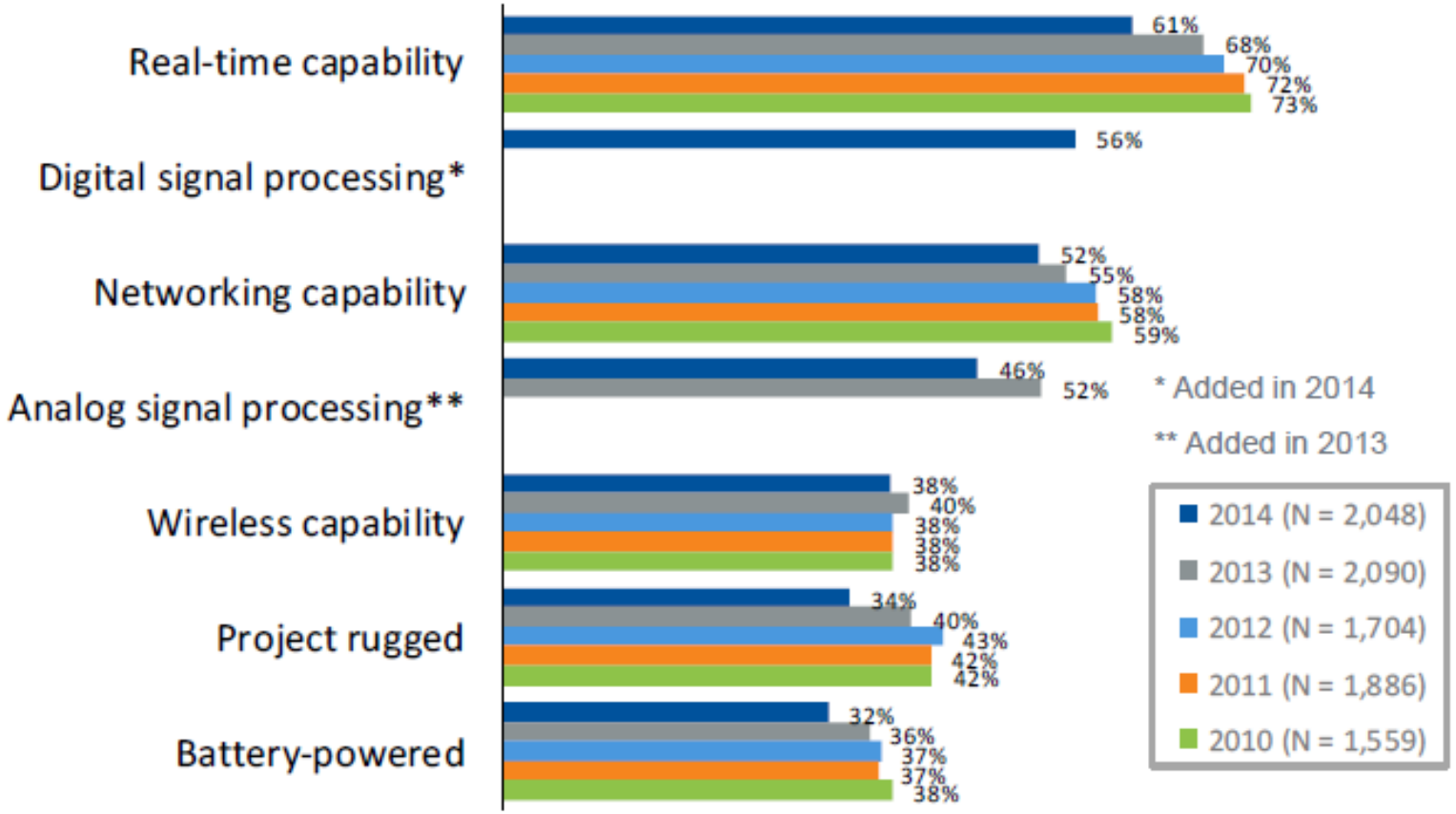
- UBM Tech (embedded magazine)
  - conducts annual **online** survey of worldwide embedded systems markets
    - types of technology used
    - embedded development process and tools,
    - applications, methods/ processes,
    - operating systems
    - chips, technology and brands



  - trended over three to five years.
  - **WARNING: most focus is on United States**
  - http://**bd.eduweb.hhs.nl**/es/2014-embedded-market-study-then-now-whats-next.pdf

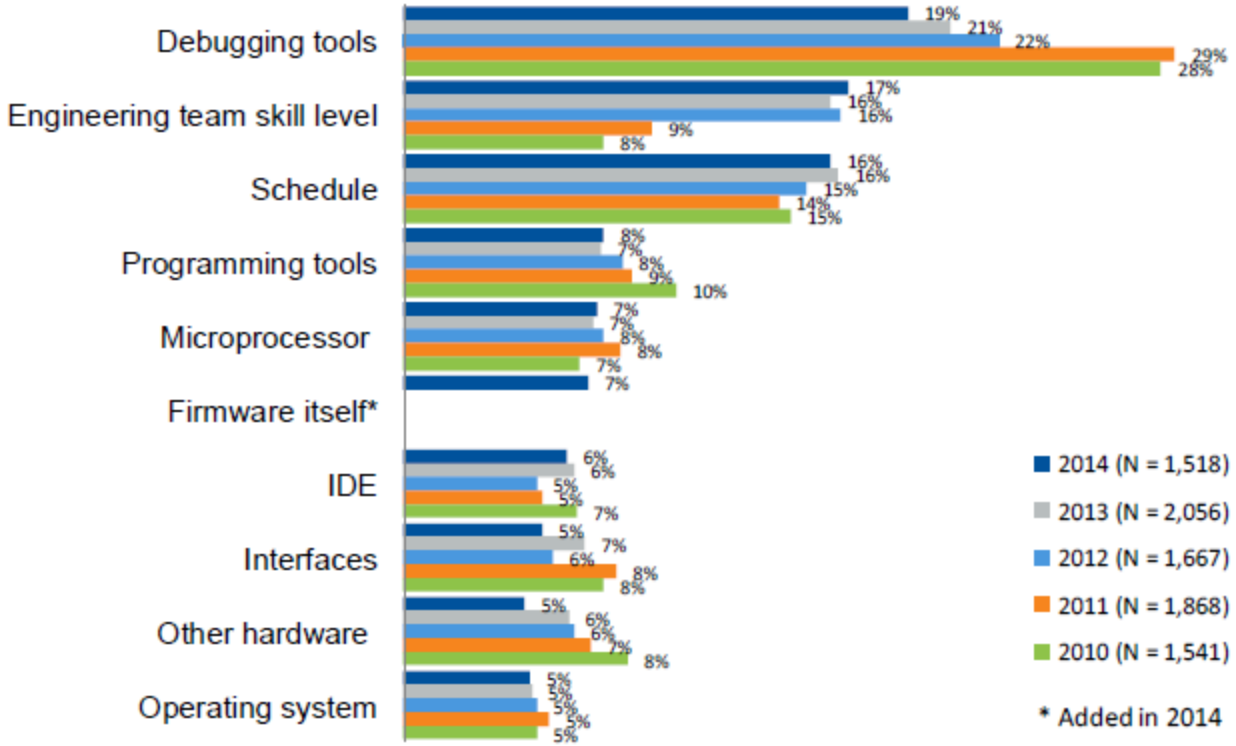
2014 Embedded Market Study

- Important Embedded System Capabilities



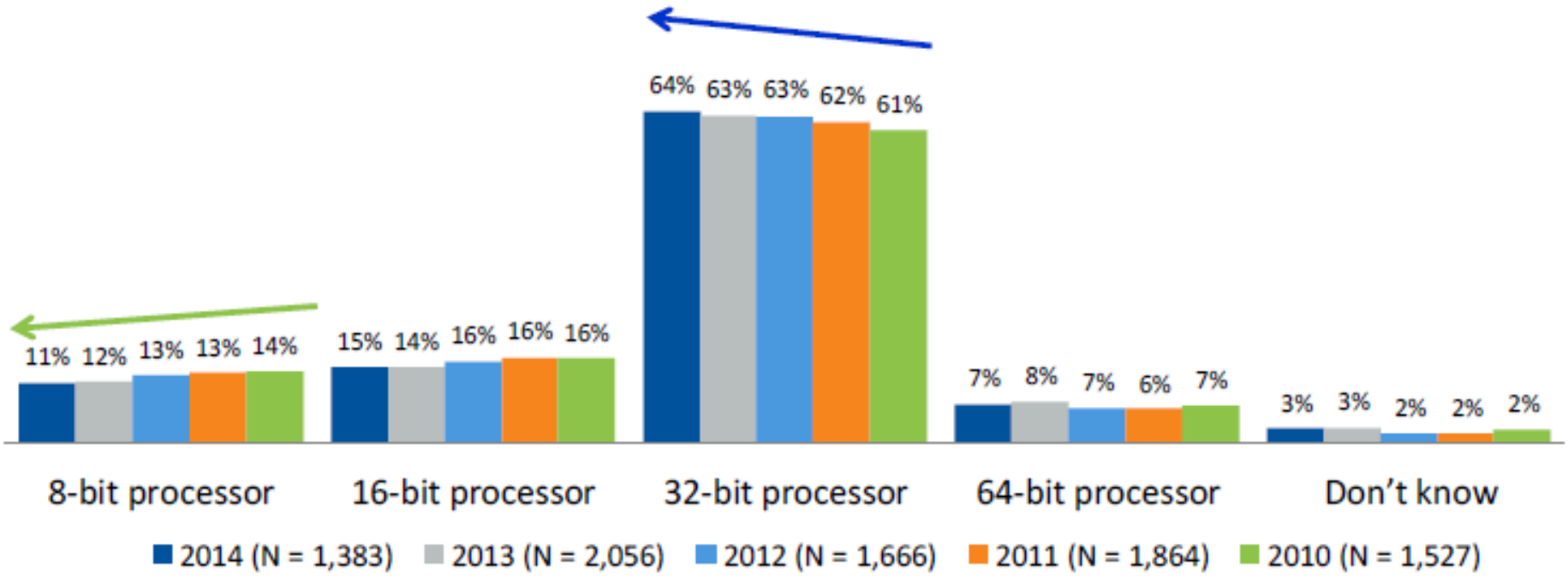
2014 Embedded Market Study

- If you could improve one thing about your embedded design activities, what would it be?



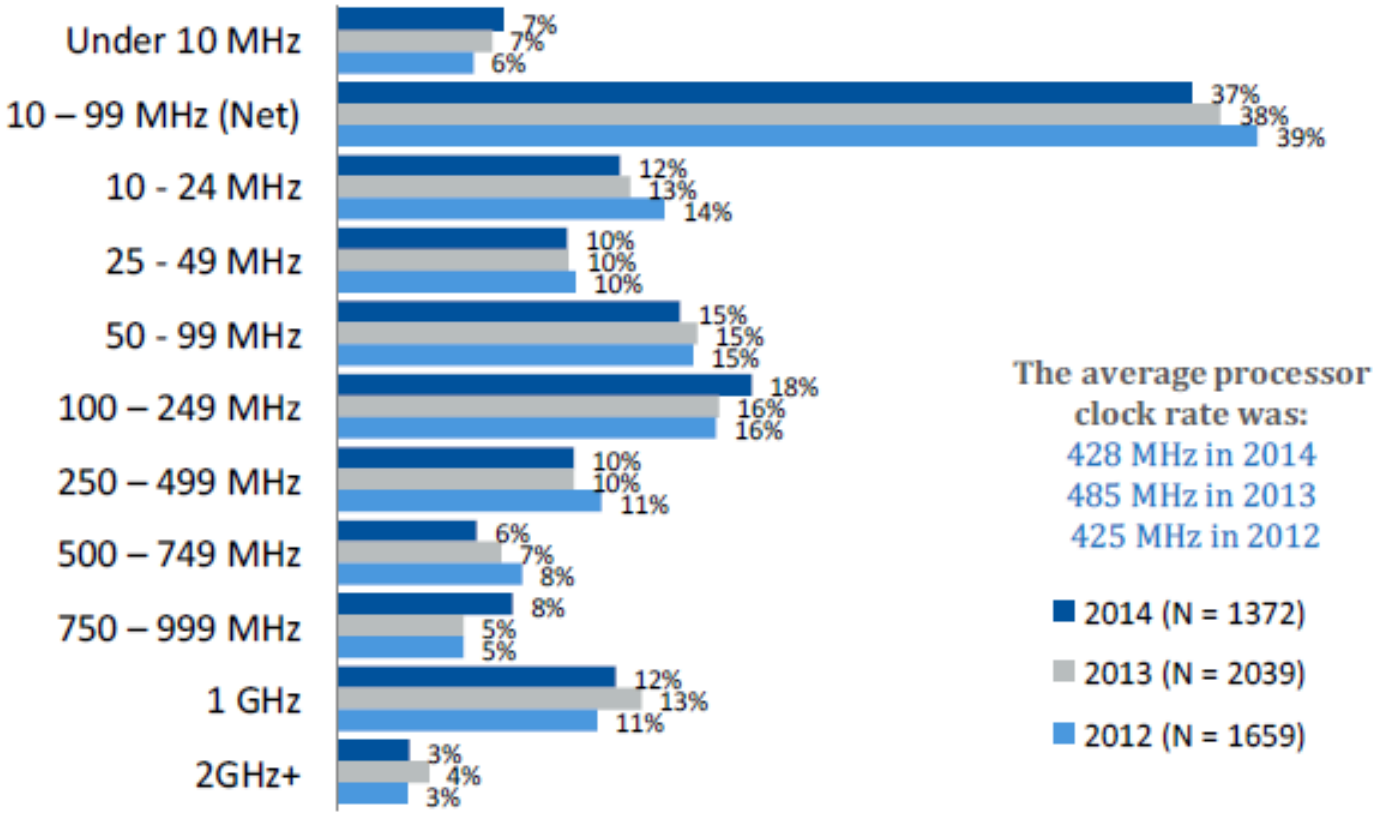
2014 Embedded Market Study

- current main processor size:



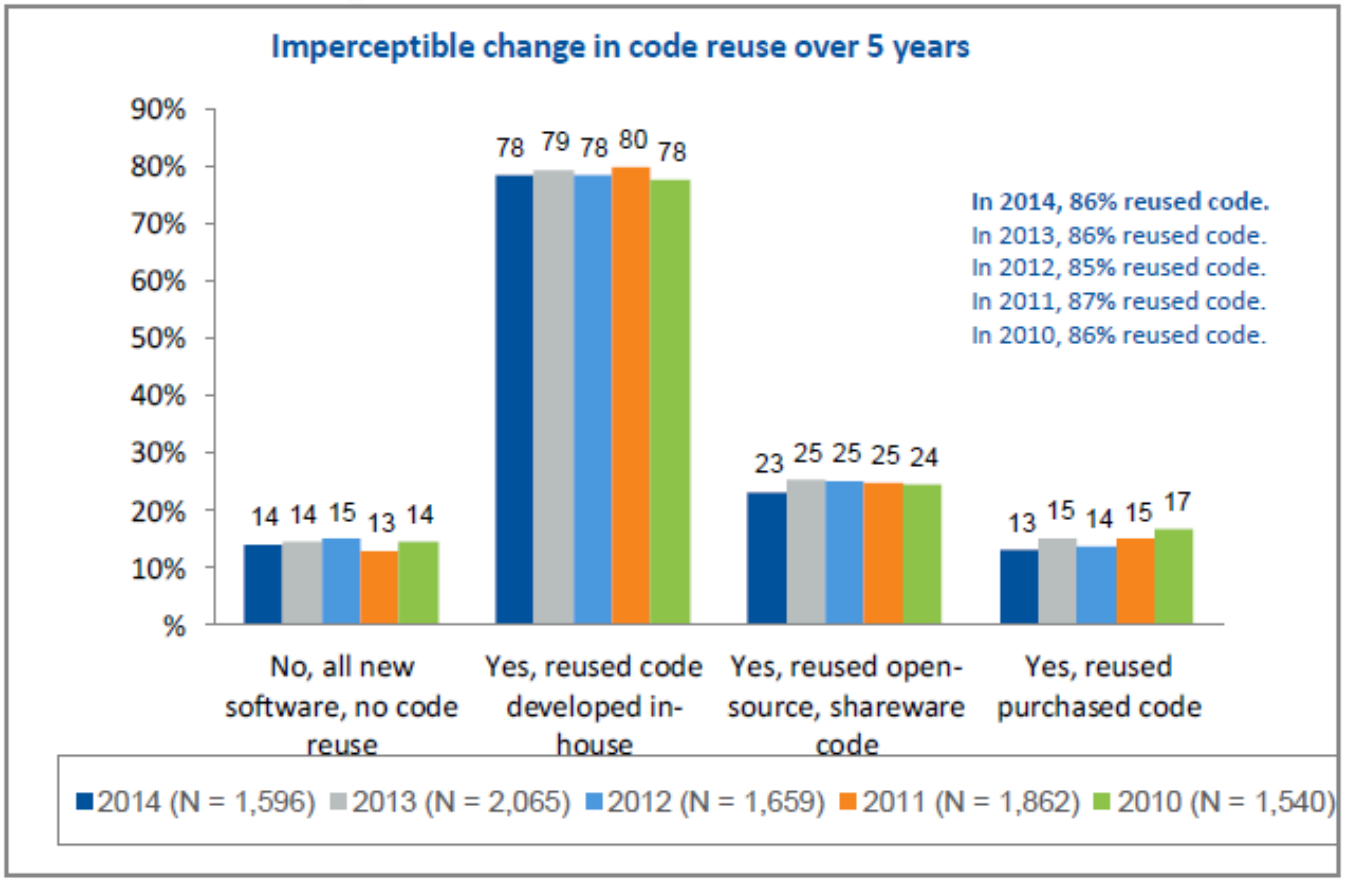
2014 Embedded Market Study

- current main processor clock rate:



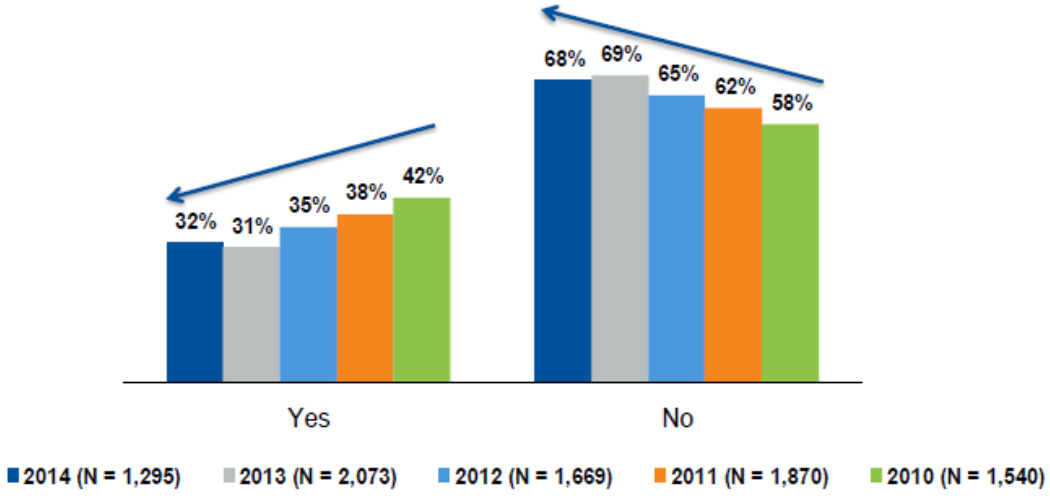
2014 Embedded Market Study

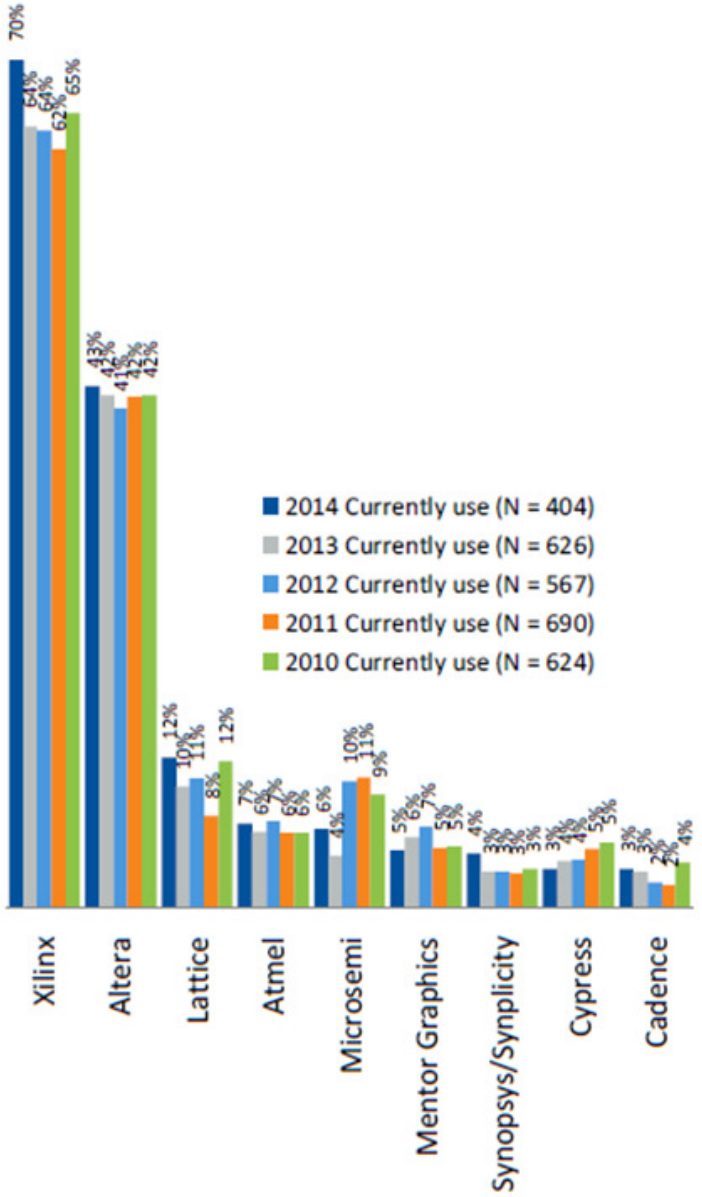
- Do you reuse code?



2014 Embedded Market Study

- Does current design use programmable logic?
- If so, which vendor?



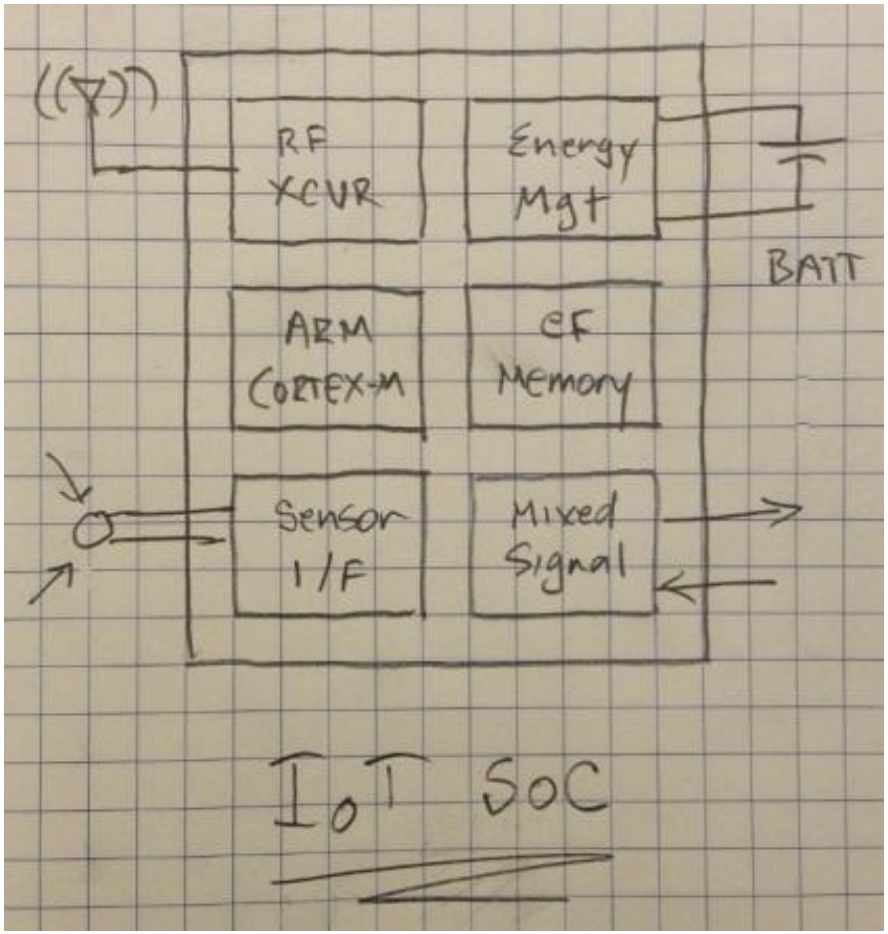


2014 Embedded Market Study

- Programmable Logic: Key Messages
  - FPGA usage is trending steadily downward
    - 45% six years ago to 32% this year.
    - may indicate a pause in the trend
  - Gradual decline of FPGAs/programmable logic usage in **upcoming** embedded projects:
    - 60% said “yes” in 2005, down to 41% in 2014
  - Not needing the functionality, cost and difficulty programming are the main reasons for not using customizable chips/FPGAs.

Future Drivers - the IoT?

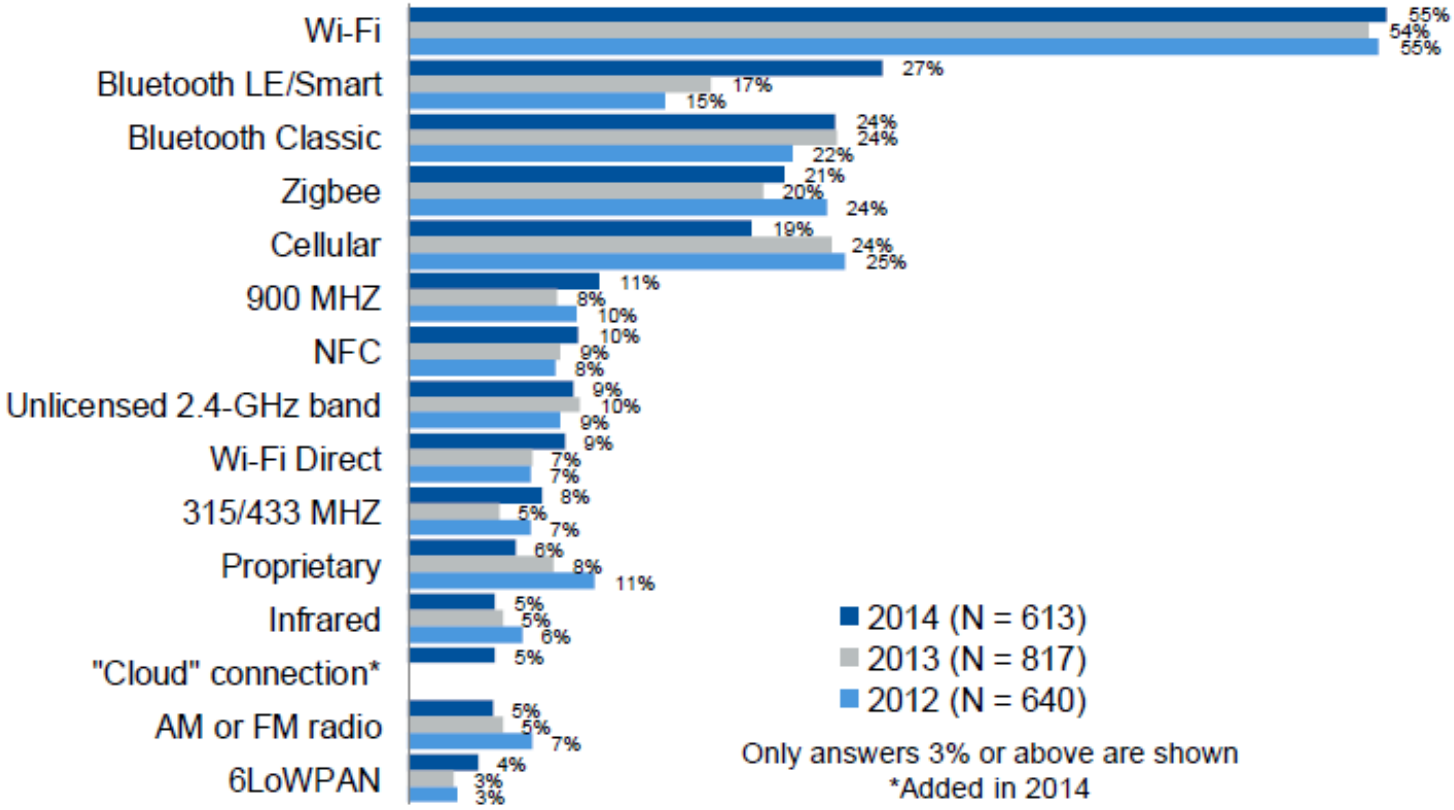
- Sensor interface
- low-energy microcontrollers
  - 8 – 32 bit
- wireless technology
  - ZigBee
  - 802.15.4 (various flavors)
  - Bluetooth low-energy solution (BLE)
  - proprietary standards
- Energy management
- memory



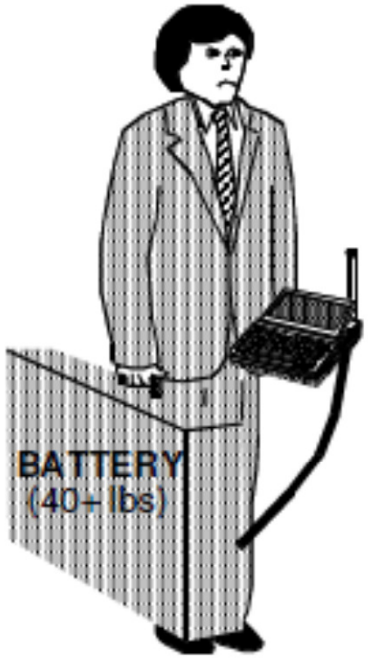
Source: http://www.eetimes.com/document.asp?doc_id=1321706

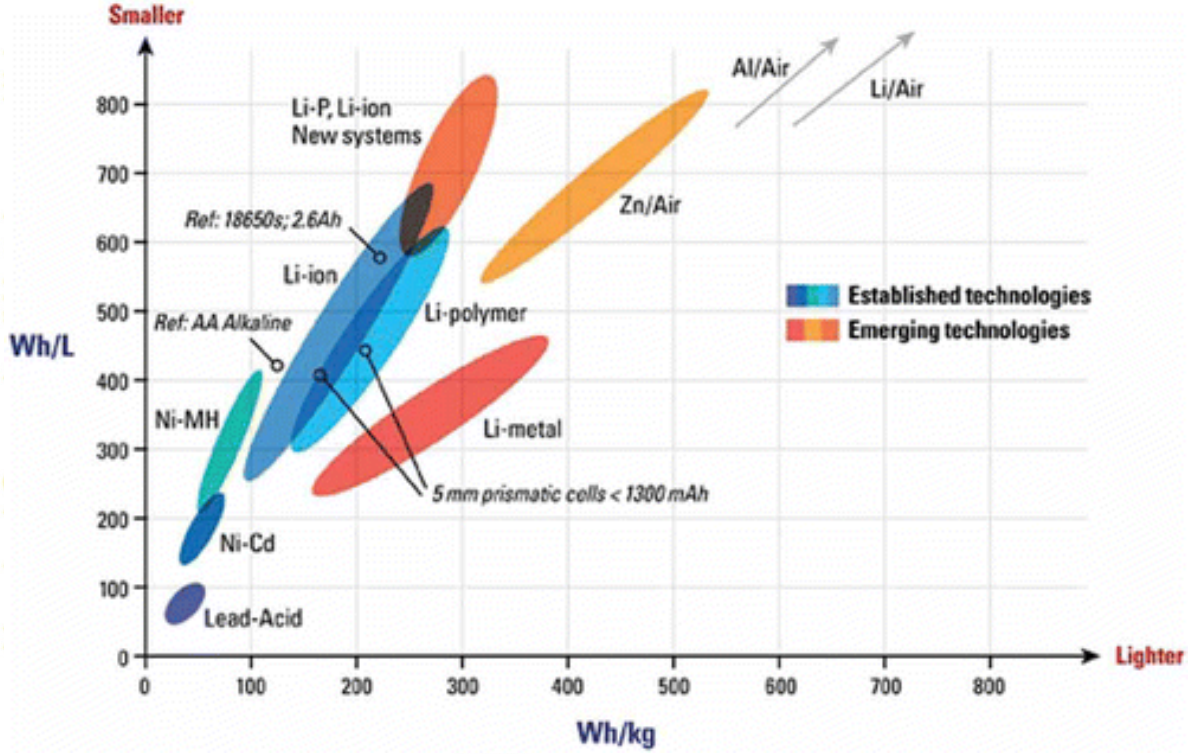
2014 Embedded Market Study

- Wireless Designs



Future Drivers - Energy





Multimedia Terminals

Laptop Computers

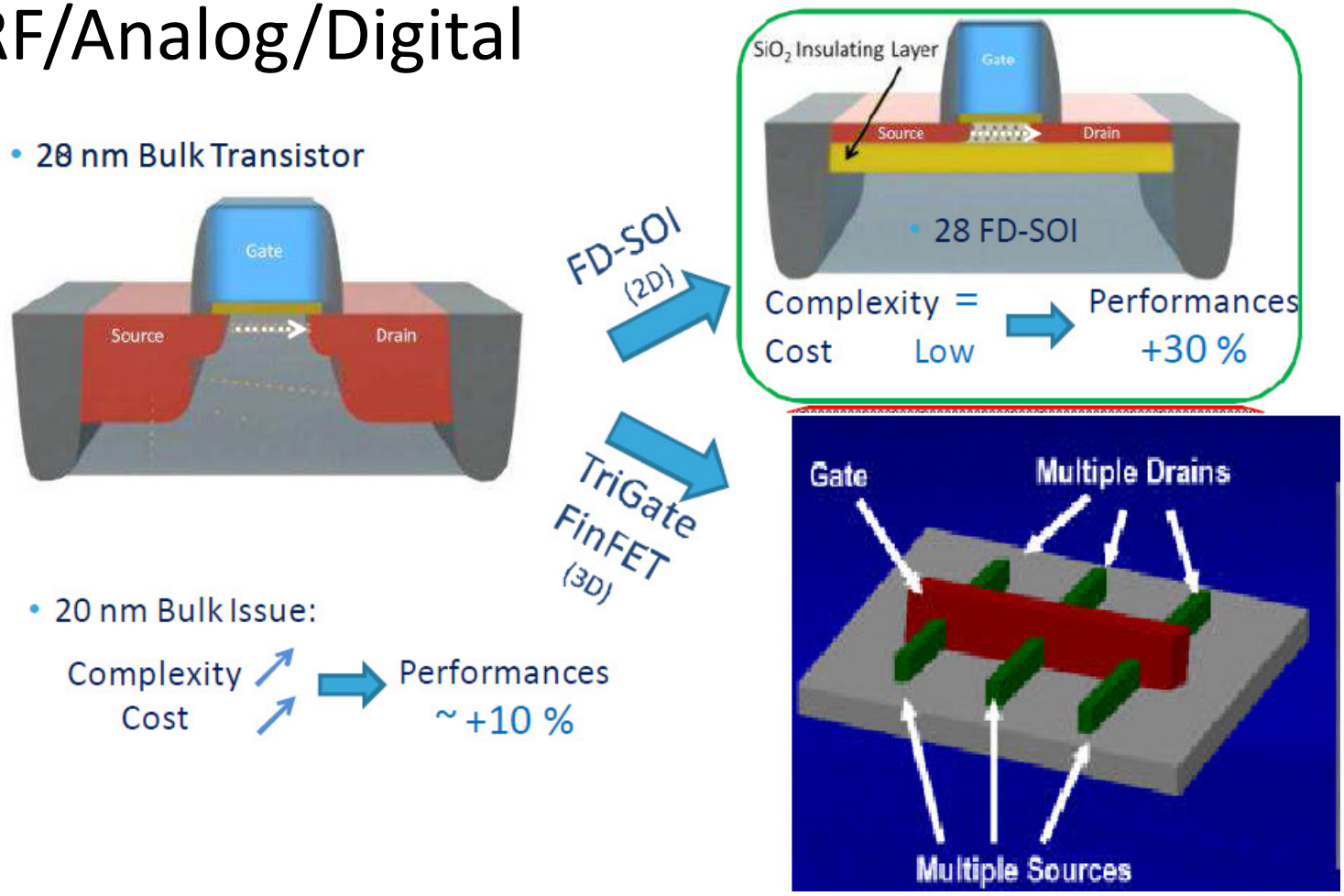
Digital Cellular Telephony

Expected Battery Lifetime increase over next 5 years: 30-40%

Portability

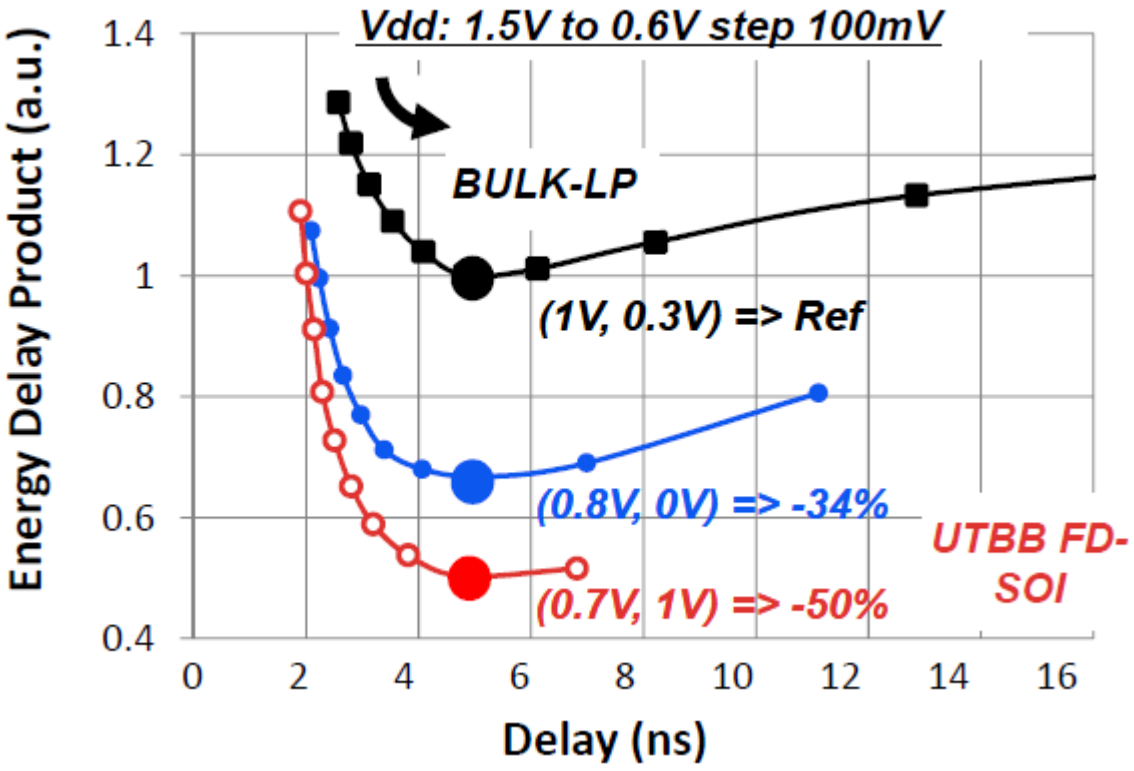
Future Drivers - Technology

- Mixed RF/Analog/Digital



Future Drivers - Technology

- UTBB-FDSOI - Energy Efficiency

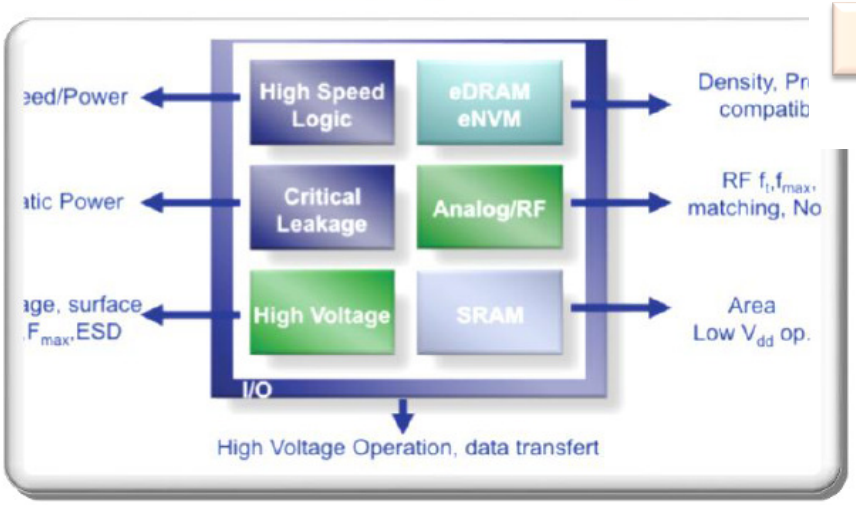


Future Drivers – 3D Packaging

- 3D Stacking Technology

2D SOC

"All-in-One chip system integration"



All functions on 28nm lithography

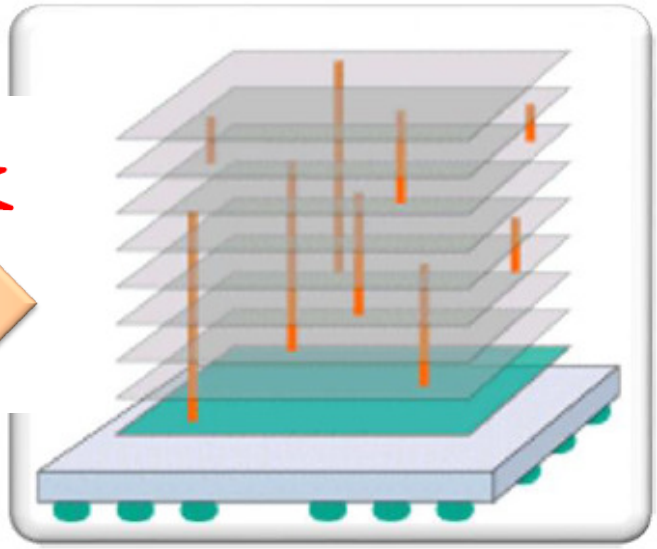
→ Chip area ↑, Cost ↑

2.5D?

Evolution or Revolution?

3DIC / 3D SoC

"De-integrated & Re-integrated SOC"

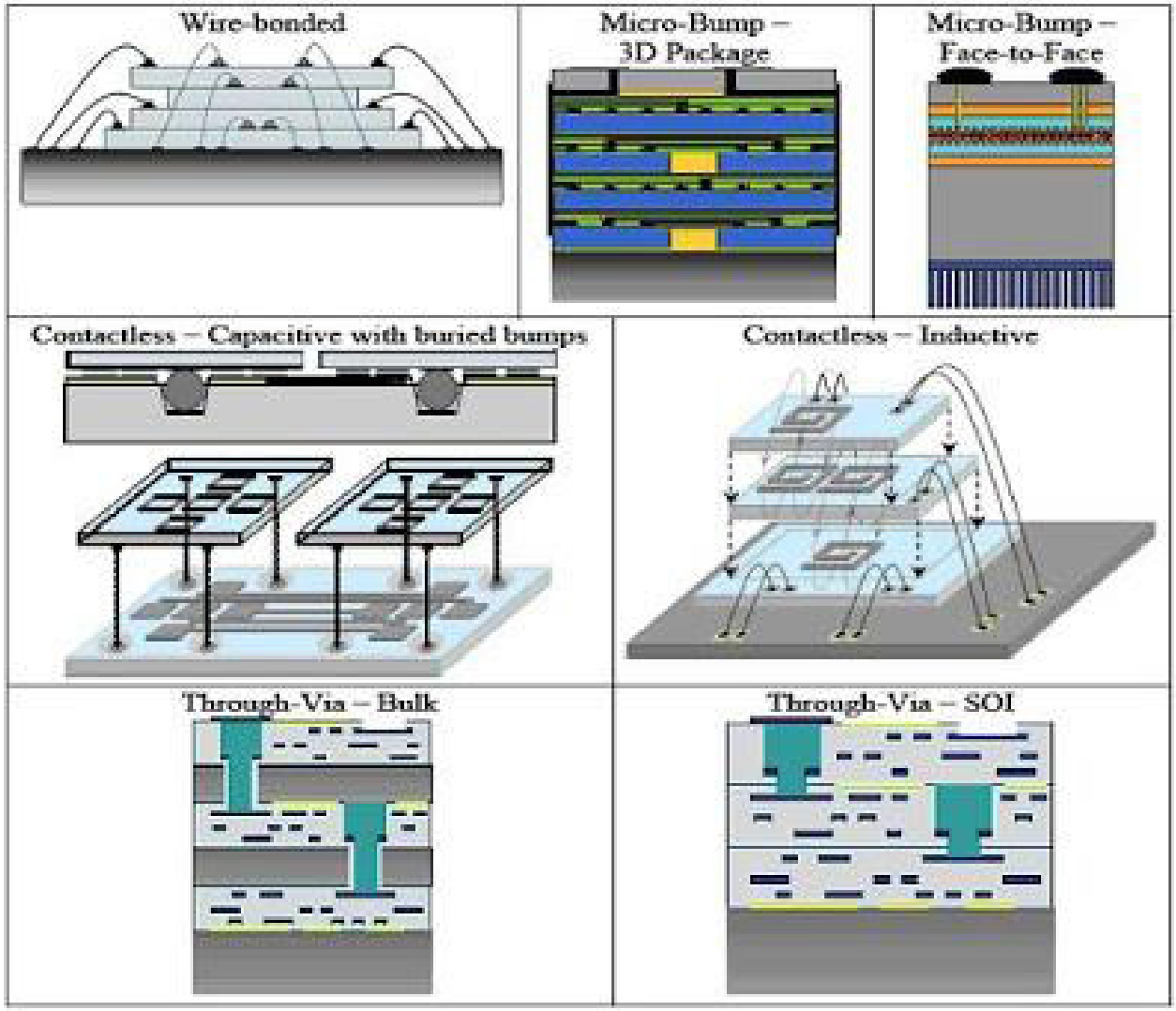


MEMS	130 nm	200 mm
Memory	45 nm	300 mm
Logic	22 nm ?	450 mm ?
Analog	90 nm	300 mm

Source: Yole, 2.5D, 3DIC & TSV Interconnects Patent Analysis, May 2013

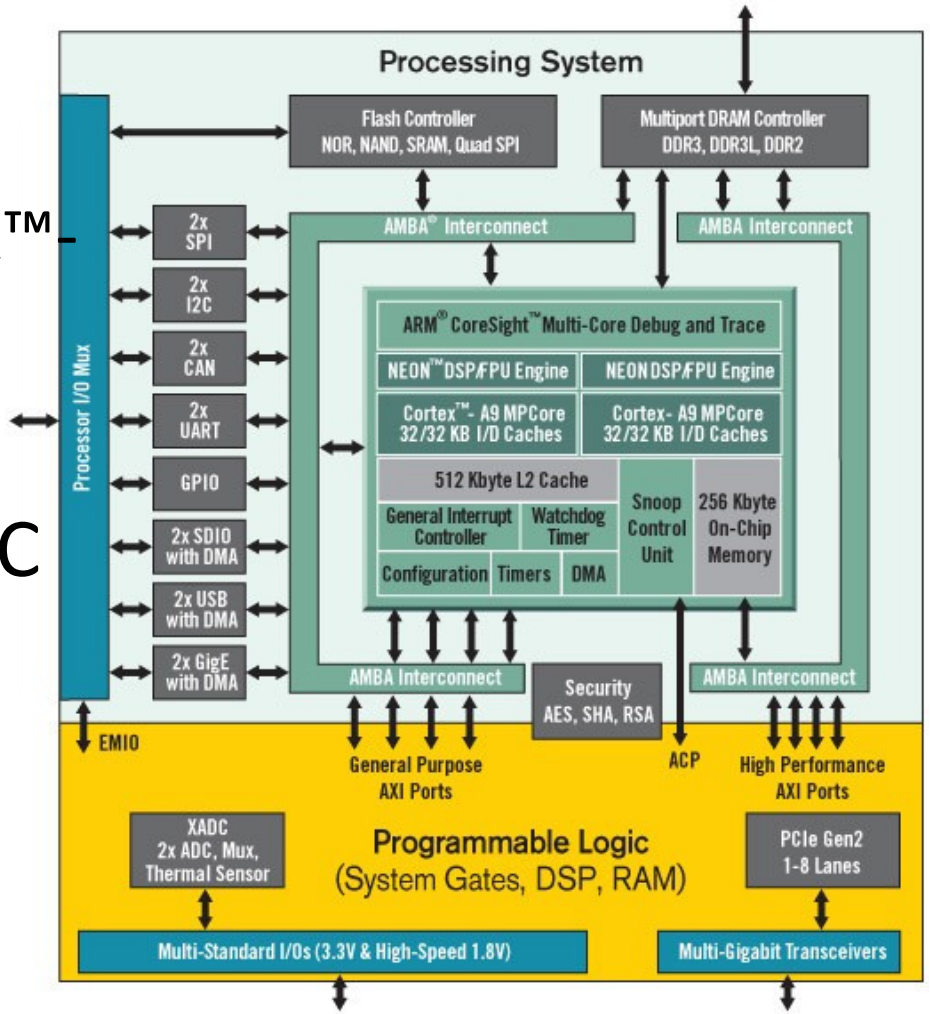
Future Drivers – 3D

- 3D stacking methods

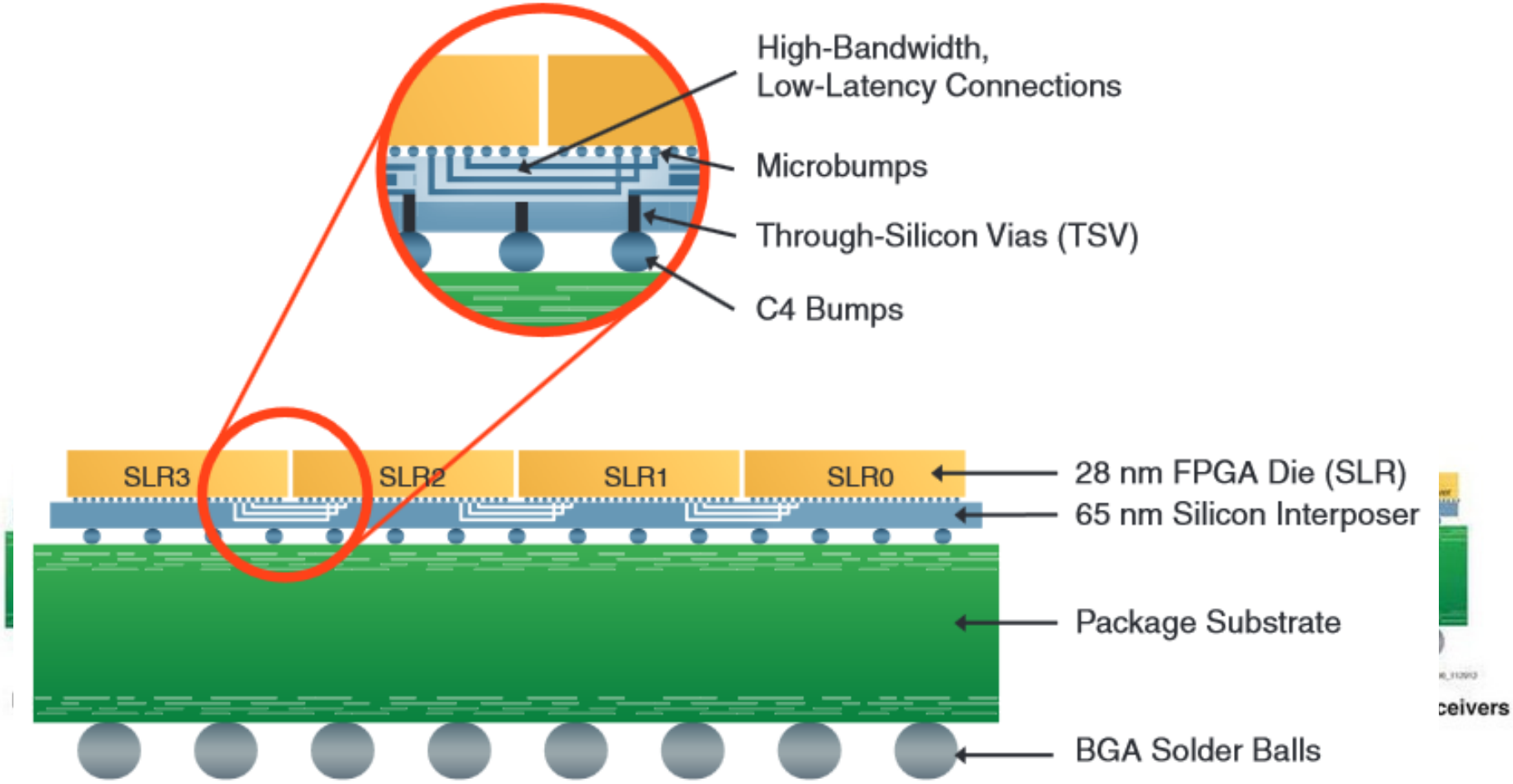


Recent Examples - Xilinx

- Zynq-7000
  - ARM® dual-core Cortex™-A9 processors
  - Programmable logic
- Zynq UltraScale+ MPSoC
  - Quad-core Cortex A53
  - Peripherals
  - Programmable Logic



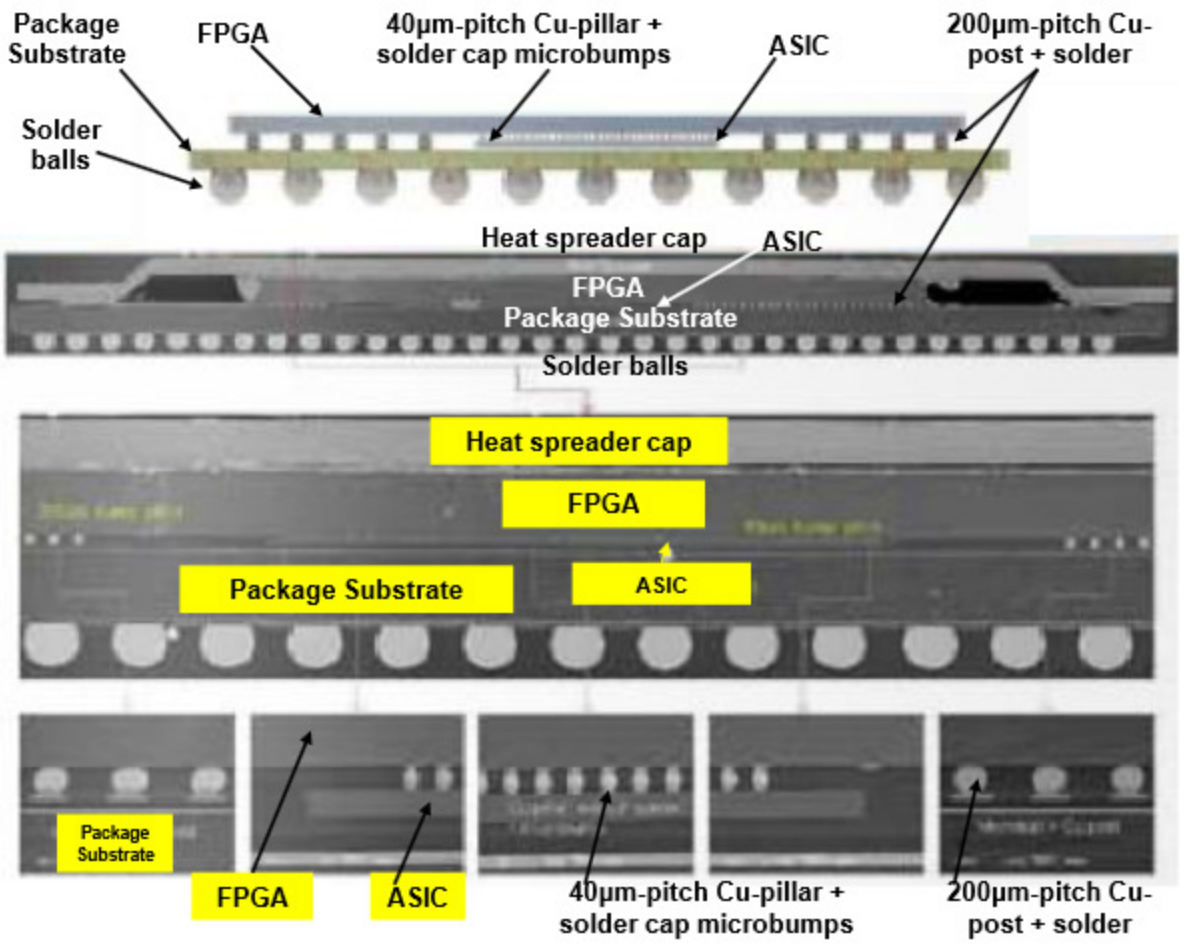
Recent Examples - Xilinx



Source: http://www.xilinx.com/products/silicon-devices/3dic.html

Recent Examples - Altera

- *AMCOR "POSSUM" process*
  - *multi-stacked die without TSVs*
  - *daughter die mounted face to face with mother die then mounted onto a substrate*

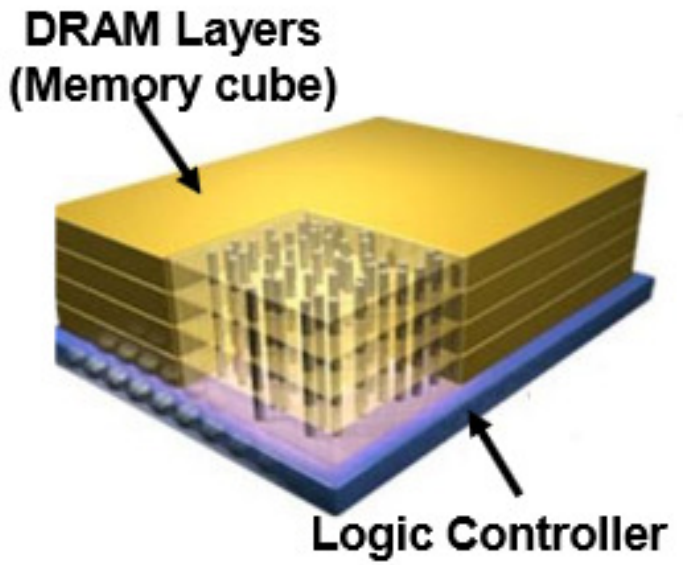


Source: http://s3.amazonaws.com/sdieee/1817-SanDiego CPMTDL_Lau_advancedpackaging.pdf

Hybrid Memory Cube (HMC)

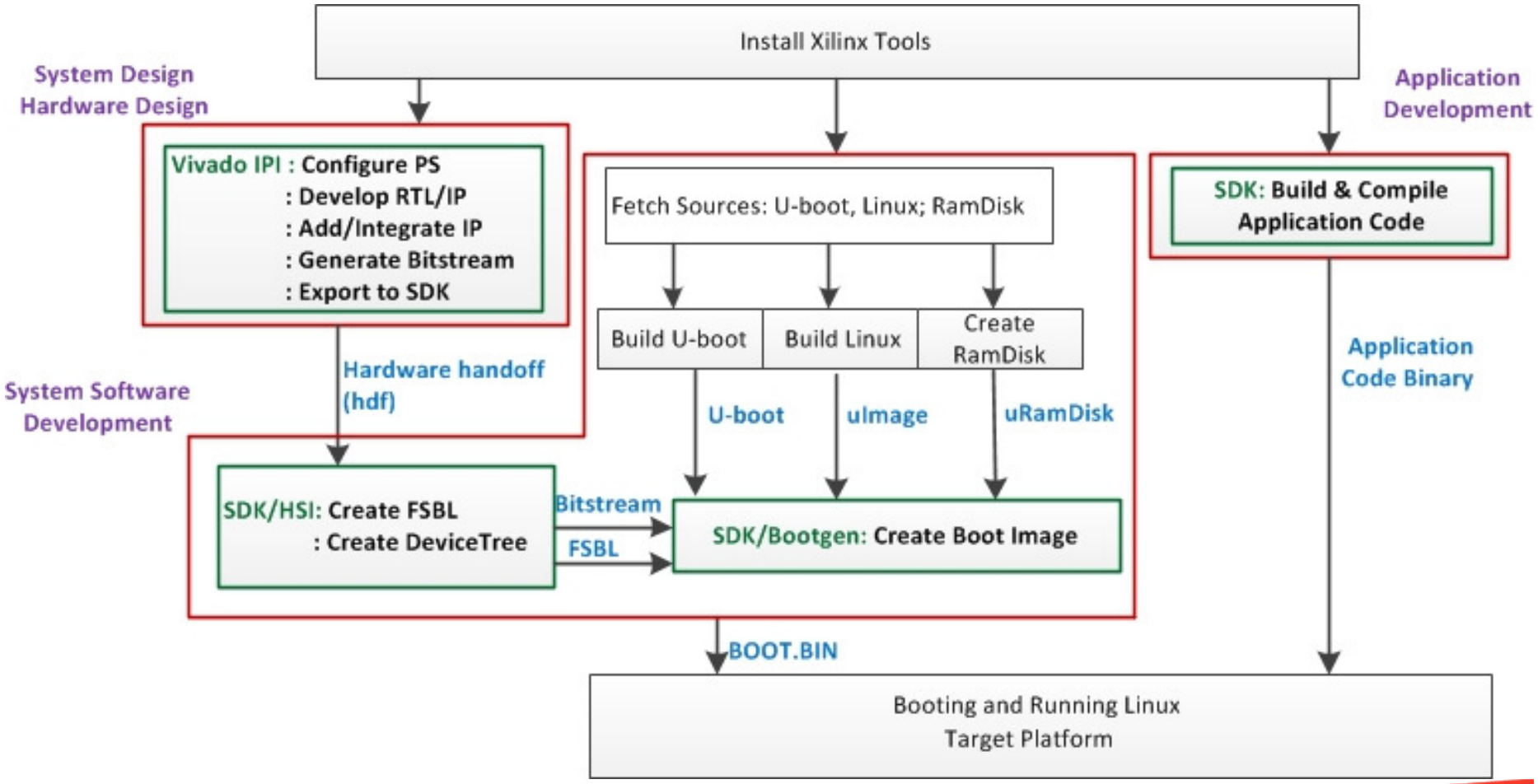
The HMC consortium already has 8 members:

- Micron
- Samsung
- Altera
- ARM
- IBM
- Open-Silicon
- SK Hynix
- Xilinx

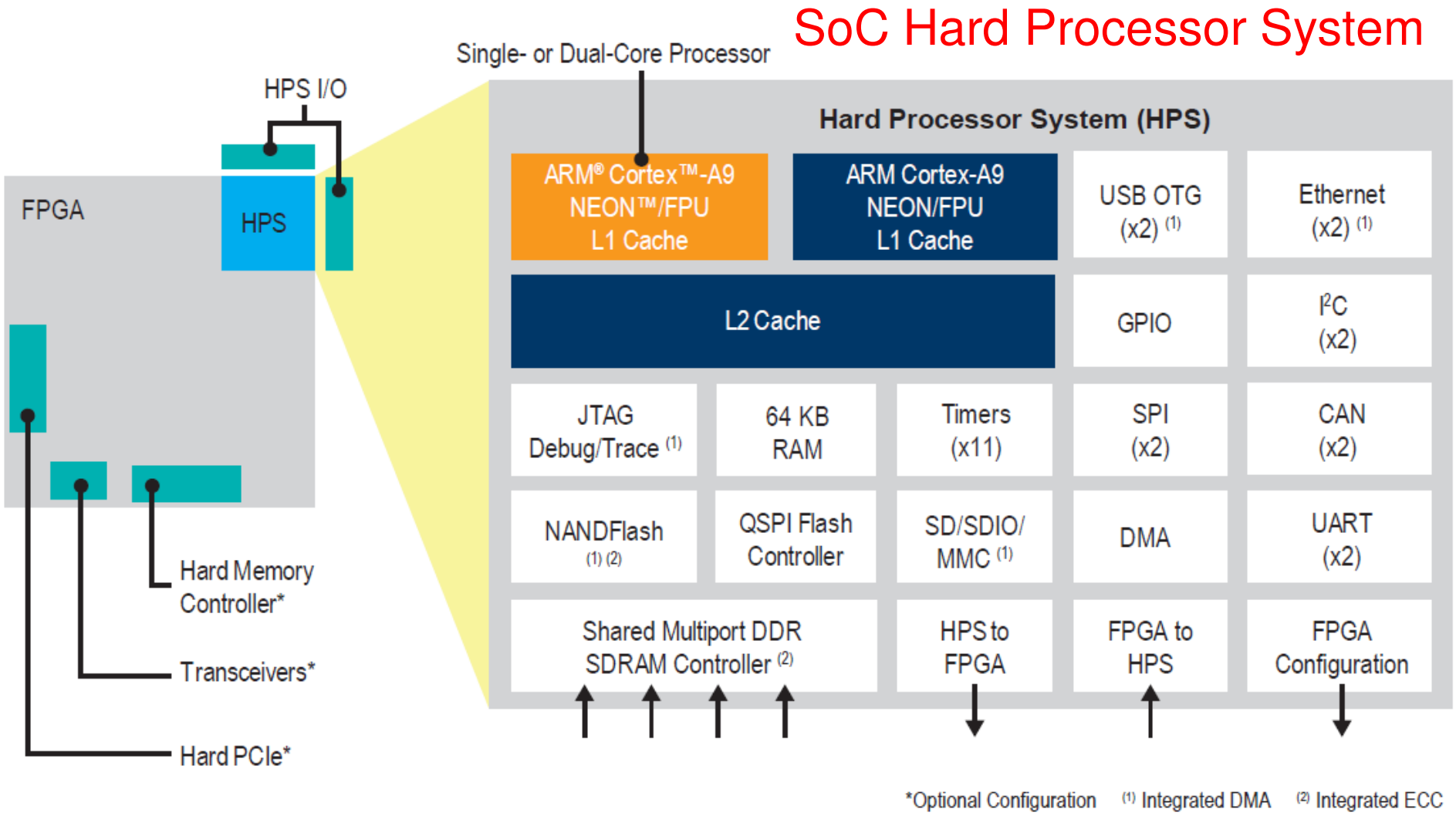


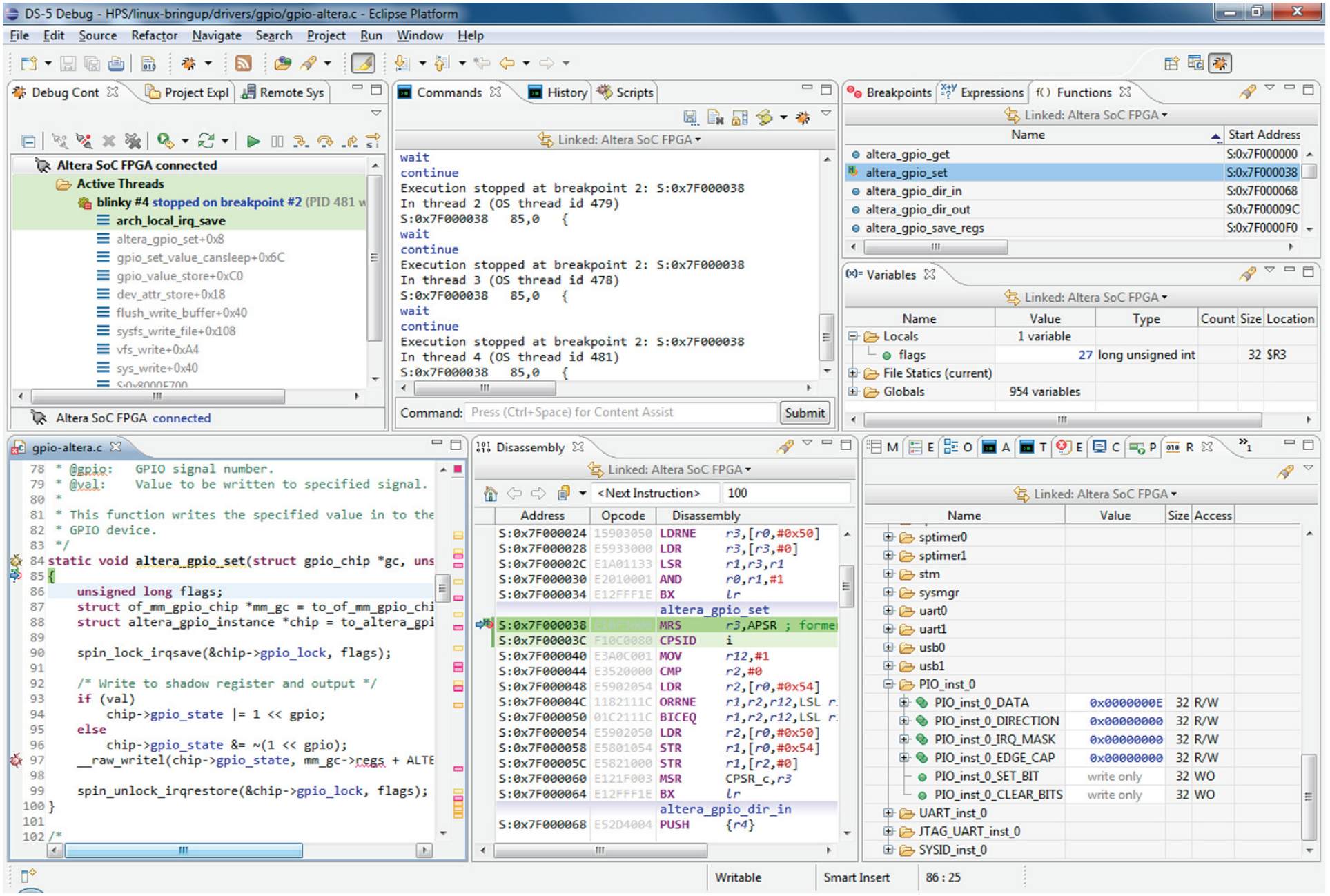
Source: http://s3.amazonaws.com/sdieee/1817-SanDiegoCPMTDL_Lau_advancedpackaging.pdf

Xilinx Design Flow



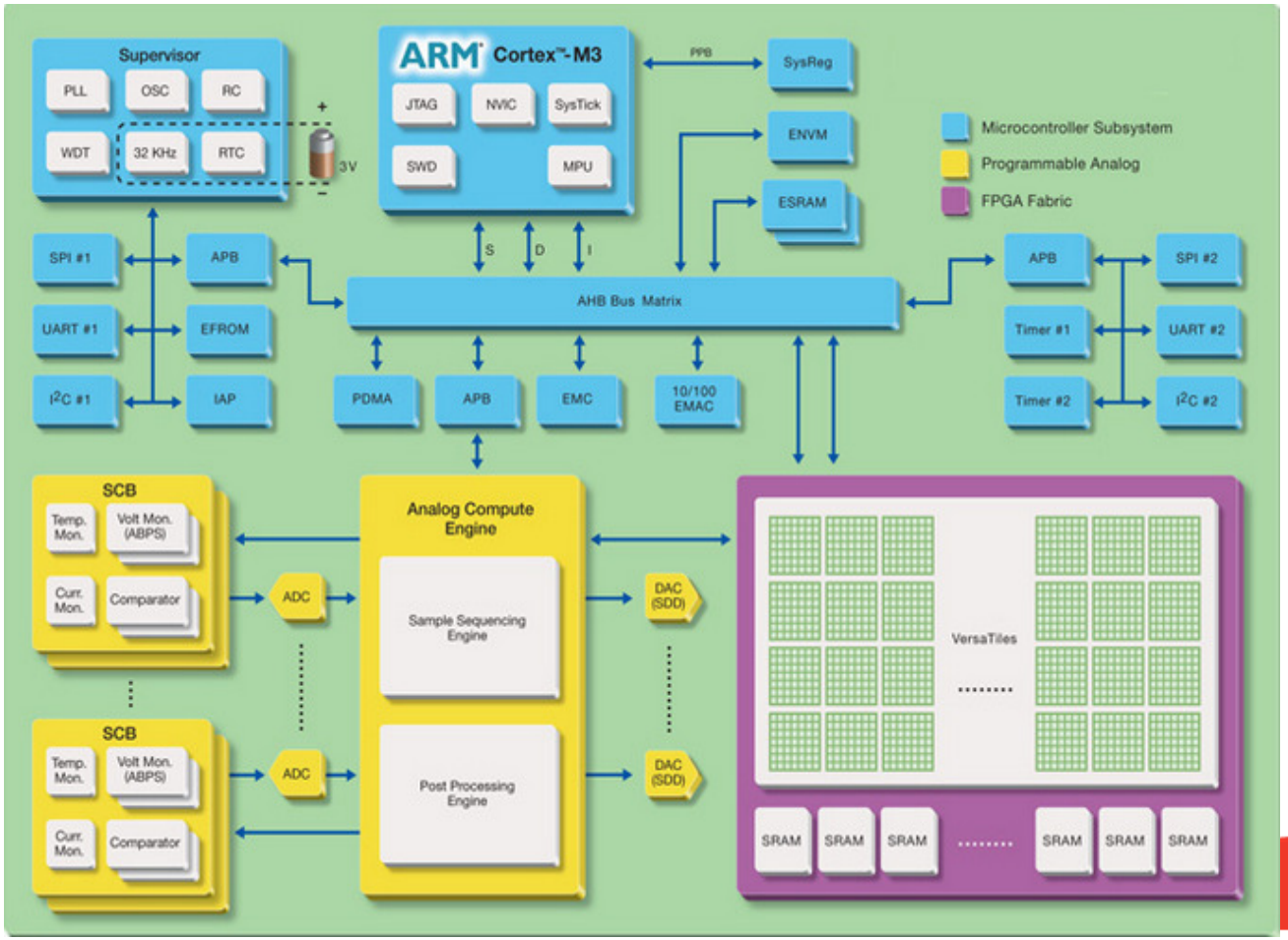
Recent Examples - Altera




DS-5 Debug - HPS/linux-bringup/drivers/gpio/gpio-altera.c - Eclipse Platform
File Edit Source Refactor Navigate Search Project Run Window Help
Debug Cont
Project Expl
Remote Sys
Altera SoC FPGA connected
Active Threads
blinky #4 stopped on breakpoint #2 (PID 481
arch_local_irq_save
altera_gpio_set+0x8
gpio_set_value_cansleep+0x6C
gpio_value_store+0xC0
dev_attr_store+0x18
flush_write_buffer+0x40
sysfs_write_file+0x108
vfs_write+0xA4
sys_write+0x40
Altera SoC FPGA connected
Commands
History
Scripts
Linked: Altera SoC FPGA
wait
continue
Execution stopped at breakpoint 2: S:0x7F000038
In thread 2 (OS thread id 479)
S:0x7F000038 85,0 {
wait
continue
Execution stopped at breakpoint 2: S:0x7F000038
In thread 3 (OS thread id 478)
S:0x7F000038 85,0 {
wait
continue
Execution stopped at breakpoint 2: S:0x7F000038
In thread 4 (OS thread id 481)
S:0x7F000038 85,0 {
Command: Press (Ctrl+Space) for Content Assist
Submit
Breakpoints
Expressions
Functions
Linked: Altera SoC FPGA
Name
Start Address
altera_gpio_get S:0x7F000000
altera_gpio_set S:0x7F000038
altera_gpio_dir_in S:0x7F000068
altera_gpio_dir_out S:0x7F00009C
altera_gpio_save_regs S:0x7F0000F0
Variables
Linked: Altera SoC FPGA
Name
Value
Type
Count
Size
Location
Locals
1 variable
flags
27
long unsigned int
32
$R3
File Statics (current)
Globals
954 variables
gpio-altera.c
78 * @gpio: GPIO signal number.
79 * @val: Value to be written to specified signal.
80 *
81 * This function writes the specified value in to the
82 * GPIO device.
83 */
84 static void altera_gpio_set(struct gpio_chip *gc, uns
85 {
86 unsigned long flags;
87 struct of_mm_gpio_chip *mm_gc = to_of_mm_gpio_chi
88 struct altera_gpio_instance *chip = to_altera_gpi
89
90 spin_lock_irqsave(&chip->gpio_lock, flags);
91
92 /* Write to shadow register and output */
93 if (val)
94 chip->gpio_state |= 1 << gpio;
95 else
96 chip->gpio_state &= ~(1 << gpio);
97 __raw_writel(chip->gpio_state, mm_gc->regs + ALTE
98
99 spin_unlock_irqrestore(&chip->gpio_lock, flags);
100 }
101
102 /*
Disassembly
Linked: Altera SoC FPGA
<Next Instruction>
100
Address
Opcode
Disassembly
S:0x7F000024 15903050 LDRNE r3,[r0,#0x50]
S:0x7F000028 E5933000 LDR r3,[r3,#0]
S:0x7F00002C E1A01133 LSR r1,r3,r1
S:0x7F000030 E2010001 AND r0,r1,#1
S:0x7F000034 E12FFF1E BX lr
altera_gpio_set
S:0x7F000038 E10F3000 MRS r3,APSR ; forme
S:0x7F00003C F10C0080 CPSID i
S:0x7F000040 E3A0C001 MOV r12,#1
S:0x7F000044 E3520000 CMP r2,#0
S:0x7F000048 E5902054 LDR r2,[r0,#0x54]
S:0x7F00004C 1182111C ORRNE r1,r2,r12,LSL r
S:0x7F000050 01C2111C BICEQ r1,r2,r12,LSL r
S:0x7F000054 E5902050 LDR r2,[r0,#0x50]
S:0x7F000058 E5801054 STR r1,[r0,#0x54]
S:0x7F00005C E5821000 STR r1,[r2,#0]
S:0x7F000060 E121F003 MSR CPSR_c,r3
S:0x7F000064 E12FFF1E BX lr
altera_gpio_dir_in
S:0x7F000068 E52D4004 PUSH {r4}
M E O A T E C P R
Linked: Altera SoC FPGA
Name
Value
Size
Access
sptimer0
sptimer1
stm
sysmgr
uart0
uart1
usb0
usb1
PIO_inst_0
PIO_inst_0_DATA 0x0000000E 32 R/W
PIO_inst_0_DIRECTION 0x00000000 32 R/W
PIO_inst_0_IRQ_MASK 0x00000000 32 R/W
PIO_inst_0_EDGE_CAP 0x00000000 32 R/W
PIO_inst_0_SET_BIT write only 32 WO
PIO_inst_0_CLEAR_BITS write only 32 WO
UART_inst_0
JTAG_UART_inst_0
SYSID_inst_0
Writable
Smart Insert
86 : 25

Recent Examples - MicroSemi

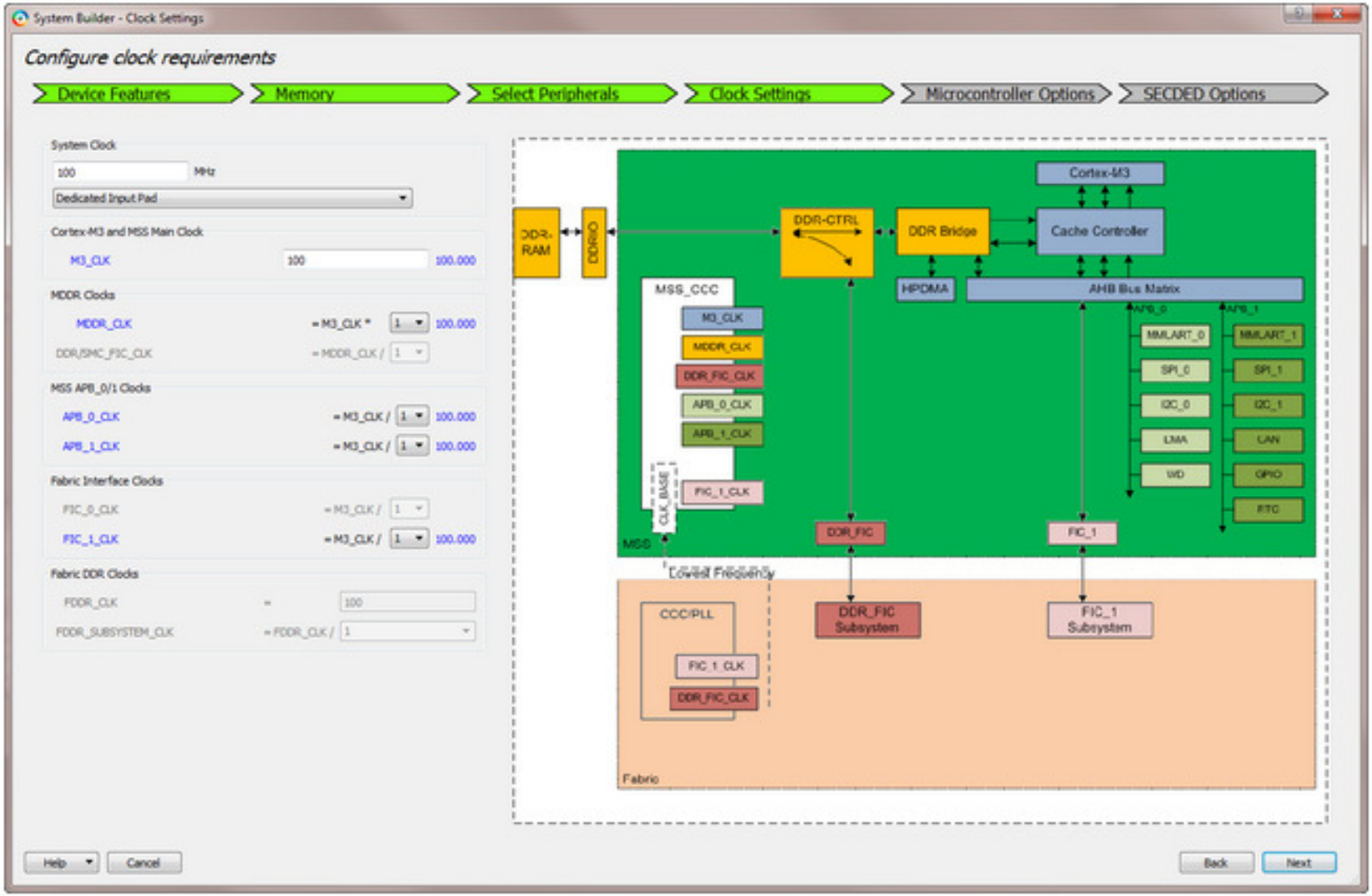
SmartFusion System-on-Chip FPGA



- Hard 32-bit ARM Cortex-M3 microcontroller
- Programmable analog
  - ADC/DAC
  - Comparators
  - Analog computation
- voltage/current/ temperature monitors,
- FPGA fabric

Libero® SoC

System Builder



Some Final Words

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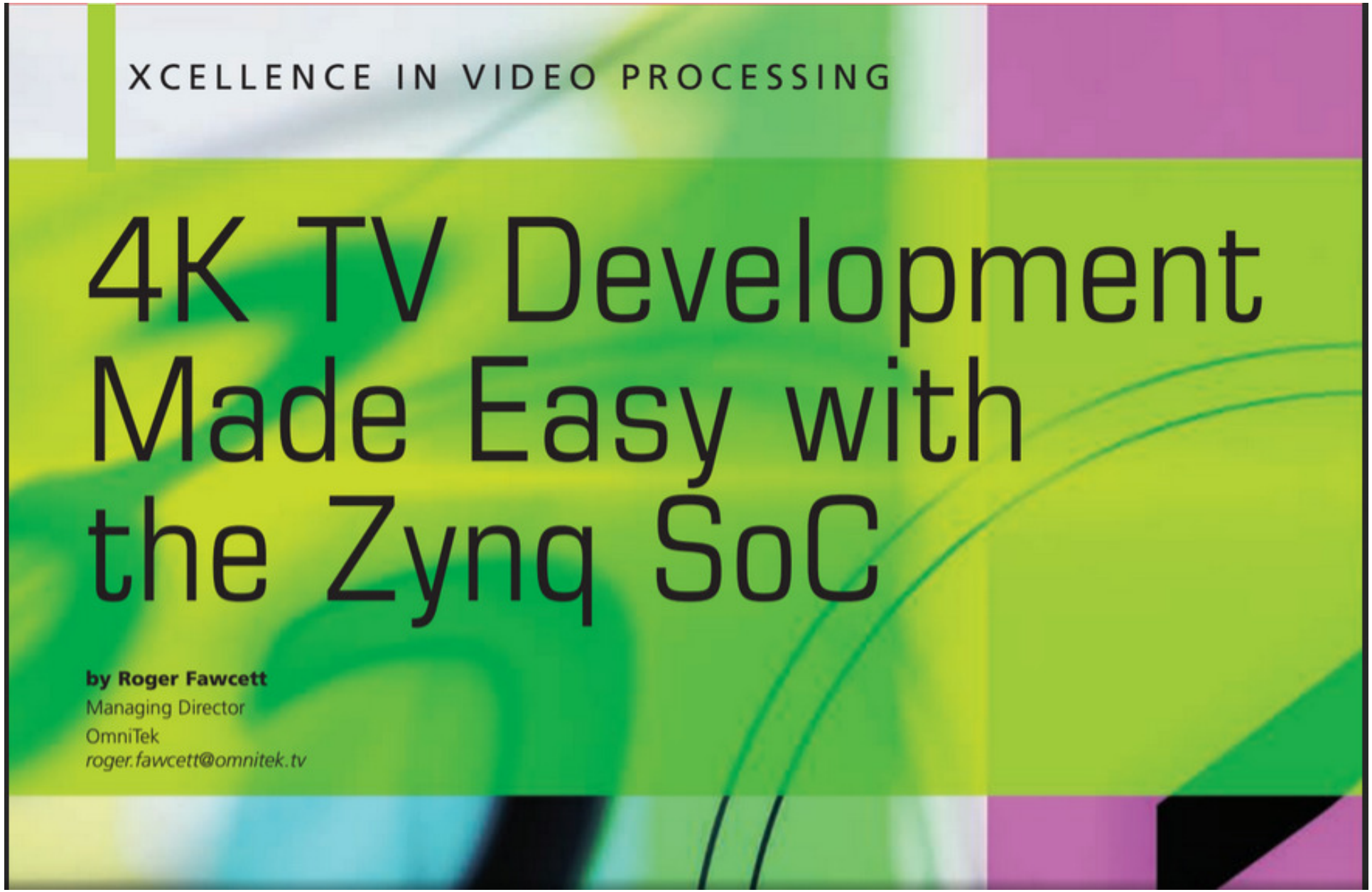
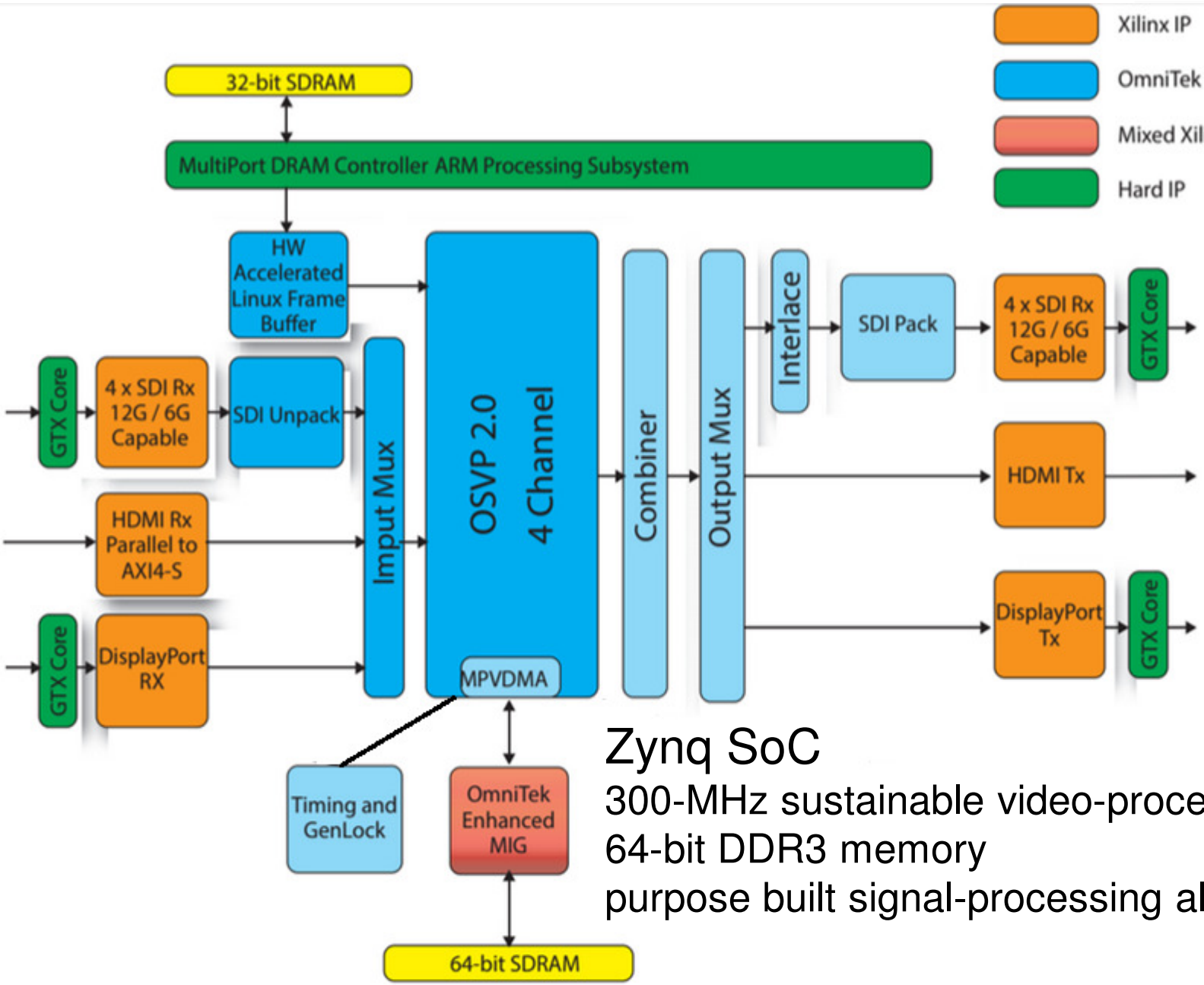


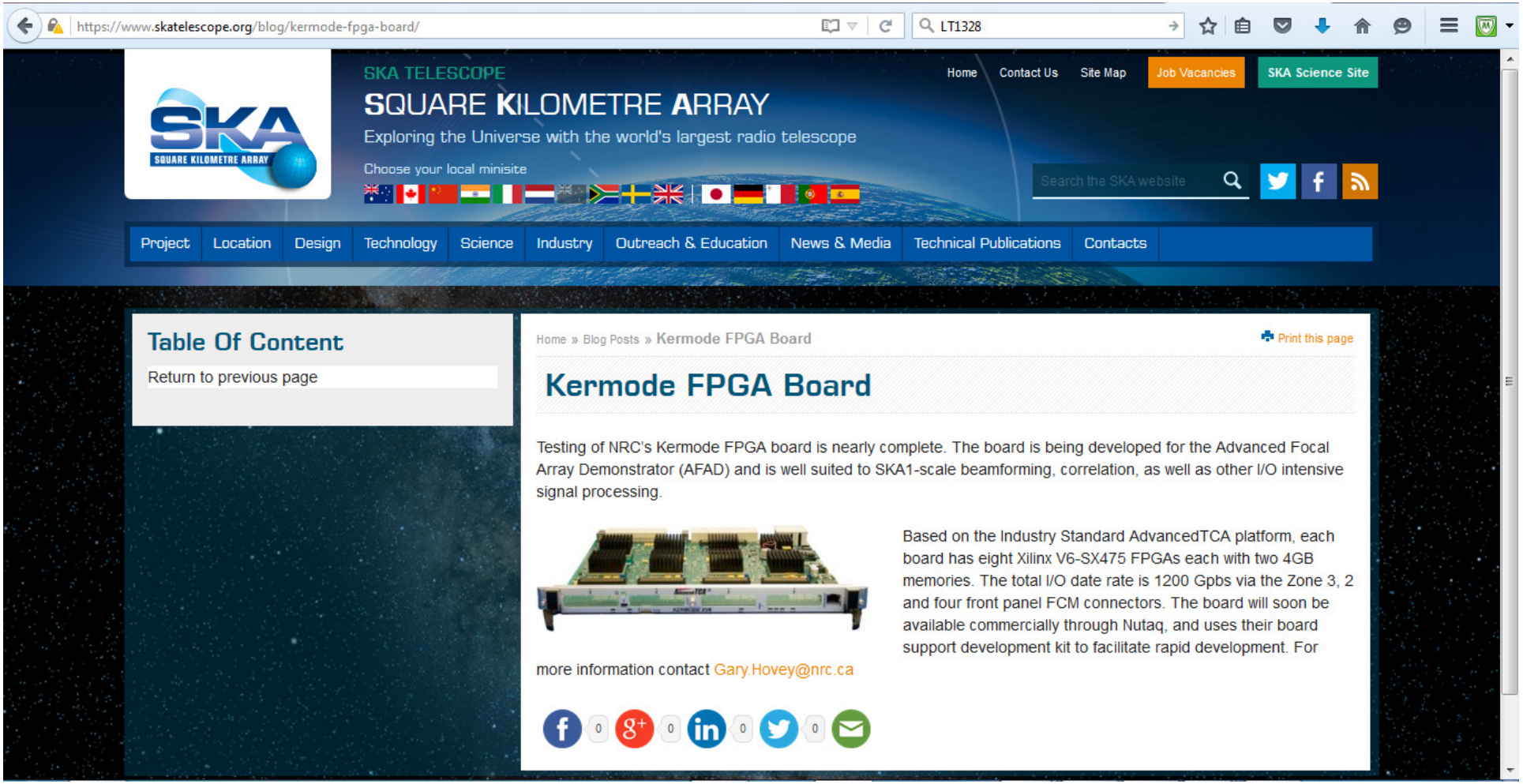


Zynq SoC

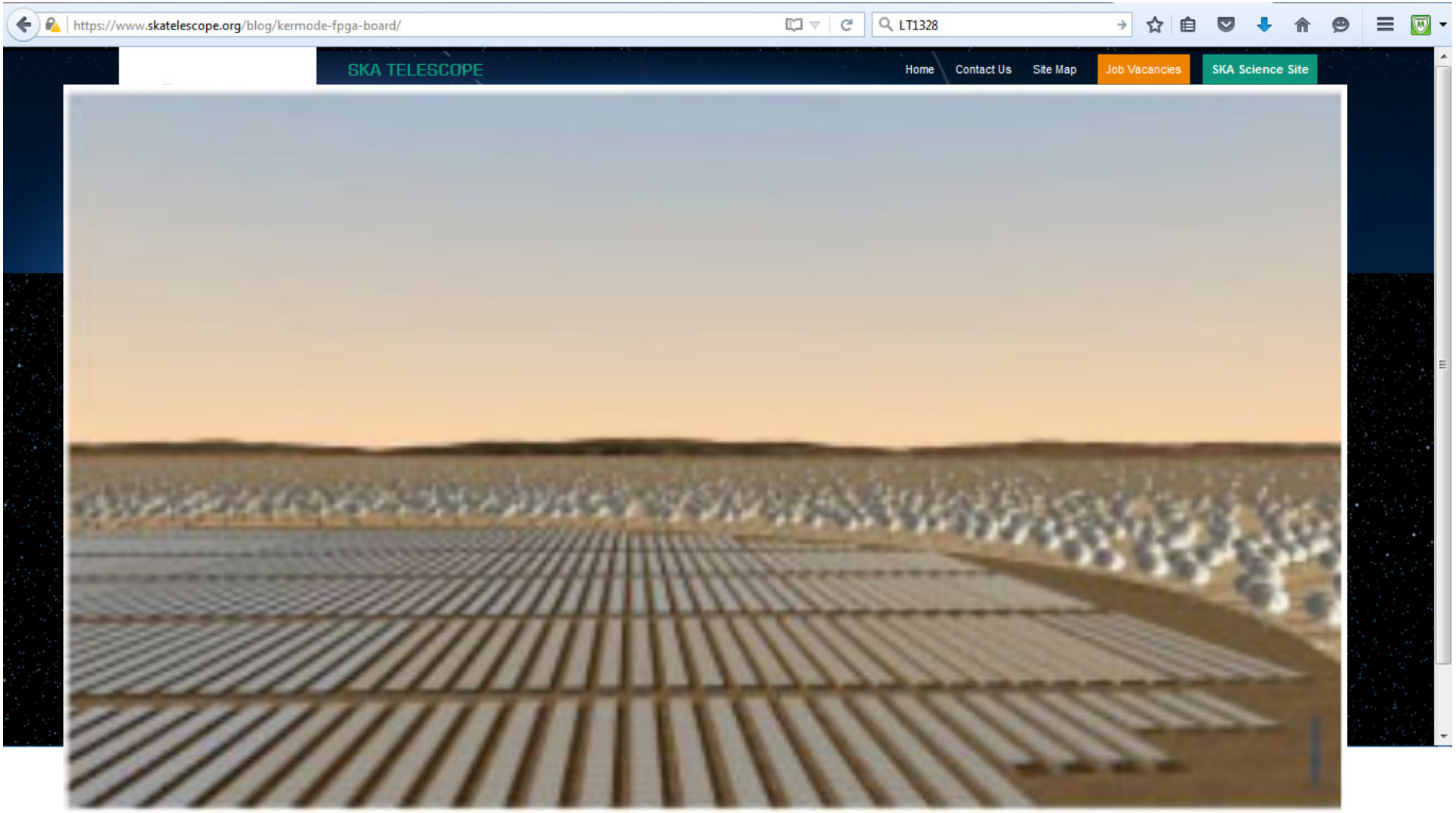
300-MHz sustainable video-processing

64-bit DDR3 memory

purpose built signal-processing algorithms



- 8 Xilinx V6-SX475 FPGAs
  - each with two 4GB memories
- total I/O date rate: 1200 Gpbs



  - each with two 4GB memories

- total I/O date rate is 1200 Gpbs

Conclusions – my guesses

- SoC design is hard – and getting harder
  - Tools try to help but still limited
- FPGA usage is trending steadily downward
  - My guess is because of perceived design difficulty combined with ease of software reuse
- Complex programmable SoC devices (e.g. Zynq) may struggle in the IoT space
  - Due to cost & power issues
  - But might be OK due to flexibility and time to market

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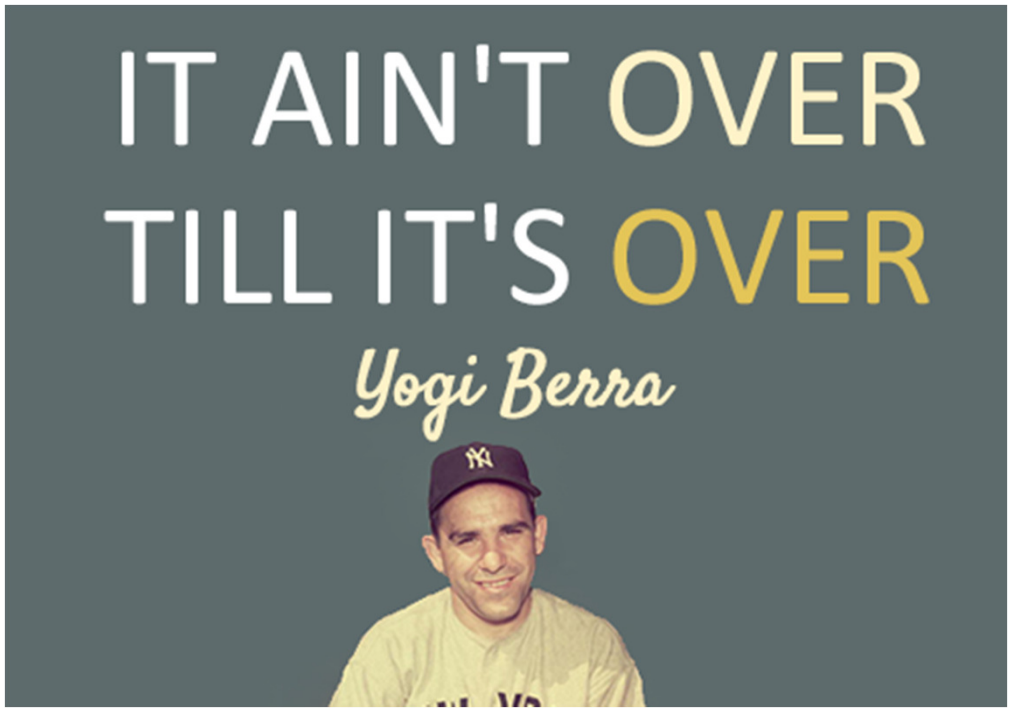
Recent Trends in System On Chip Modeling

T



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