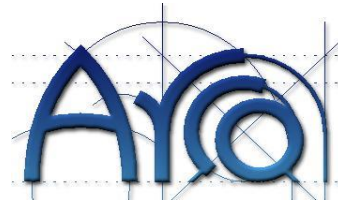


# ICTP-IAEA SCHOOL ON HYBRID RECONFIGURABLE DEVICES FOR SCIENTIFIC INSTRUMENTATION

## Vivado Design Methodology

Grupo de Arquitectura y Redes de Computadores



Universidad de Castilla-La Mancha



Julio Daniel Dondo  
[Juliodaniel.dondo@uclm.es](mailto:Juliodaniel.dondo@uclm.es)

# Hw design gap

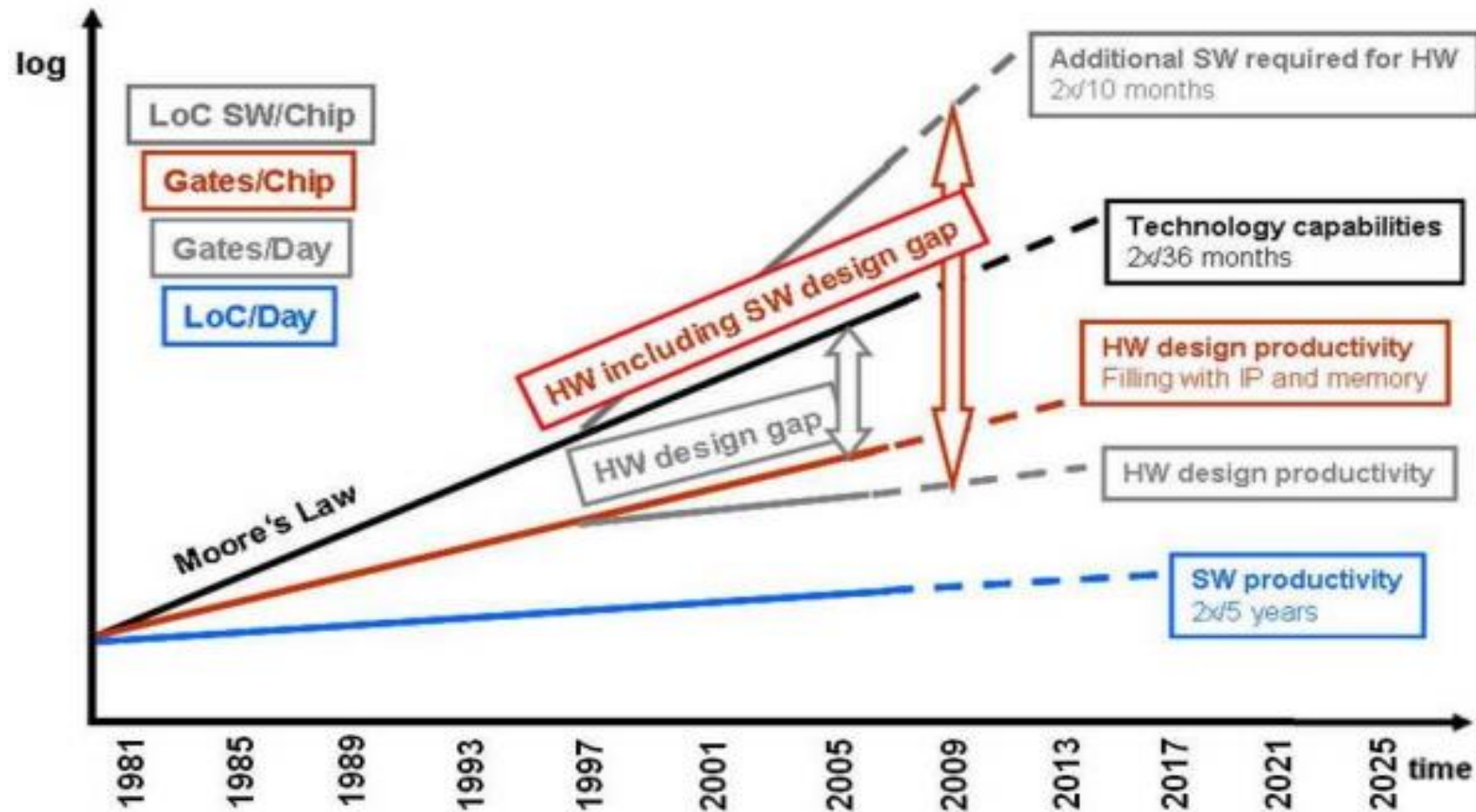
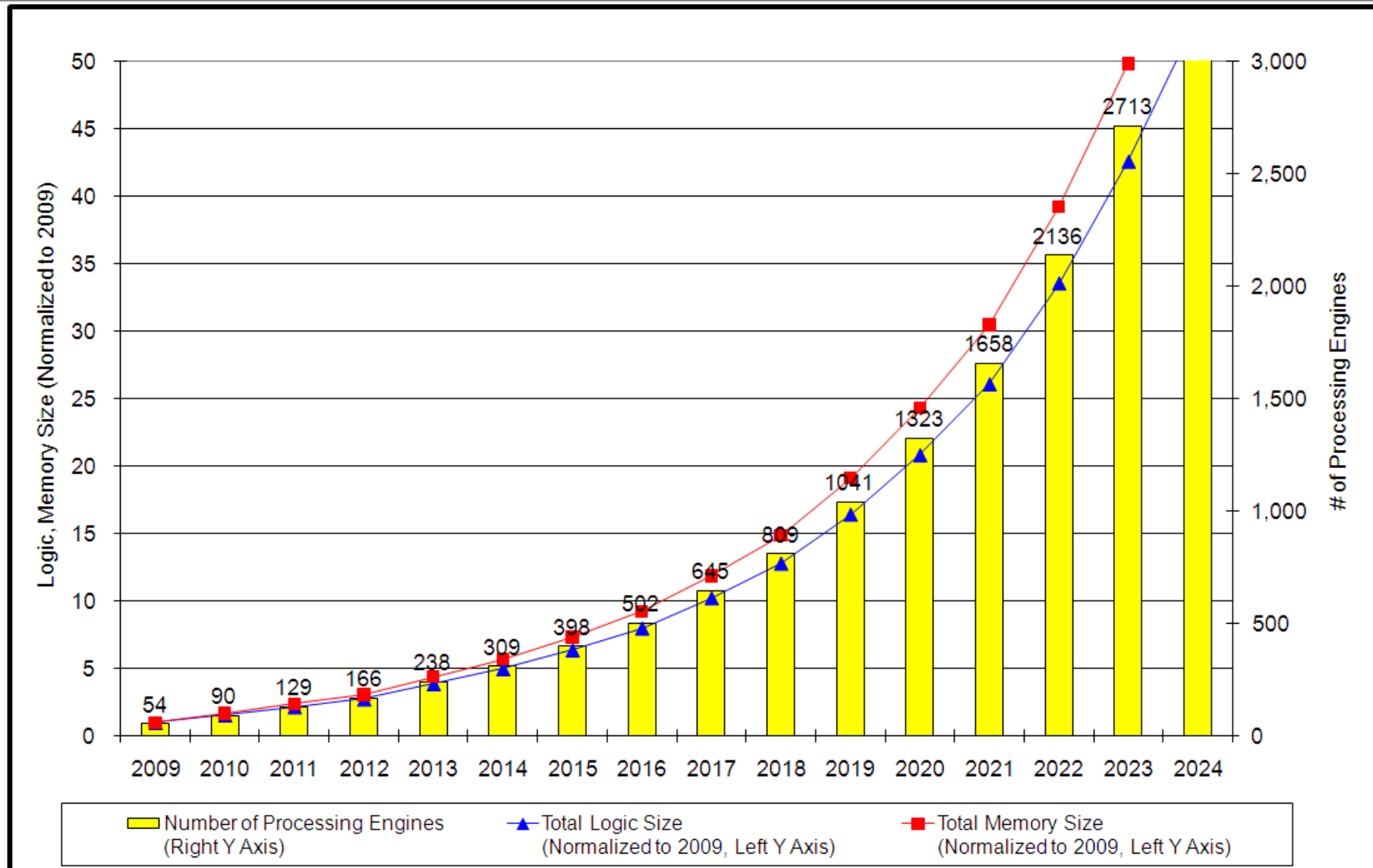


Figure DESN3 Hardware and Software Design Gaps versus Time<sup>5</sup>

THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: 2009

# SoC Design complexity trends



*SOC Consumer Portable Design Complexity Trends (ITRS 2010)*

# New challenges

- New capacities => new and better tools
- **Need for Design Methodology**
- **Time to market**
- **Early estimation of project schedule and cost**
- **Best practices**

# UltraFast Design Methodology

Xilinx Documentation Navigator 2014.4 - Design Hub View

Catalog View Design Hub View ug908-vivado-programming-debugging.pdf

Design Hubs 2014.11.18 (Xilinx Design Tools 2014.4/14.7)

**XIL**  
 ALL PRO

▲ Vivado Design Checklists  
 My Methodology Checklist  
 Create Design Checklist...

▲ Vivado 2014.4 - Design Hubs  
 Design Flows Overview  
 High-Level Synthesis (C based)  
 Designing with IP  
 Using IP Integrator  
 Applying Design Constraints  
 Power Estimation & Optimization  
 Simulation  
 Synthesis & Implementation  
 Partial Reconfiguration  
 System Generator for DSP  
 Timing Closure & Design Analysis  
 Programming & Debug

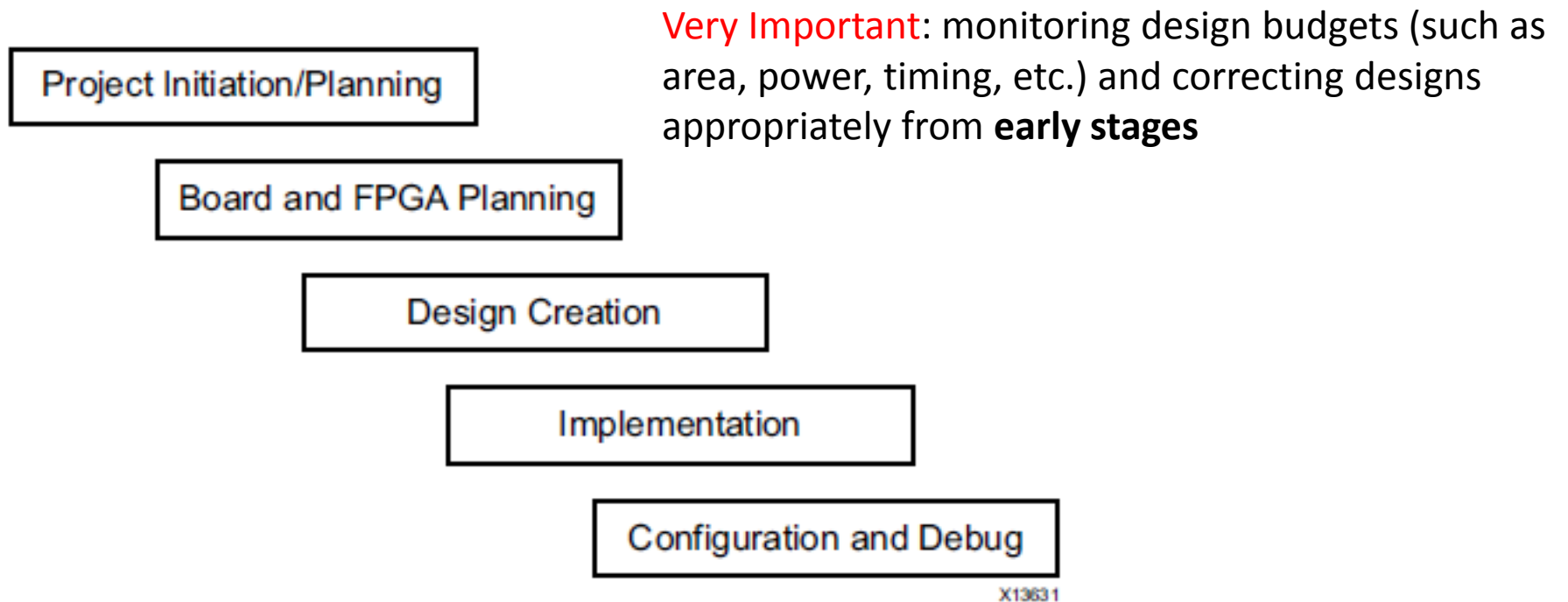
▲ Embedded Design  
 PetaLinux Tools  
 Software Development Kit (SDK)

## UltraFast Design Methodology Checklist

V1.0 - Last Modified by User on 2015-06-01 (Checklist Template: V1.2)

Title	Page	Project Introduction	Board and FPGA Planning	Design Creation	Implementation	Configuration and Debug	References
✓ 1.1 - Project Introduction						<input checked="" type="checkbox"/>	References
✓ 1.1.1 - General Project Overview						<input checked="" type="checkbox"/>	
✓ Have you had an introductory design review and planning meeting with a Xilinx representative yet?							
Action: Setup a kickoff meeting with a Xilinx representative to discuss the design and implementation strategy.							
✓ Have you reviewed the FPGA design recommendations provided in the UltraFast Design Methodology Guide for the Vivado Design Suite (UG949)?							UG949: UltraFast Design Methodology Guide Vivado Design Suite
Action: Read the UltraFast Design Methodology Guide for the Vivado Design Suite (UG949). This checklist links to sections of UG949 for more information about specific topics.							
✓ 1.2 - Xilinx Documentation and Training						<input checked="" type="checkbox"/>	References
✓ 1.2.1 - Xilinx Training						<input checked="" type="checkbox"/>	
✓ Are you and your team proficient with the Vivado Design Suite? Have you investigated the latest Vivado Training offerings?							Xilinx.com > Support - Training
The Vivado Design Suite has evolved into a premier design environment with a lot of capabilities and user options. Proper training can ensure the design team quickly becomes efficient with Vivado tools.							
Actions							
- Attend a regularly scheduled Xilinx training class or request an onsite class.							
- Perform Web-based online training classes.							
✓ 1.2.2 - QuickTake Video and Software Tutorials, User Guides						<input checked="" type="checkbox"/>	UG949: Vivado Design Suite Flows
✓ Have you explored the available software training collateral?							UG949: Accessing the QuickTake Video Tuto Xilinx.com > Vivado Video Tutorials Vivado Software Tutorials Vivado User Guides
Xilinx provides a host of Video and Software Tutorials aimed at quickly bringing users up to speed with the Vivado Design Suite. The Vivado User Guides provide detailed information about using the various features of the Vivado Design Suite.							
Actions							
- View the relevant QuickTake Video Tutorials. Download the videos for the best viewing quality.							
- Perform the software tutorials to walk through example exercises.							
- Review the Vivado Design Suite User Guides.							
✓ 1.2.3 - Documentation Navigator						<input checked="" type="checkbox"/>	UG949: Vivado Design Suite Flows

# Design Process

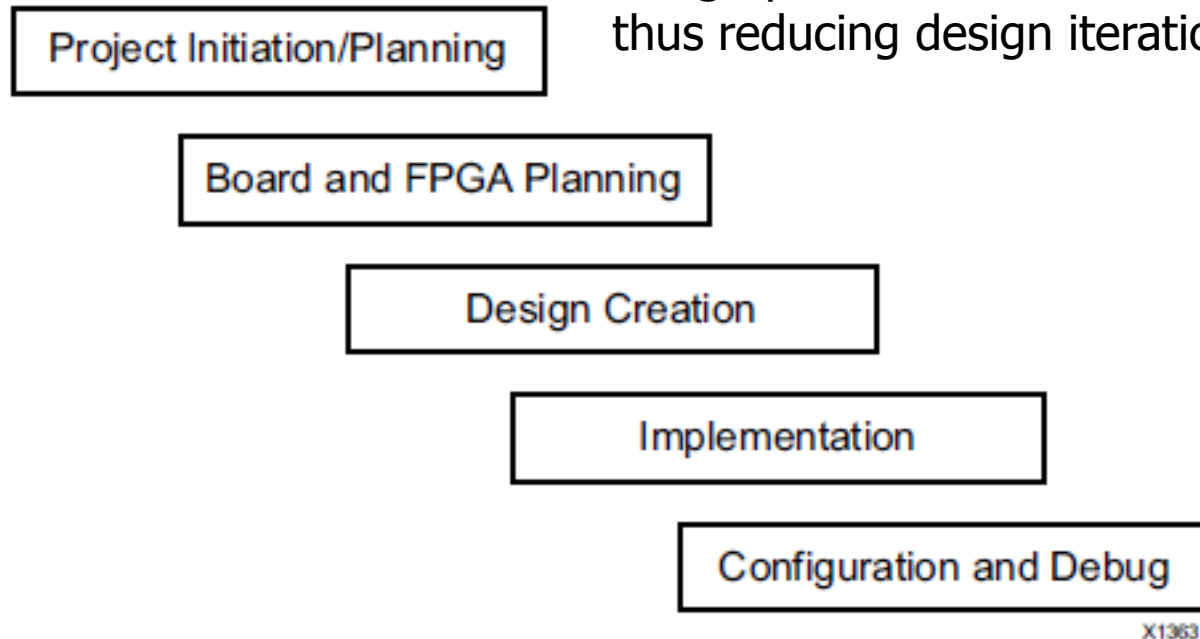


**Very important:** creating correct timing constraints for the system, before entering the implementation phase

Steps in design process

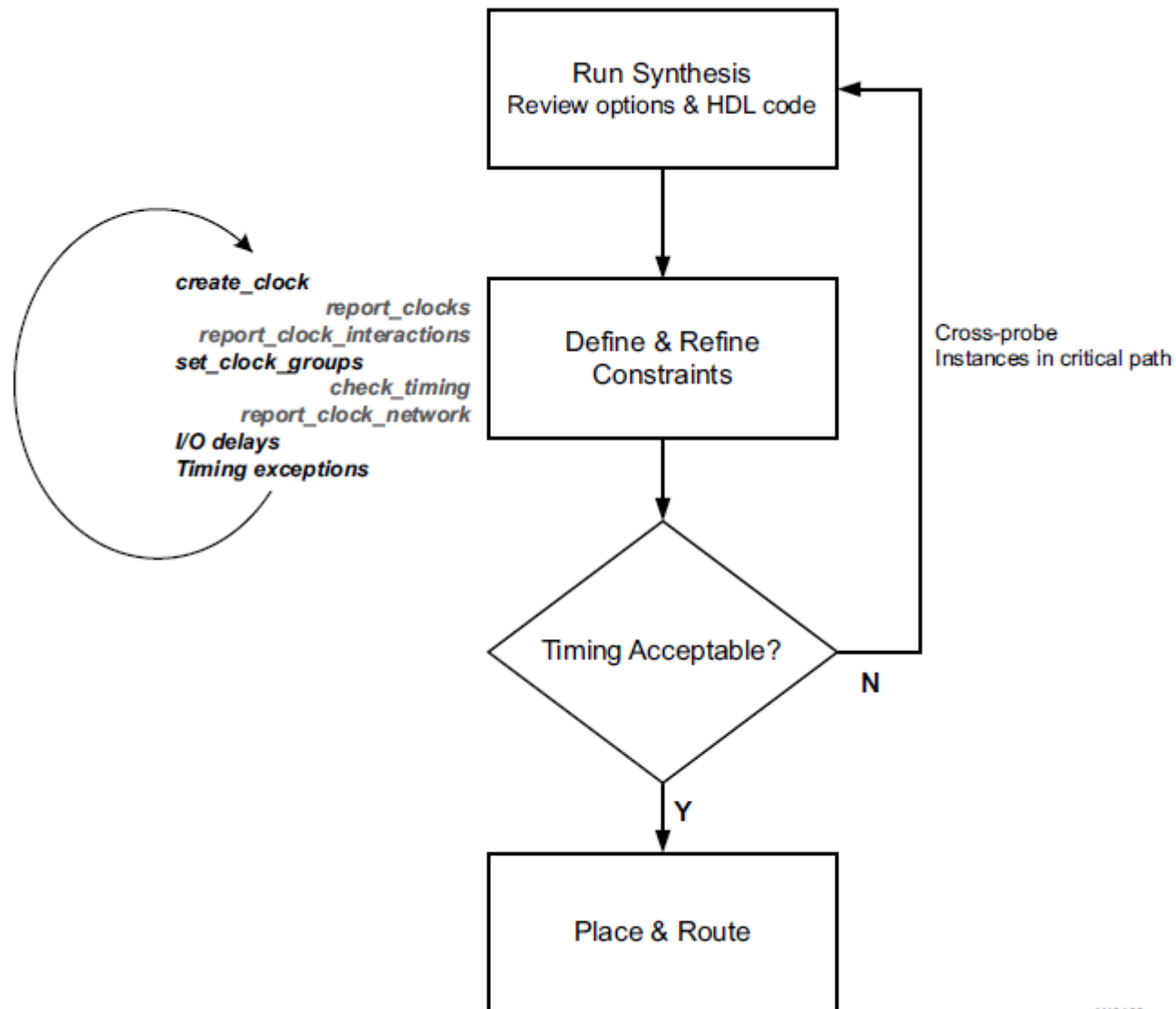
# Design Process

The Vivado Design Suite provides you with design analysis capabilities at each design stage. This allows for design and tool setting modifications earlier in the design processes where they have less overall schedule impact, thus reducing design iterations and accelerating productivity.



Steps in design process

# Design Process

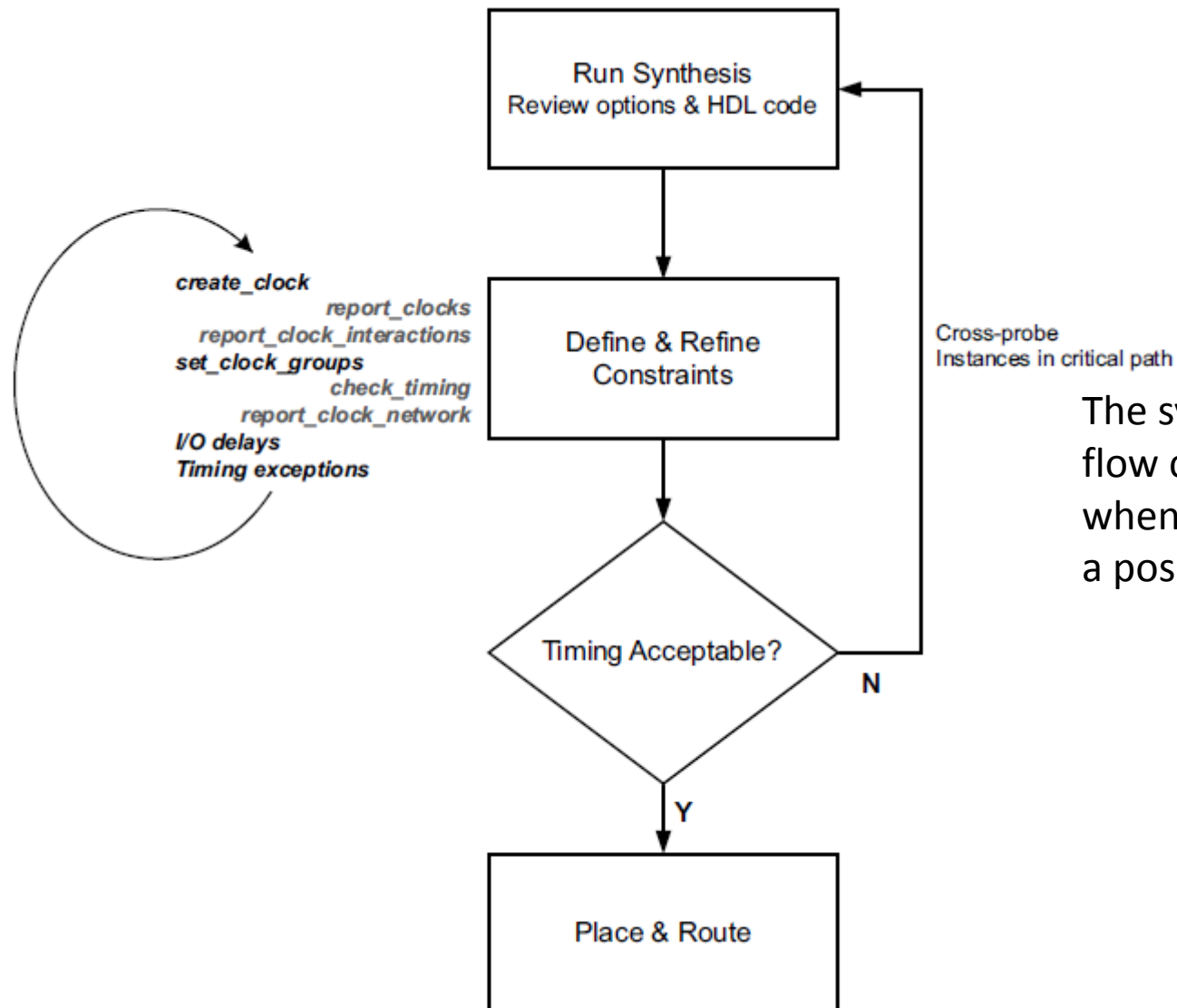


X13422

Design methodology for rapid convergence



# Design Process

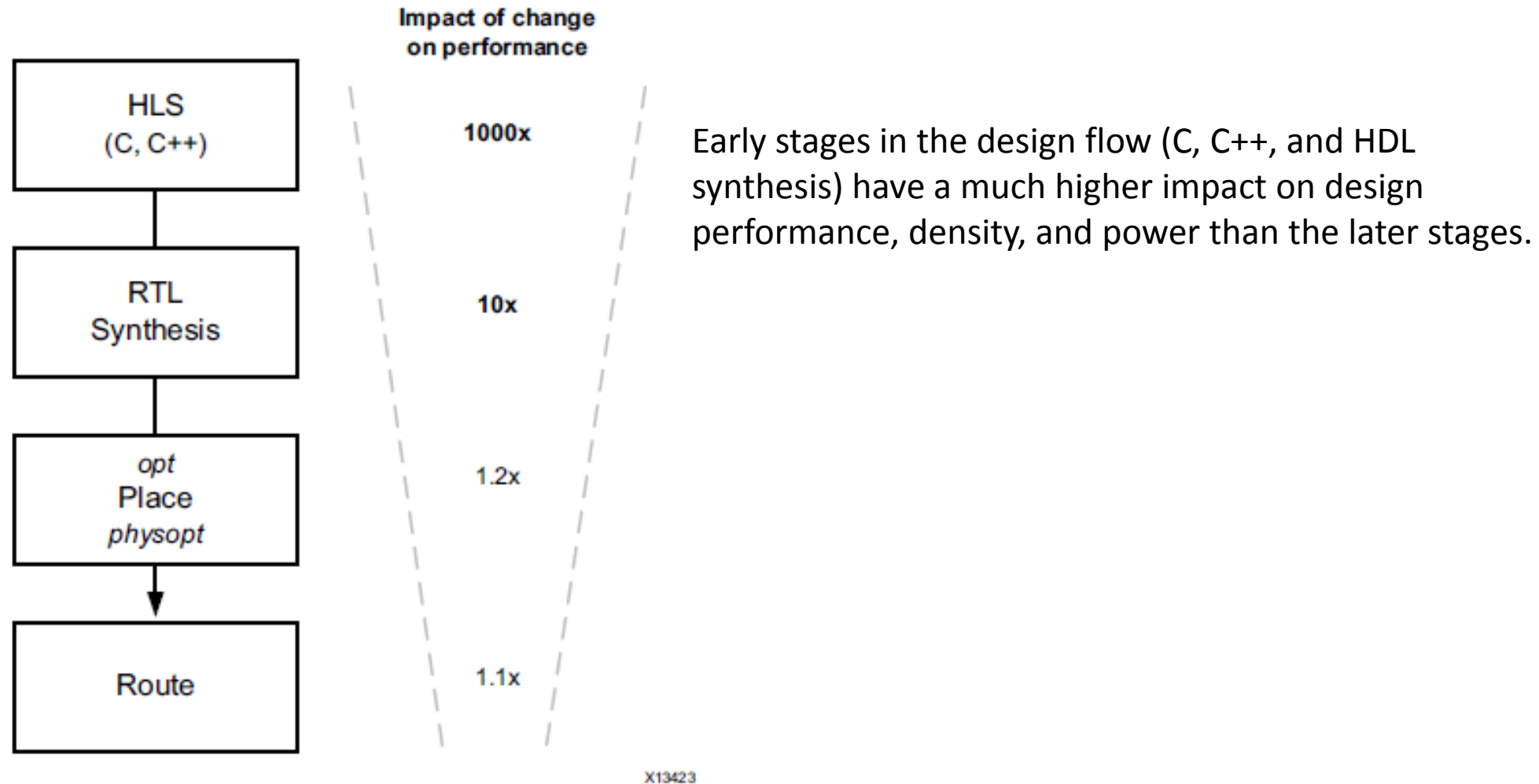


The synthesis portion of the design flow can be considered complete when the design goals are met with a positive margin

X13422

Design methodology for rapid convergence

# Design Process



Impact of Design Changes throughout the flow

# Design Flows

- *RTL to Bitstream*
- *Embedded Processor Design Flow*
- *High-Level C-based Synthesis Flow*
- *Partial Reconfiguration Design Flow*

# Vivado Design Suite

- The Vivado Design Suite replaces Xilinx ISE® Design Suite of tools.
- It replaces all of the ISE Design Suite point tools, such as Project Navigator, Xilinx Synthesis Technology (XST), implementation, CORE Generator™ tool, Timing Constraints Editor, ISE Simulator (ISim), ChipScope™ Analyzer, Xilinx Power Analyzer, FPGA Editor, PlanAhead™ design tool, and SmartXplorer.
- All of these capabilities are now built directly into the Vivado Design Suite

# Vivado Design Suite

The Vivado Design Suite supports the following established industry design standards:

- Tcl
- AXI4, IP-XACT
- Synopsys design constraints (SDC)
- Verilog, VHDL, SystemVerilog
- SystemC, C, C++, OpenCL

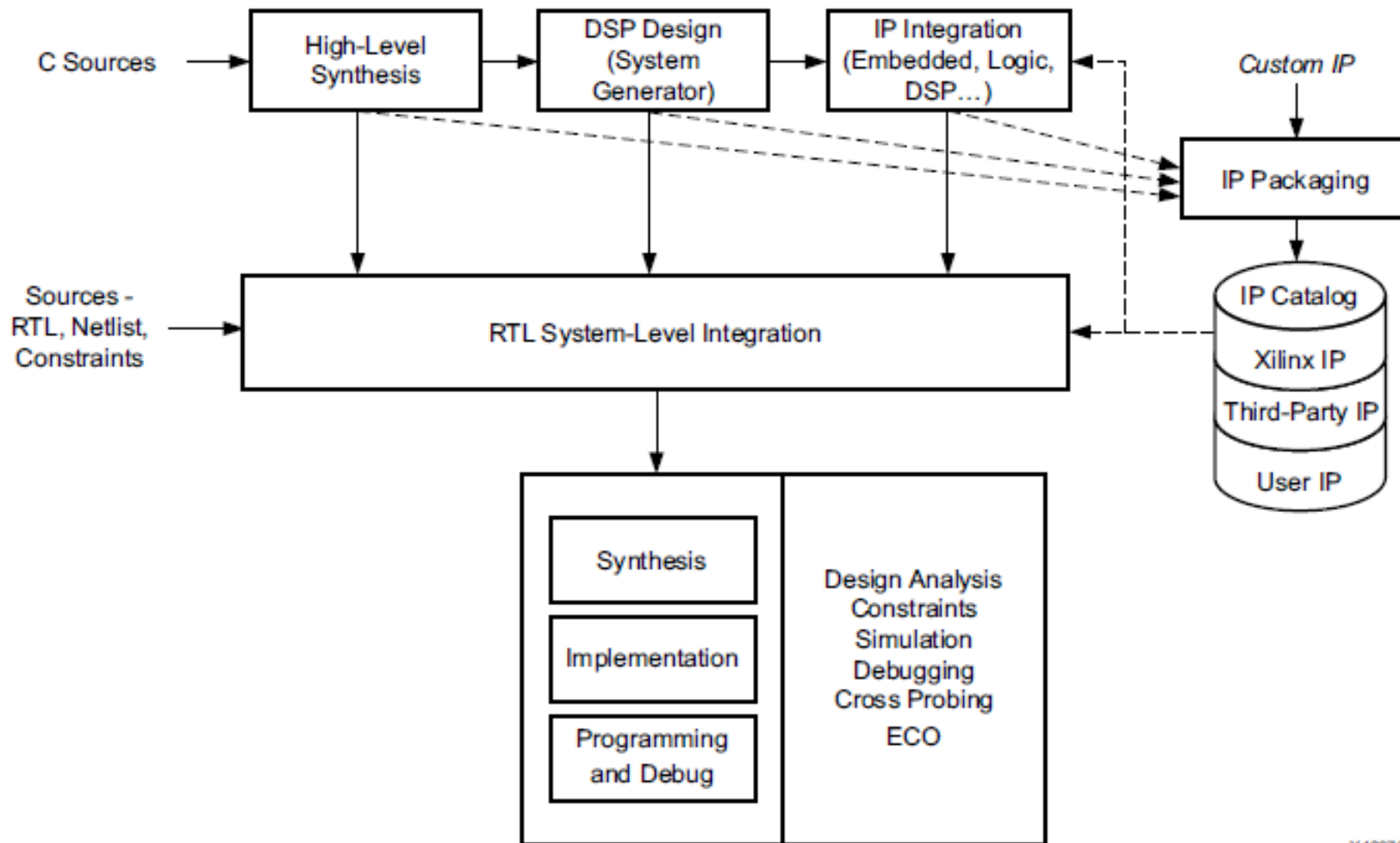
# Vivado Design Suite

You can interact with the Vivado Design Suite using:

- GUI-based commands in the Vivado IDE
- Tcl commands entered in the Tcl Console in the bottom of the Vivado IDE,
- Tcl Commands entered in the Vivado Design Suite Tcl shell outside the Vivado IDE,
- or running Tcl scripts from the Vivado IDE or in the Vivado Design Suite Tcl shell
  - A Tcl script can contain Tcl commands covering the entire design synthesis and implementation flow, including all necessary reports generated for design analysis at any point in the design flow
- A mix of GUI-based and Tcl commands

# Vivado High Level Design Flow

- Vivado Design Suite High-Level Design Flow

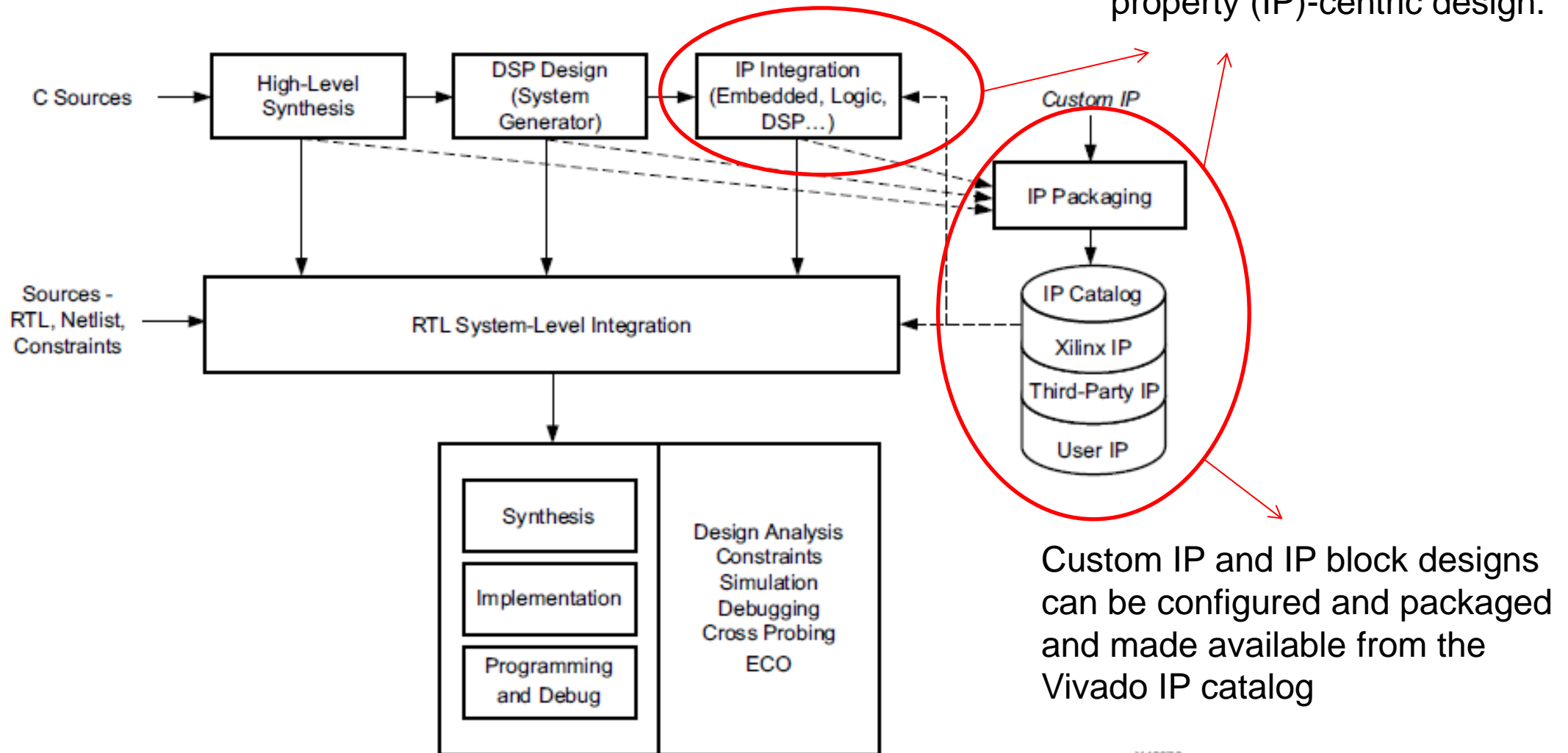


X12973

# Vivado High Level Design Flow

- Vivado Design Suite High-Level Design Flow

Focused on intellectual property (IP)-centric design.





# Use models

- **Project Mode**

- A directory structure is created on disk
- A runs infrastructure is used to manage the automated synthesis and implementation process and to track run status.
- The entire design flow can be run with a single click.
- The entire flow can also be scripted using Tcl commands.

- **Non-Project Mode**

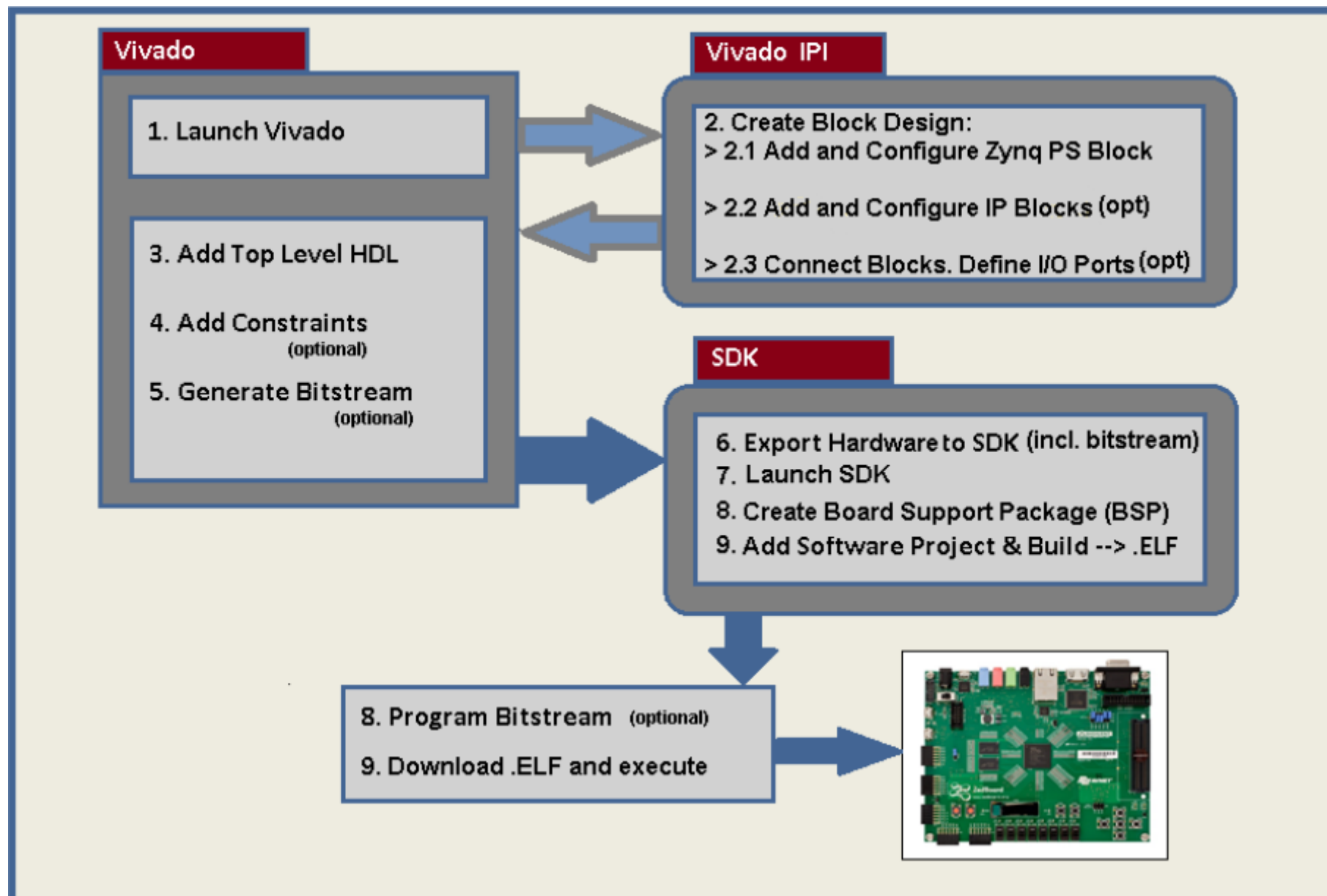
- Sources are accessed from their current locations
- Each design step is run individually using Tcl commands, and design parameters and implementation options are set using Tcl commands.
- You can save design checkpoints and create reports at any stage of the design process using Tcl. In addition, you can open the Vivado IDE at each design stage for design analysis and constraints assignment.

# Use models

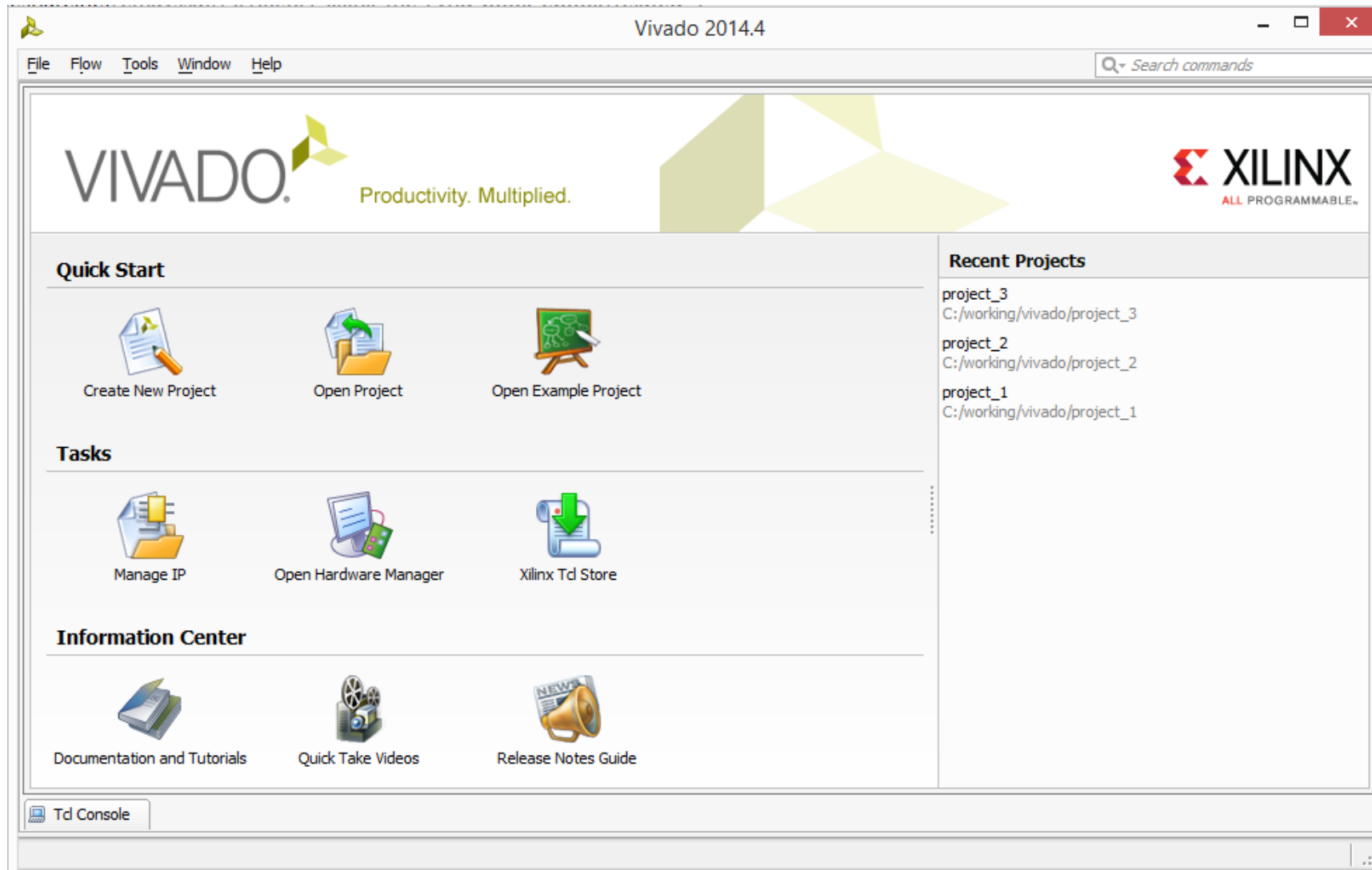
Flow Element	Project Mode	Non-Project Mode
Design Source File Management	Automatic	Manual
Flow Navigation	Guided	Manual
Flow Customization	Limited	Unlimited
Reporting	Automatic	Manual
Analysis Stages	Designs only	Designs and design checkpoints

## Project Mode versus Non-Project Mode Features

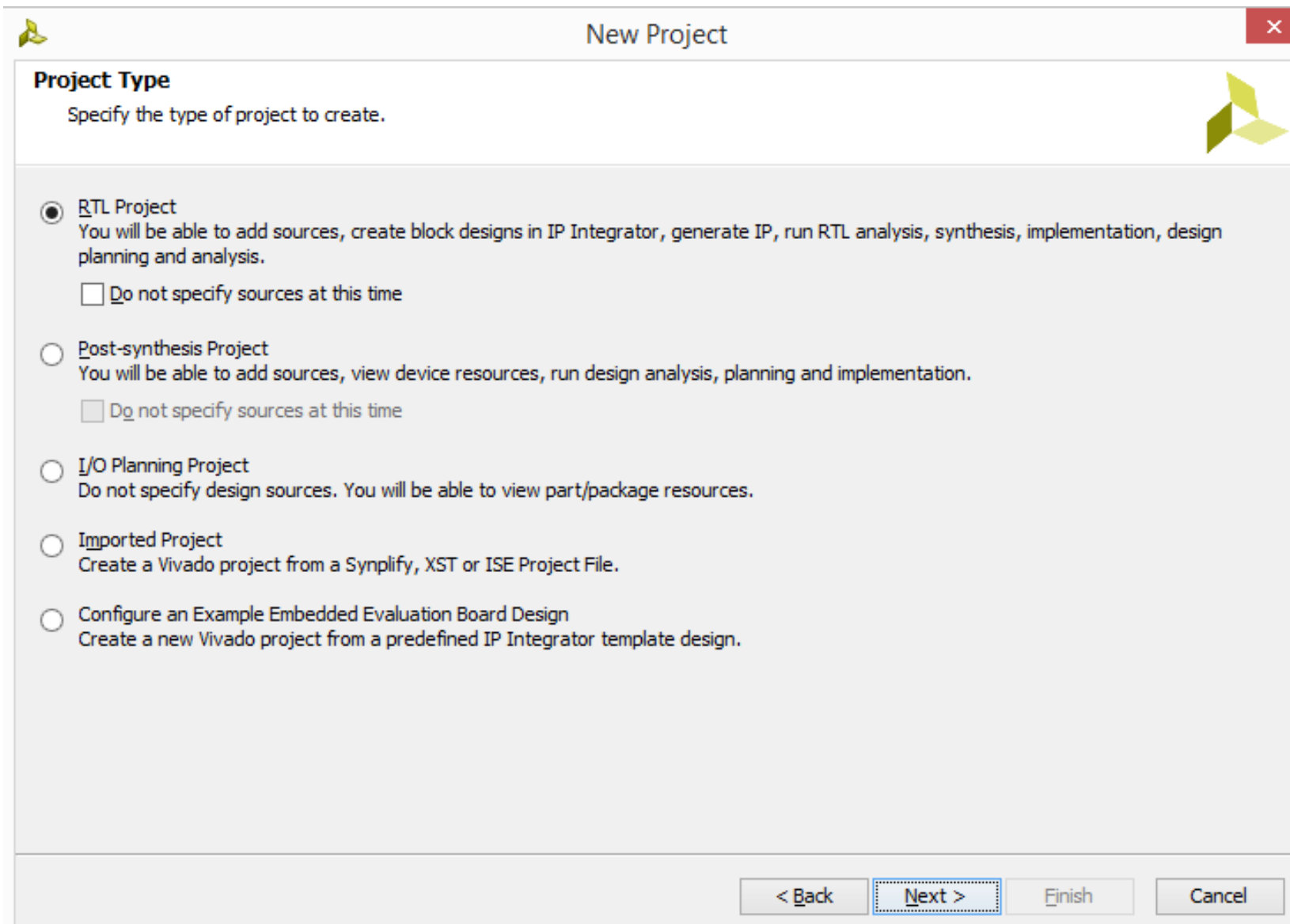
# Design Process



# Launch Vivado



# Creating Projects in Vivado



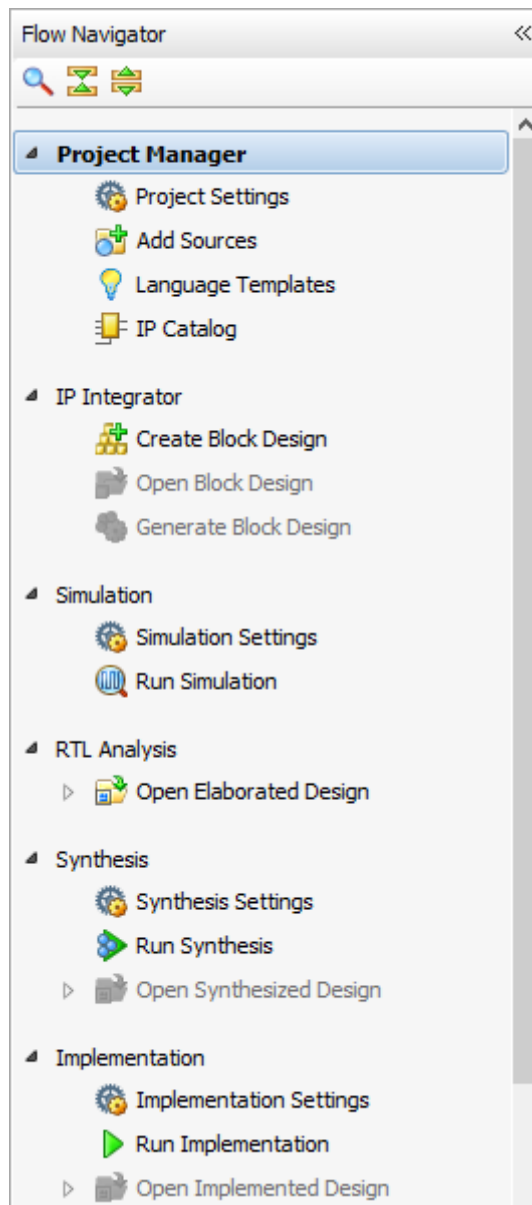
**New Project**

**Project Type**  
Specify the type of project to create.

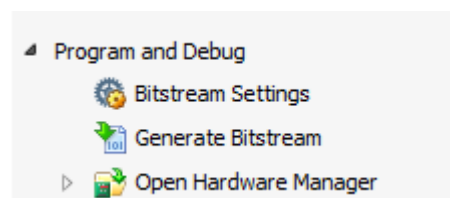
- ☒ **RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
☐ Do not specify sources at this time
- ☐ **Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.  
☐ Do not specify sources at this time
- ☐ **I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.
- ☐ **Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.
- ☐ **Configure an Example Embedded Evaluation Board Design**  
Create a new Vivado project from a predefined IP Integrator template design.

< Back   **Next >**   Finish   Cancel

# Flow Navigator in Vivado



It provides control over the major design process tasks, such as project configuration, synthesis, implementation, and bitstream generation



# Main Design Flow Features

- Vivado Synthesis
- Vivado implementation
- Vivado timing analysis
- Vivado power analysis
- Bitstream Generation

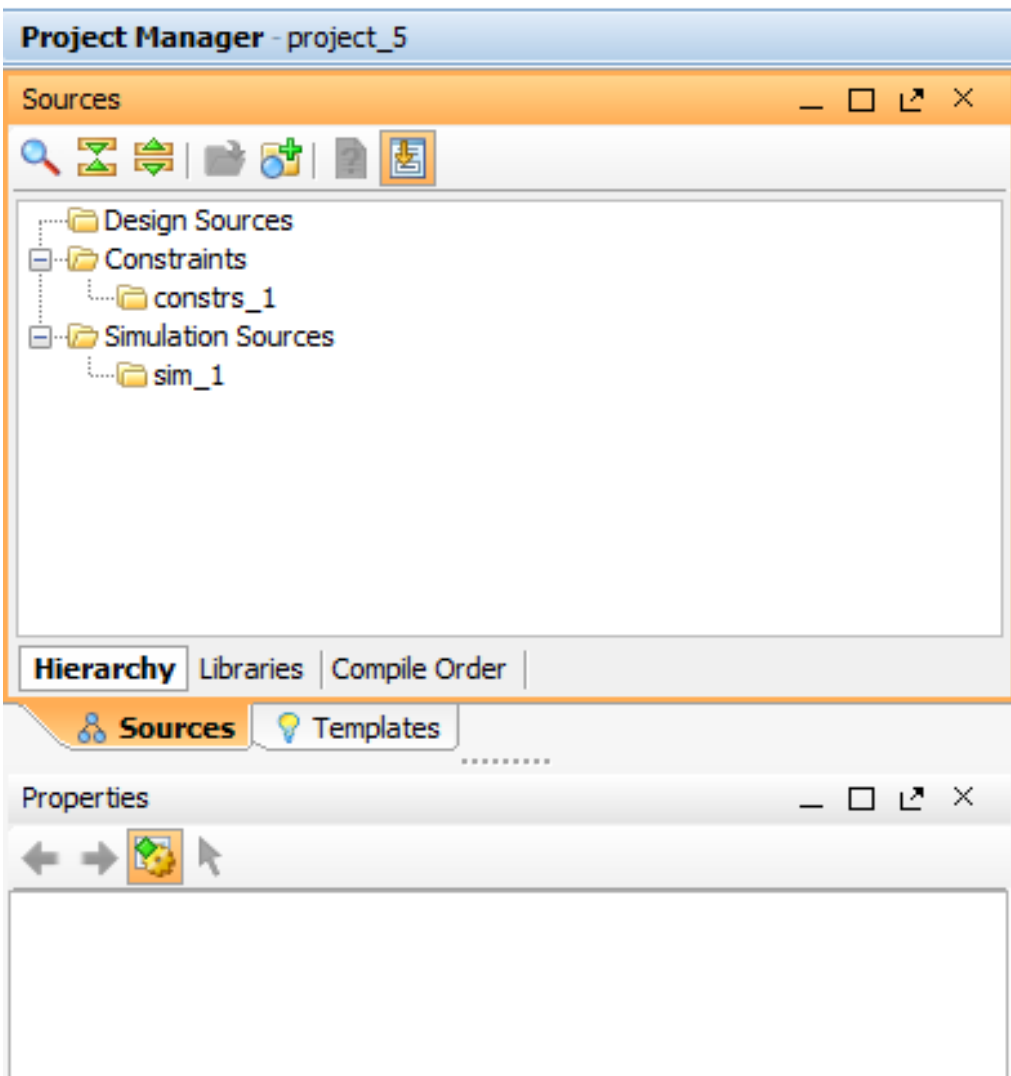
timing driven and use SDC or XDC format constraints

Various reports and analysis features are available at each stage of the design process

You can create multiple runs to experiment with different synthesis or implementation options, timing and physical constraints, or design configuration

Some advanced options are available for implementation, such as Vivado power optimization, Vivado physical optimizer, and run strategies, which assist you with design closure.

# ■ Performing System-Level Design Entry

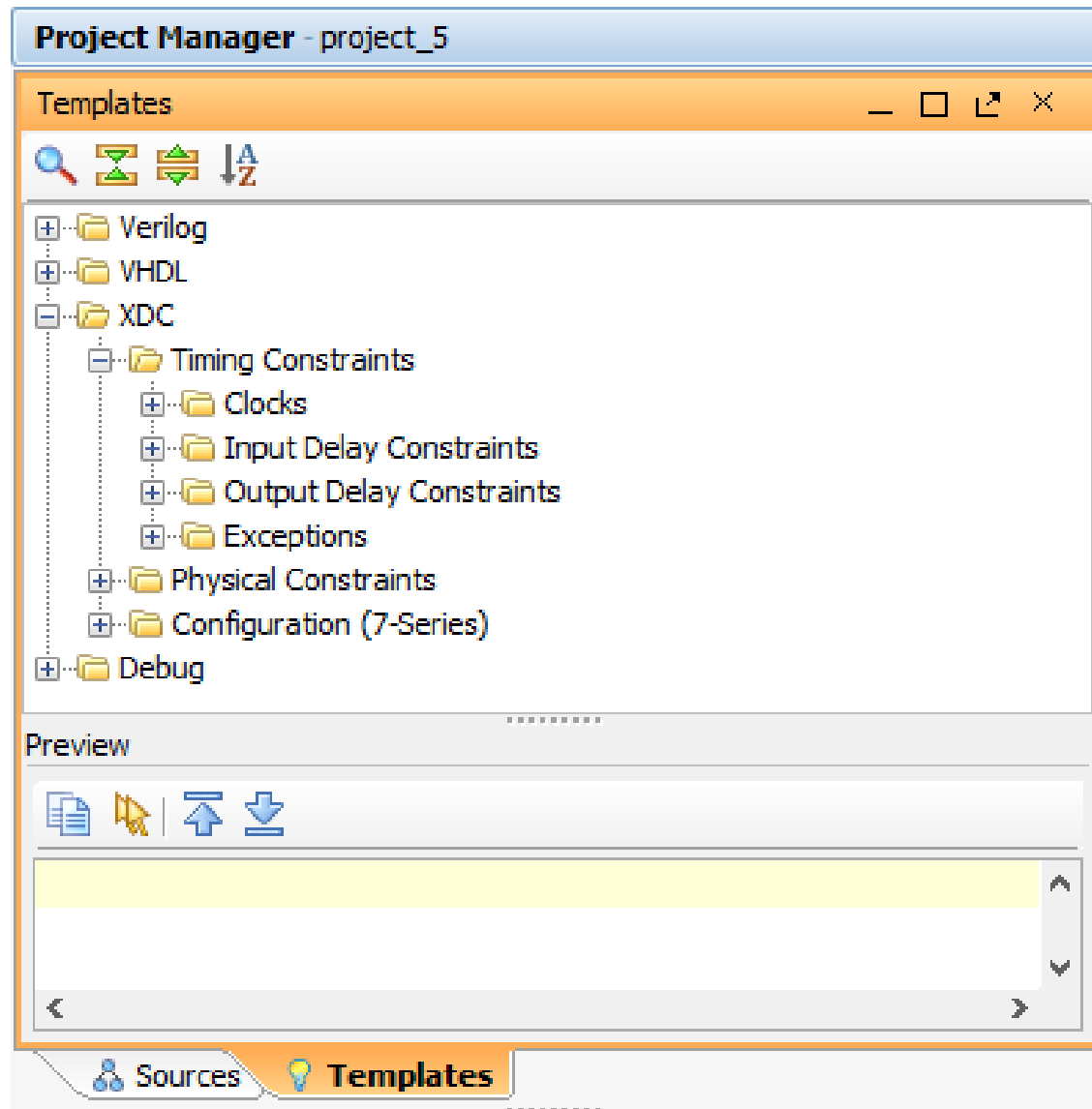


**Automated Hierarchical Source File Compilation and Management**

**The Sources window updates the status of the project sources. A quick compilation of the design source files is performed**



# Working with templates



# Working with IP

The screenshot shows the Xilinx IP Catalog window. The top bar has tabs for 'Diagram' and 'IP Catalog'. Below the tabs is a search bar. The main area is a table listing various IP blocks. The 'Accumulator' block is selected and highlighted in blue. Below the table is a 'Details' section for the selected 'Accumulator' block.

Name	AXI4	Status	License	VLNV
Reed-Solomon Decoder	AXI4-Stream	Production	Purchase	xilinx.com:ip ^
<b>Accumulator</b>		<b>Production</b>	<b>Included</b>	<b>xilinx.com:ip</b>
Color Filter Array Interpolation	AXI4, AXI4-Stream	Production	Purchase	xilinx.com:ip
AXI HWICAP	AXI4	Production	Included	xilinx.com:ip
VIO (Virtual Input/Output)		Production	Included	xilinx.com:ip
AXI Central Direct Memory Access	AXI4	Production	Included	xilinx.com:ip
Complex Multiplier	AXI4-Stream	Production	Included	xilinx.com:ip
AHB-Lite to AXI Bridge	AXI4	Production	Included	xilinx.com:ip
Local Memory Bus (LMB) 1.0		Production	Included	xilinx.com:ip
LTE DL Channel Encoder		Production	Purchase	xilinx.com:ip
Video Scaler	AXI4, AXI4-Stream	Production	Purchase	xilinx.com:ip
Processor System Reset		Production	Included	xilinx.com:ip v

**Details**

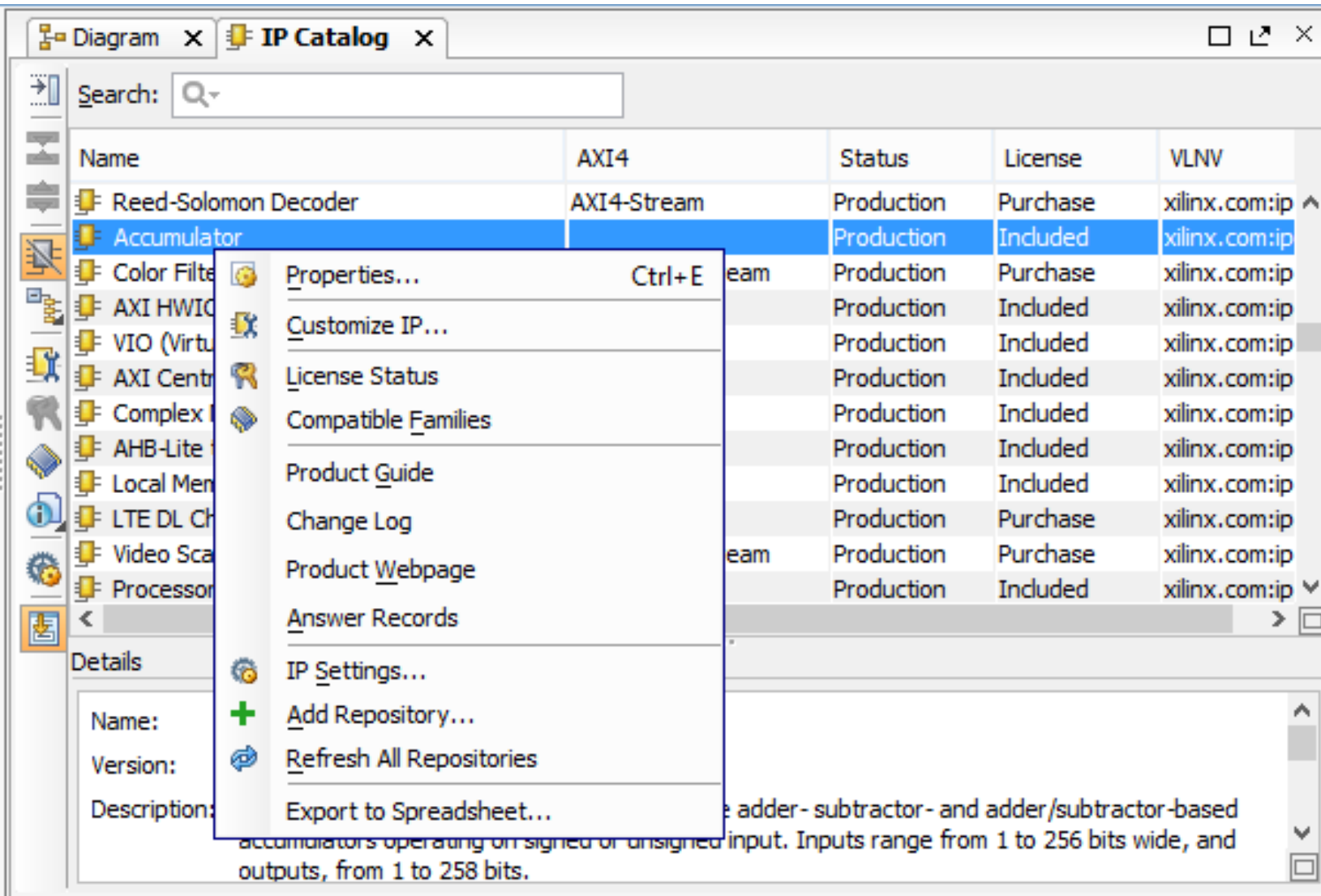
Name: **Accumulator**

Version: 12.0 (Rev. 5)

Description: The Xilinx LogiCORE Accumulator can generate adder- subtractor- and adder/subtractor-based accumulators operating on signed or unsigned input. Inputs range from 1 to 256 bits wide, and outputs, from 1 to 258 bits.

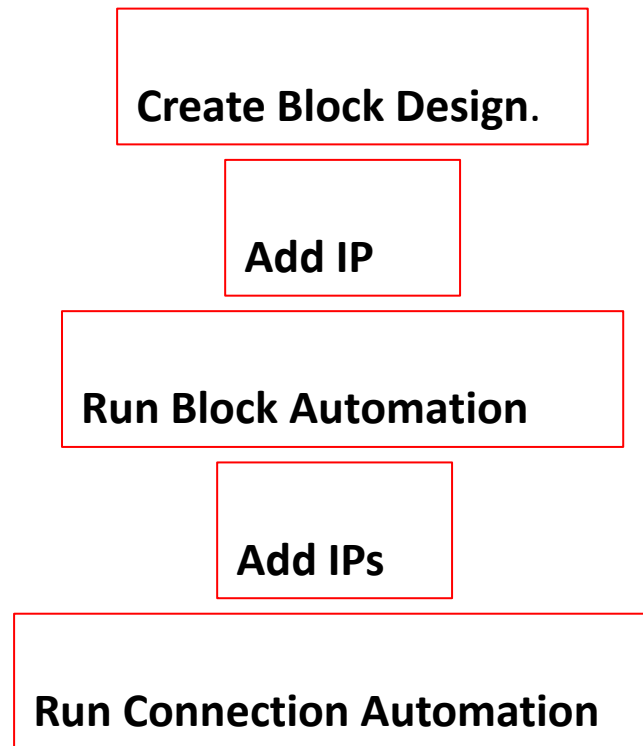
The IP catalog provides quick access to the IP for configuration, instantiation, and validation of IP.

# Working with IP

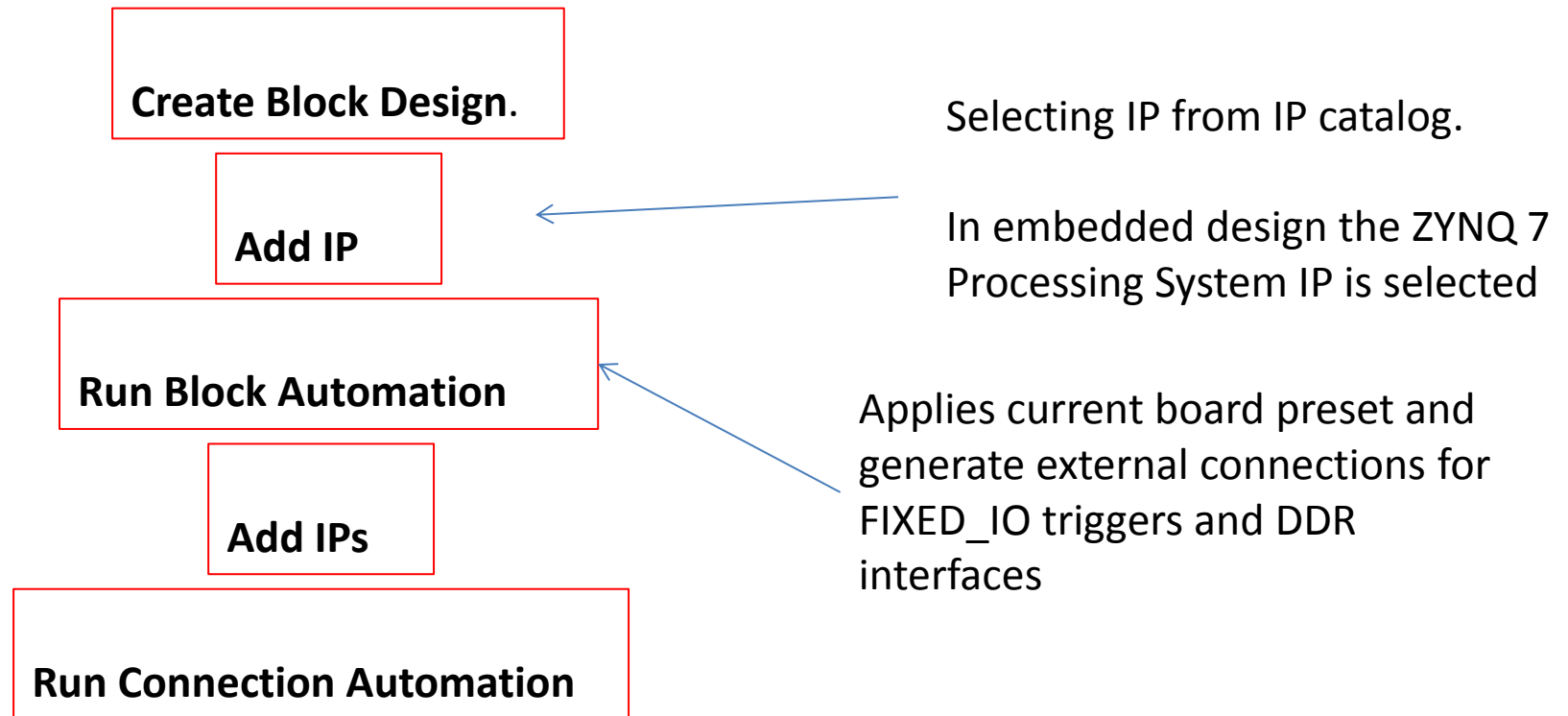


The IP catalog provides quick access to the IP for configuration, instantiation, and validation of IP.

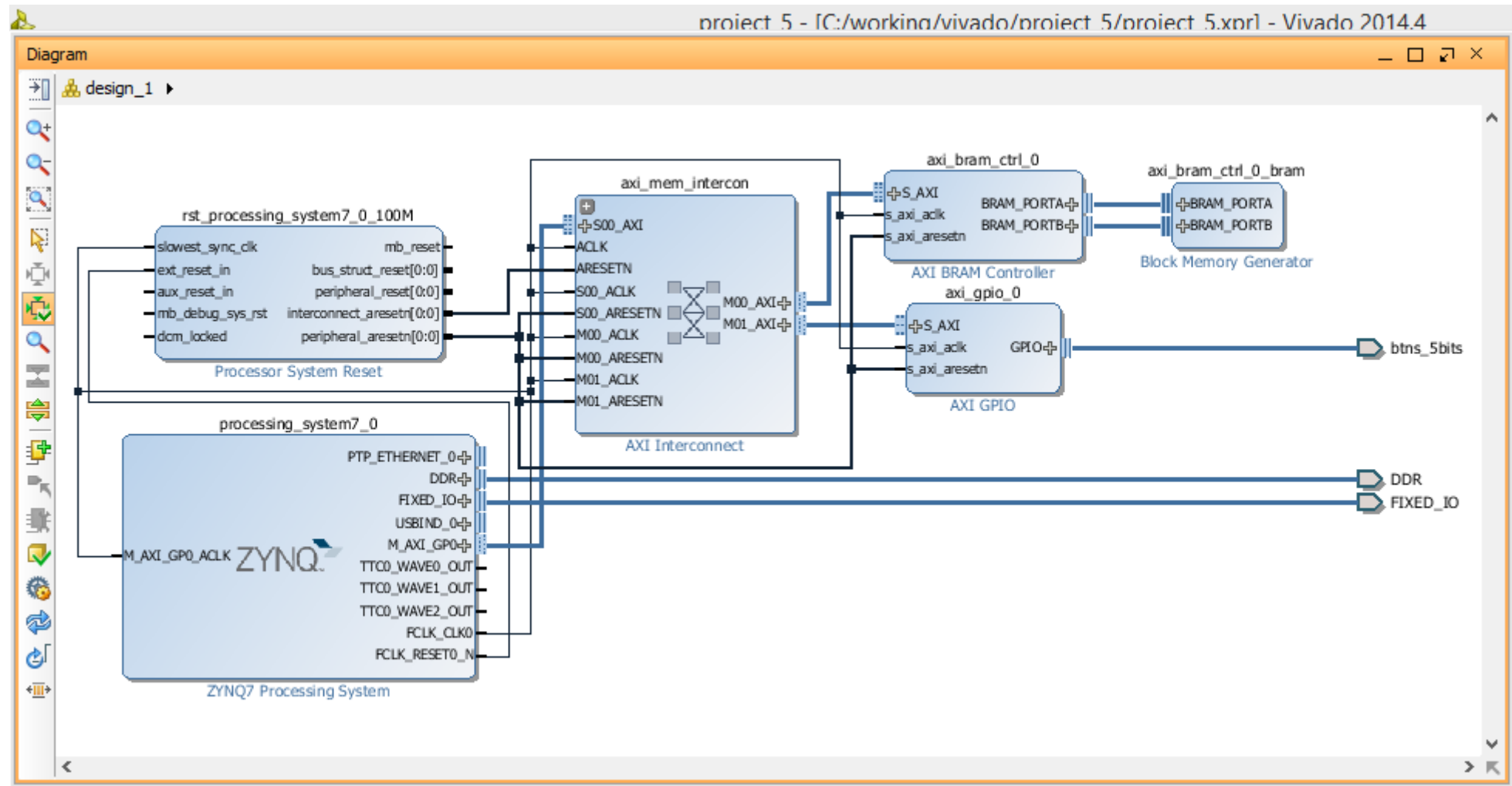
# ■ Creating an IP Integrator design



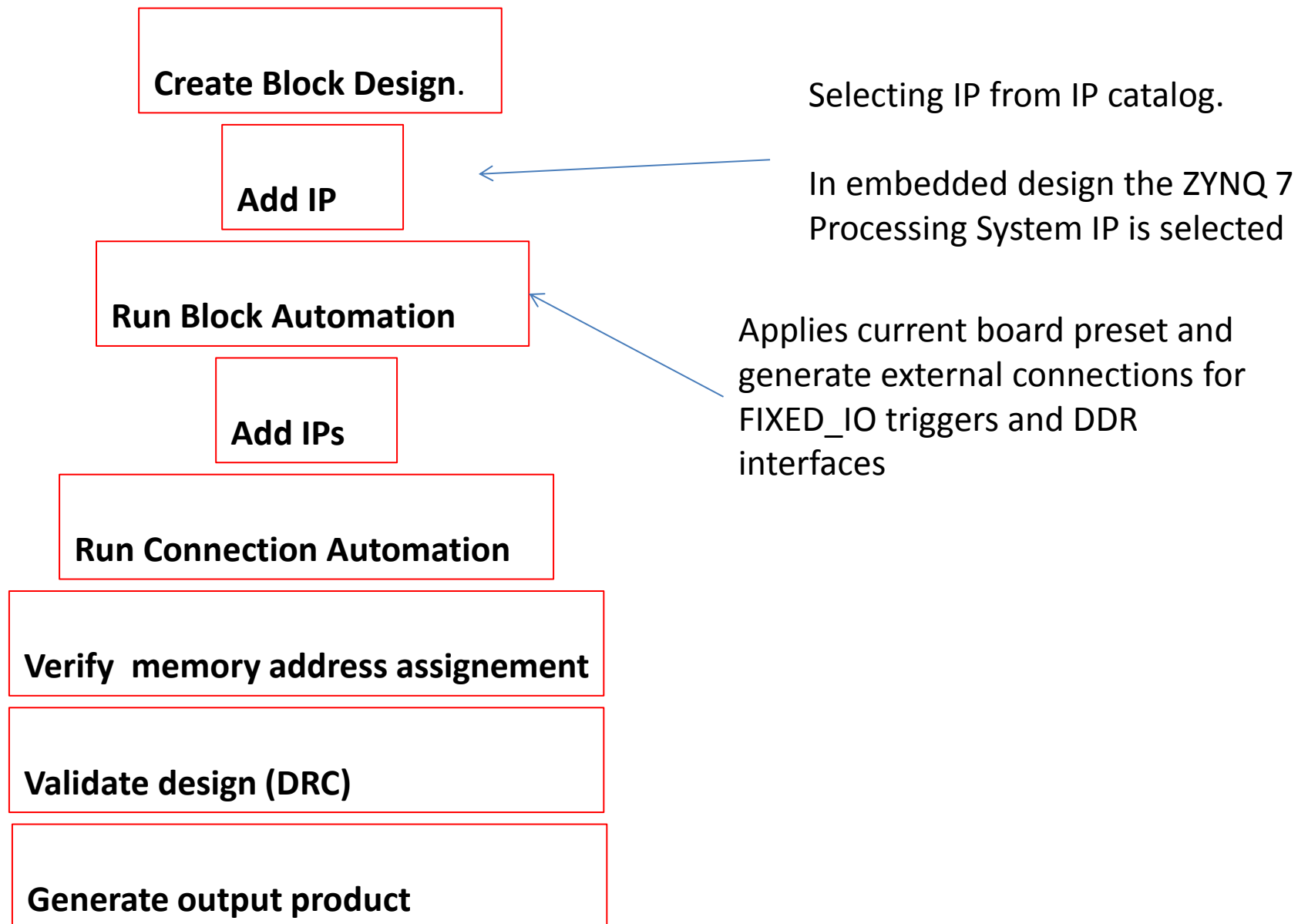
# ■ Creating an IP Integrator design



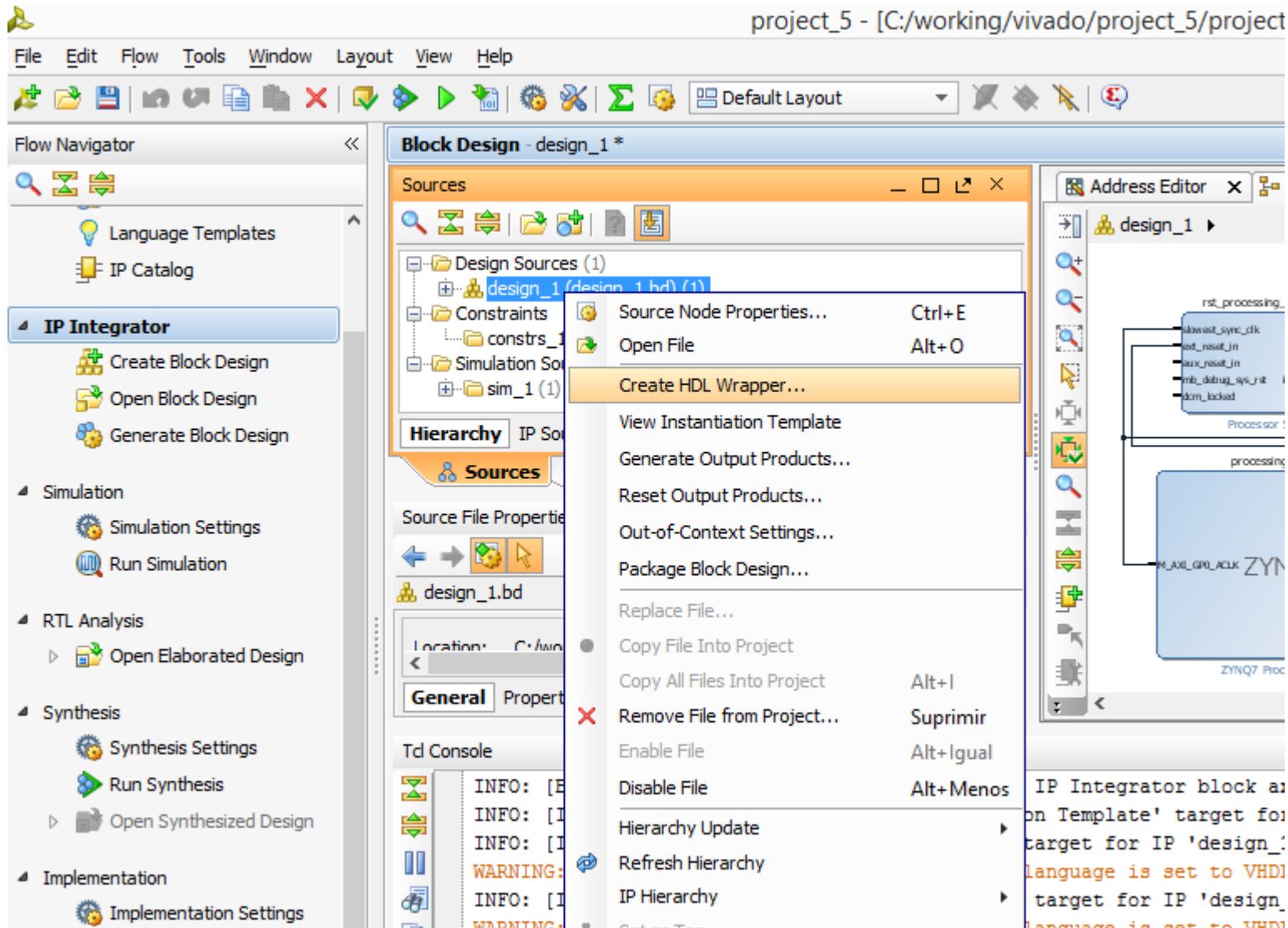
# Creating an IP Integrator design



# ■ Creating an IP Integrator design



9



## Generating VHDL wrapper



# Embedded Processor Hardware Design

PS + PL

- Creating an embedded processor hardware design involves the IP integrator feature of the Vivado Design Suite. In the Vivado IP integrator environment, you instantiate, configure, and assemble the processor core and its interfaces.
- After the design is compiled through implementation, it is exported to the Xilinx Software Development Kit (SDK) for use in the software development and validation flows
- Simulation and debug features

# Embedded System Hardware Design

## PS + PL

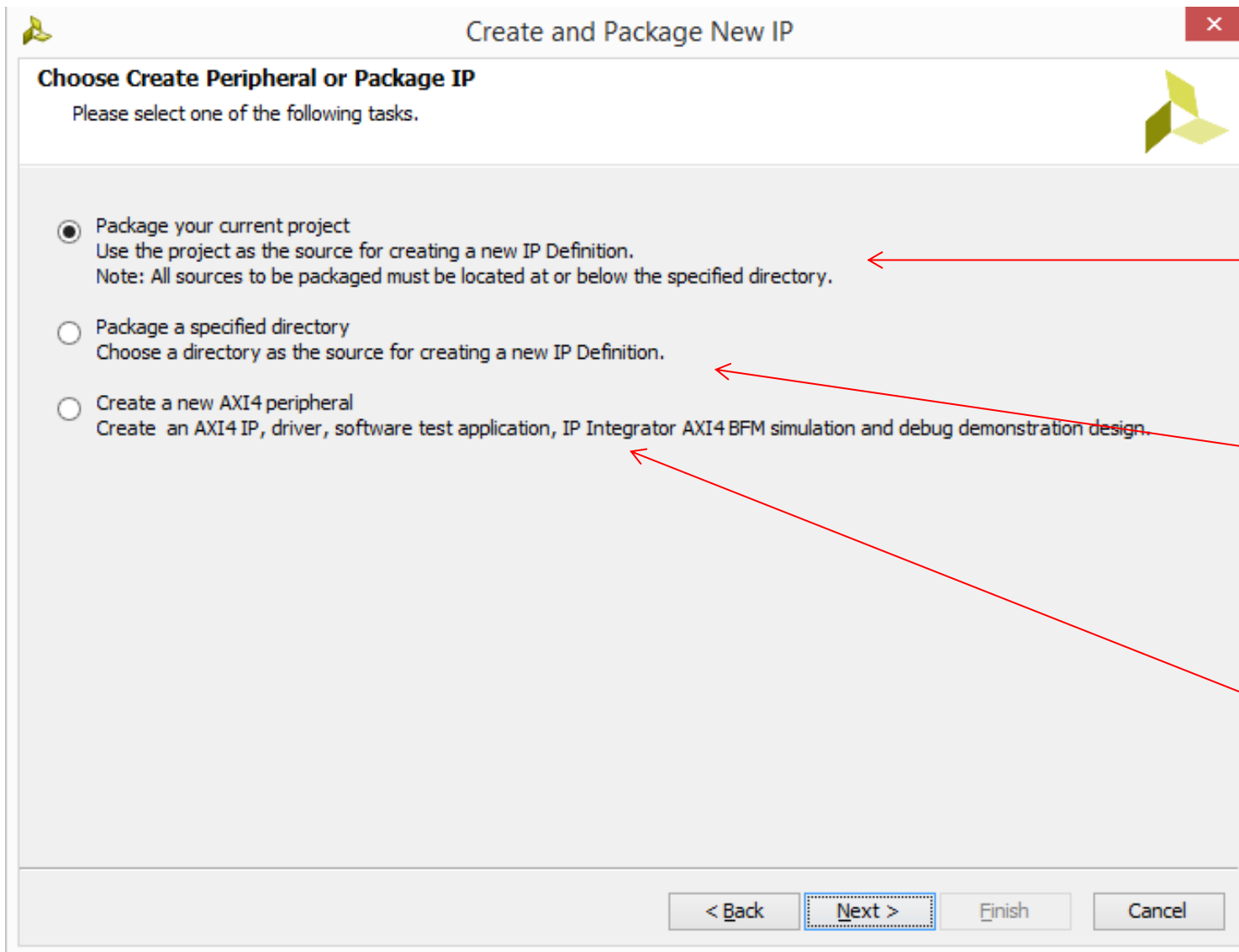
- Hardware Ips can be added in PL part.
- IP can include logic, embedded processors, digital signal processing (DSP) modules, or C-based DSP algorithm designs.
- Custom IP is packaged following IP-XACT protocol and then made available through the Vivado IP catalog
- Xilinx IP utilizes the AMBA AXI4 interconnect standard to enable faster system-level integration

# Embedded System Hardware Design

## PS + PL

- You can interactively configure and connect IP using a block design style interface
- Connection automation is provided as well as a set of DRCs to ensure proper IP configuration and connectivity.
- Connecting the IP using standard interfaces saves time over traditional RTL-based connectivity.
- These IP block designs are then validated, packaged, and treated as a single design source.

# Create and Package new IP

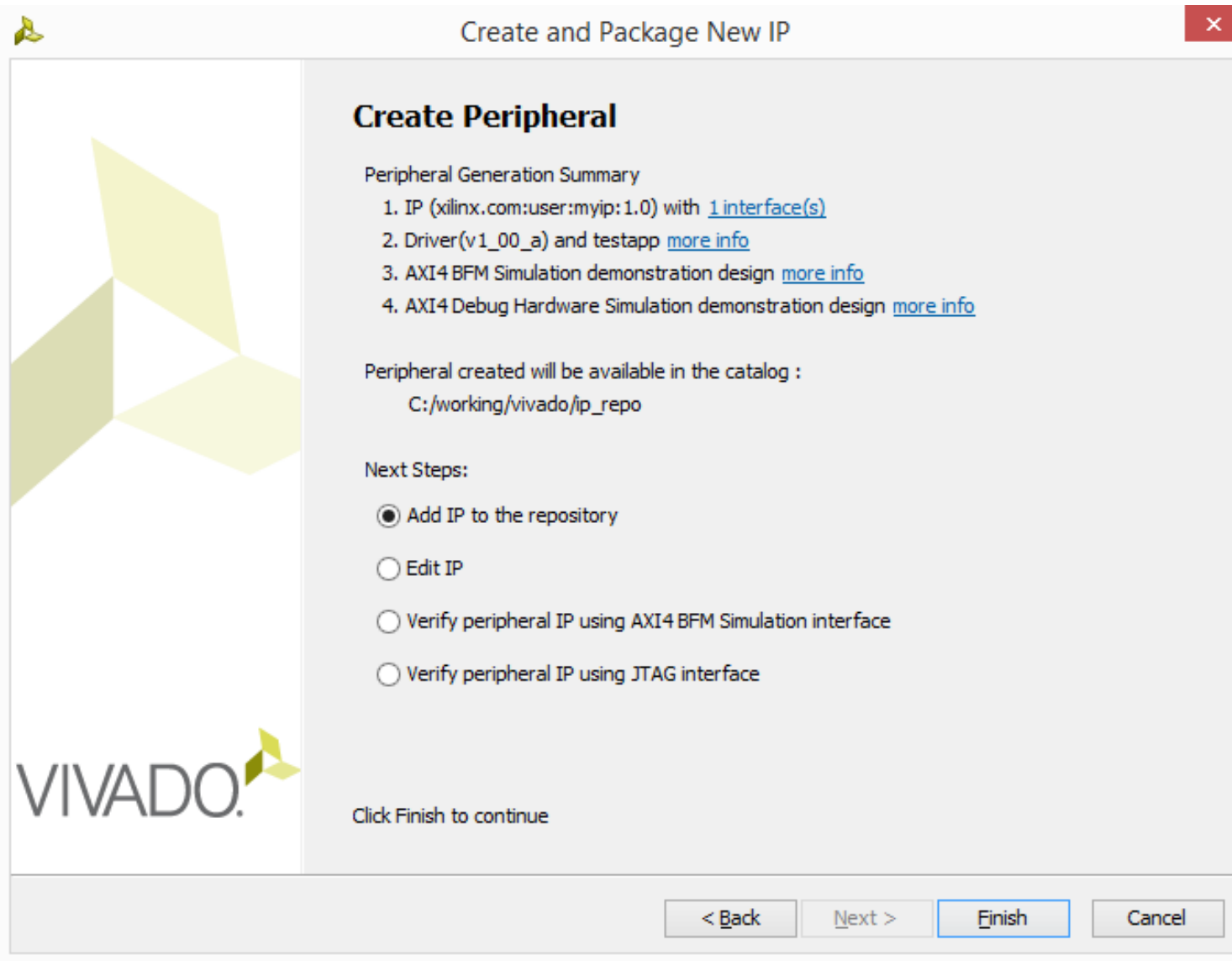


This option lets you package the files associated with your current Vivado project

This option lets you package the files underneath a specific directory within the file system

This option lets you create and package a new AXI4 peripheral with master or slave interface mode.

# Create and Package new IP



# DSP Design

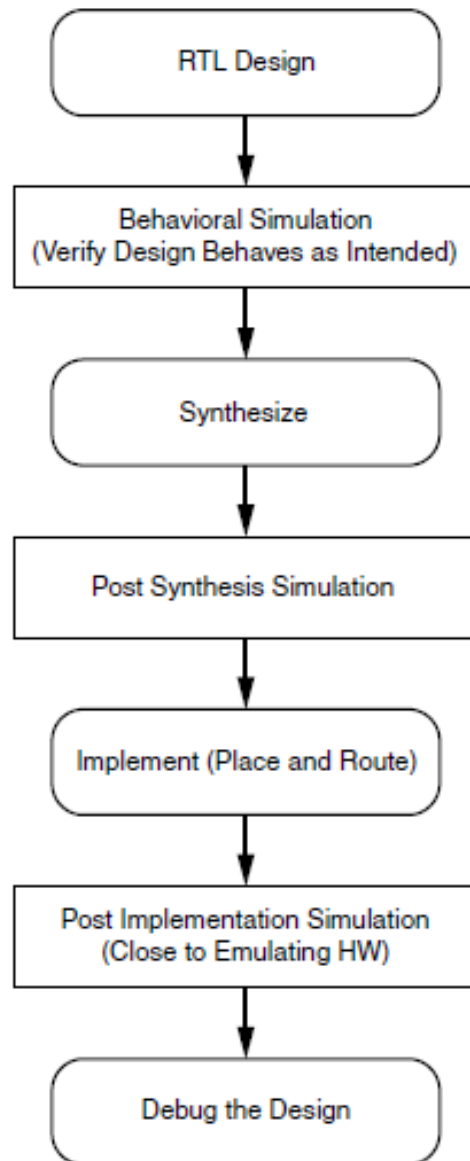
- The Vivado Design Suite is also integrated directly with the **Xilinx System Generator tool** to provide a solution for implementing DSP functions
- The C-based High-Level Synthesis (HLS) tool within the Vivado Design Suite enables you to describe various DSP functions in the design using C, C++, System C, and OpenCL languages
- C-to-RTL synthesis transforms the C-based design into an RTL module that can be packaged and implemented with the rest of the design. This module can then be instantiated into the RTL design or within Vivado IP integrator

System Generator is a DSP design tool from Xilinx that enables the use of the MathWorks model-based Simulink® design environment for FPGA design.

# Design Analysis and Verification

- Design analysis and verification is enabled at each stage of the flow.
- Design analysis features include logic simulation, I/O and clock planning, power analysis, constraint definition and timing analysis, design rule checks (DRC), visualization of design logic, analysis and modification of implementation results, and programming and debugging.

# Simulation flow



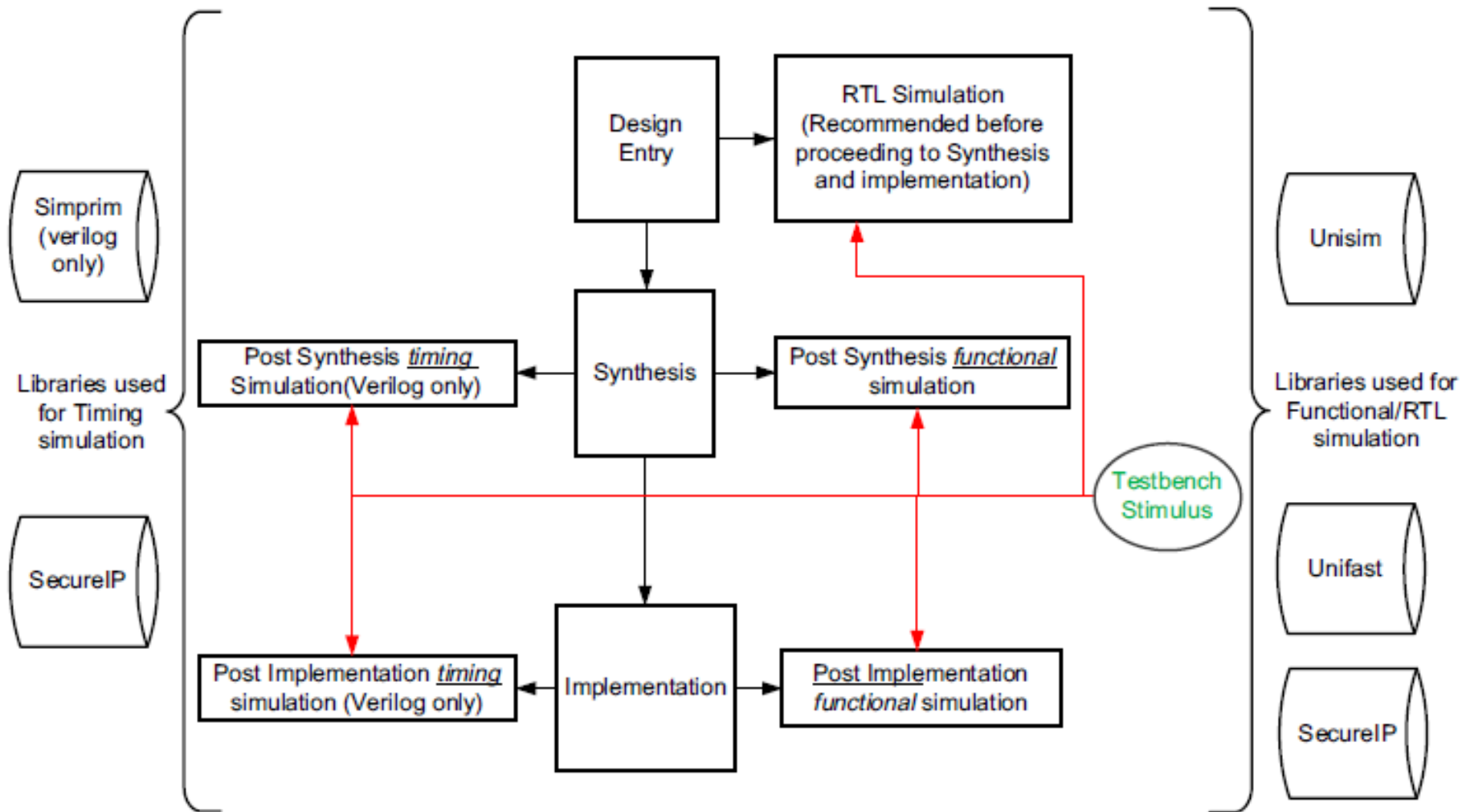
The process of simulation includes:

- Creating a test bench that reflects the simulation actions you want to run
- Selecting and declaring the libraries you need to use
- Compiling your libraries (if using a third-party simulator)
- Netlist generation (if performing post-synthesis or post-implementation simulation)
- Understanding the use of global reset and 3-state in Xilinx devices



# Simulation flow

Simulation at various points in the design flow



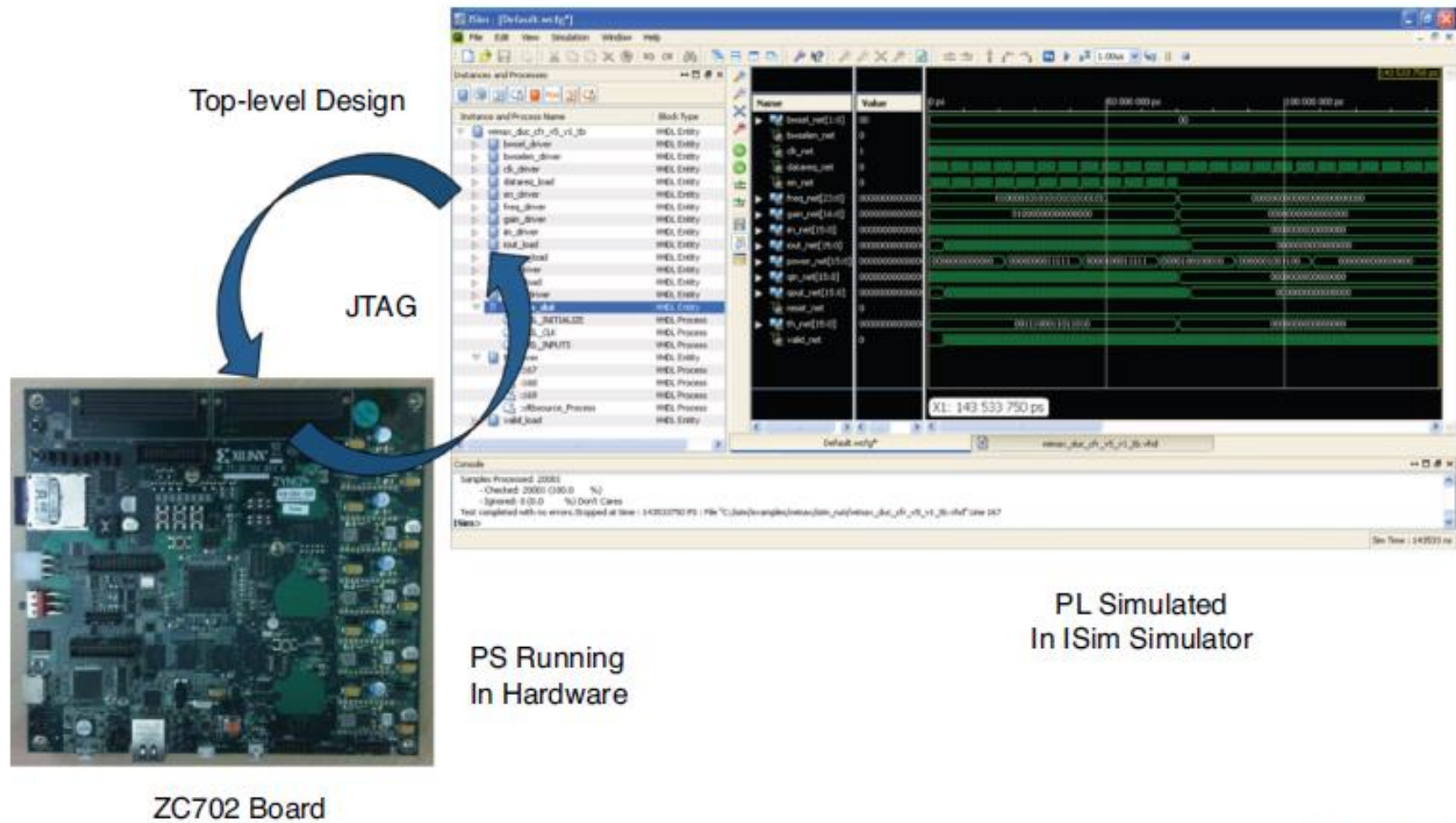
# Simulation libraries

Library Name	Description	VHDL Library Name	Verilog Library Name
UNISIM	Functional simulation of Xilinx primitives.	UNISIM	UNISIMS_VER
UNIMACRO	Functional simulation of Xilinx macros.	UNIMACRO	UNIMACRO_VER
UNIFAST	Fast simulation library.	UNIFAST	UNIFAST_VER
SIMPRIM	Timing simulation of Xilinx primitives.	N/A	SIMPRIMS_VER <sup>a</sup>
SECUREIP	Simulation library for both functional and timing simulation of Xilinx device features, such as the: <ul style="list-style-type: none"><li>• PCIe<sup>®</sup> IP</li><li>• Gigabit Transceiver</li></ul>	SECUREIP	SECUREIP

# Soported Simulators

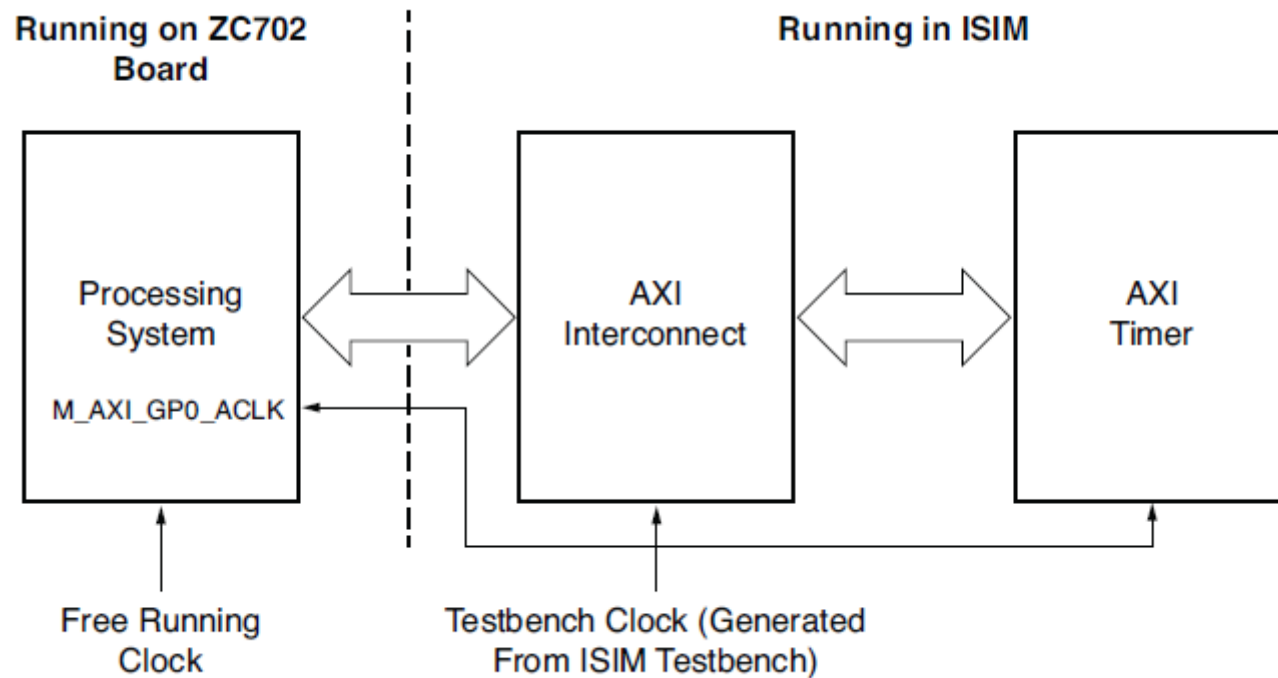
- Vivado simulator: Integrated in the Vivado IDE.
- Mentor Graphics QuestaSim/ModelSim: Integrated in the Vivado IDE.
- Cadence Incisive Enterprise Simulator (IES).
- Synopsys VCS and VCS MX.
- Aldec Active-HDL and Rivera-PRO\*.

# HIL simulation



XAPP744\_01\_090512

# HIL simulation



XAPP744\_04\_090512

# BFM simulation

- The Xilinx® LogiCORE™ IP AXI Bus Functional Model (BFM) cores, developed for Xilinx by Cadence® Design Systems, support the simulation of customer-designed AXI-based IP.
- AXI BFM cores support all versions of AXI (AXI3, AXI4, AXI4-Lite, and AXI4-Stream).
- The BFM's are encrypted Verilog modules.
- BFM operation is controlled by using a sequence of Verilog tasks contained in a Verilog-syntax text file

# Documentation and tutorials

Xilinx Documentation Navigator 2014.4 - Catalog View

Catalog View | Design Hub View | ug1118-vivado-creating-packaging-custom-ip.pdf

Catalog 2014.11.18 | Update Catalog... | Xilinx Design Tools 2014.4/14.7 | Vivado Docs

Document Filters

- ☐ UltraScale
- ☒ Zynq-7000
- ☐ 7 Series
- ☐ Virtex-6
- ☐ Virtex-5
- ☐ Spartan-6
- ☐ CoolRunner
- ☐ Design Tools
  - ☐ ChipScope
  - ☐ EDK and SDK
  - ☐ ISE
  - ☐ PetaLinux
  - ☐ PlanAhead
  - ☐ System Generator
  - ☒ Vivado
- ☐ IP
  - ☐ IP
- ☒ Document Types
  - ☒ Application Notes
  - ☒ Characterization Reports
  - ☒ Customer Notices
  - ☒ Data Sheets
  - ☒ Design Advisories
  - ☒ Design Hubs
  - ☒ Errata
  - ☒ Help
  - ☒ Methodology Guides
  - ☒ Package Specifications
  - ☒ Product Guides
  - ☒ Product Pages

Displaying 329 of 3328 Documents (Collapsed Items)

	Doc ID	Version	MB	Published	Status
<b>Zynq-7000: Data Sheets</b>					
Zynq-7000 All Programmable SoC Overview	DS190	V1.8	0.7	2015-05-27	Recent Update
Zynq-7000 All Programmable SoC Product Table	XMP087	V1.11	0.0	2015-05-27	Recent Update
Zynq-7000 All Programmable SoC (Z-7010, Z-7015, and Z-7020) Data Sheet: DC and AC Switching Characteristics Data Sheet	DS187	V1.15	2.2	2015-02-23	Current
Zynq-7000 All Programmable SoC (Z-7030, Z-7045, and Z-7100) DC and AC Switching Characteristics Data Sheet	DS191	V1.14	2.6	2015-02-23	Current
XA Zynq-7000 All Programmable SoC Overview	DS188	V1.2	0.8	2014-10-10	Current
Defense-Grade Zynq-7000Q All Programmable SoC	DS196	V1.2	0.6	2014-11-25	Current
Zynq-7000 Bus Functional Model v2.0 Data Sheet	DS897	V2.0	0.2	2014-10-01	Current
Zynq-7000 Bus Functional Model v1.1 Data Sheet	DS897	V1.1	0.3	2013-05-24	Current
<b>Zynq-7000: User Guides</b>					
Zynq-7000 All Programmable SoC Software Developers Guide	UG821	V10.0	1.6	2014-03-10	Current
Zynq-7000 All Programmable SoC Technical Reference Manual	UG585	V1.10	16.2	2015-04-09	Current
Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide	UG933	V1.9	2.6	2015-05-22	Recent Update
Zynq-7000 All Programmable SoC Packaging and Pinout Specification	UG865	V1.5	7.1	2014-11-17	Current
Programming ARM TrustZone Architecture on the Xilinx Zynq-7000 All Programmable SoC User Guide	UG1019	V1.0	0.8	2014-05-06	Current
7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide	UG480	V1.7	3.0	2015-05-19	Recent Update
Device Reliability Report - Second Quarter 2014	UG116	V10.2.1	2.3	2015-03-09	Current
<b>Zynq-7000: Embedded Design Documents</b>					
Vivado Design Suite User Guide: Embedded Processor Hardware Design	UG898	V2014.3	15.2	2014-10-16	Current
Vivado Design Suite Tutorial: Embedded Processor Hardware Design	UG940	V2014.3	4.4	2014-10-01	Current
Zynq-7000 All Programmable SoC: Concepts, Tools, and Techniques Guide (ISE Design Suite)	UG873	V14.6	3.7	2013-06-19	Current
The Zynq Book					

# Thank you for your attention

**Contact information**

**[Juliodaniel.dondo@uclm.es](mailto:Juliodaniel.dondo@uclm.es)**