Joint ICTP-IAEA School on
Systems-on-Chip based on
FPGA for Scientific Instrumentation
and Reconfigurable Computing

System on a Programable Chip (SoPC)

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Some background from you….

Who knows about VHDL/Verilog?

Who knows about FPGA?

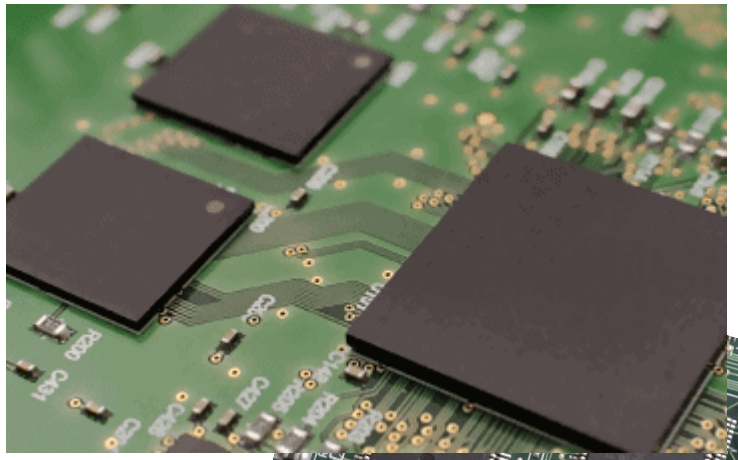
Who knows about SoC?

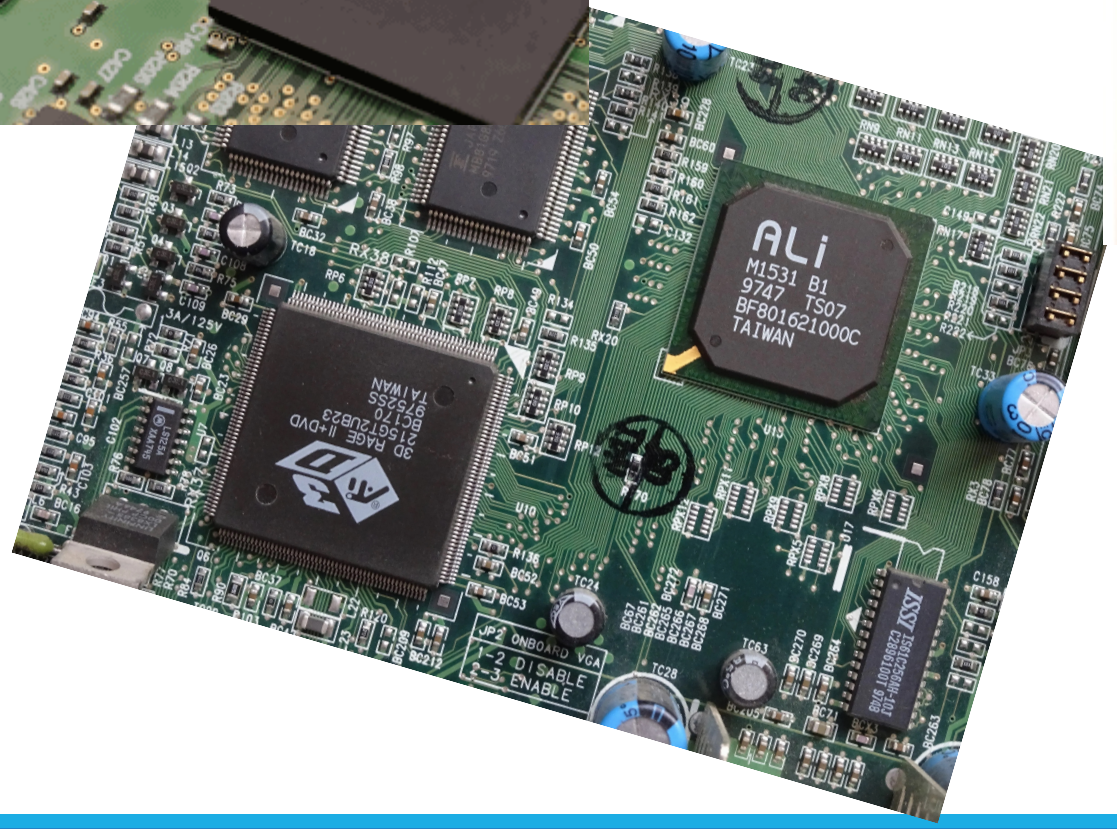
Who knows about ….. ?

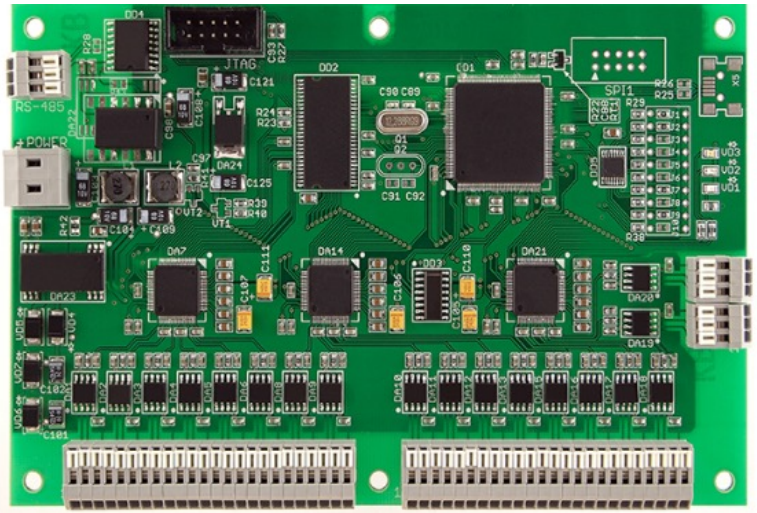
Who knows about ‘C’?

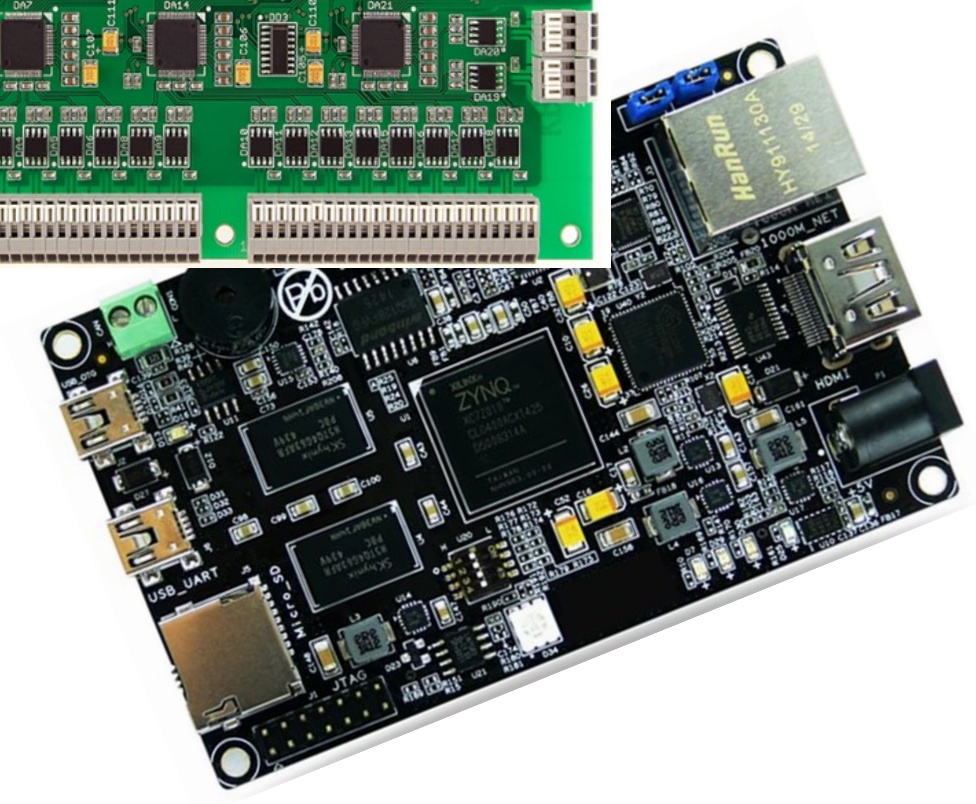
Who knows about ….. ?

Integrated Ciruitcs - High Level View

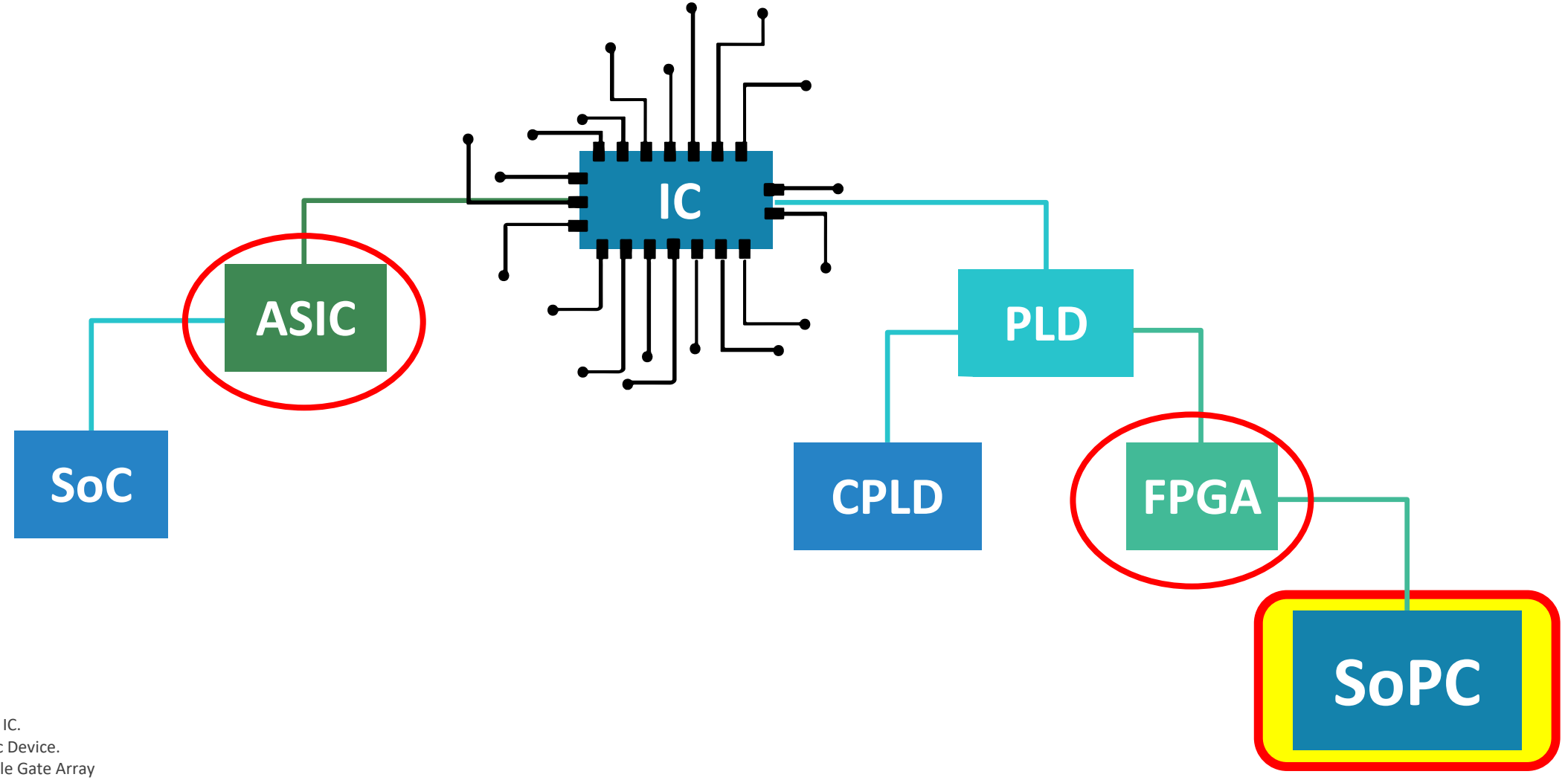








Integrated Circuit App Clasification



ASIC: application specific IC.
PLD: Programmable Logic Device.
FPGA: Field Programmable Gate Array
SoC: System on a Chip.
SoPC: System on a Programmable Chip.

What is an ASIC ?

An **application-specific integrated circuit** (**ASIC**) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use.

Modern **ASICs** often include entire microprocessors, memory blocks, interface blocks and other large building blocks. Such an **ASIC** is often termed a **SoC** (System-on-a-Chip).

Designers of digital ASICs often use a **Hardware Description Language** (HDL), such as **Verilog** or **VHDL**, to describe the functionality of **ASICs**.

What is an *FPGA* ?

F Field

P Programmable

G Gate

A Array

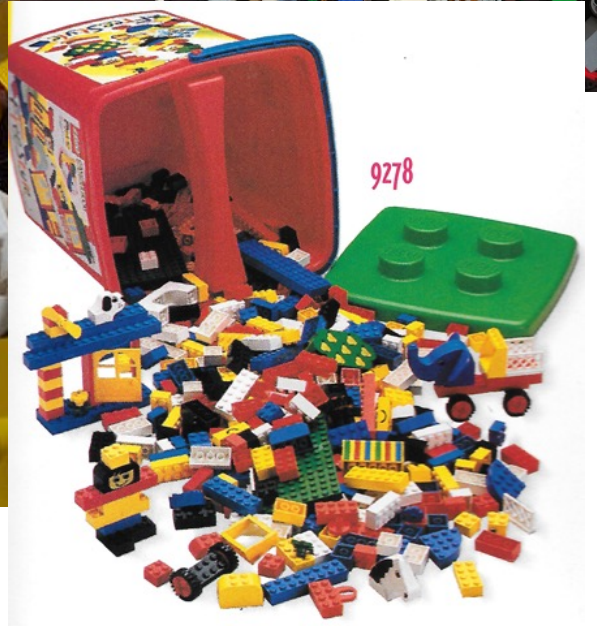
What is an FPGA ?

A **field-programmable gate array** (**FPGA**) is an integrated circuit (IC) *designed to be configured* by a customer or a designer after manufacturing (that is the reason of the term *field programmable*).

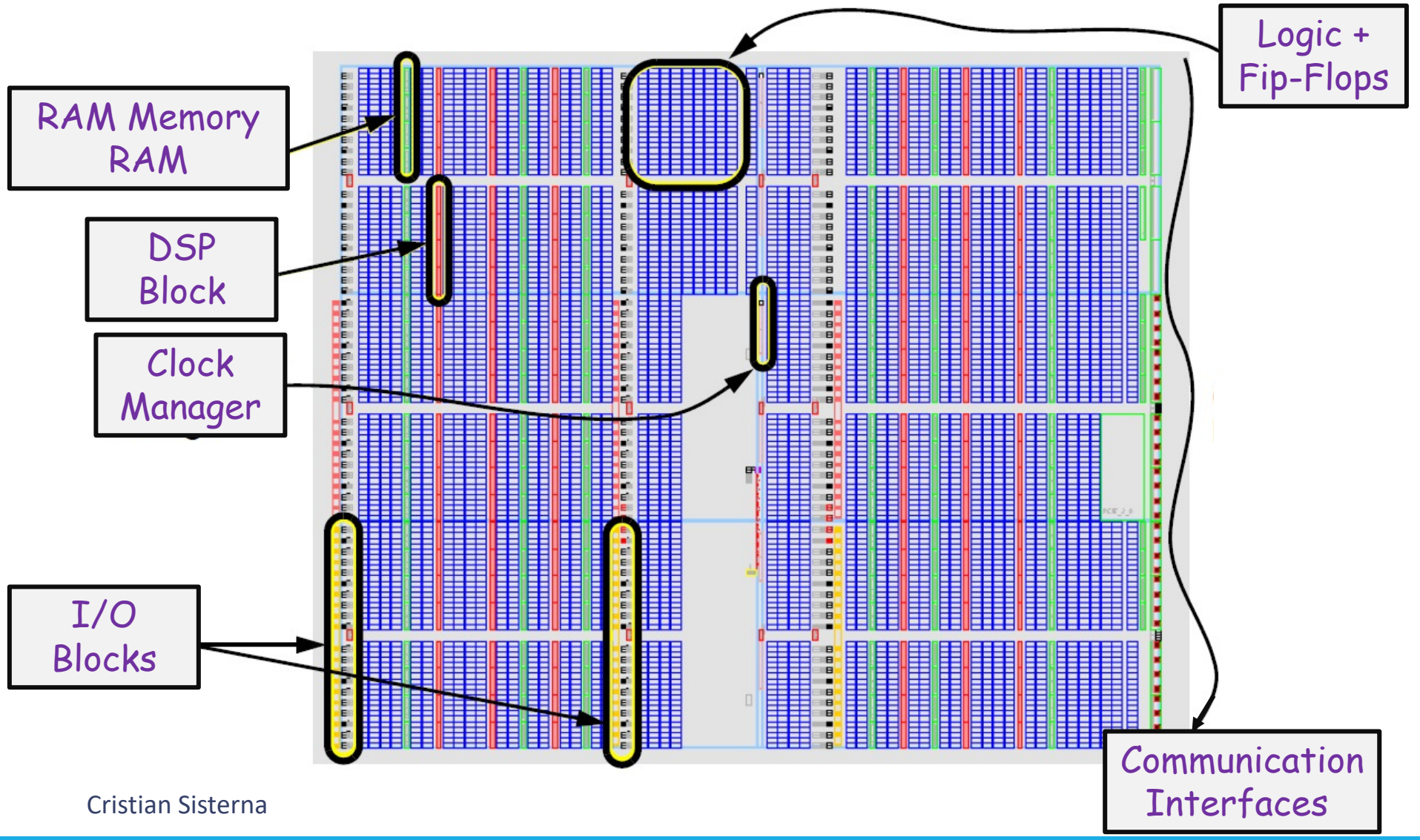
FPGA are not made to be application-specific as opposed to **ASICs**.

FPGA configuration is generally specified using an HDL language (either Verilog or VHDL) .

FPGA ~ Lego Bricks



FPGA Basic Architectural View

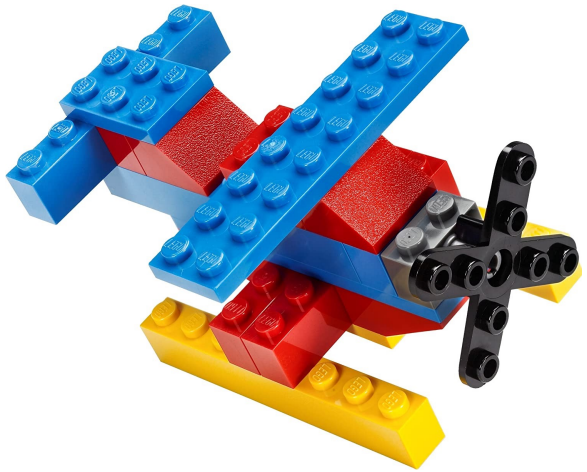


Cristian Sisterna

ASIC – FPGA

ASIC

FPGA 1



FPGA 2

What is a SoC ?

A **S**ystem-**o**n-a-**C**hip (SoC) is an integrated circuit that integrates most or all components of a computer or other electronic system.

A **SoC** usually includes a Central Processing Unit (CPU), Memories, I/O interfaces, Digital Signal Processing (DSP) blocks, digital-analog mixed signals components, etc., all on a single IC.

System-on-a-Chip (SoC)

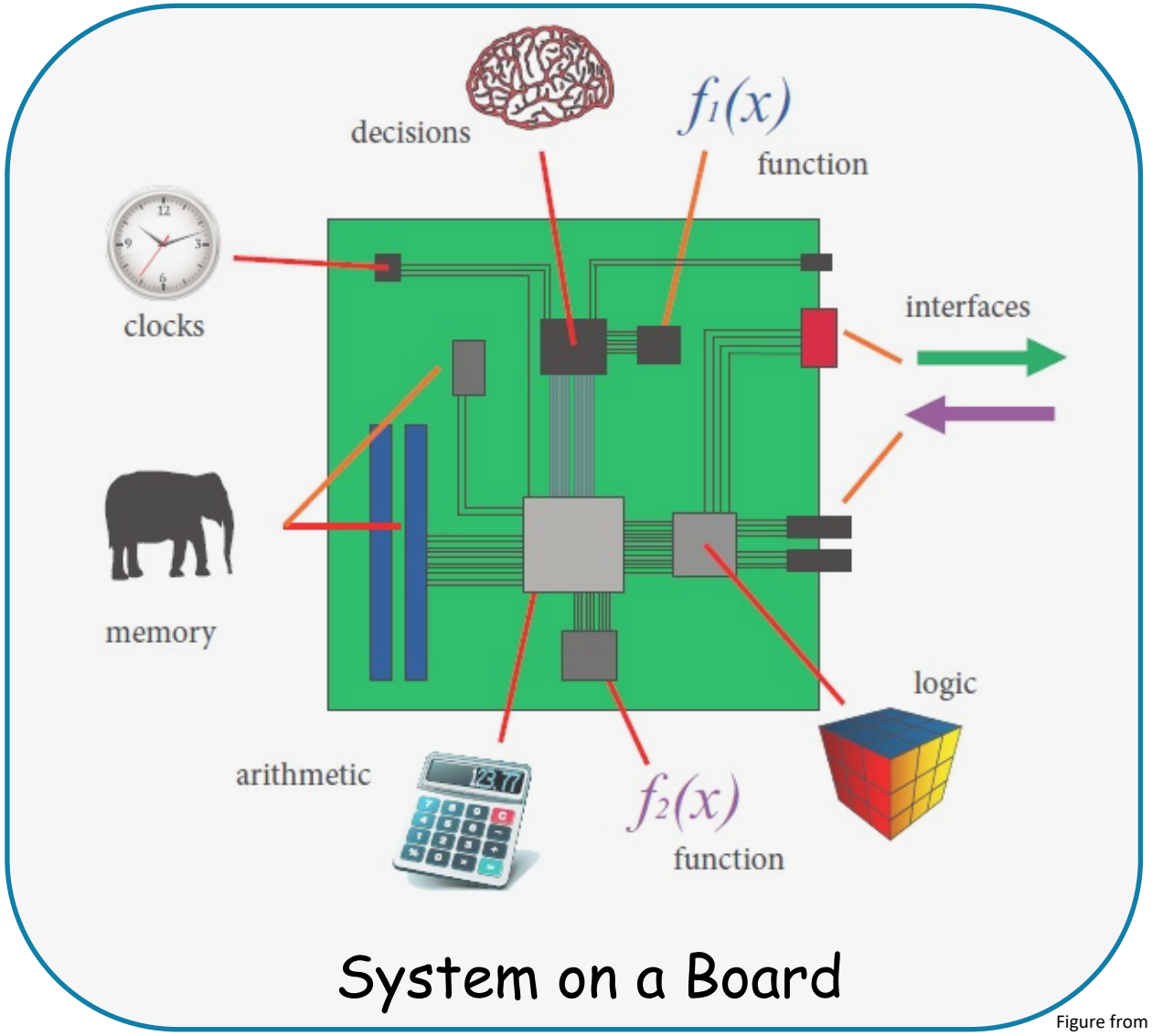
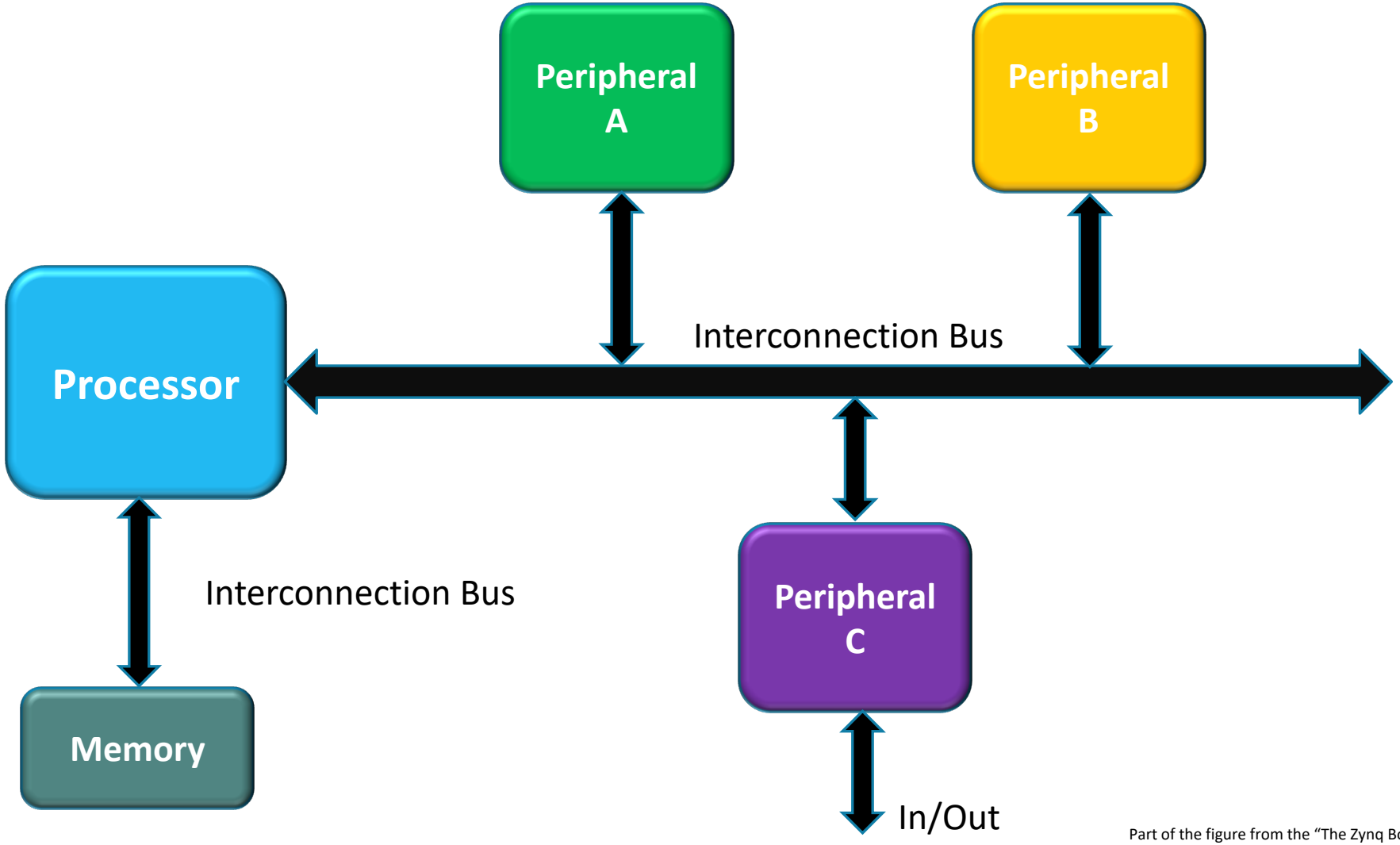


Figure from the "The Zynq Book

A *SIMPLE* View of an Embedded SoC



Part of the figure from the "The Zynq Book"

SoPC: Software System, Hardware System

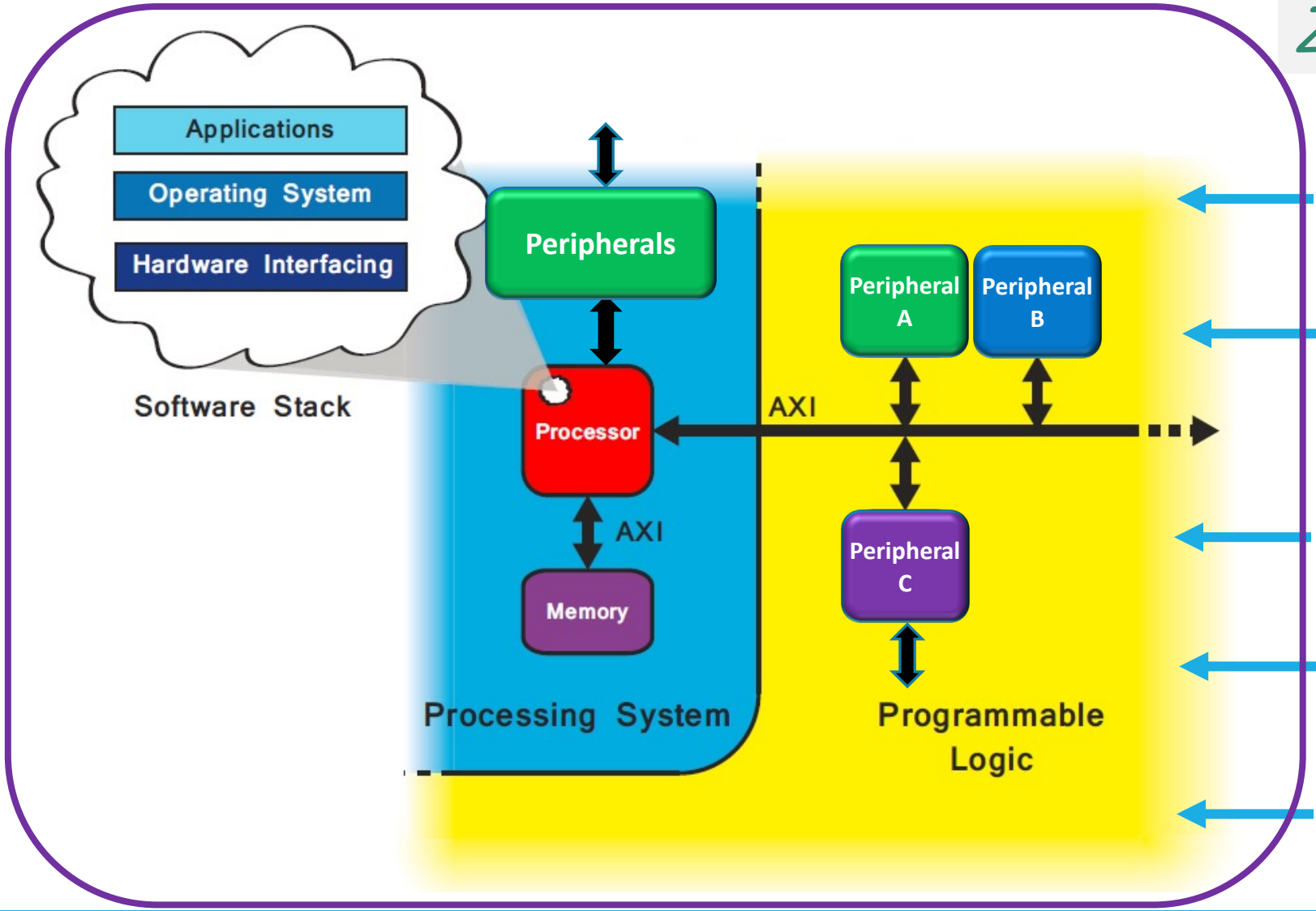


Figure from the "The Zynq Book"

ASIC SoC vs System on Programmable Chip (SoPC)

ASIC SoC

- Development Time
- Cost
- Lack of flexibility
- Great performance
- Tiny size
- Very large amount of logic
- Power Efficient
- Support analog and mixed signal designs

SoPC

- Great flexibility
- Fast time-to-market
- Upgrade-ability in the field
- Availability of IP cores
- Cheap and easy to use development tools
- Lower performance
- Power hungry

SmartFusion2 (Microchip)

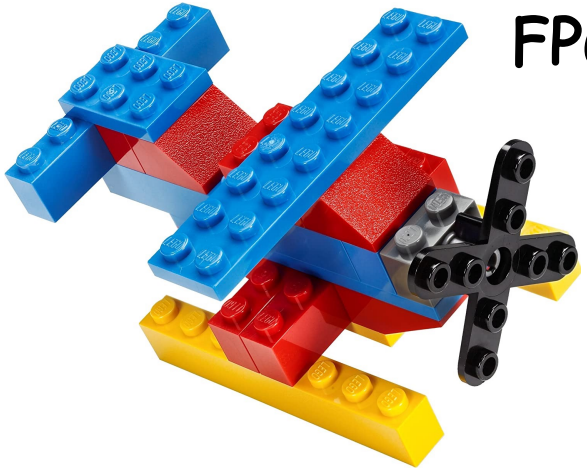
Zynq/Ultra Scale (Xilinx-AMD)

Stratix (Intel)

SoPC

ASIC – FPGA - SoPC

ASIC

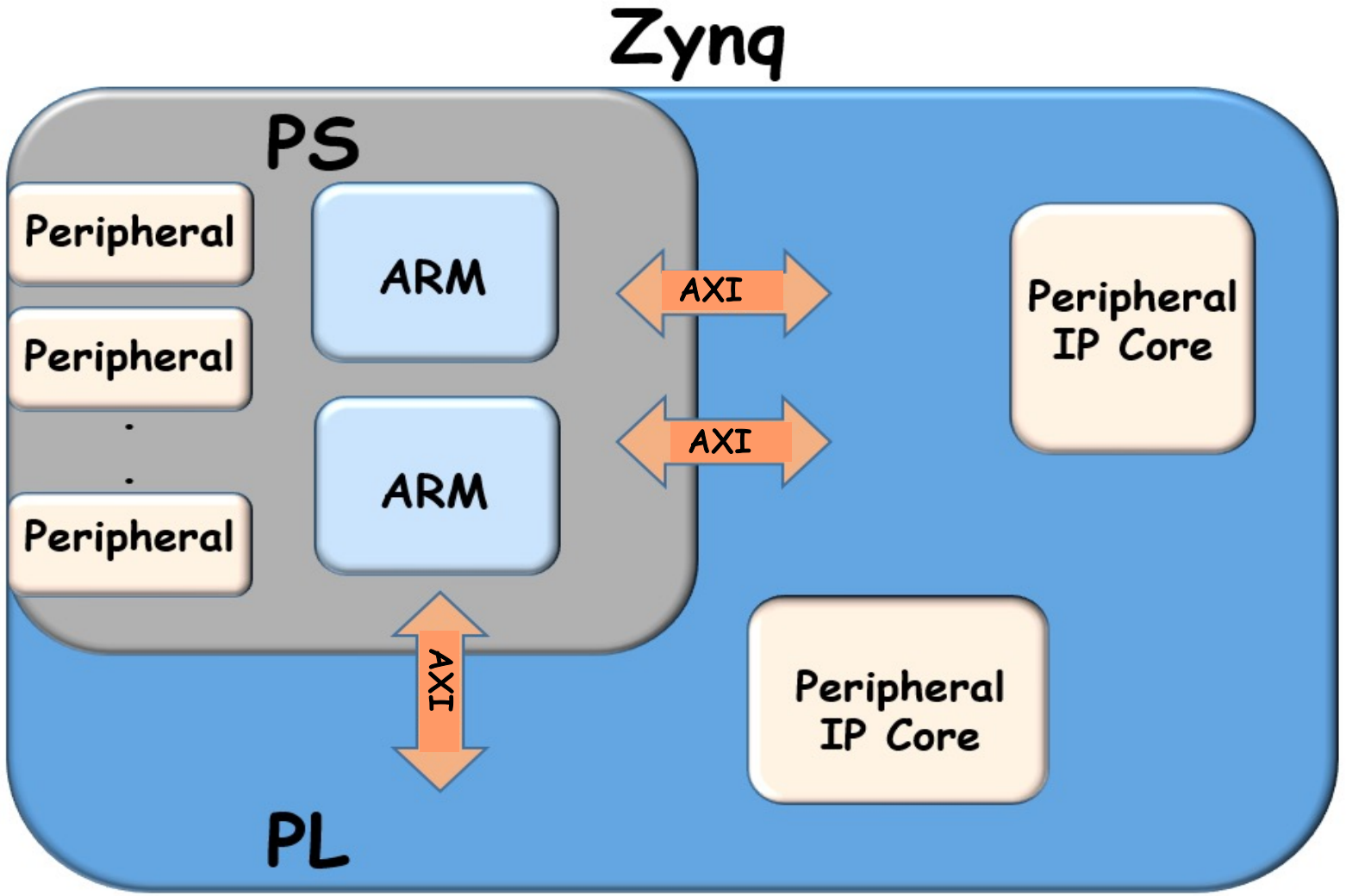


FPGA 1

FPGA 2

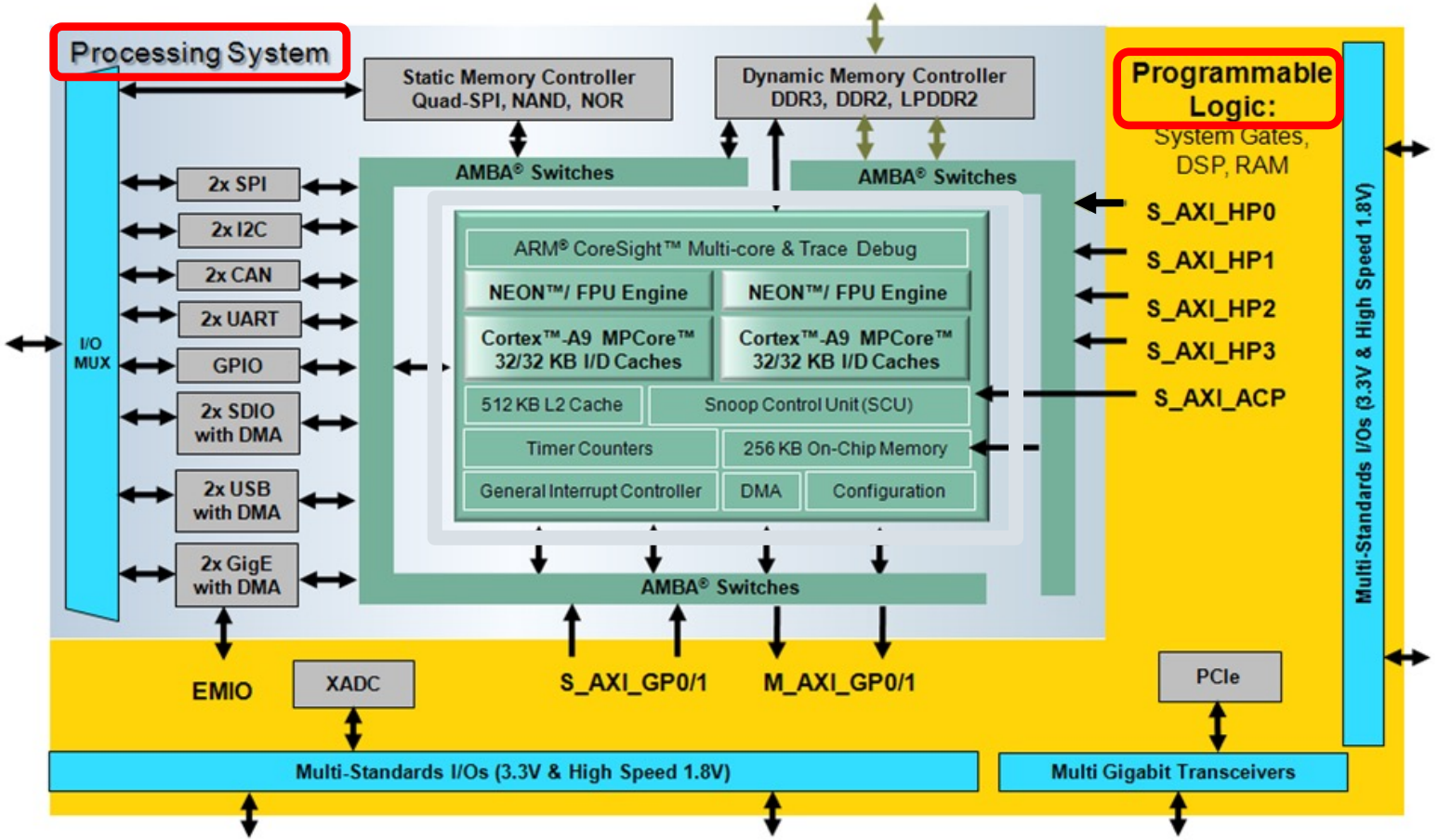
FPGA + ASIC = SoPC

A Simple View of the *AMD Zynq SoPC*



System on Programmable Chip (SoPC)

A SoPC family integrates in a single chip the software programmability of an ARM®-based processor with the hardware configurability of an FPGA



Zynq - AMD SoPC

Architectural View of the *AMD Zynq SoPC*

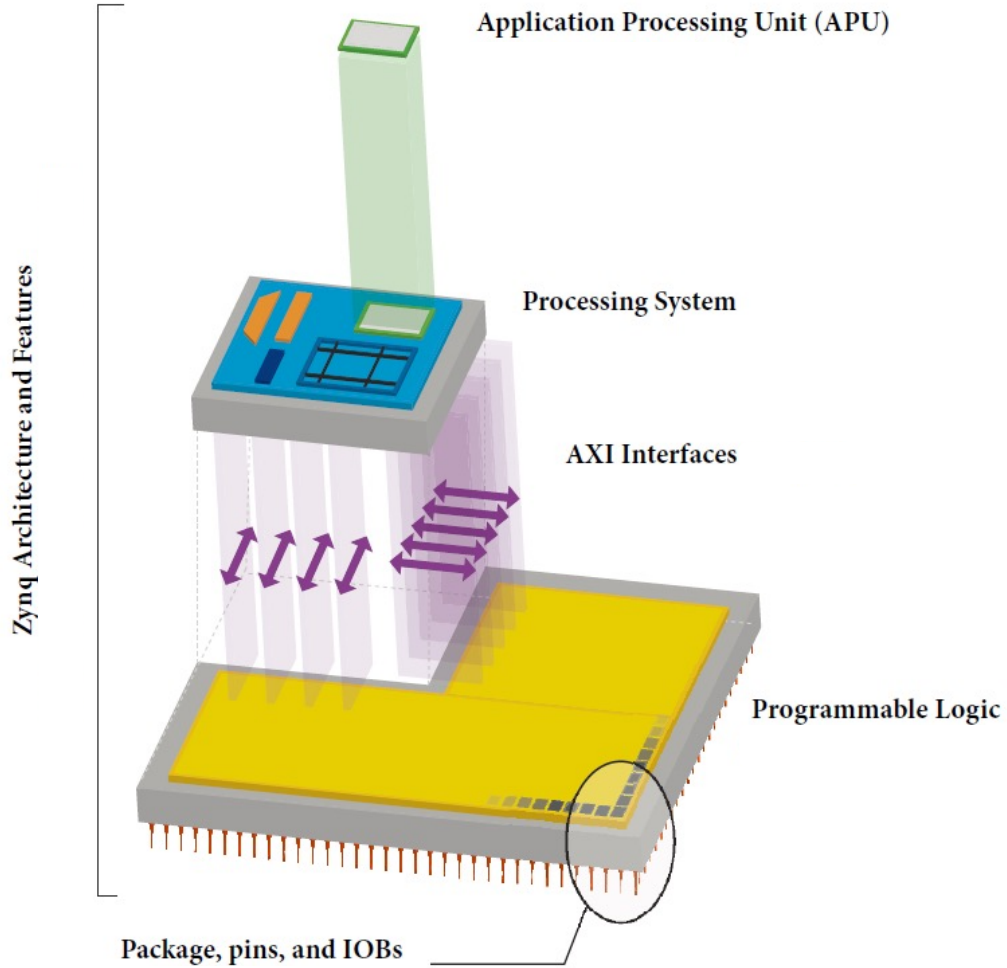
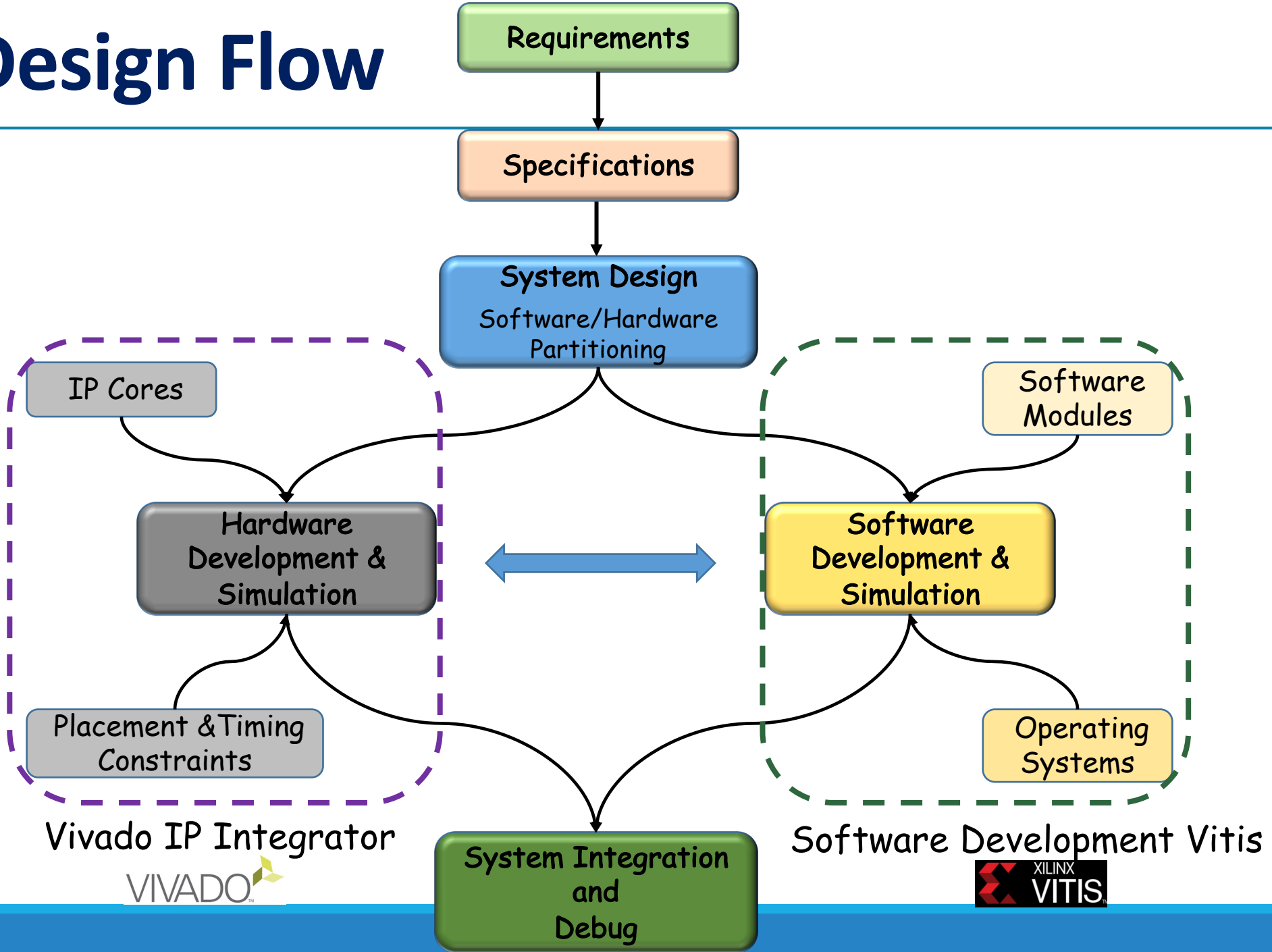


Figure from the "The Zynq Book"

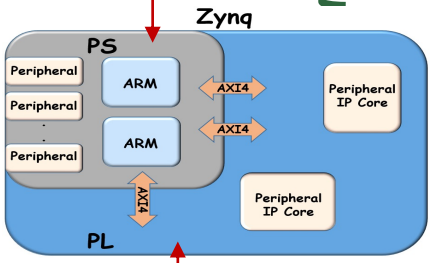
SoPC Design Flow



Hardware and Software Layers in a SoPC

.elf

Software Stack
(Vitis)



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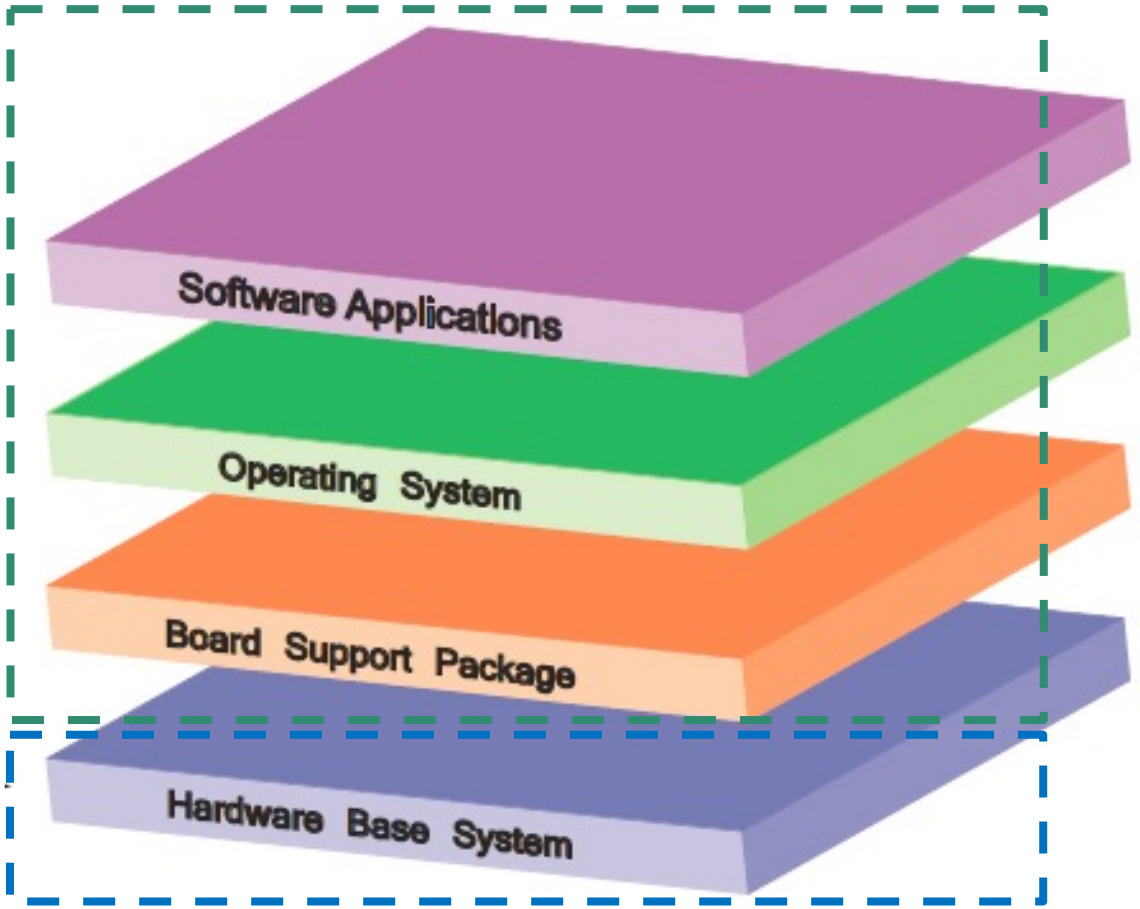
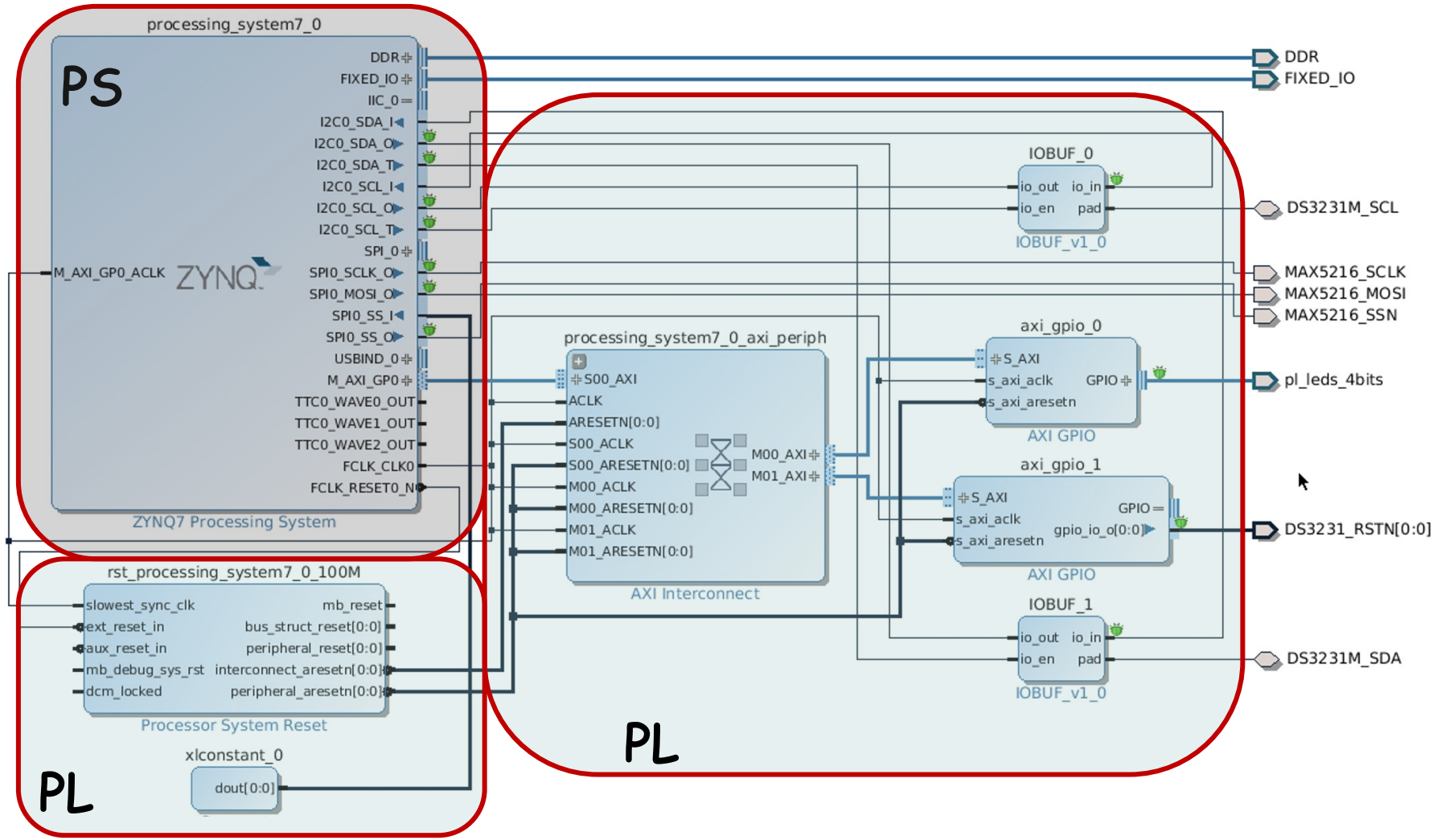
Custom
Hardware-FPGA
(Vivado)



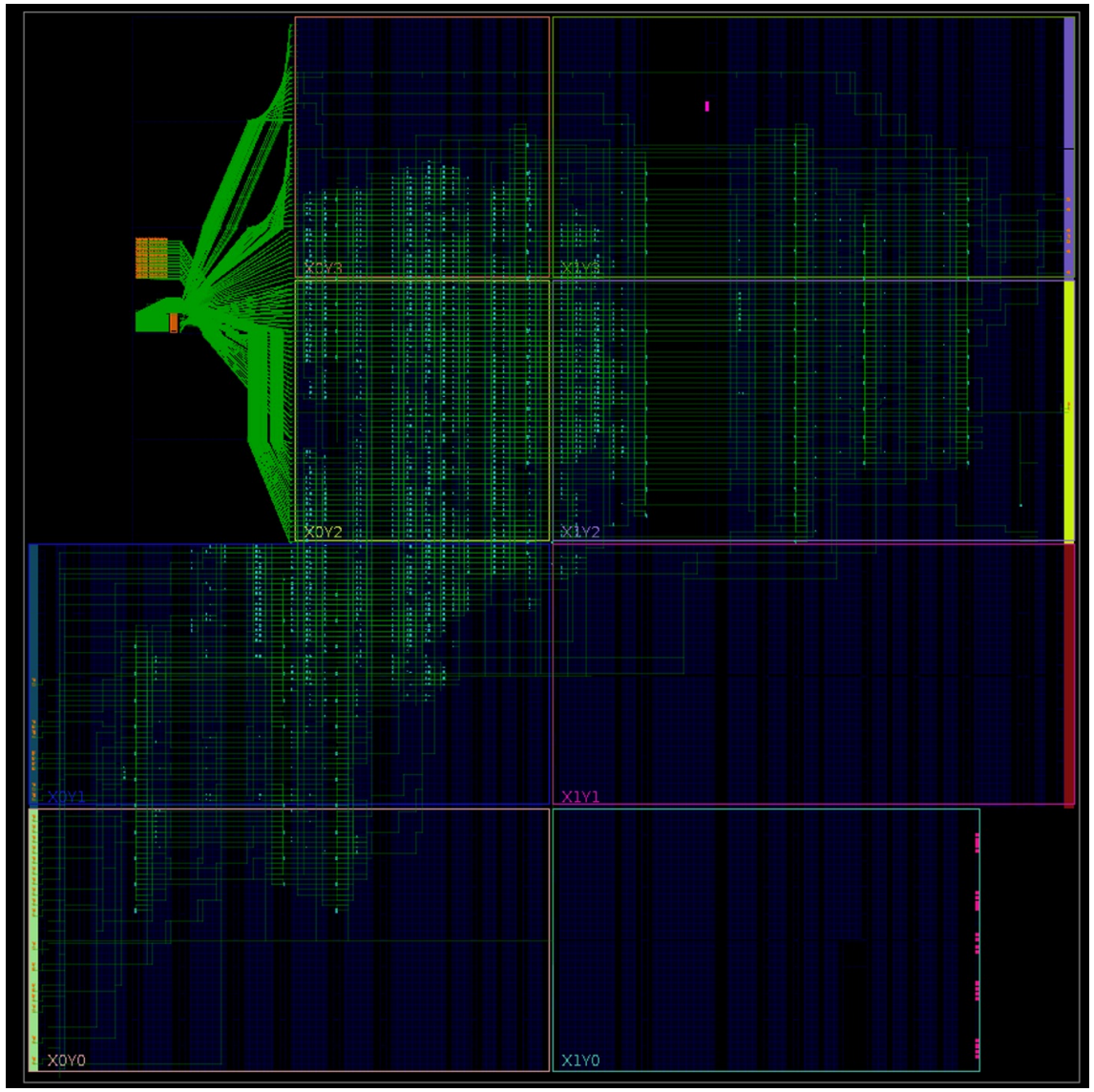
Export
to
Vitis

Figure from the "The Zynq Book"

Zynq Block Design in Vivado – PS + PL



Internal Zynq View – System Placed & Routed



SoC FPGAs Market Availability

Table 1: Commercially-Available SoC FPGAs

	Altera SoC FPGAs	Xilinx Zynq-7000 EPP	Microsemi SmartFusion2
Processor	ARM Cortex-A9	ARM Cortex-A9	ARM Cortex-M3
Processor Class	Application processor	Application processor	Microcontroller
Single or Dual Core	Single or Dual	Dual	Single
Processor Max. Frequency	1.05 GHz	1.0 GHz	166 MHz
L1 Cache	Data: 32 KB Instruction: 32 KB	Data: 32 KB Instruction: 32 KB	No data cache Instruction: 8 KB
L2 Cache	Unified: 512 KB, with error correction code (ECC)	Unified: 512 KB	Not available
Memory Management Unit (MMU)	Yes	Yes	Yes
Floating-Point Unit/NEON™ Multimedia Engine	Yes	Yes	Not available
Acceleration Coherency Port (ACP)	Yes	Yes	Not available
Interrupt Controller	Generic (GIC)	Generic (GIC)	Nested, vectored (NVIC)
On-Chip Processor RAM	64 KB, with ECC	256 KB, no ECC	64 KB, no ECC
Direct Memory Access Controller	8-channel ARM DMA330 32 peripheral requests (FPGA + hard processor system)	8-channel ARM DMA3304 peripheral requests (FPGA only)	1-channel HPDMA 4 requests
External Memory Controller	Yes	Yes	Yes
Memory Types Supported	LPDDR2, DDR2, DDR3L, DDR3	LPDDR2, DDR2, DDR3L, DDR3	LPDDR, DDR2, DDR3
External Memory ECC	16 bit, 32 bit	16 bit	8 bit, 16 bit, 32 bit
External Memory Bus Max. Frequency	400 MHz (Cyclone® V SoC), 533 MHz (Arria® V SoC)	533 MHz	333 MHz
Processor Peripherals	1x quad SPI controller with 4 chip selects 1x NAND controller (single- and multilevel cell - MLC or SLC) 2x 10/100/1G Ethernet controller 2x USB 2.0 On-the-Go (OTG) controller 1x SD/MMC/SDIO controller 2x UART 4x I2C controller 2x CAN controller 2x SPI master, 2x SPI slave controller 4x 32 bit general-purpose timers 2x 32 bit watchdog timers	1x quad SPI or dual quad SPI controller with 2 chip selects x static memory controller (NAND-SLC, NOR, or SSRAM) 2x 10/100/1G Ethernet controller 2x USB 2.0 OTG controller 2x SD/SDIO controller 2x UART 2x I2C controller 2x CAN controller 2x SPI controllers (master or slave) 2x 16 bit triple-mode timer/counters 1x 24 bit watchdog timer	1x 10/100/1G Ethernet controller 2x USB 2.0 OTG controller 2x UART 2x I2C controller 1x CAN controller 2x SPI 2x general-purpose timers 1x watchdog timer 1x real-time clock (RTC)
FPGA Fabric	Cyclone V, Arria V	Artix-7, Kintex-7	Fusion2
FPGA Logic Density Range	25 K to 462 K LE	28 K to 444 K LC	6 K to 146 K LE
Hardened Memory Controllers in FPGA	Up to 3, with ECC	Not available	Not available
High-speed Transceivers	Available at all densities	Higher-density devices only	Higher-density devices only
Analog Mixed Signal (AMS)	Not available	2 x 12-bit, 1 MSPS analog-to- digital converters (ADCs)	Not available
Boot Sequence	Processor first, FPGA first, or both simultaneous	Processor first	Processor boot, FPGA non- volatile

Source: Intel, ab1_soc_fpga.pdf

FPGAs Soft Processors

Sources:

- HDL Code
- Netlist
- Placed & Routed netlist

Common Soft-processors:

- RISC-V
- LEON
- 8051
- OpenRISC

When to use it:

- Cost-sensitive applications
- App where the processor is just a support
- Processor configurability and upgradeability

FPGA Hard Processors (SoPC)

- √ **Xilinx**:
  - √ ARM Cortex A9-dual in Zynq devices
  - √ Cortex A-53 in MPSoC (Zynq Uktrascale+)
- √ **Intel-Altera**
  - √ Cortex A9 dual core in Arria V SoC and Cyclone V SoC
  - √ Cortex A53 in Stratix 10 SoC using 14nm Intel process
- √ **Microchip (former Actel)**
  - √ Smart Fusion uses a Cortex M3 (at 100Mhz) and programmable analog

FPGAs vs Processors

FPGA	Processor
Perform multiple instruction at once. Execution is done in parallel/concurrently. Hence, minimize the latency and maximizes the throughput	Performs only one instruction at a time, because the execution is sequential.
Provides ultra-high memory bandwidth. Dedicated DDR memory blocks for Rd/Wr.	Limited memory bandwidth.
Provides constant latency for each iteration.	Latency depends on the operating system load, and sometimes, on the compilation options.
A microcontroller or a microprocessor can be implemented within an FPGA.	It is not possible to implement an FPGA in a processor.
Very high data processing throughput.	Lower data processing throughput.
It could be expensive.	Usually is cheap.
User-configurable logic, dedicated DSP blocks.	Fixed arithmetic engines.
User configurable I/O ports – Multiple I/O standards.	Fixed, dedicated I/O ports.
Compute intensive algorithms. Massive parallel operations. High data rate computation.	Decision making. Complex Analysis. Block-oriented tasks.

Zynq SoPC *ZedBoard* – Board to be used in the Labs