The Abdus Salam
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IAEA

Joint ICTP-IAEA School on
Systems-on-Chip based on
FPGA for Scientific Instrumentation
and Reconfigurable Computing

The RVI communication block: ComBlock

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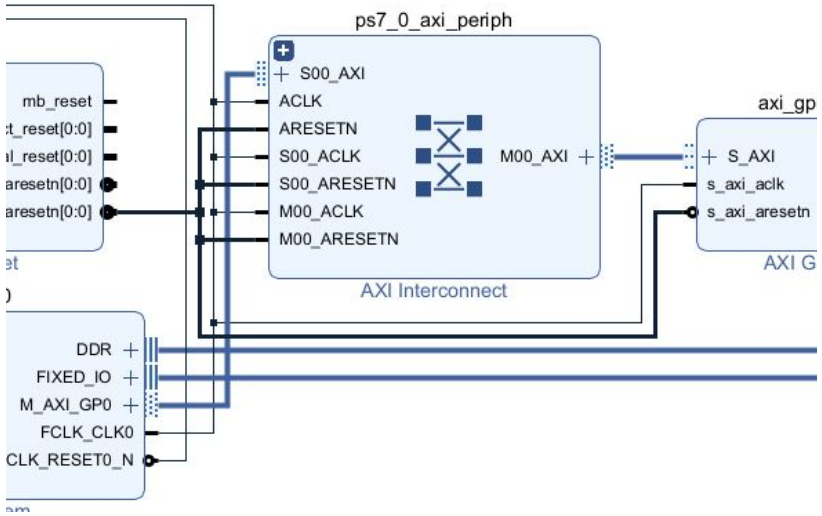
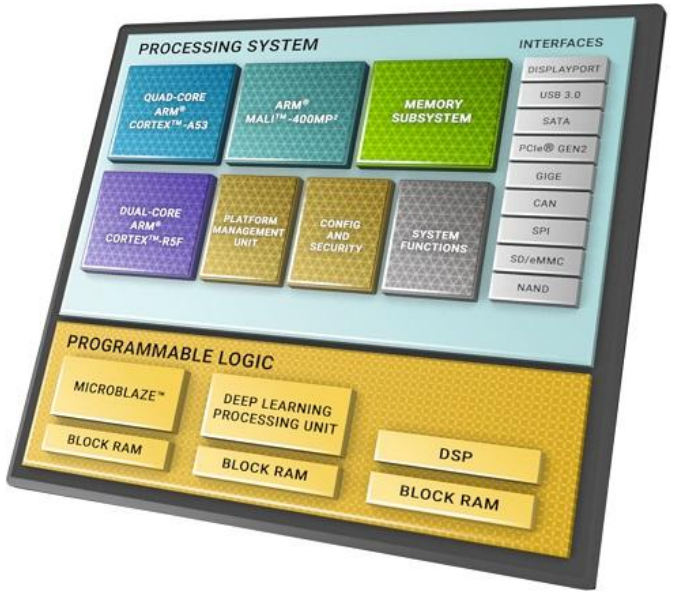
2023

Introduction

- Vendor specific interconnects (AXI, AVALON, Chiplink).
- What we learned yesterday?
  - AXI interconnect,
  - memory address,
  - data.
- Communication Block (ComBlock).

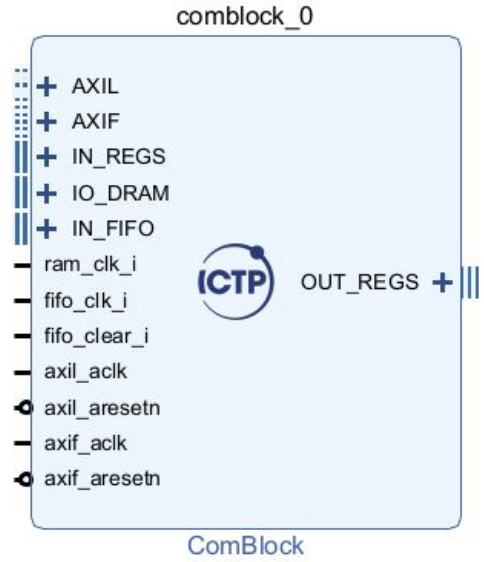




What is the ComBlock?

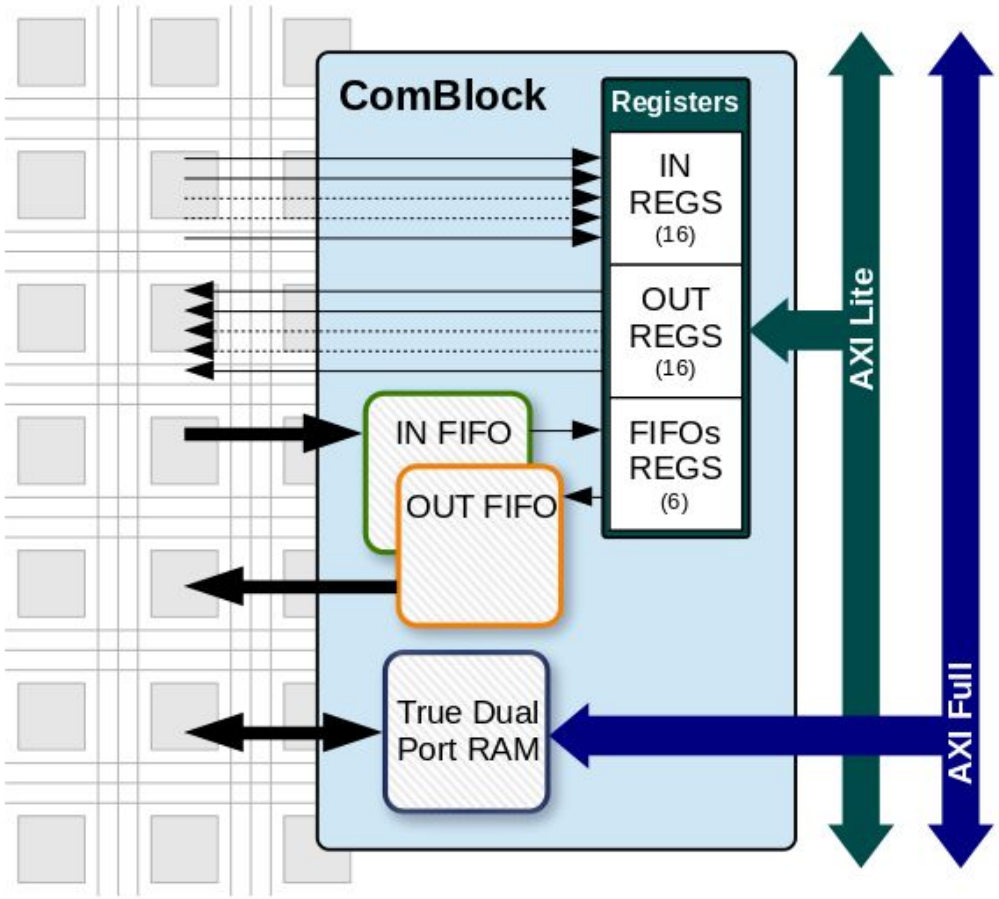
A communication block that abstracts you from the AXI protocol.

- Interconnect: AXI - Known interfaces (registers, RAM and FIFOs).
- Configurable resources, width, length, etc.
- Simple Clock-Domain-Crossing with FIFOs and TDPRAM.
- C driver for easy complete project integration.



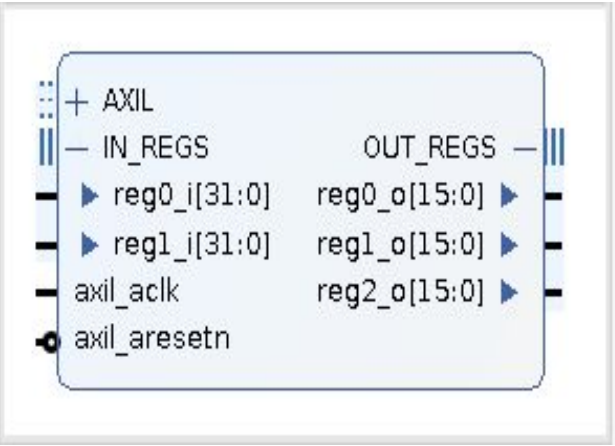
Features

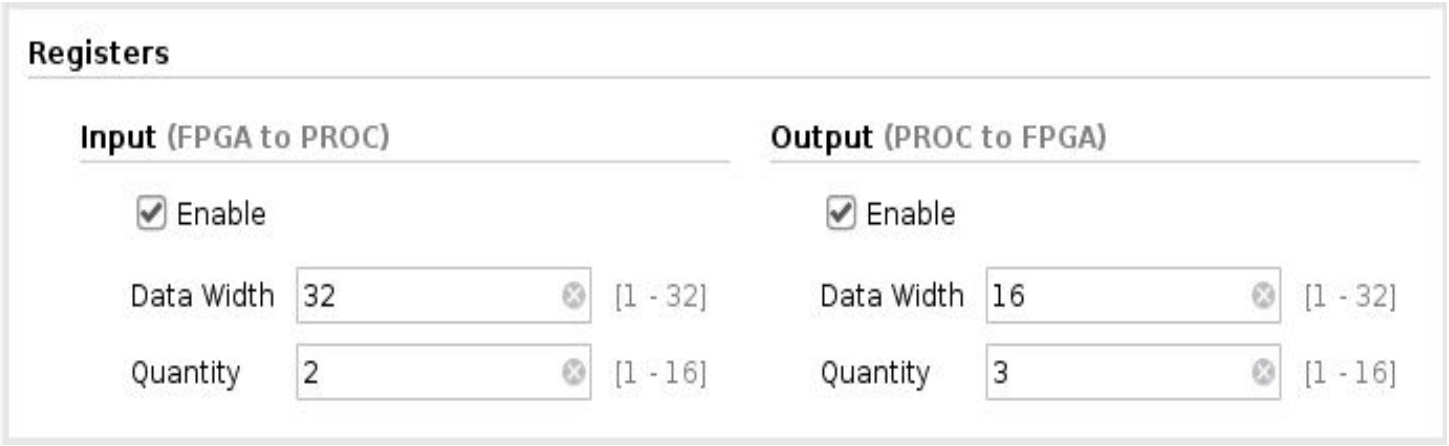
- I/O Registers, I/O FIFOS, and TDPRAM.
- AXI Lite: Registers and FIFOs.
- AXI Full: TDPRAM.



Registers

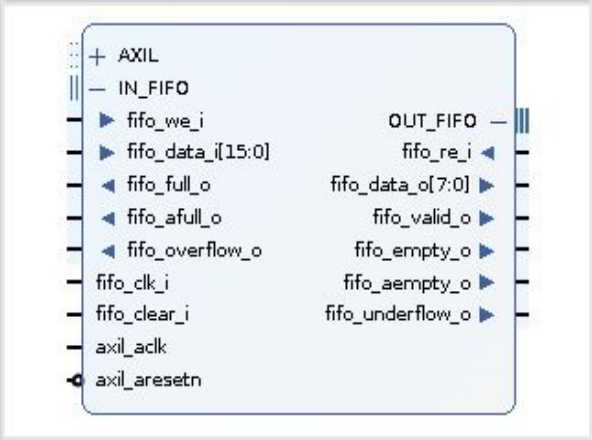
- 16 input registers (FPGA to Processor).
- 16 output registers (Processor to FPGA).
- User configurable data width, 1-32 bits.
- Input and output independently enabled.





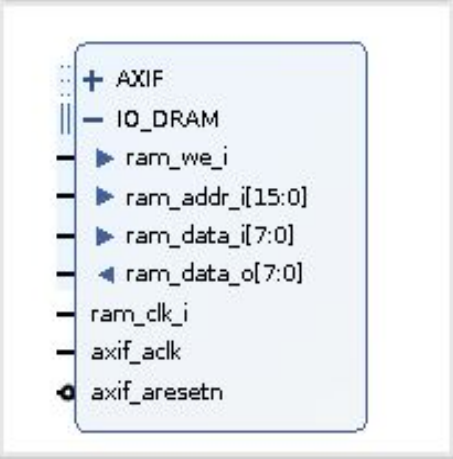
FIFOs

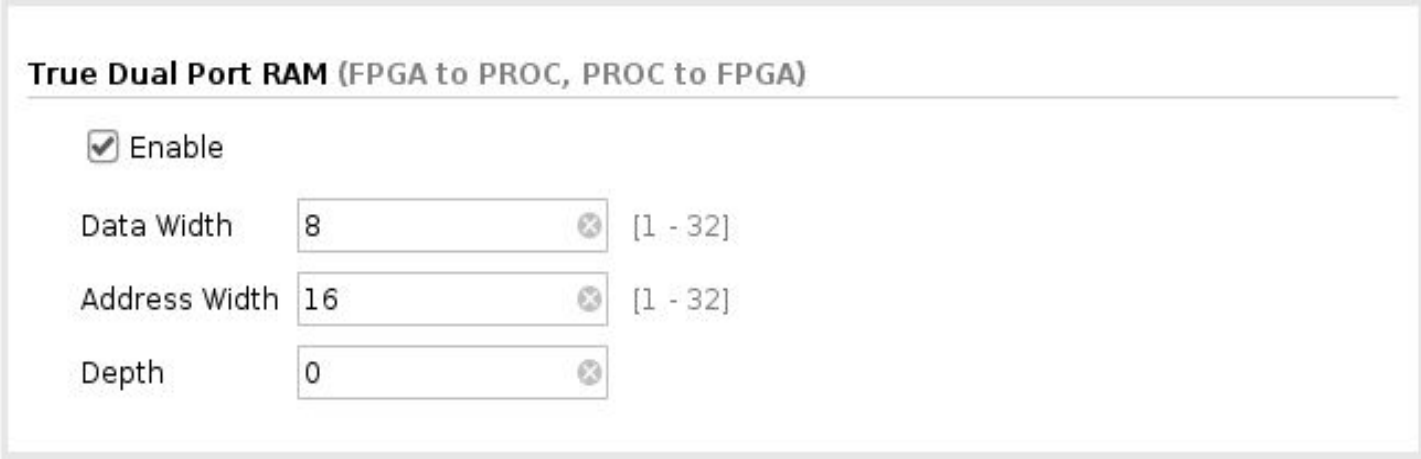
- Input and output FIFOs.
- Customizable width and depth.
- Asynchronous.
- Control registers on the Processor's side.



TDPRAM

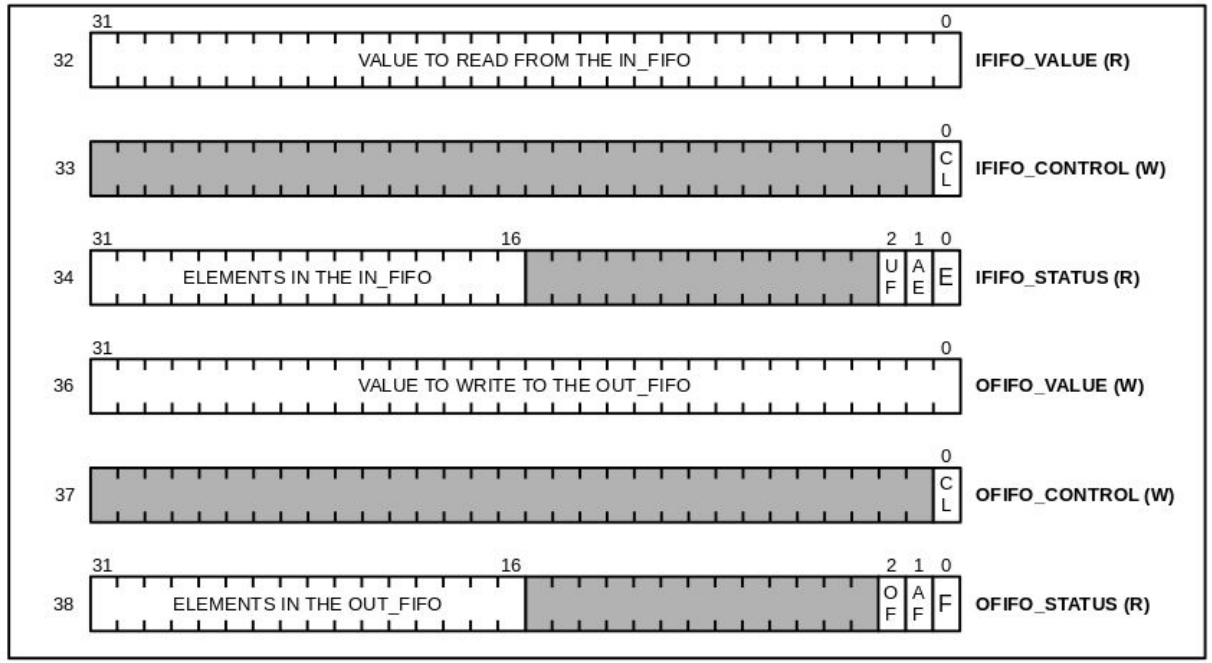
- Bidirectional.
- Clock-domain-crossing.
- Configurable depth, width and address width.





Processor interaction

- Device information in **xparameters.h.**
- Register mappings in **comblock.h**.
- CB_IREG, CB_OREG, ...
- Control registers.



C Drivers

- Read and write functions **single memory position**:

```
void cbWrite(UINTPTR baseaddr, u32 reg, u32 value)

u32 cbRead(UINTPTR baseaddr, u32 reg)
```

- Read and write several **contiguous memory positions**:

```
void cbWriteBulk(UINTPTR baseaddr, int *buffer, u32 depth)

void cbReadBulk(int *buffer, UINTPTR baseaddr, u32 depth)
```

Where and how to get it?

- Hosted on GitLab:

```
git clone https://gitlab.com/ictp-mlab/core-comblock.git
```

- Completely open source under BSD 3-clause license.
- Rodrigo Melo, collaboration between the Multidisciplinary Laboratory (MLAB) from The Abdus Salam International Centre for Theoretical Physics (ICTP, Italy) and the FPGA division of Micro and Nanotechnology from the National Institute of Industrial Technology (INTI, Argentina).

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Introduction to Lab 2

ComBlock and RTL instantiation

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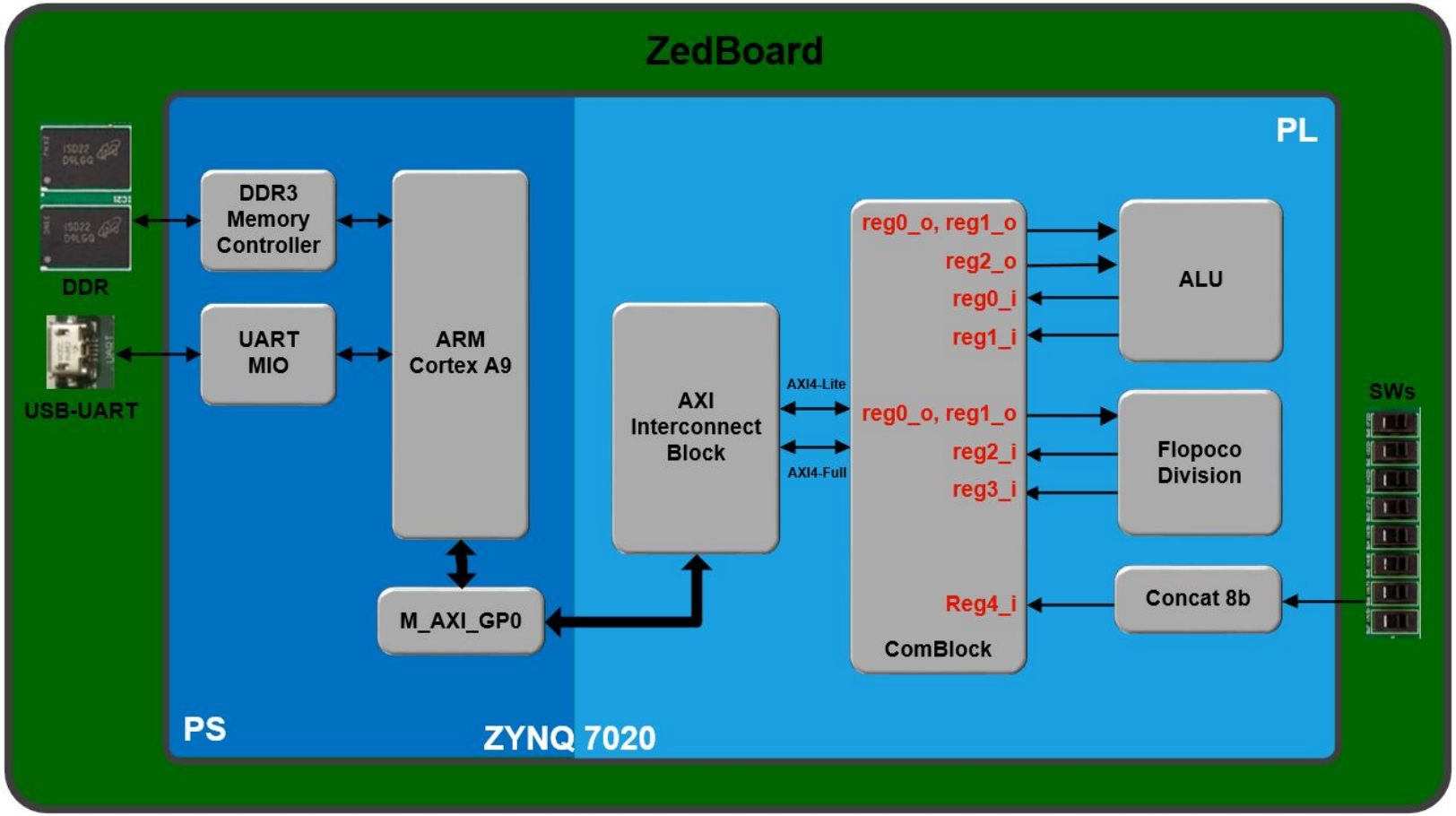
Objectives

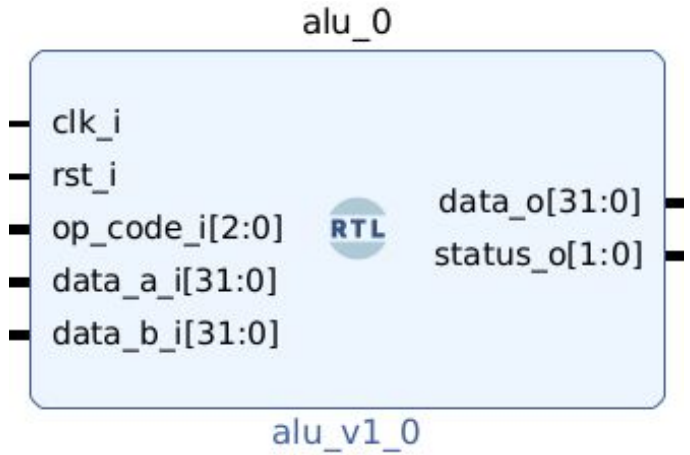
- Simulate a simple Arithmetic Logic Unit and understand the VHDL code.
- Use and configuration of the ComBlock IP.
- Understand the data transfer between PL and PS using ComBlock IP.
- Instantiate RTL blocks and control them through the ComBlock registers.
- Perform unsigned integer arithmetic operations.

Design description



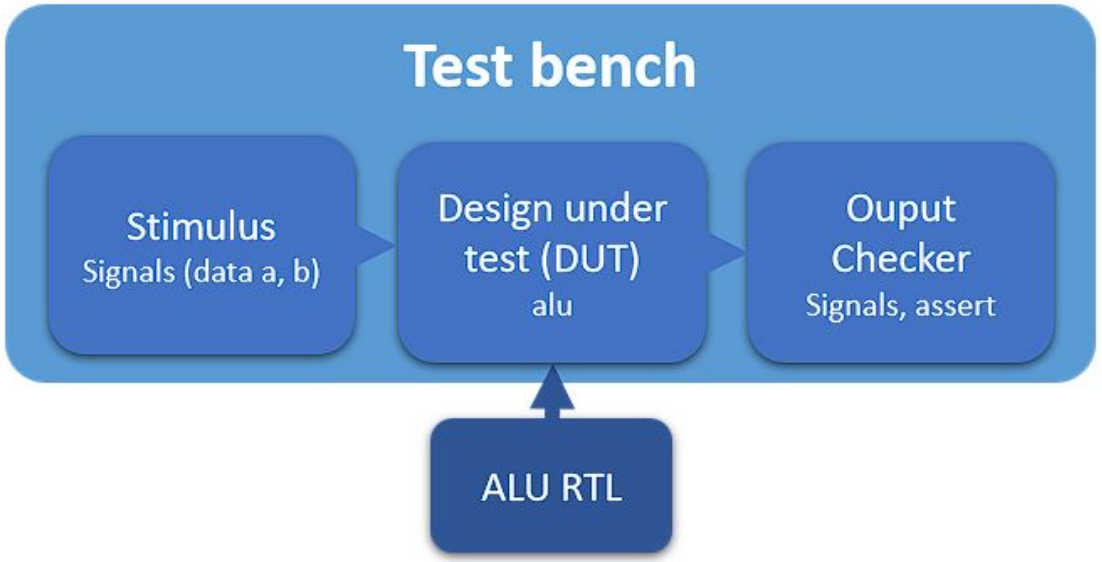
ALU and Division Block

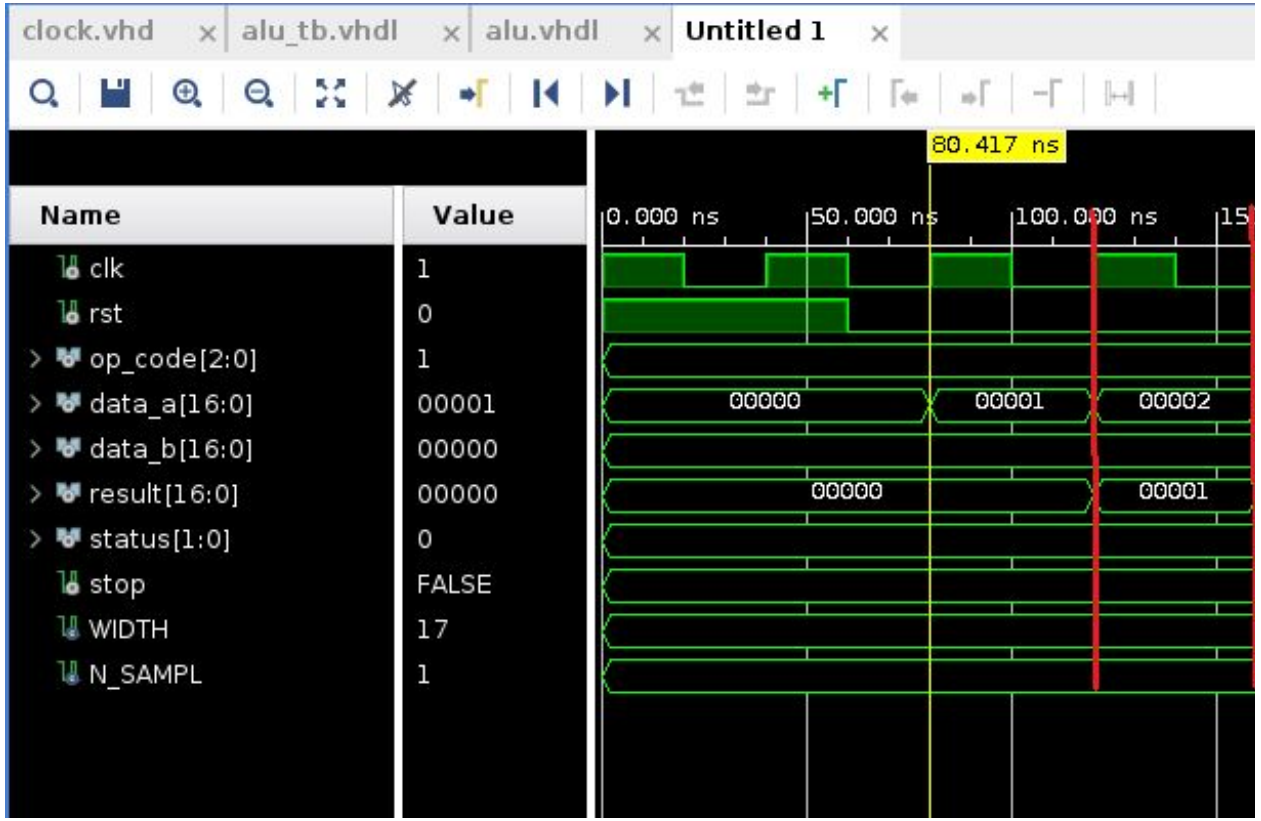
- RTL block, VHDL coded.
- Unsigned integer data.
- Customizable data width.



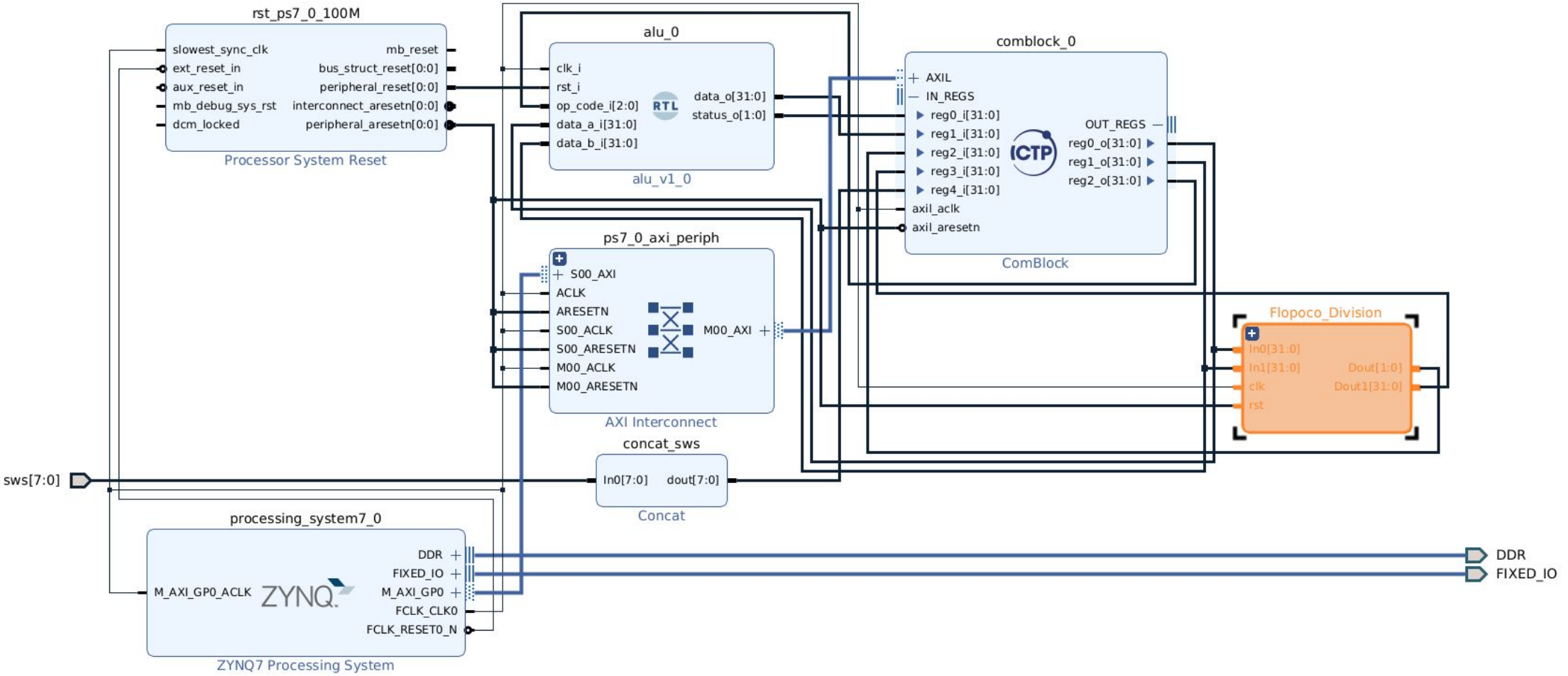
- RTL block, VHDL, generated by **Flopoco**.
- 32 bit floating point representation.

Simulation


Test bench
Stimulus
Signals (data a, b)
Design under test (DUT)
alu
Ouput Checker
Signals, assert
ALU RTL


clock.vhd
alu_tb.vhdl
alu.vhdl
Untitled 1
80.417 ns
Name
Value
0.000 ns
50.000 ns
100.000 ns
clk 1
rst 0
op_code[2:0] 1
data_a[16:0] 00001
data_b[16:0] 00000
result[16:0] 00000
status[1:0] 0
stop FALSE
WIDTH 17
N_SAMPL 1
00000
00001
00002
00000
00001

Hardware creation



Software

- C driver, use ComBlock instructions.
- Configuration and data exchange.
- Unsigned integer arithmetic operations.
- Select the operation with an SW.
- Identify and print status flag.

```
### Testing the Comblock Registers
Data in A=10, B=5
operation status: 0
operation option = 0, result = 0
operation status: 0
operation option = 1, result = 15
operation status: 0
operation option = 2, result = 5
operation status: 0
operation option = 3, result = 0
operation status: 0
operation option = 4, result = 0
operation status: 0
operation option = 5, result = 0
operation status: 0
operation option = 6, result = 0
operation status: 0
operation option = 7, result = 320
operation exn: 0
division R = 320
sws value: 9
```

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Thank you!

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