



The Abdus Salam  
**International Centre  
for Theoretical Physics**



**IAEA**

**Joint ICTP-IAEA School on  
Systems-on-Chip based on  
FPGA for Scientific Instrumentation  
and Reconfigurable Computing**



## **Introduction to Laboratory 4**

# **SoC-FPGA DAQ system and TCL**

**Prepared by**

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## Lab 4: Objectives

- Learn how to work in a collaborative environment with version control tools, employing **tcl** commands for hardware recreation.

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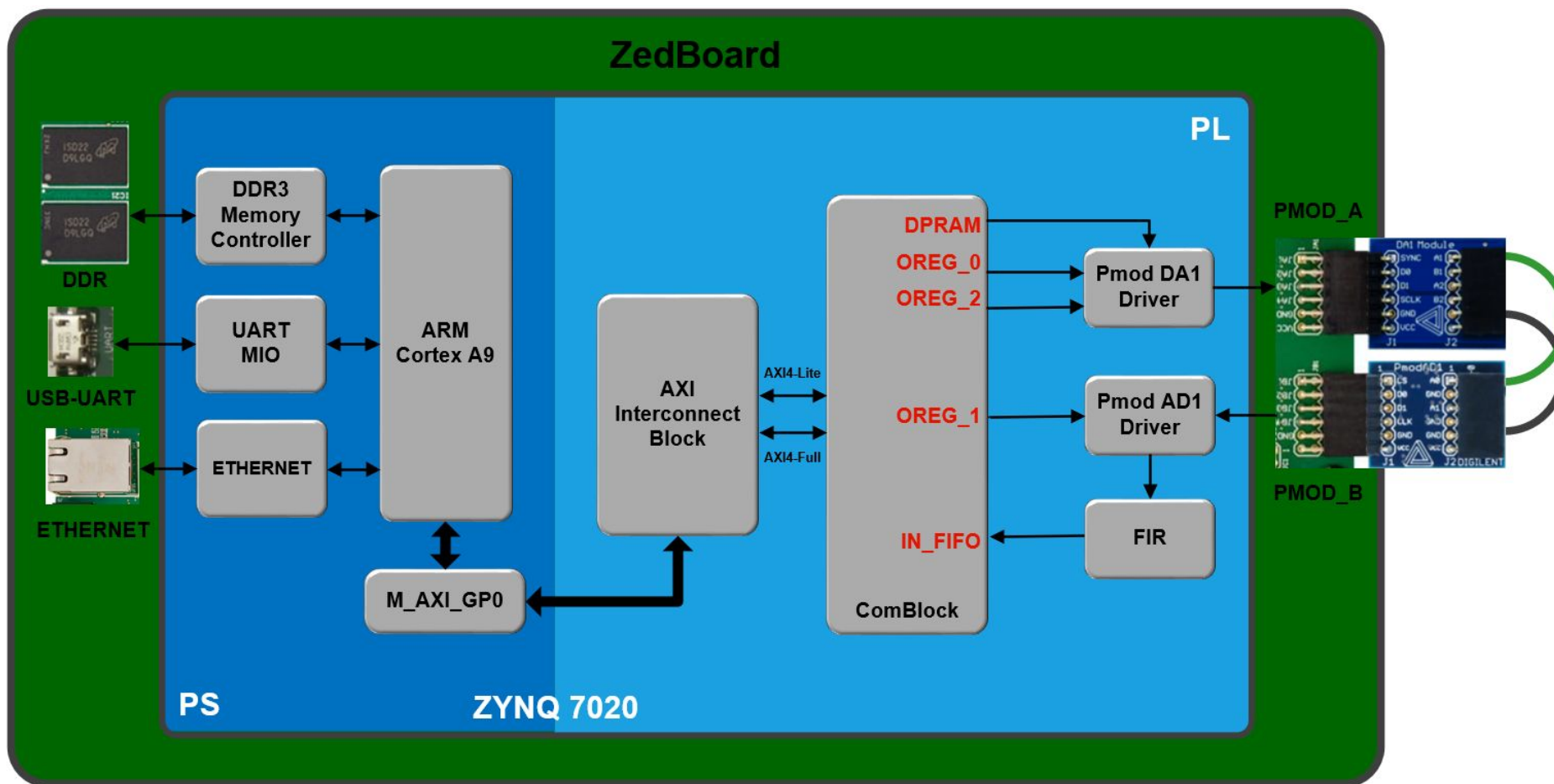
## Lab 4: Objectives

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- Integrate PMOD modules into the hardware design to control and acquire signals in the analog domain from the SoC.

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- Integrate PMOD modules into the hardware design to control and acquire signals in the analog domain from the SoPC.
- Understand the benefits of a higher abstraction level when using the **UDMA** environment for interaction.

# Design description



Learn how to work in a collaborative environment with version control tools, employing **tcl** commands for hardware recreation.

- Git-compatible text-based source code
  - Reproducibility
  - Collaboration
  - Reliability
  - Complex deployments

# Using TCL to create a block design

Vivado - Hardware block design

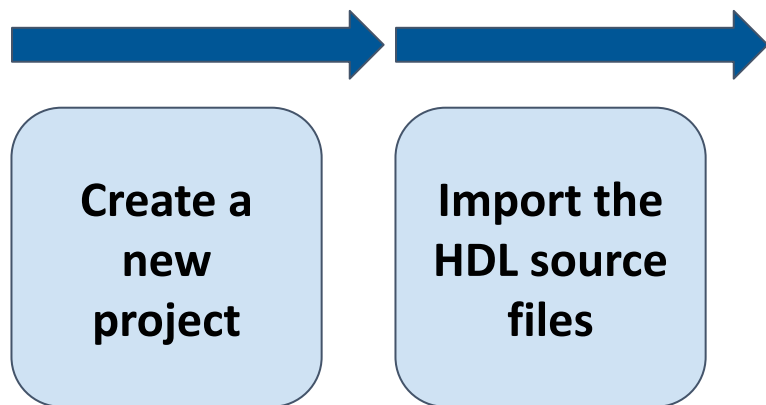


**Create a  
new  
project**



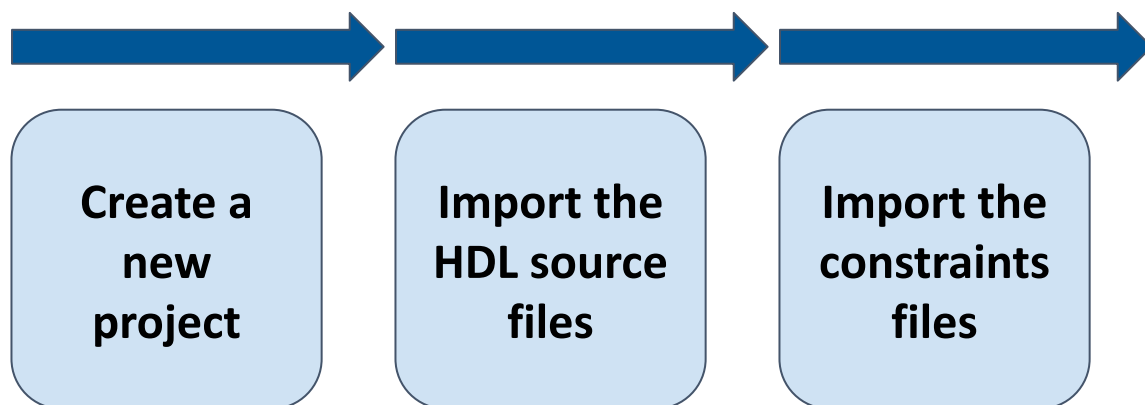
# Using TCL to create a block design

## Vivado - Hardware block design



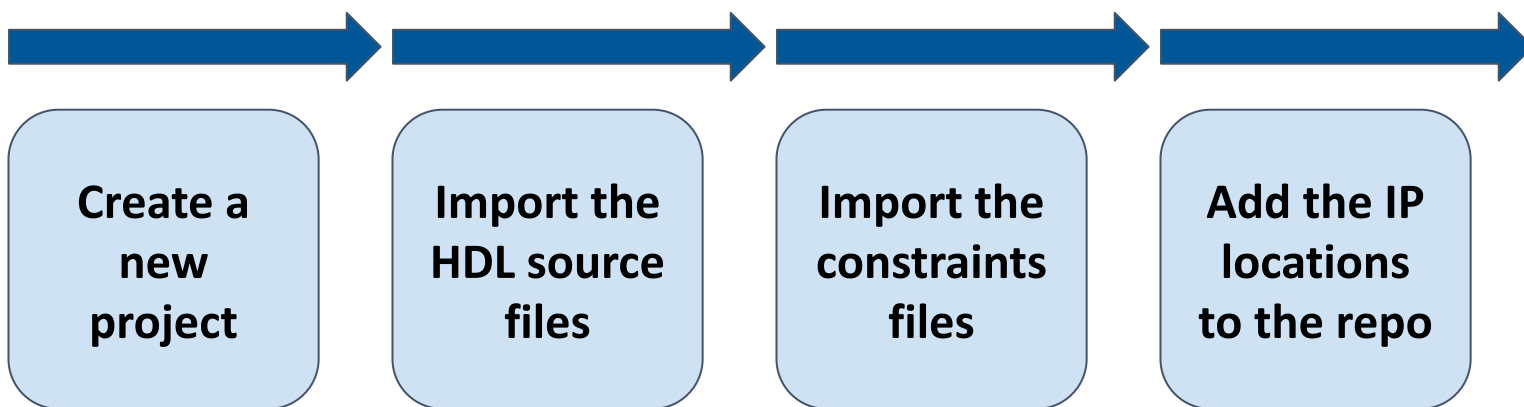
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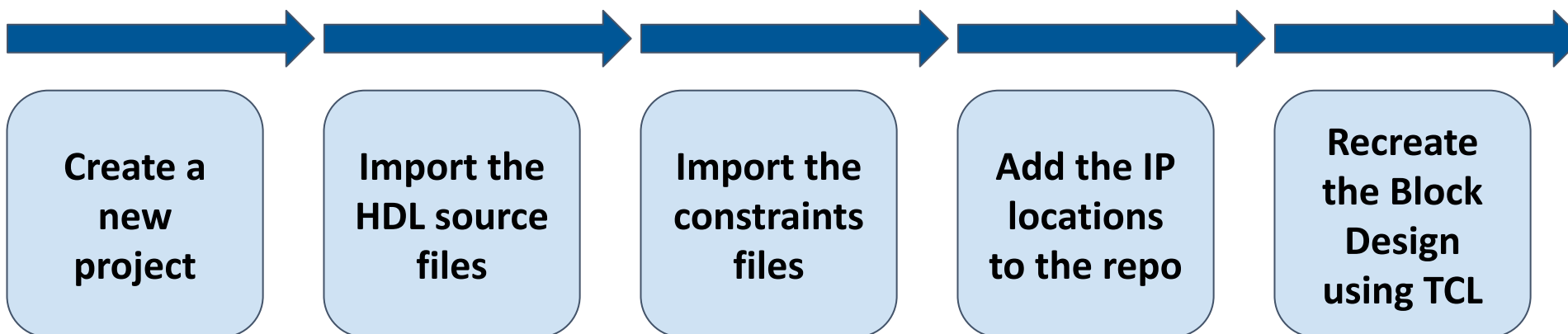
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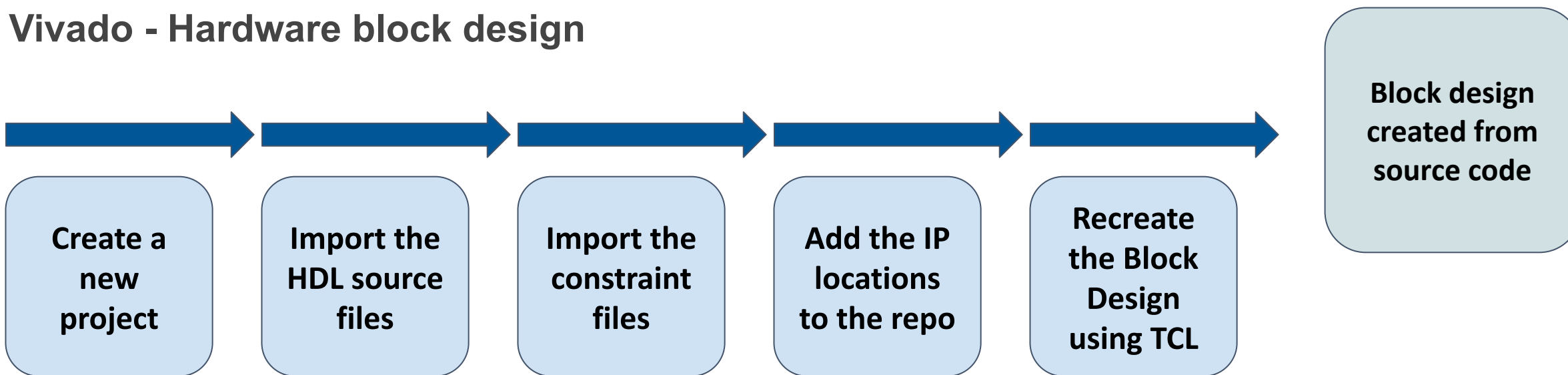
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## Vivado - Hardware block design



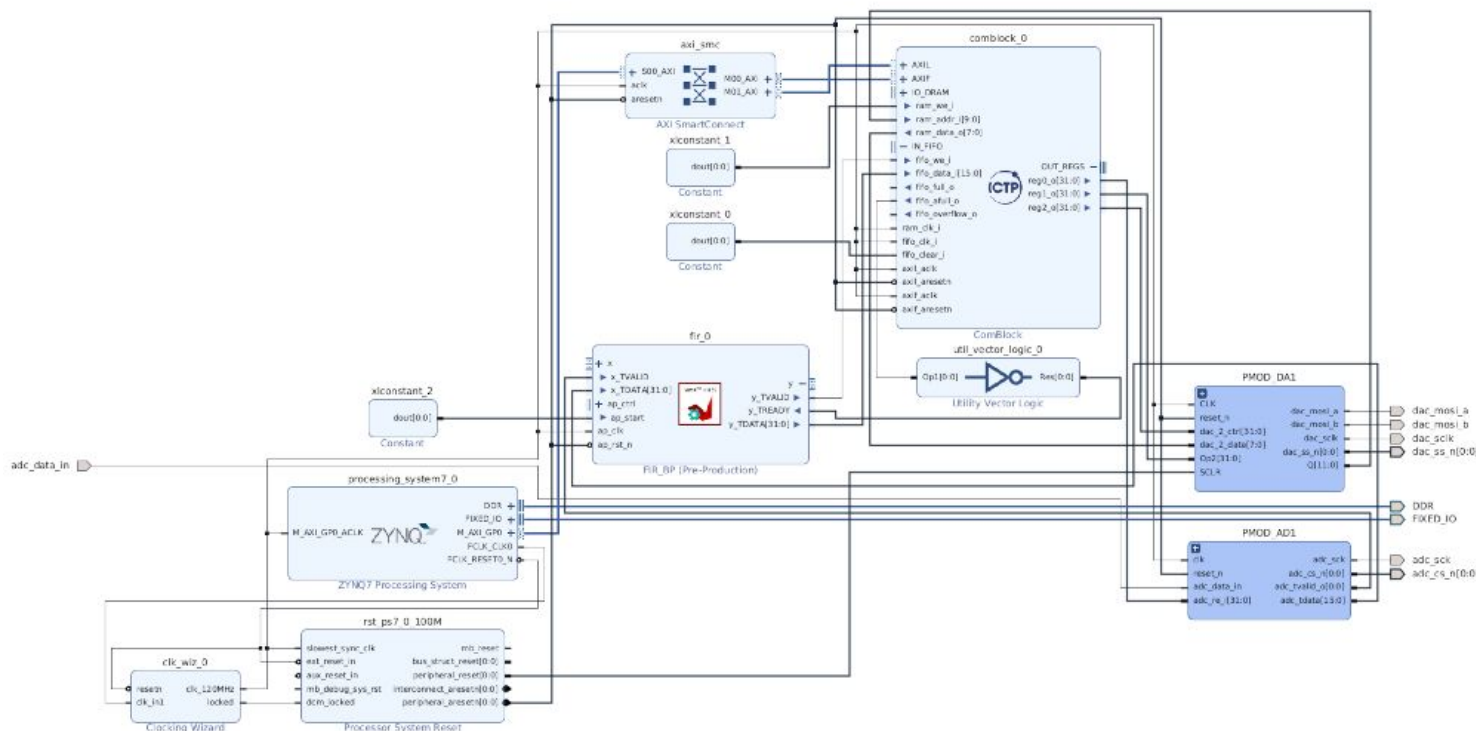
# Using TCL to create a block design

## Vivado - Hardware block design



# Using TCL to create a block design

## Vivado - Expected block design



# Creating the bitstream

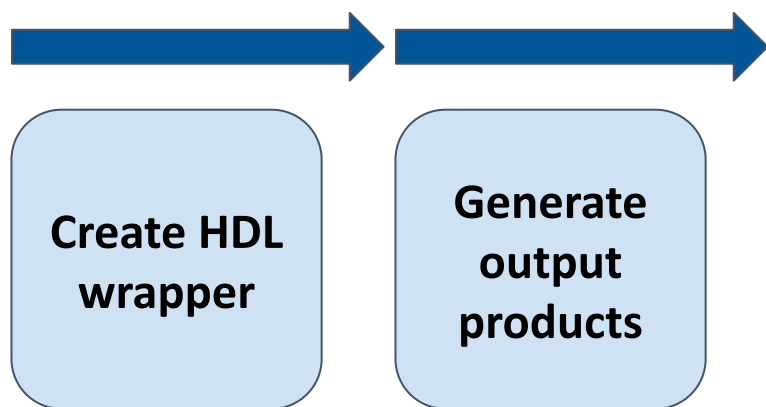
From hardware block design to bitstream



**Create HDL  
wrapper**

# Creating the bitstream

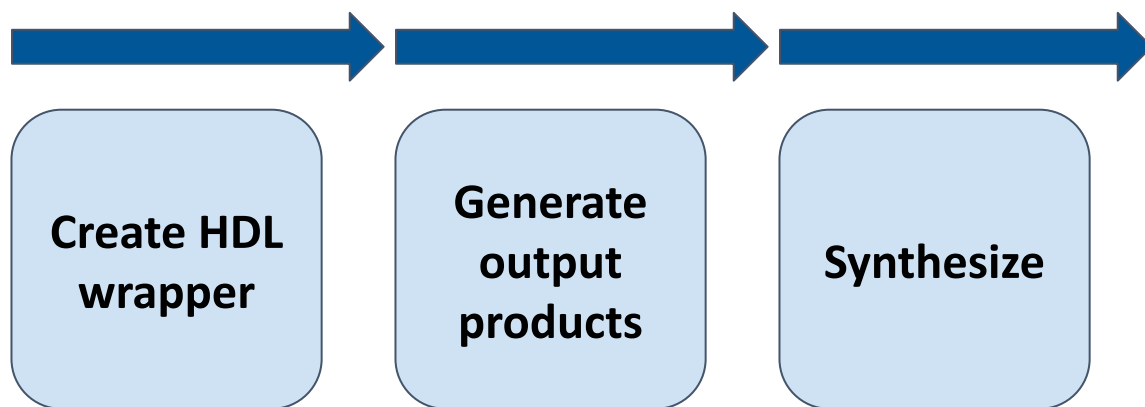
From hardware block design to bitstream





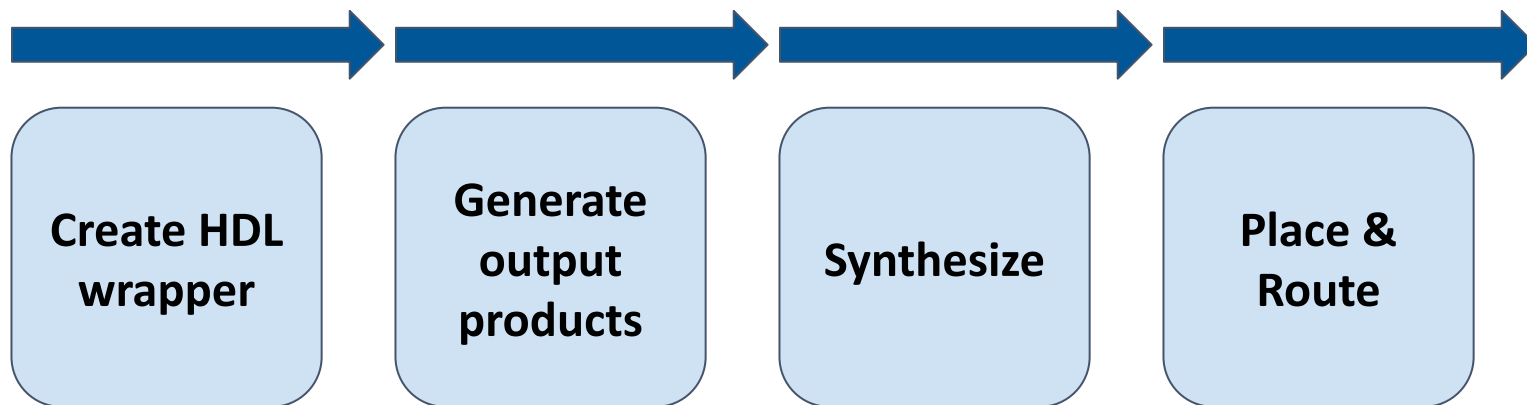
# Creating the bitstream

From hardware block design to bitstream



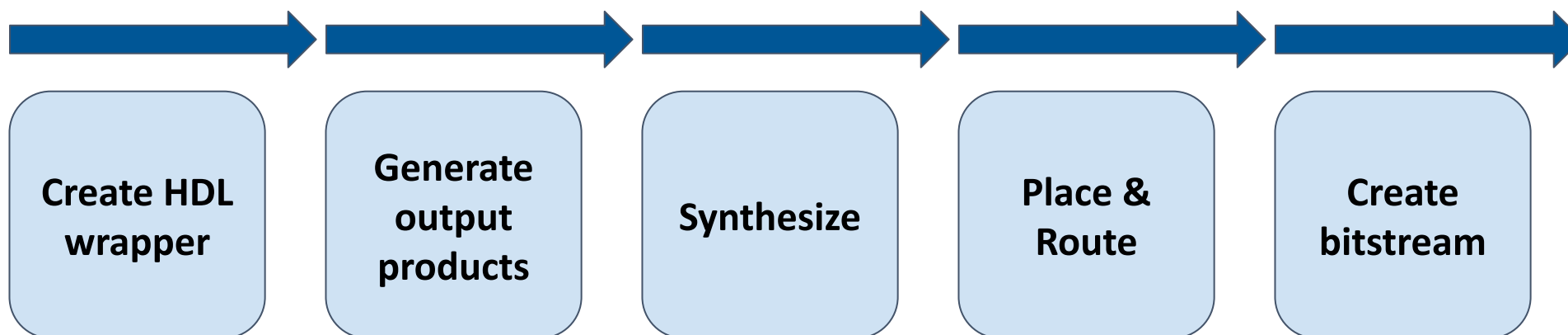
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From hardware block design to bitstream



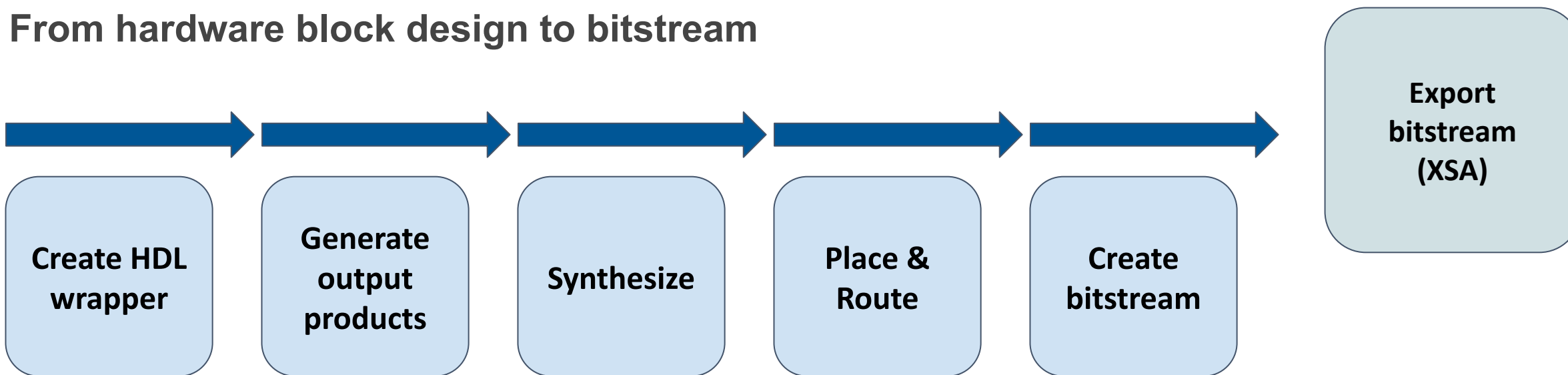
# Creating the bitstream

From hardware block design to bitstream



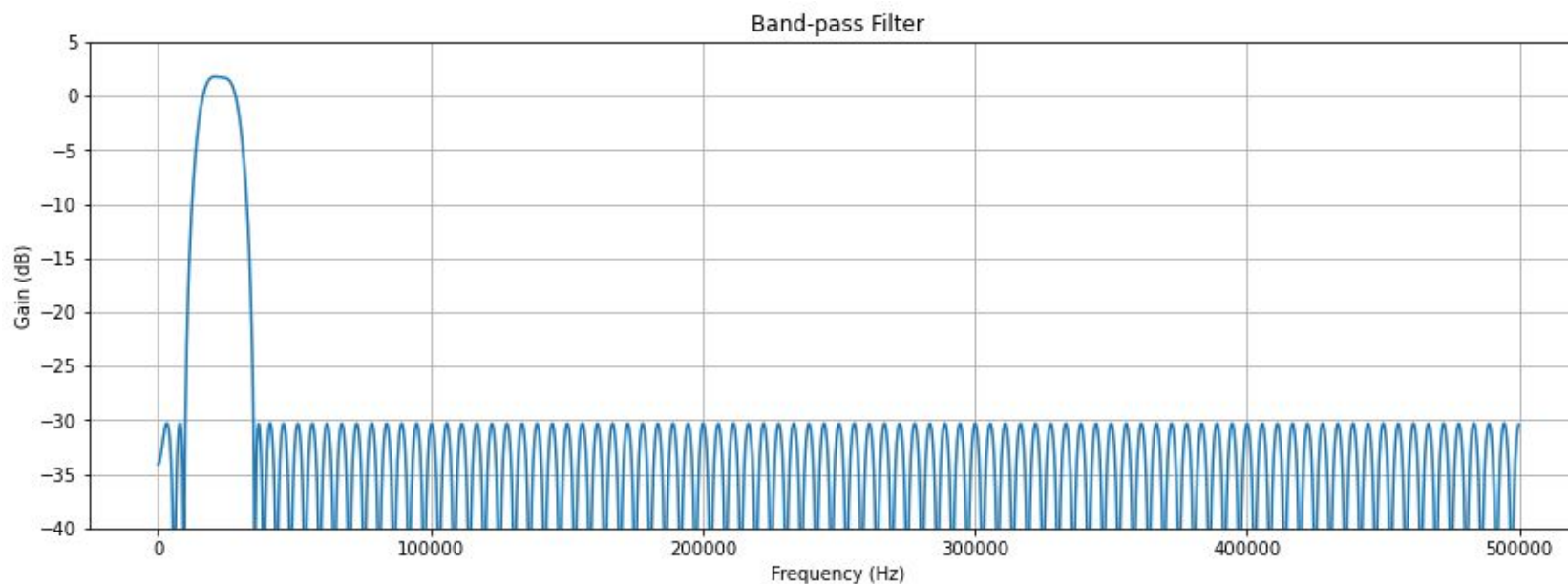
# Creating the bitstream

From hardware block design to bitstream



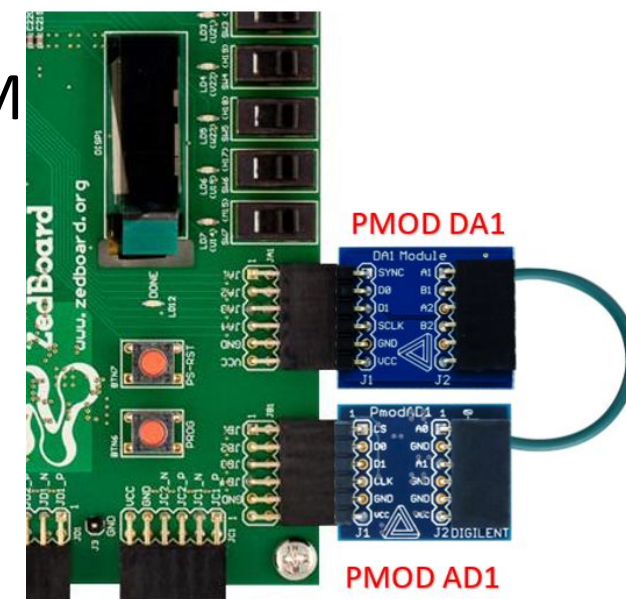
Perform the instantiation of an IP core previously designed through High-level Synthesis (HLS) tool.

- Finite-impulse response (FIR) bandpass filter implemented in HLS
- Instantiation in Vivado Block Design



## Integrate PMOD modules into the hardware design to control and acquire signals in the analog domain from the SoPC.

- A/D and D/A Control - using ComBlock's output registers
  - Start conversion, data format
- D/A converter (1 Msps)
  - Arbitrary waveform generator using ComBlock's DP-RAM
- A/D converter (1 Msps)
  - Digitizing analog output from D/A (wire loopback)
  - Data acquisition using ComBlock's Input FIFO

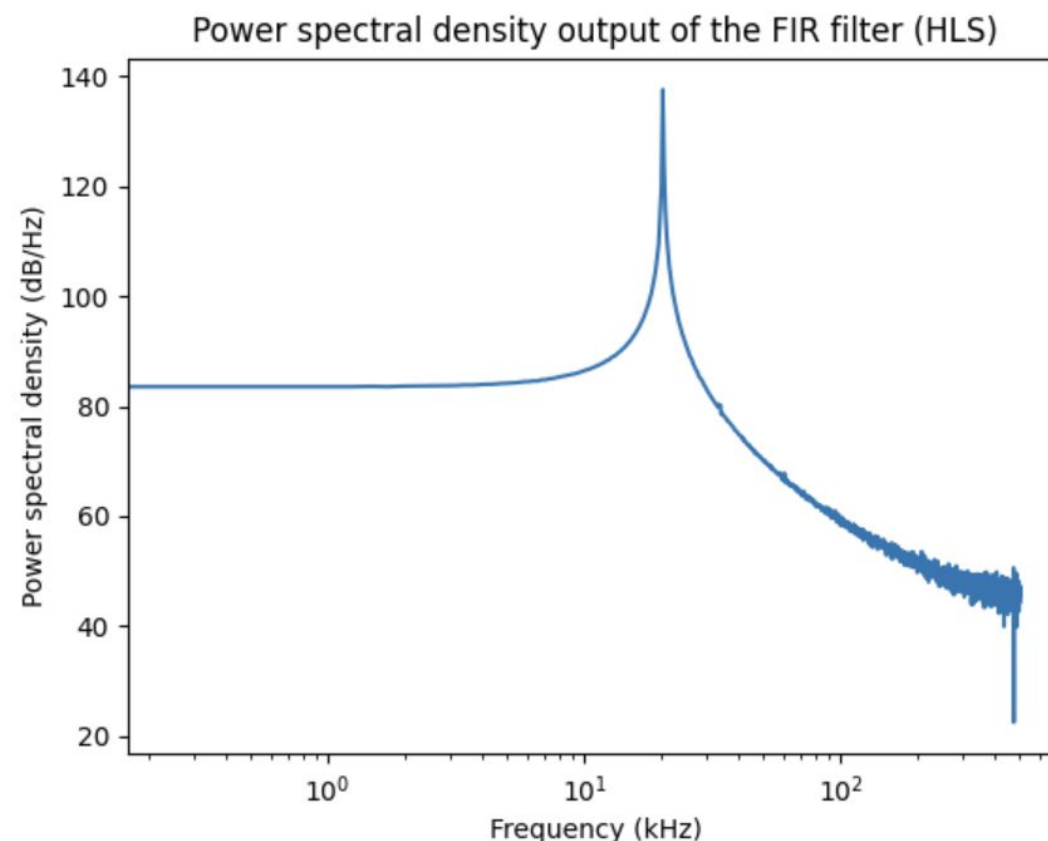


## Understand the benefits of a higher abstraction level when using the UDMA environment for interaction.

- UDMA in Jupyter Notebook to interface the ComBlock in the PL remotely
  - Arbitrary waveforms from Python numeric libraries
  - Plotting and recording A/D data using Matplotlib (Python)
  - Using markdown to document within the Jupyter Notebook

## Understand the benefits of a higher abstraction level when using the UDMA environment for interaction.

- Post-processing of recorded data in Jupyter Notebook
  - FFT of the bandpass filter response
- Challenges
  - Experimental bode plot
  - Changing HLS FIR filter response







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**Thank you!**

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