



Joint ICTP-IAEA School on Systems-on-Chip based on FPGA for Scientific Instrumentation and Reconfigurable Computing



Project 1 - Stage 2

Digital Pulse Processing for Isotope Identification

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Stage 2 Digital pulse processing for isotope identification





Before starting Pulse shape comparison Pull the repo 😉 Fitted (ideal) pulse 1.0 --- Experimental data 0.8 Parameters from Stage 1 0.6 Nal(TI) detector • CLYC detector \circ $\tau_{\rm d}$ ~ 1.20 μ s \circ $\tau_{d} \sim 4.97 \mu s$ 0.4 ο *τ*^r ~ 0.22 μs • *τ*^r ~ 0.47 μs 0.2 0.0 10 20 0 30 40 Time (µs)





Lab Project 1 - stage 2: specific objectives

- Build a digital pulse processing system (DPP) to compute the energy spectrum in the SoC/FPGA
- Identify the provided isotope source by its energy spectrum

Methodology

- Compute the 32-bit unsigned representation of the parameters from Stage 1
- Build up the DPP system using the provided IP cores
- Include the oscilloscope block to assess the signal shapes
- Use the ComBlock's features:
 - Output registers to set the parameters for the IP cores
 - DP RAM to store the real-time data from the histogram generator (spectrum)
 - \circ $\;$ Input FIFO to store the oscilloscope traces
- Add the missing code into the base Jupyter Notebook (JN) to complete the system with UDMA





Stage 2.1 - DPP design in SoC





Design description - DPP overview



Design description - Analog front-end

Design description - Oscilloscope (trigger logic)

Trigger logic - basic oscilloscope core

- Input registers
 - Pulse length (in sample units)
 - Threshold level (in ADC units)
 - Samples before trigger (delay)
- Output stream
 - $\circ \quad \text{Captured pulse} \\$

Design description - DPP

Continuous processing (triggerless)

- Pulse shaper
 - Trapezoid/triangle output
- Peak detector
 - Finds peak of trapezoid
- Histogram
 - Stores each amplitude as a value in the RAM address

Design description - DPP data path

Design description - D/A output

Outputs to external oscilloscope

- Original trace
- Pulse shaper
 - Trapezoid output
 - Pulse output
 - Square output
- Peak detector
 - Peak seeking

Uses multiplexer (MUX) for output selection

Design description - D/A output

Stage 2.2 - Isotope identification

• Set the working parameters for the IP cores using ComBlock output registers.

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- Use the embedded oscilloscope to visualize the raw data (from ComBlock I-FIFO) in JN.

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- Use the embedded oscilloscope to visualize the raw data (from ComBlock I-FIFO).
- Reset and record the spectrum from the detector with a source placed closeby.

- Set the working parameters for the IP cores using ComBlock output registers.
- Verify the functionality of the DPP subsystems using the MUX and D/A output.
- Use the embedded oscilloscope to visualize the raw data (from ComBlock I-FIFO).
- Reset and record the spectrum from the detector with a source placed closeby.
- Determine the isotope placed close to the detector by inspecting the resulting spectrum.

Challenge - Energy calibration

- Gaussian fit of the photopeak
- Baseline as base energy point

Outcomes

- Calibrated energy scale
- Detector resolution at Cs-137 photopeak

Just before starting

- Do NOT use a host (local) computer physically connected to the ZedBoard+detector setup.
- Request access to the ZedBoard (attach) setup only AFTER you finished coding the Jupyter Notebook.

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Thank you!