WELCOME to the

Workshop on Fully-Programmable Systems-on-Chip for Scientific Applications

27 October – 31 October, 2024

Qatar University, Doha, Qatar

Workshop Programme

• Workshop website: https://indico.ictp.it/event/10522
  (detailed schedule & list of participants)

• **Daily timetable (8:00: breakfast, 8:30 – 17:00)**

Timetable	
8:30 - 10:30	lectures
10:30 - 11:00	**coffee-break**
11:00 - 12:30	lectures
12:30 - 13:30	**lunch**
13:30 - 15:30	lectures / lab activities
15:30 - 15:50	**coffee-break**
15:50 - 17:00	lab activities

• Workshop's email (secretariat): smr3983@ictp.it
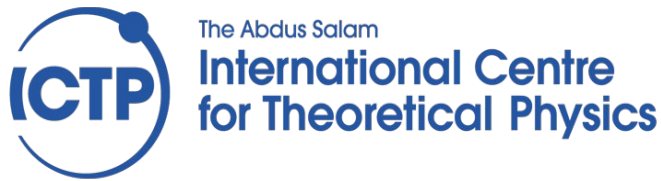
Participants

- Requests for participation: 283 applicants from 63 different nationalities

- **Selected: 50 participants from 21 different nationalities**

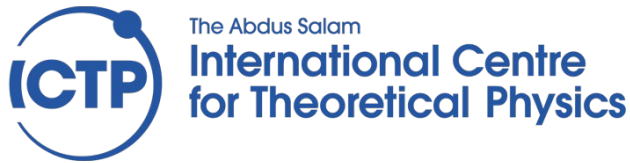|		
Algeria	Iraq	UK
Bangladesh	India	Pakistan
Colombia	Indonesia	Sudan
Georgia	Philippines	Jordan
Oman	Malaysia	Egypt
Croatia	Mexico	Tunisia
Qatar	Palestine	Syria

Workshop's Directors

Mohammed Al-Hitmi (QU, Qatar)

Faycal Bensaali (QU, Qatar)

Muhammad Enamul Hoque Chowdhury (QU, Qatar)
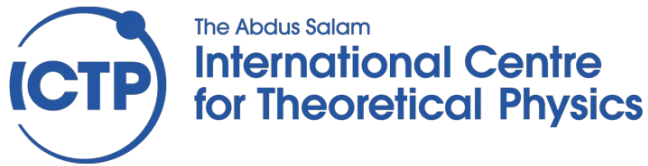
Andres Cicuttin (ICTP, Italy)

Maria Liz Crespo (ICTP, Italy)

Muhammad Salman Khan (QU, Qatar)

Sawal Hamid Md Ali (UKM, Malaysia)

Mohamed S. Mohamed Ali (QU, Qatar)

Mamun Bin Ibne Reaz (IUB, Bangladesh)

Faculty (Lecturers & Lab Tutors)

BALLINA ESCOBAR Maynor (ICTP, Italy)

BOGOVAC Mladen (IAEA, Austria)

GARCIA ORDOÑEZ Luis (ICTP, Italy)

MOLINA Romina (ICTP, Italy)

RINCON CALLE Fernando (UCLM, Spain)

SILVA Agustin (TII, United Arab Emirates)

SISTERNA Cristian (UNSJ, Argentina)

Main Topics

FPGA and System-on-Chip (SoC) technology
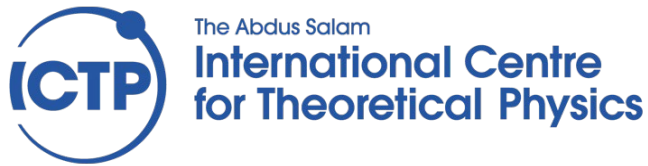
SoC Architecture and Design Methodology

C for Embedded Systems

VHDL (Hardware Description Language)

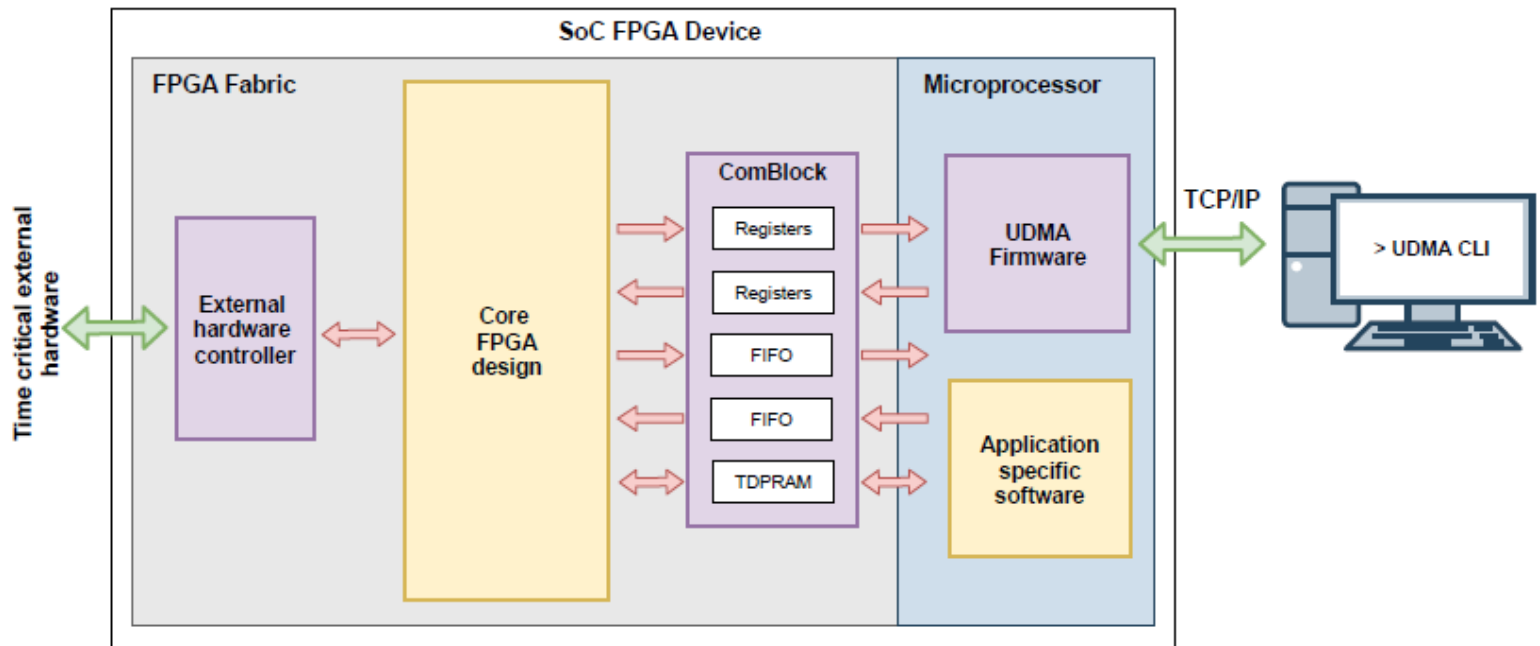High Level Synthesis (HLS)

Real Time Operating System

Reconfigurable Virtual Instrumentation (RVI) on SoC-FPGA

Lab Activities

- Virtual Machines (VM)

- Vivado IDE 2022.2 (Xilinx)

- ZedBoard: Xilinx Zynq-7000 All-Programmable SoC

- GitLab (guides for lab activities)

- Lab Tutors will assist you during the lab activities

• **SoC-FPGA Development Framework:**

Projects

- **Machine Learning on SoC-FPGA**

  - FPGA for Accelerating Machine Learning Algorithms

  - Model Training and Compression

  - Integration with hls4ml tool & Inference Assessment

- **Digital Pulse Processing (DPP) Techniques for Detectors**

  - Pulse Acquisition and Detector Characterization (SiPM)

  - DPP for X-ray Photon Detection and Energy Measurement

  - DPP for Isotope Identification
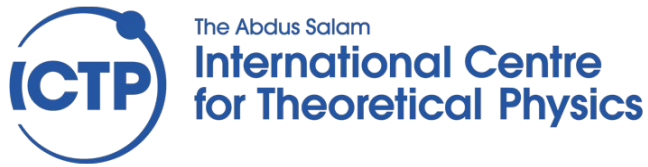
Recommendations:

1) Be on time

2) Attend at least 90% of the lectures + labs to receive the Diploma

3) Feel free to ask questions!

WHAT ABOUT YOU?

NAME

COUNTRY

UNIVERSITY / INSTITUTE

AREA OF RESEARCH

INTEREST IN THE SCHOOL