

Workshop on
Fully Programmable
Systems-on-Chip for
Scientific Applications

Zynq Evaluation and Development Board

Cristian Sisterna

Senior Associate, ICTP-MLAB



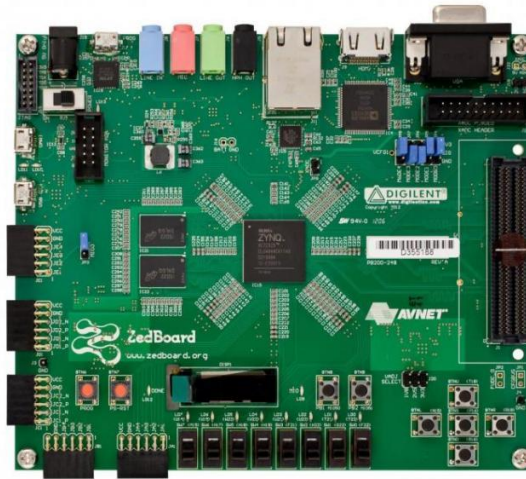
Universidad Nacional San Juan- Argentina



ZedBoard

AVNET

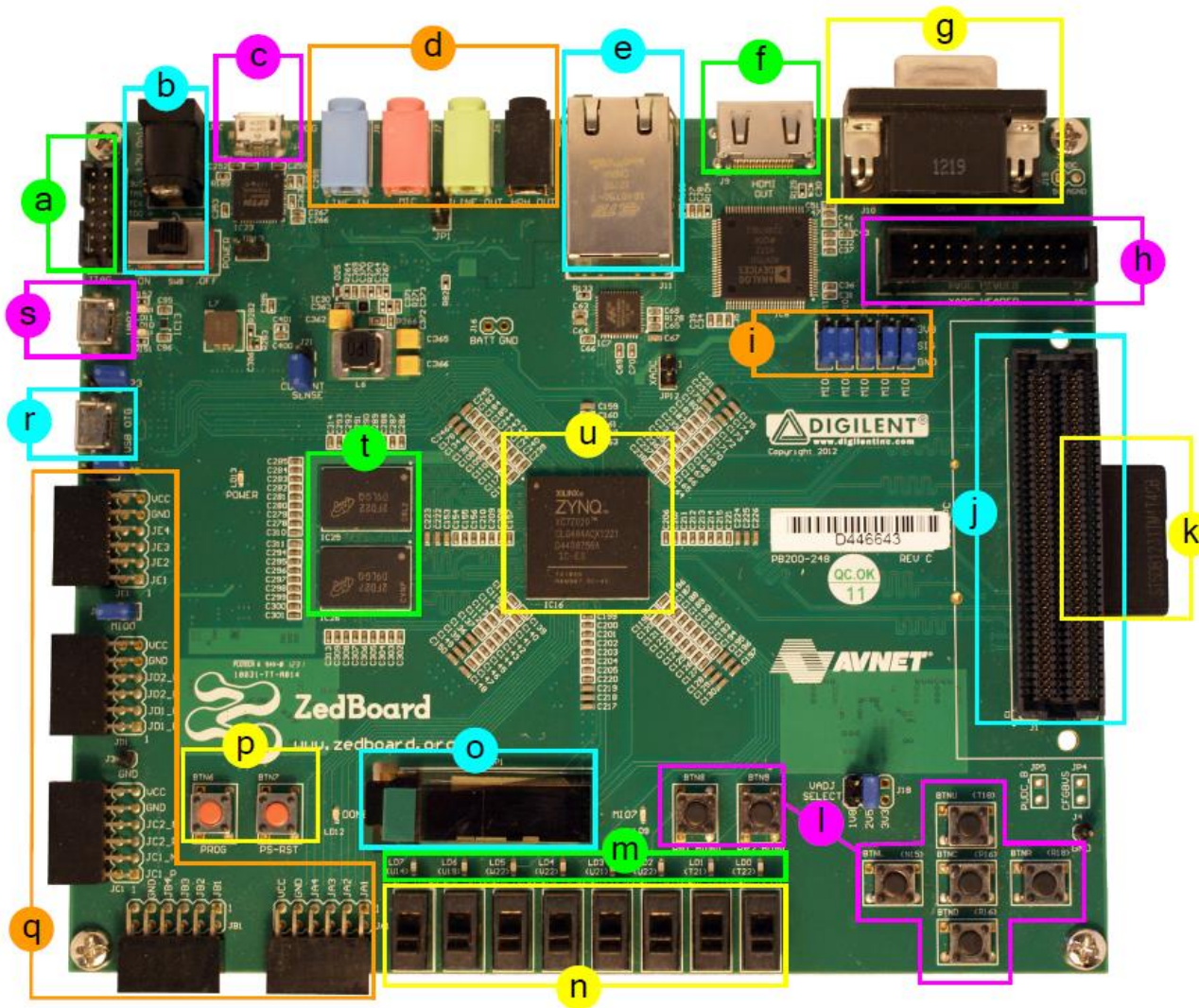
ZedBoard™ is a complete development kit for designers interested in exploring designs using the AMD Xilinx Zynq®-7000 All Programmable SoC. The board contains all the necessary interfaces and supporting functions to enable a wide range of applications. The expandability features of the board make it ideal for rapid prototyping and proof-of-concept development.



DIGILENT

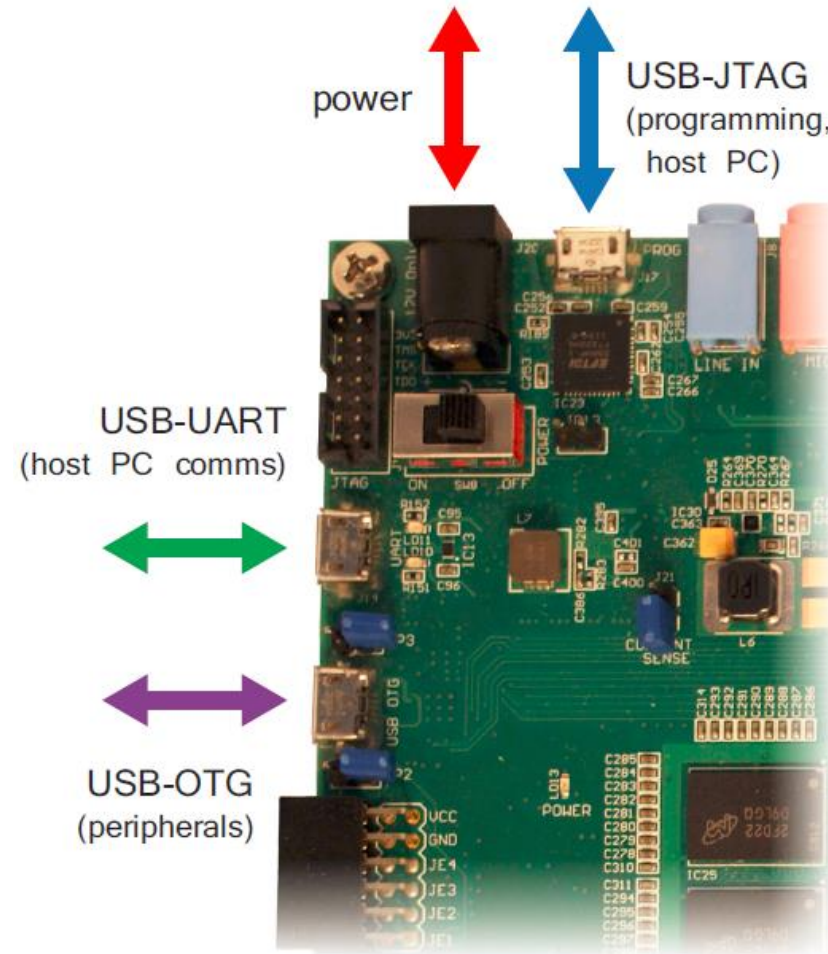
ZedBoard™ is a low-cost development board for the Xilinx Zynq-7000 all programmable SoC (AP SoC). This board contains everything necessary to create a Linux®, Android®, Windows®, or other OS/RTOS based design. Additionally, several expansion connectors expose the processing system and programmable logic I/Os for easy user access.

ZedBoard Main Components



- a** Xilinx JTAG connector
- b** Power input and switch
- c** USB-JTAG (programming)
- d** Audio ports
- e** Ethernet port
- f** HDMI port (output)
- g** VGA port
- h** XADC header port
- i** Configuration jumpers
- j** FMC connector
- k** SD card (underside)
- l** User push buttons
- m** LEDs
- n** Switches
- o** OLED display
- p** Prog & reset push buttons
- q** 5 x Pmod connector ports
- r** USB-OTG peripheral port
- s** USB-UART port
- t** DDR3 memory
- u** Zynq device (+ heatsink)

ZedBoard Main Connectors

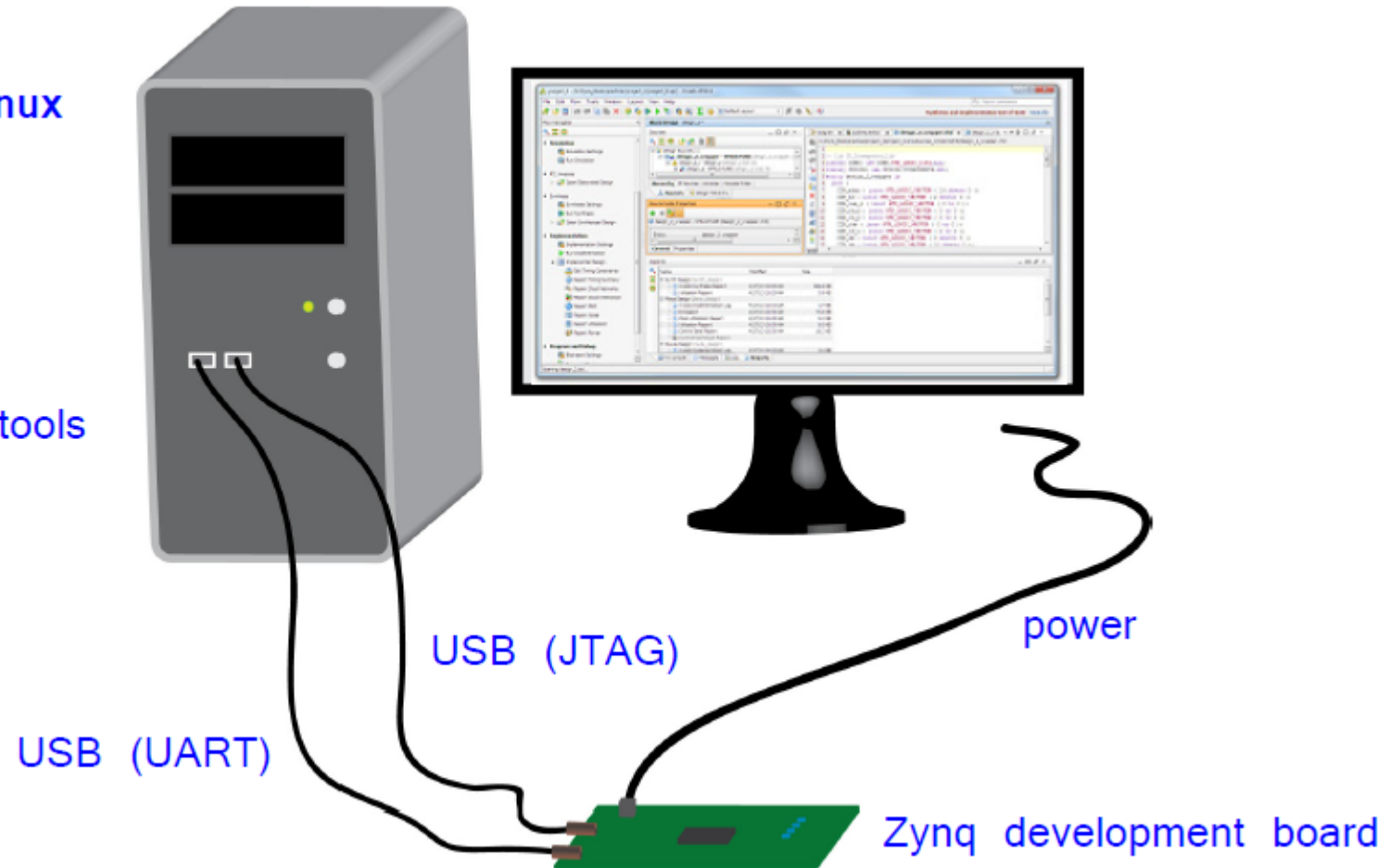


Connection Between PC-ZedBoard

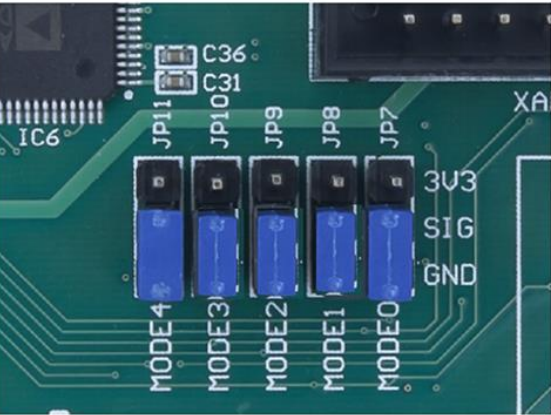
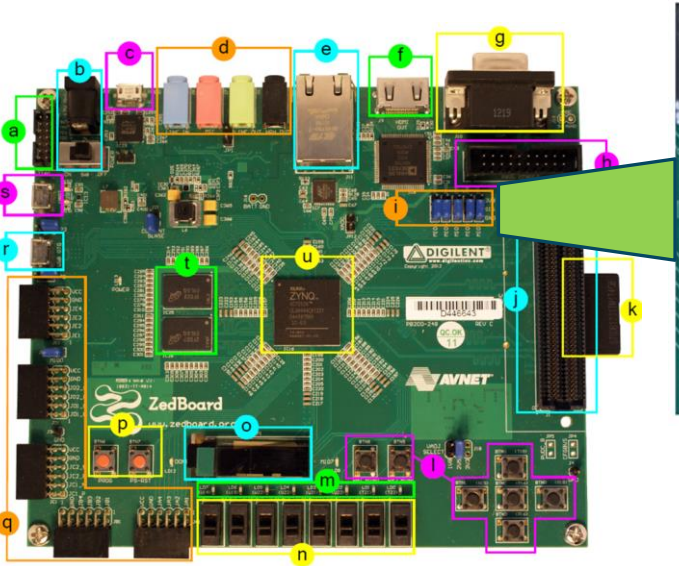
Windows / Linux
computer

16GB+ RAM

Xilinx design tools

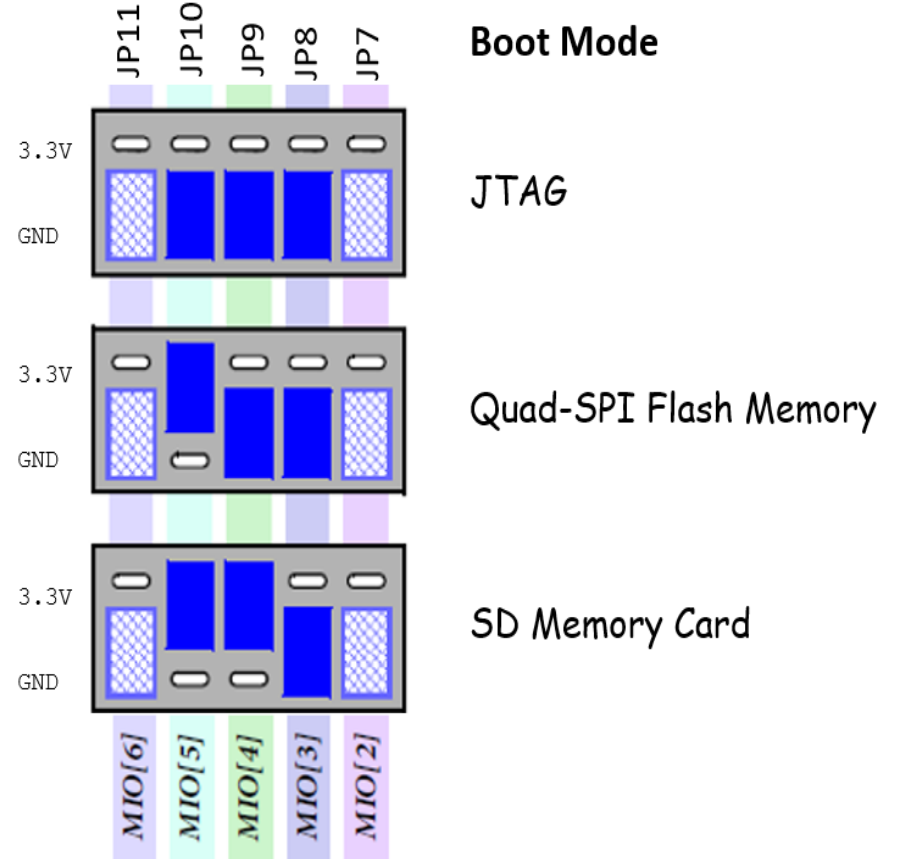


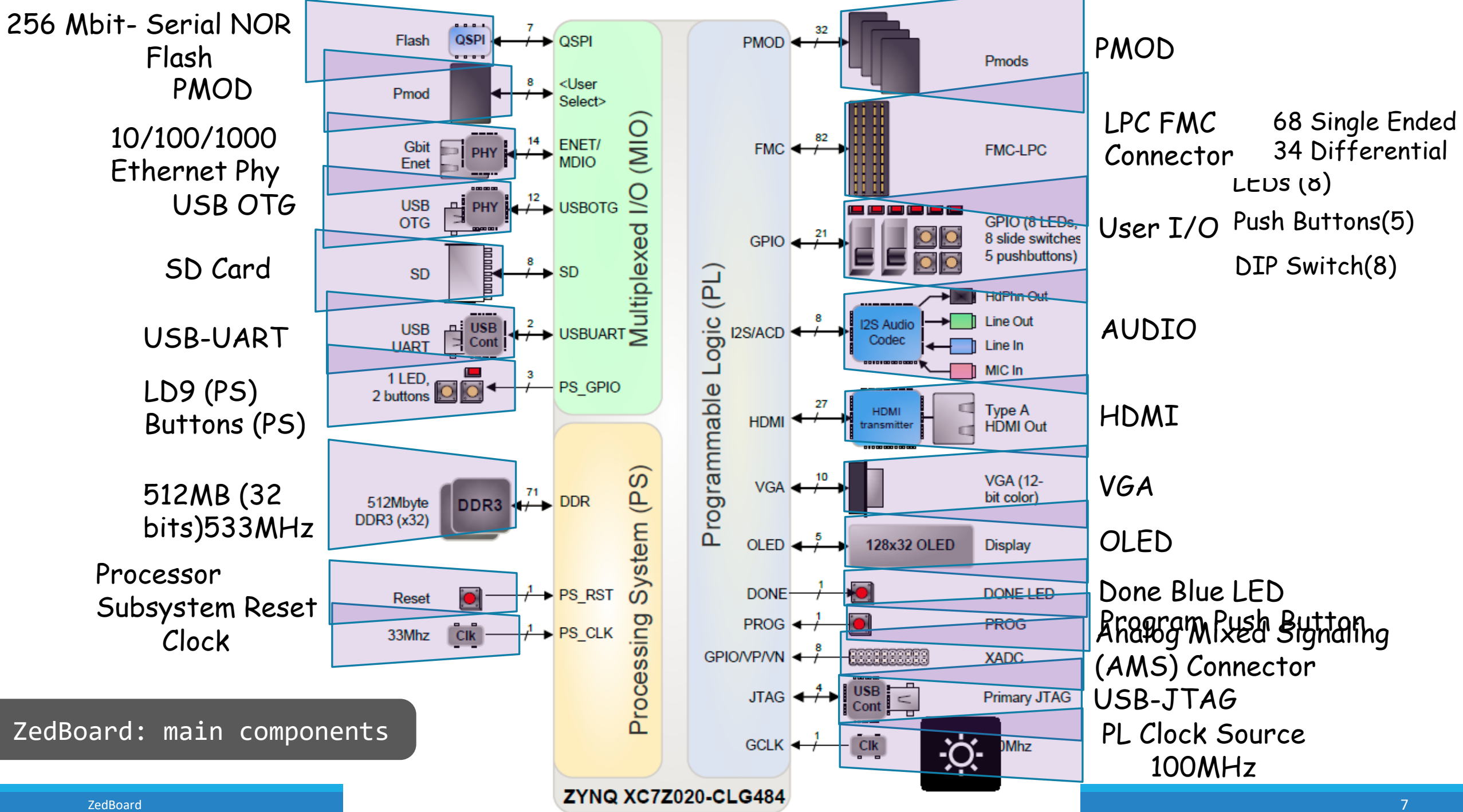
Programming the ZedBoard - Options



Connected Don't care

■ ▤





ZedBoard: main components

ZedBoard Hardware User Guide

ZedBoard

(Zynq™ Evaluation and Development)
Hardware User's Guide



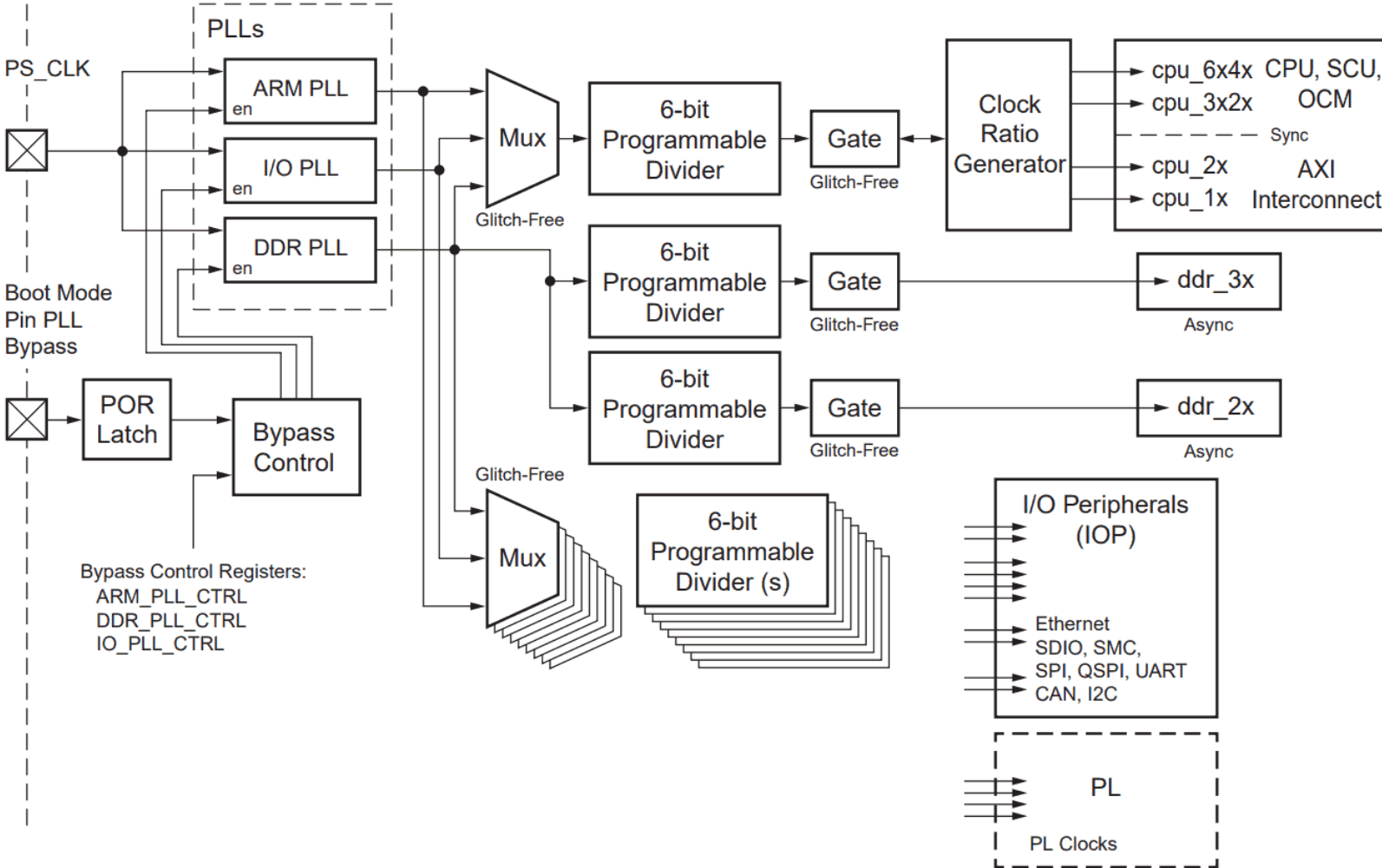
Version 2.2
27 January 2014

ZedBoard Clock Sources

2.5 Clock sources

The Zynq-7000 AP SoC's PS subsystem uses a dedicated 33.3333 MHz clock source, IC18, Fox 767-33.333333-12, with series termination. The PS infrastructure can generate up to four PLL-based clocks for the PL system. An on-board 100 MHz oscillator, IC17, Fox 767-100-136, supplies the PL subsystem clock input on bank 13, pin Y9.

Zynq Clock Resources



UG585_c25_01_102414

Zynq Clock Resources – Configuration in Vivado

The screenshot shows the Vivado Clock Configuration window. On the left is a Page Navigator with options like Zynq Block Design, PS-PL Configuration, Peripheral I/O Pins, MIO Configuration, Clock Configuration (selected), DDR Configuration, SMC Timing Calculator, and Interrupts. The main window is titled 'Clock Configuration' and has a 'Summary Report' link. It features two tabs: 'Basic Clocking' (active) and 'Advanced Clocking'. Under 'Basic Clocking', there are input fields for 'Input Frequency (MHz)' set to 33.333333 and 'CPU Clock Ratio' set to 6:2:1. Below these are search and filter icons, and a search input field. The core of the window is a table with columns: Component, Clock Source, Requested Frequency, Actual Frequency, and Range (MHz). The table is organized into expandable sections: Processor/Memory Clocks, IO Peripheral Clocks, CAN, PL Fabric Clocks, and System Debug Clocks. The 'IO Peripheral Clocks' section is expanded, showing rows for SMC, QSPI, ENET0, ENET1, SDIO, and SPI. The 'PL Fabric Clocks' section is also expanded, showing rows for FCLK_CLK0, FCLK_CLK1, FCLK_CLK2, and FCLK_CLK3. The SMC and FCLK_CLK0 rows are highlighted in blue.

Component	Clock Source	Requested Fre...	Actual Freque...	Range(MHz)
Processor/Memory Clocks				
IO Peripheral Clocks				
SMC	IO PLL	100	10.000000	10.000000 : 100.000000
QSPI	IO PLL	200	200.000000	10.000000 : 200.000000
ENET0	IO PLL	1000 Mbps	125.000000	
ENET1	IO PLL	1000 Mbps	10.000000	
SDIO	IO PLL	50	50.000000	10.000000 : 125.000000
SPI	IO PLL	166.666666	10.000000	0.000000 : 200.000000
CAN				
PL Fabric Clocks				
<input checked="" type="checkbox"/> FCLK_CLK0	IO PLL	100	100.000000	0.100000 : 250.000000
<input type="checkbox"/> FCLK_CLK1	IO PLL	50	10.000000	0.100000 : 250.000000
<input type="checkbox"/> FCLK_CLK2	IO PLL	50	10.000000	0.100000 : 250.000000
<input type="checkbox"/> FCLK_CLK3	IO PLL	50	10.000000	0.100000 : 250.000000
System Debug Clocks				

ZedBoard Available I/Os for the User (1)

2.7 User I/O

2.7.1 User Push Buttons

The ZedBoard provides 7 user GPIO push buttons to the Zynq-7000 AP SoC; five on the PL-side and two on the PS-side.

Pull-downs provide a known default state, pushing each button connects to Vcco.

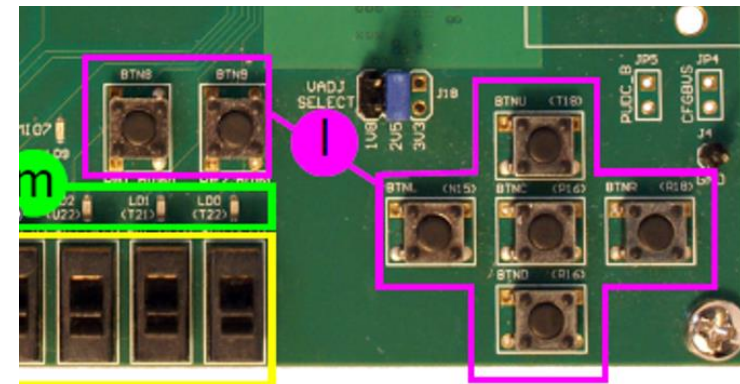
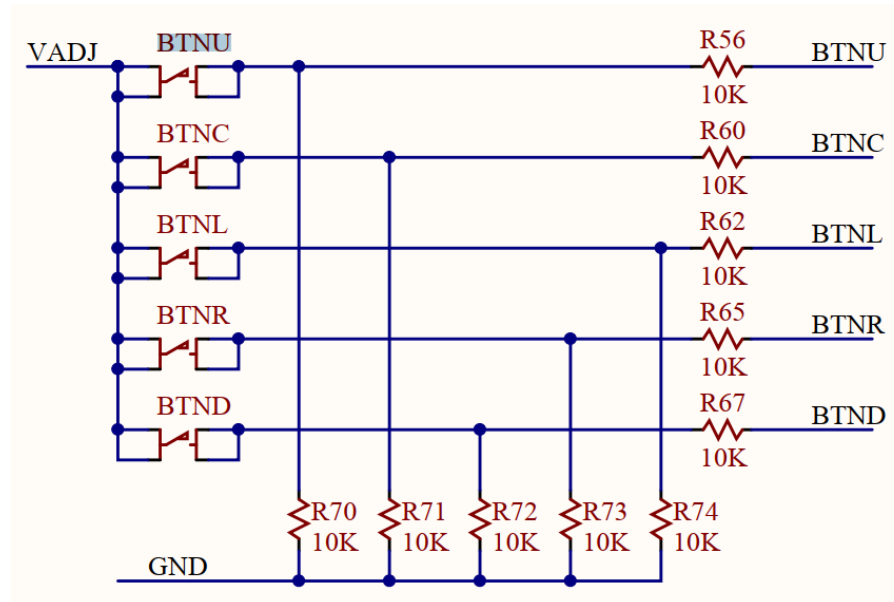


Table 12 - Push Button Connections

Signal Name	Subsection	Zynq pin
BTNU	PL	T18
BTNR	PL	R18
BTND	PL	R16
BTNC	PL	P16
BTNL	PL	N15
PB1	PS	D13 (MIO 50)
PB2	PS	C10 (MIO 51)



ZedBoard Available I/O for the User (2)

2.7.2 User DIP Switches

The ZedBoard has eight user dip switches, SW0-SW7, providing user input. SPDT switches connect the I/O through a 10kΩ resistor to the VADJ voltage supply or GND.

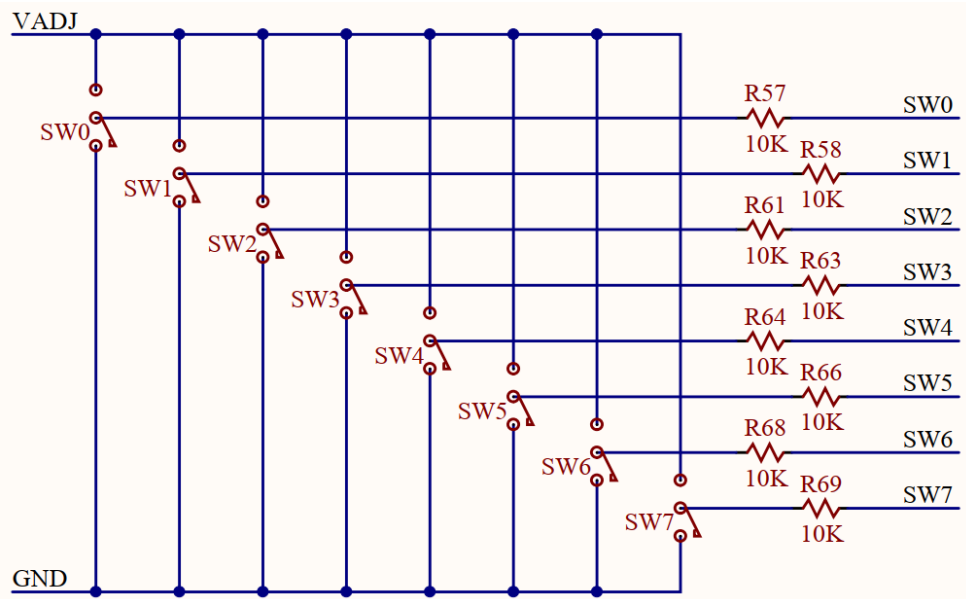
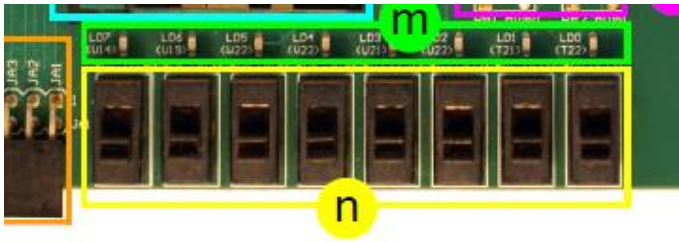
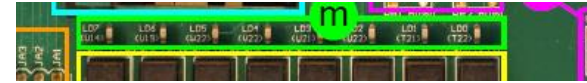


Table 13 - DIP Switch Connections

Signal Name	Zynq pin
SW0	F22
SW1	G22
SW2	H22
SW3	F21
SW4	H19
SW5	H18
SW6	H17
SW7	M15

ZedBoard Available I/O for the User (3)



2.7.3 User LEDs

The ZedBoard has eight user LEDs, LD0 – LD7. A logic high from the Zynq-7000 AP SoC I/O causes the LED to turn on. LED's are sourced from 3.3V banks through 390Ω resistors.

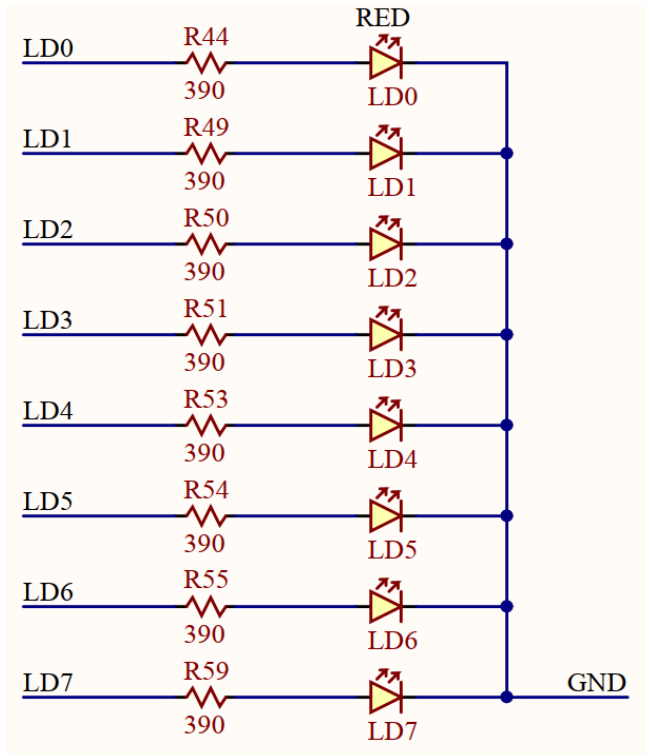


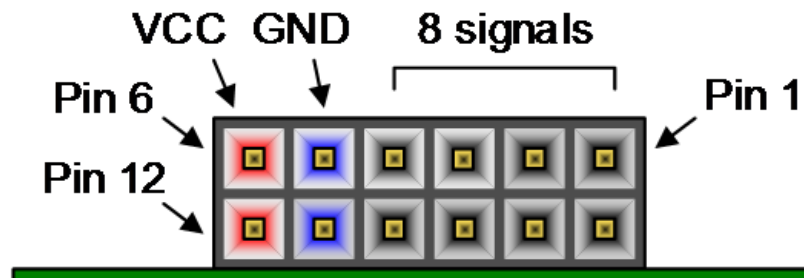
Table 14 - LED Connections

Signal Name	Subsection	Zynq pin
LD0	PL	T22
LD1	PL	T21
LD2	PL	U22
LD3	PL	U21
LD4	PL	V22
LD5	PL	W22
LD6	PL	U19
LD7	PL	U14
LD9	PS	D5 (MIO7)

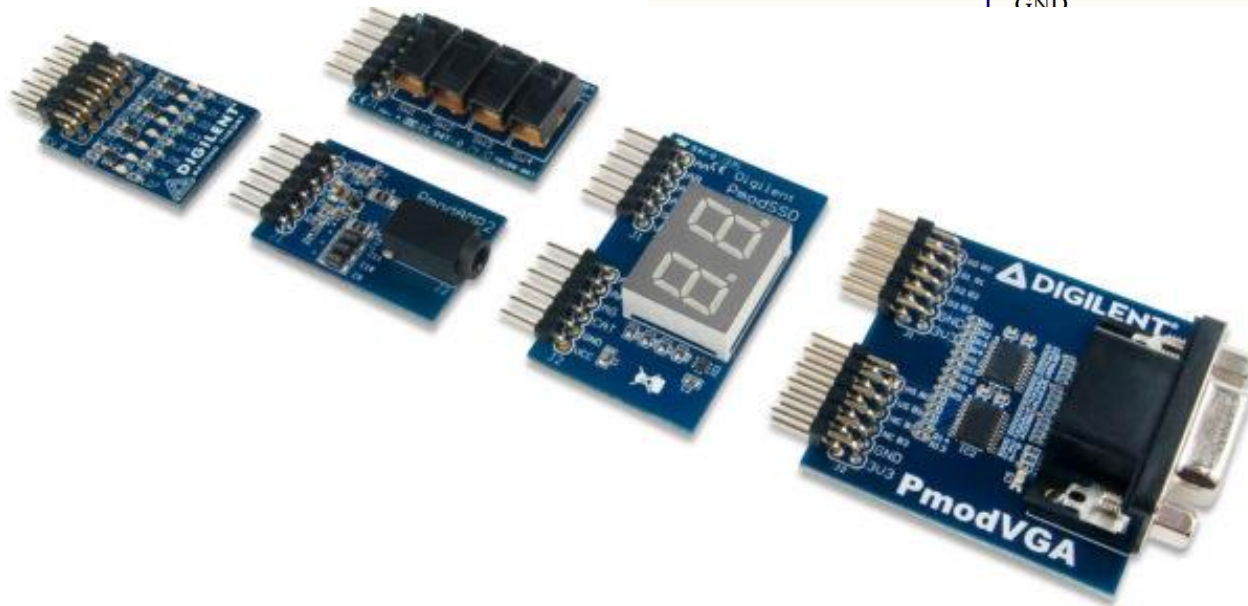
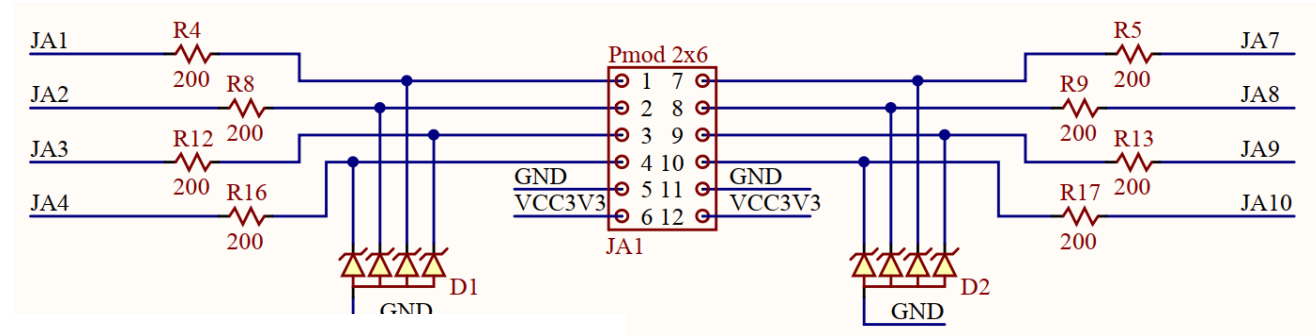
ZedBoard PMOD Connectors

Table 16 - Pmod Connections

Pmod	Signal Name	Zynq pin	Pmod	Signal Name	Zynq pin
JA1	JA1	Y11	JB1	JB1	W12
	JA2	AA11		JB2	W11
	JA3	Y10		JB3	V10
	JA4	AA9		JB4	W8
	JA7	AB11		JB7	V12
	JA8	AB10		JB8	W10
	JA9	AB9		JB9	V9
	JA10	AA8		JB10	V8

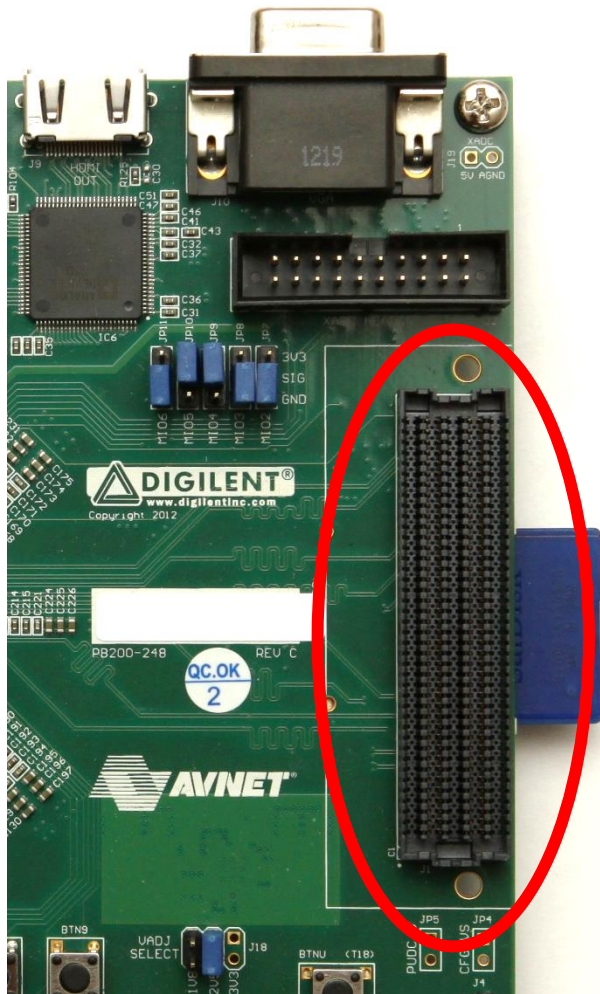


ZedBoard PMOD Boards



<https://digilent.com/reference/pmod/start>

LPC FMC Connector

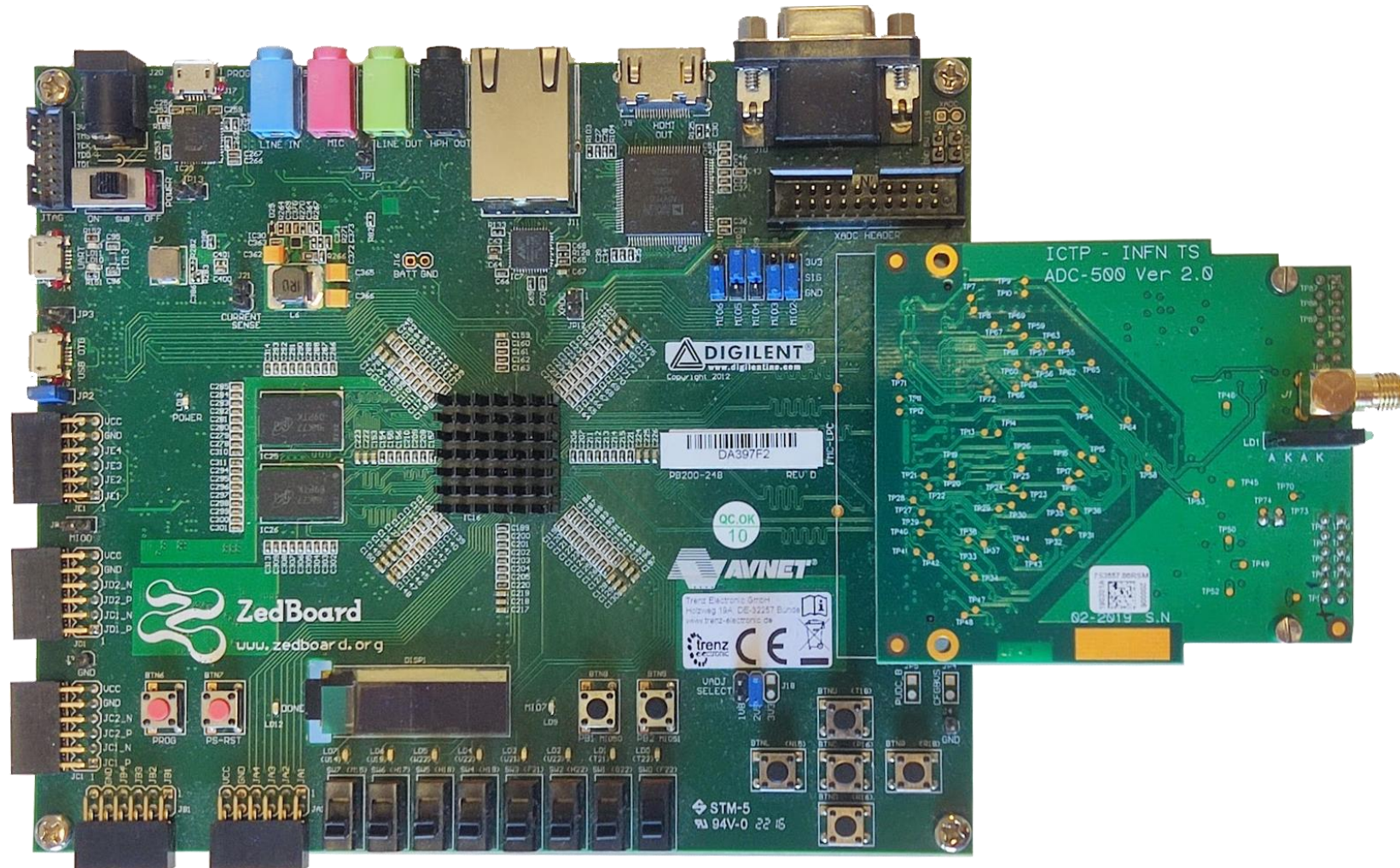


LPC: Low-Pin-Count

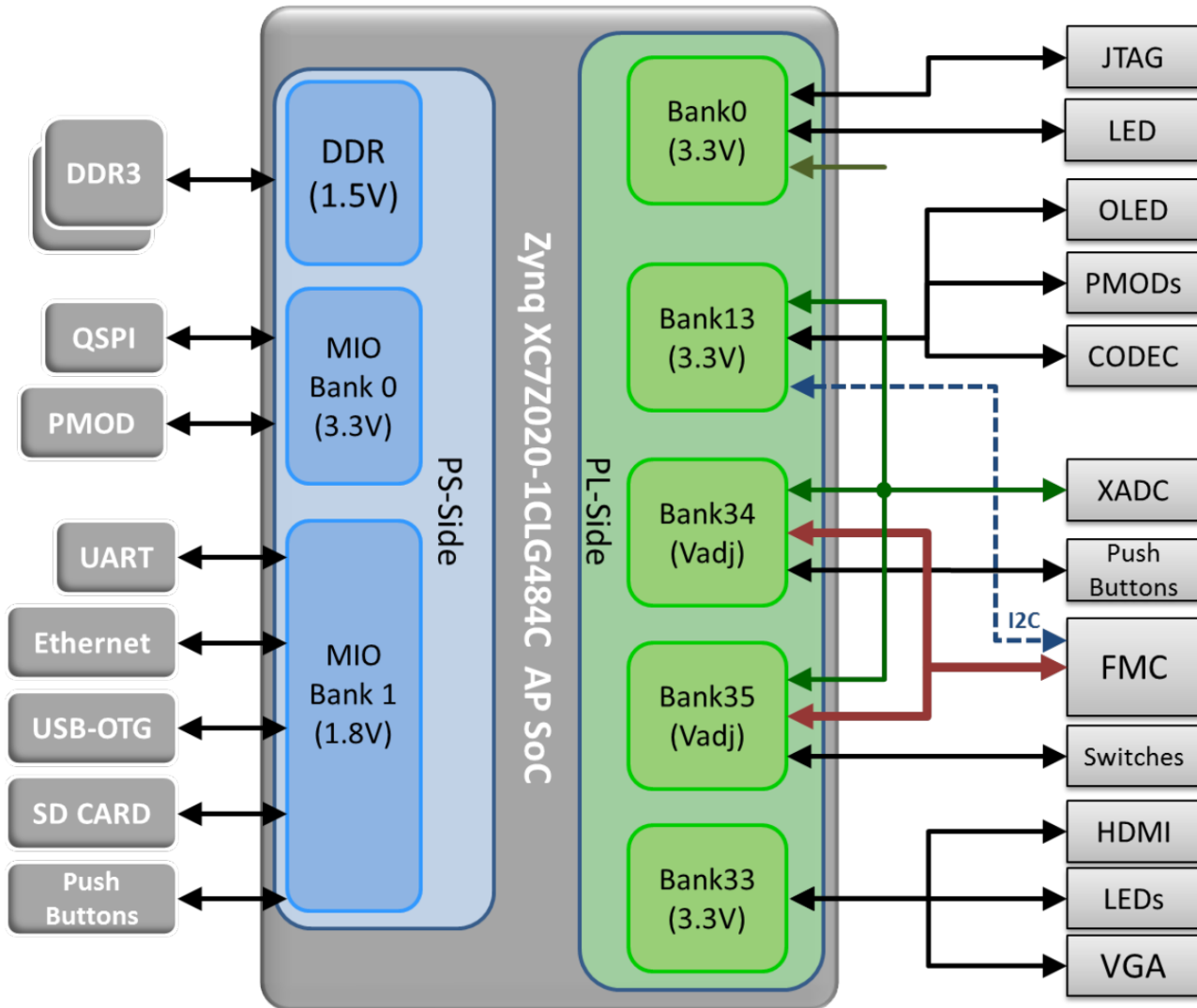
FMC: FPGA Mezzanine Card

- ✓ The LPC FMC exposes 68 single-ended I/O, which can be configured as 34 differential pairs.
- ✓ ADC500: an ICTP MLAB board is plugged into the LPC FMC and will be used in the final lab.

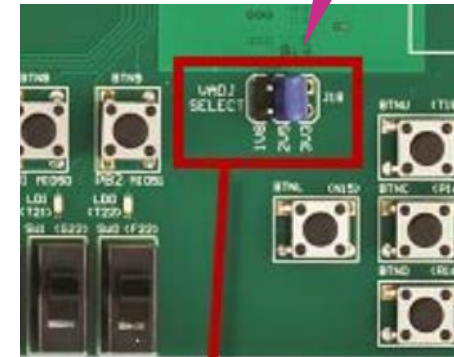
ZedBoard + ICTP-INFN ADC500



ZedBoard Bank Power Voltages



DO NOT MOVE



JP18

Vadj is selected by JP18:

- 1.8V
- 2.5V
- 3.3V