The Abdus Salam International Centre for Theoretical Physics

IAEA unesco

Workshop on Fully Programmable Systems-on-Chip for Scientific Applications

Lab 0: User environment

Maynor Ballina

IAEA International Atomic Energy Agency
Atoms for Peace and Development

IUB Independent University, Bangladesh

جامعة قطر QATAR UNIVERSITY

Universiti Kebangsaan Malaysia
The National University of Malaysia

The Abdus Salam International Centre for Theoretical Physics

Welcome: Lab tutors

Maynor Ballina (ICTP, UNIT) [Guatemala]

Dr. Luis Garcia (ICTP) [Guatemala]

Dr. Romina Molina (ICTP) [Argentina]

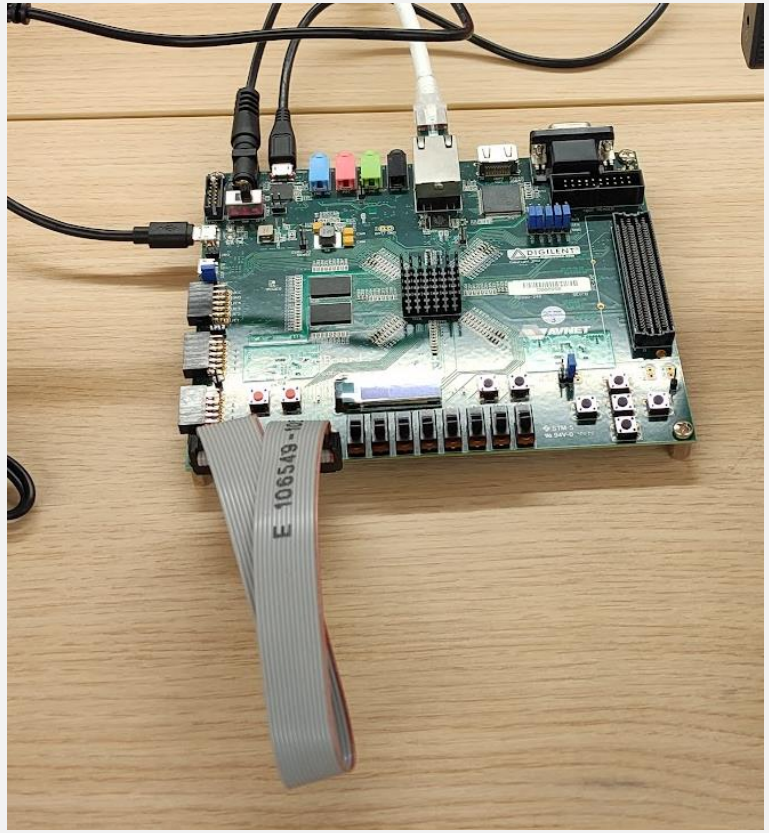
Dr. Agustin silva (TII) [Argentina]

Labs Overview:

- Lab 0: User environment
- Lab 1: Hello World and GPIO In/Out
- Lab 2: ComBlock and RTL
- Lab 3: SoC-FPGA Development Framework

Projects

- Introduction to machine learning and SoC/FPGA
- Digital Pulse Processing for Isotope Identification



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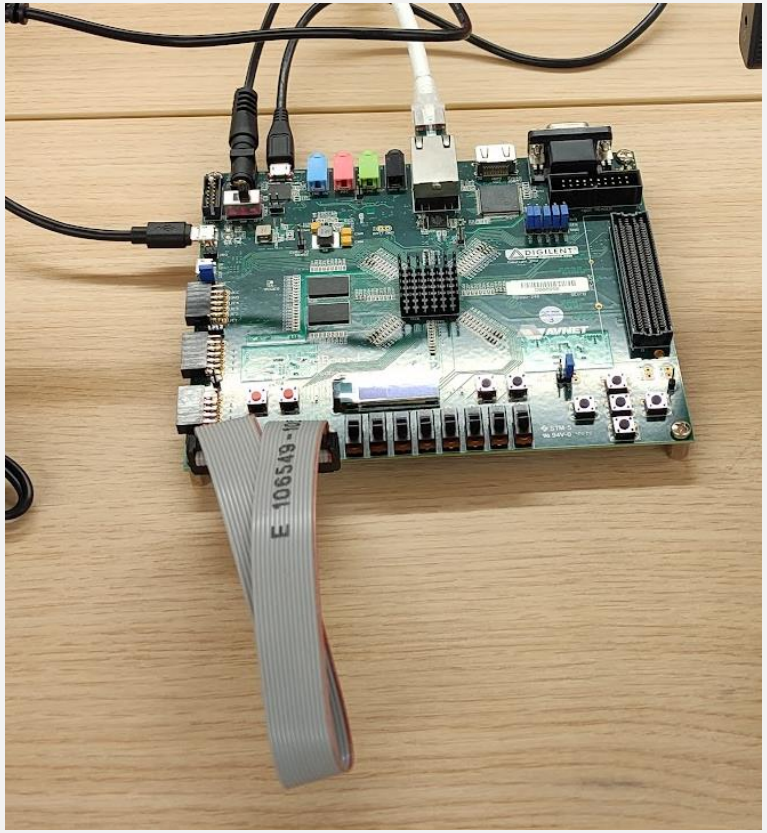
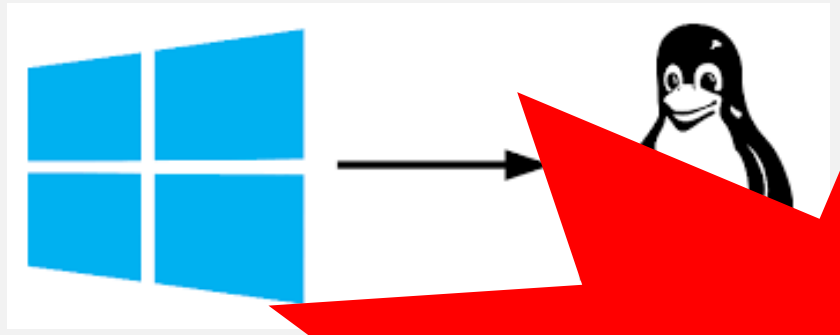


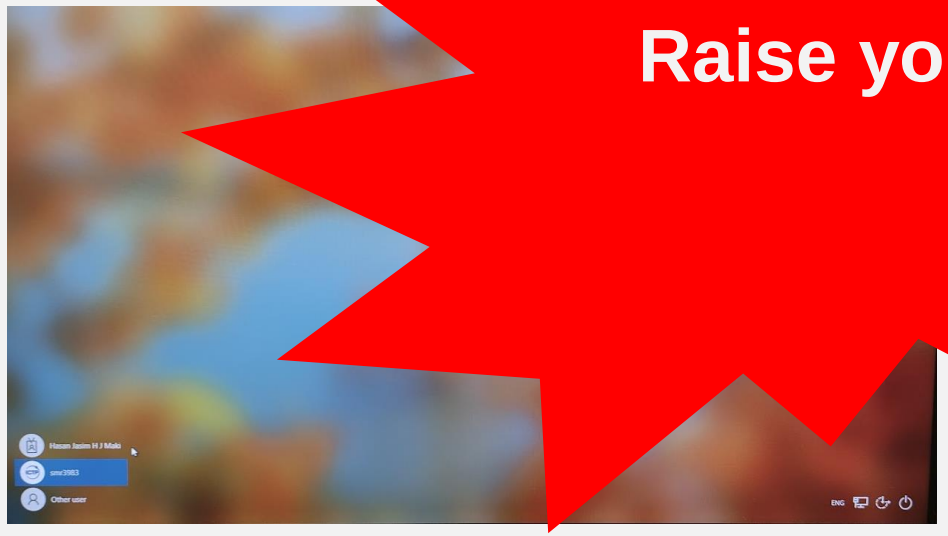
User Environment:



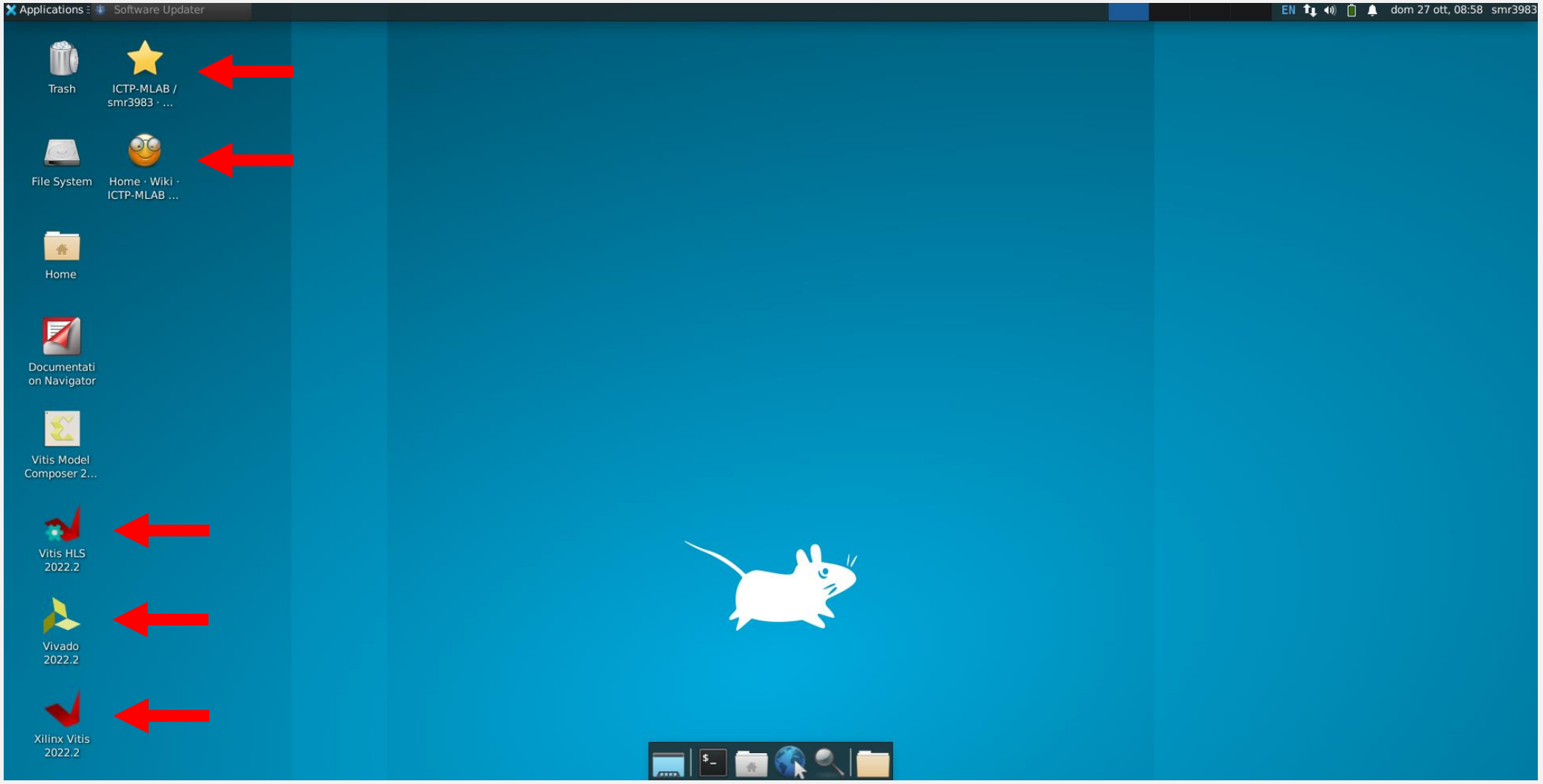
Use smr3983

3983smr!CPT24

Raise your hand



User Environment:



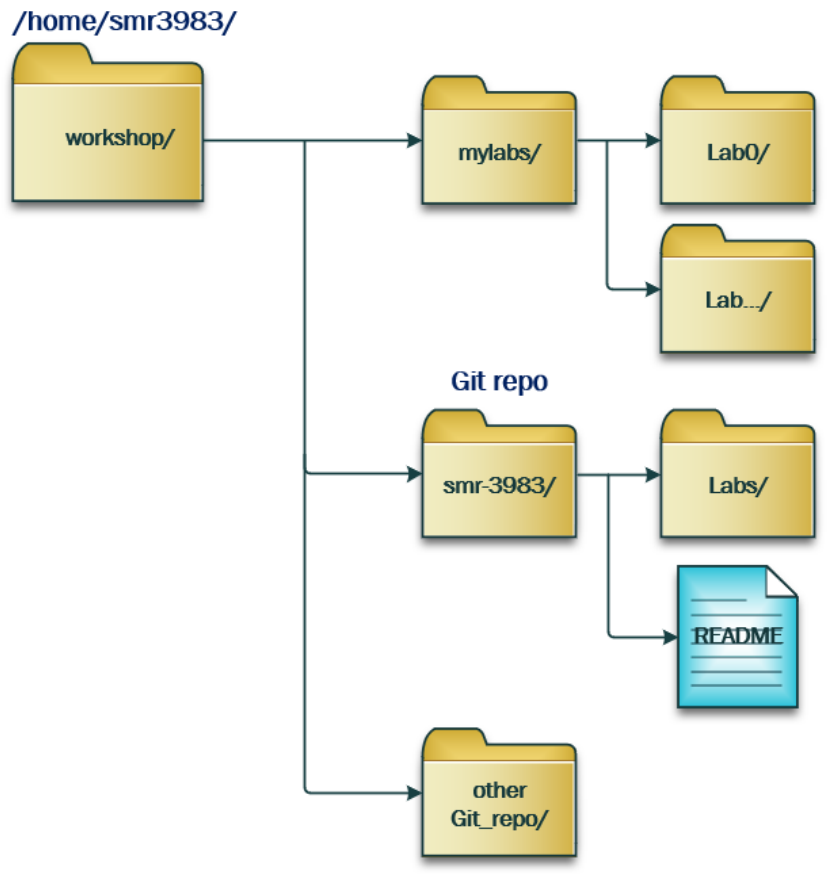
Important links:

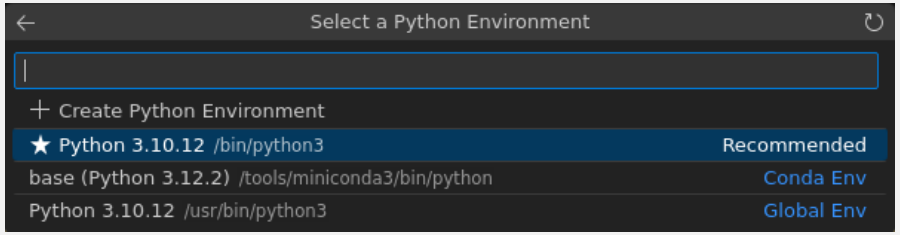
https://gitlab.com/ictp-mlab/smr-3983

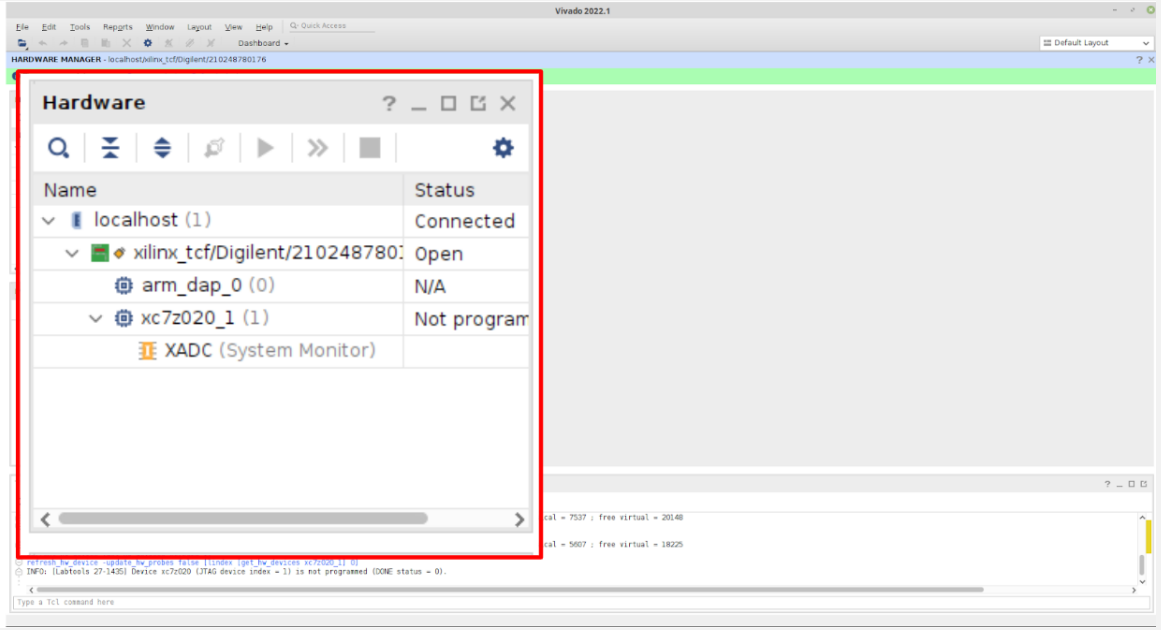
Important links:

https://gitlab.com/ictp-mlab/smr-3983/-/wikis/home

Labs 0:


/home/smr3983/
workshop/
mylabs/
Lab0/
Lab.../
Git repo
smr-3983/
Labs/
README
other
Git_repo/


Select a Python Environment
Create Python Environment
Python 3.10.12 /bin/python3
Recommended
base (Python 3.12.2) /tools/miniconda3/bin/python
Conda Env
Python 3.10.12 /usr/bin/python3
Global Env


Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Digilent/210248780
Open
arm_dap_0 (0)
N/A
xc7z020_1 (1)
XADC (System Monitor)

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Lab 1: Hello World and GPIO In/Out

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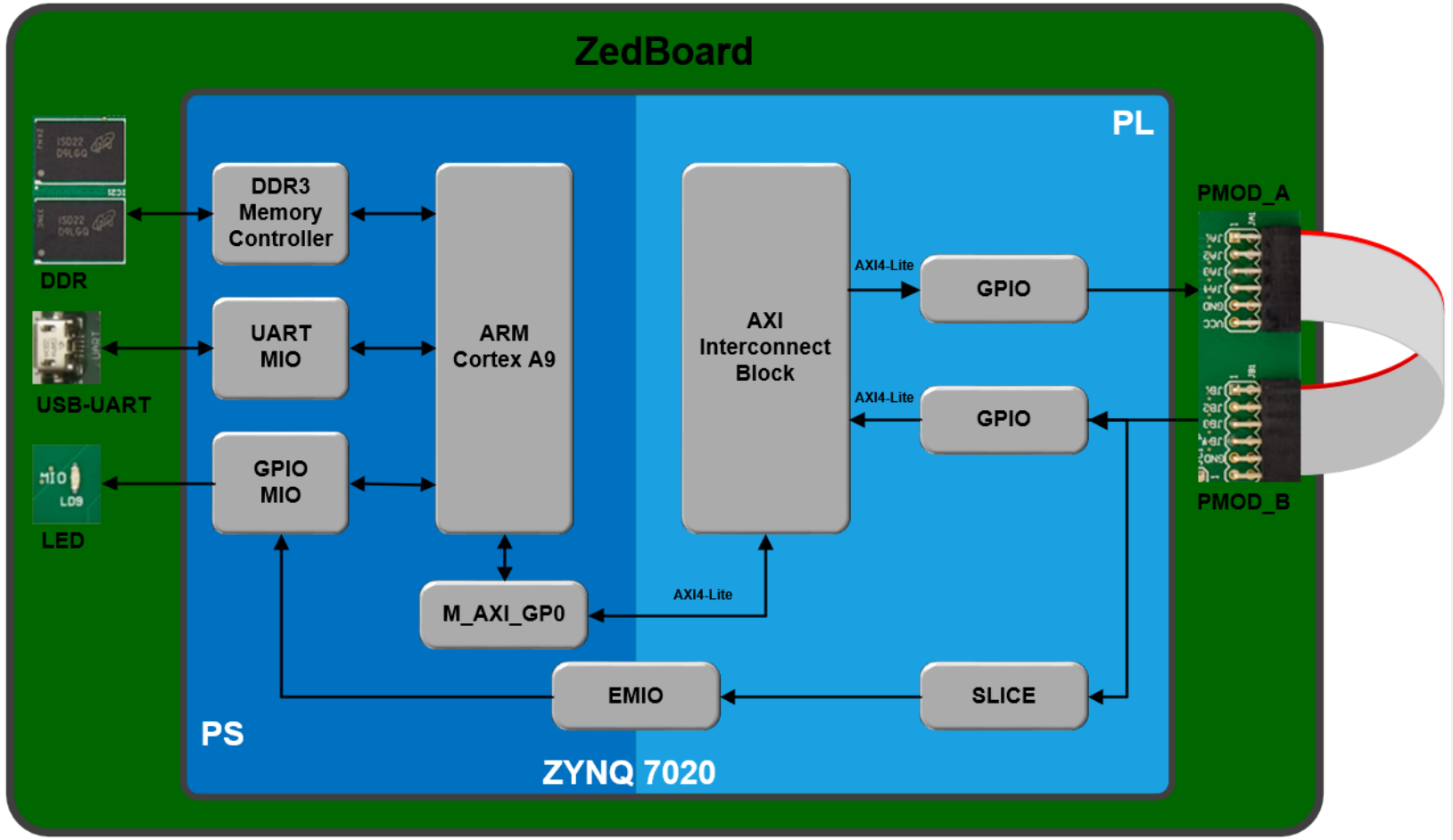
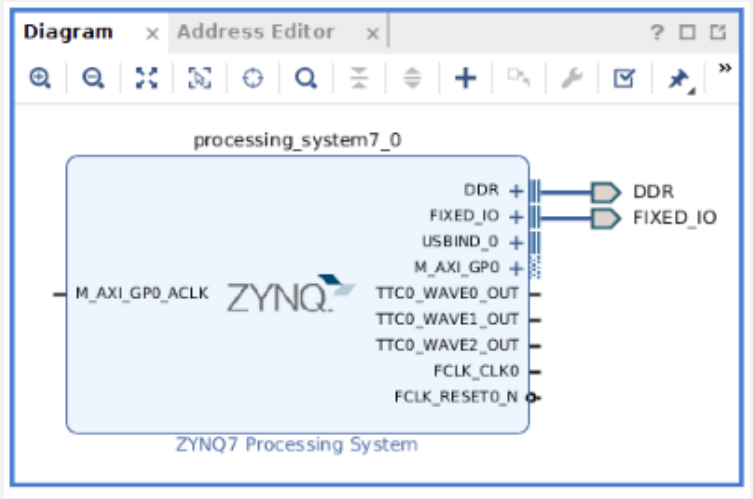
Labs 1: Objectives

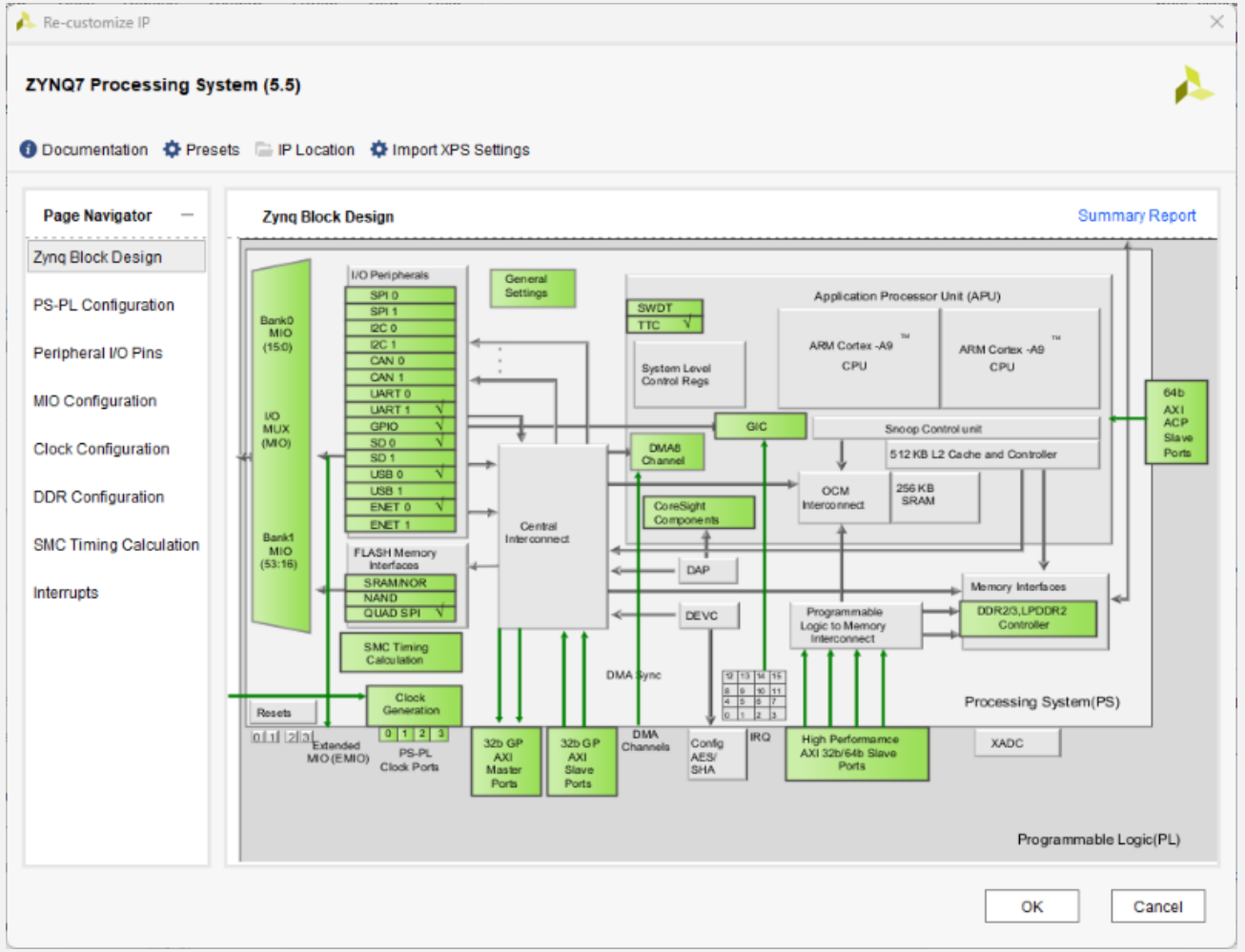
- Acquire the knowledge of the SoC-FPGA design flow using the Vitis Unified Software Platform.
- Create the hardware to configure the FPGA part of the SoC, configure the PS instantiate the GPIO blocks and understand the communication between the different components of the design
- Create the 'C' application that will run on the PS to control the reading and the writing of the generated hardware
- Test the complete design on the ZedBoard platform to verify the implementation.

Labs 1: Design description

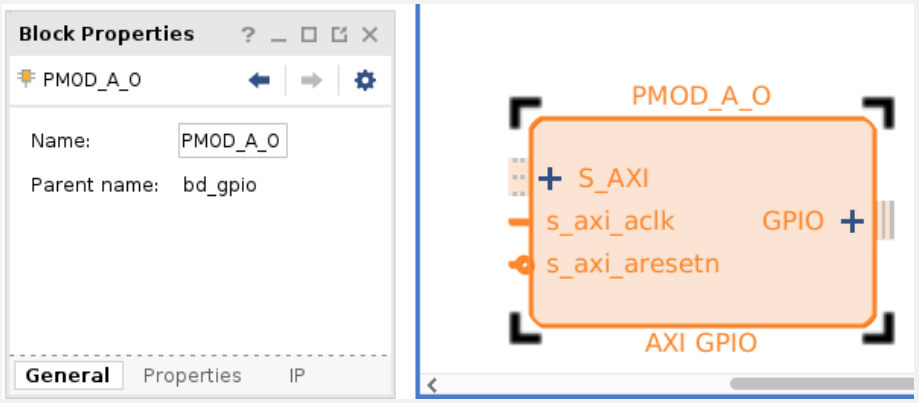


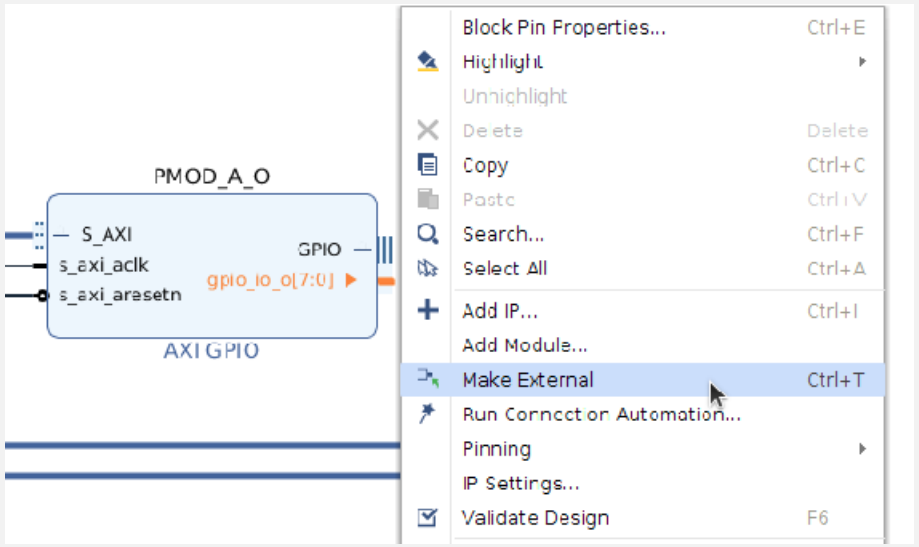
Labs 1: Hardware

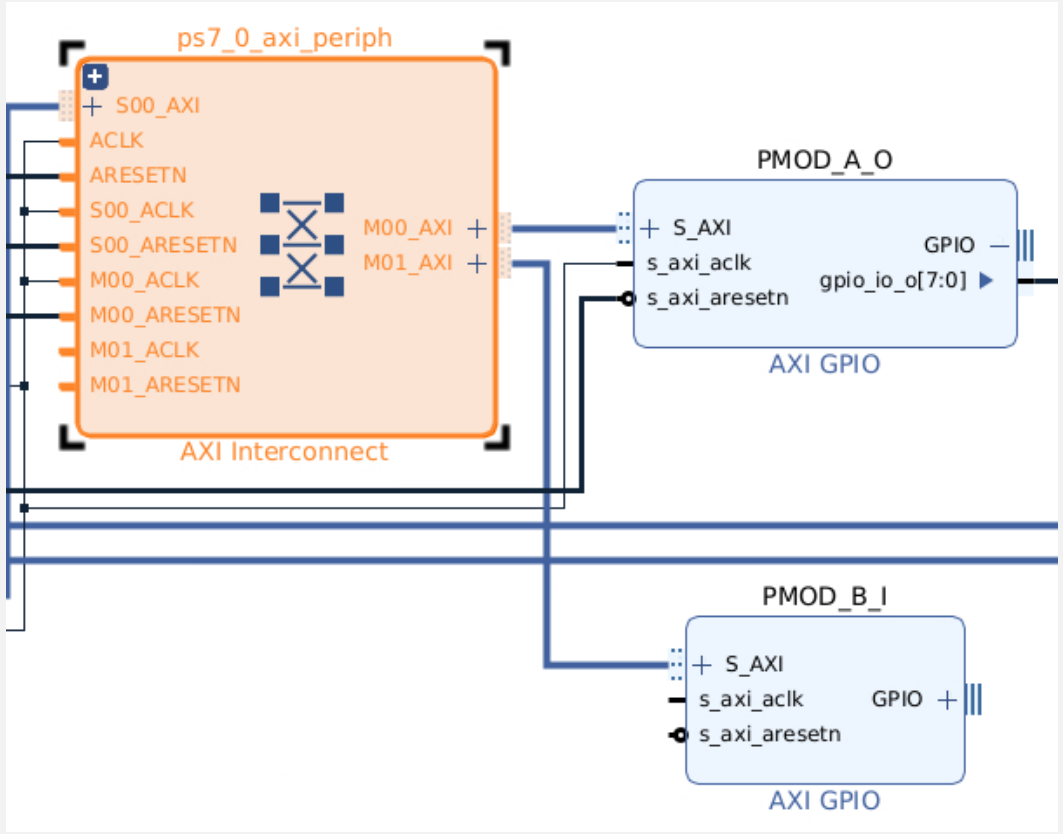




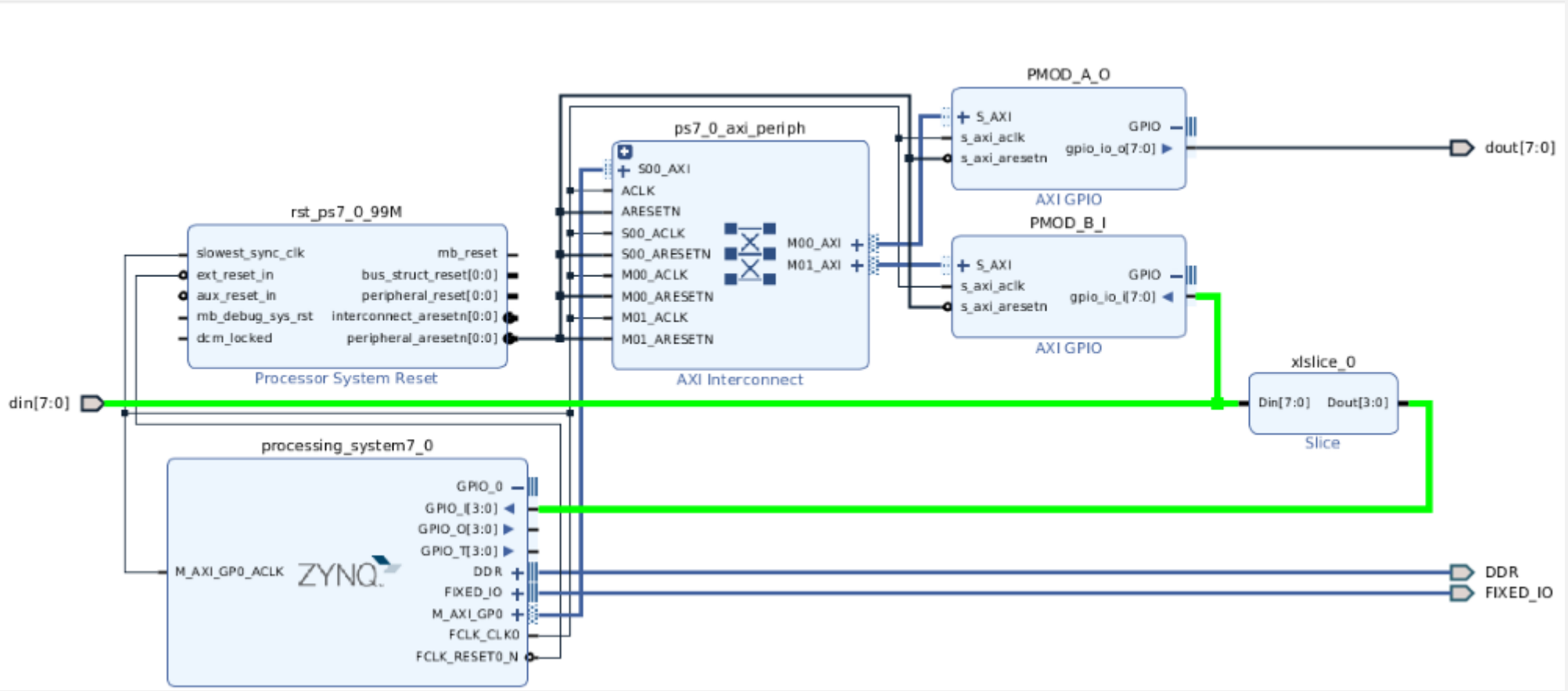
Labs 1: Steps


Block Properties
PMOD_A_0
Name:
PMOD_A_0
Parent name:
bd_gpio
General
Properties
IP
PMOD_A_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
AXI GPIO


PMOD_A_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
gpio_io_o[7:0]
AXI GPIO
Block Pin Properties... Ctrl+E
Highlight
Unhighlight
Delete Delete
Copy Ctrl+C
Paste Ctrl+V
Search... Ctrl+F
Select All Ctrl+A
Add IP... Ctrl+I
Add Module...
Make External Ctrl+T
Run Connection Automation...
Pinning
IP Settings...
Validate Design F6

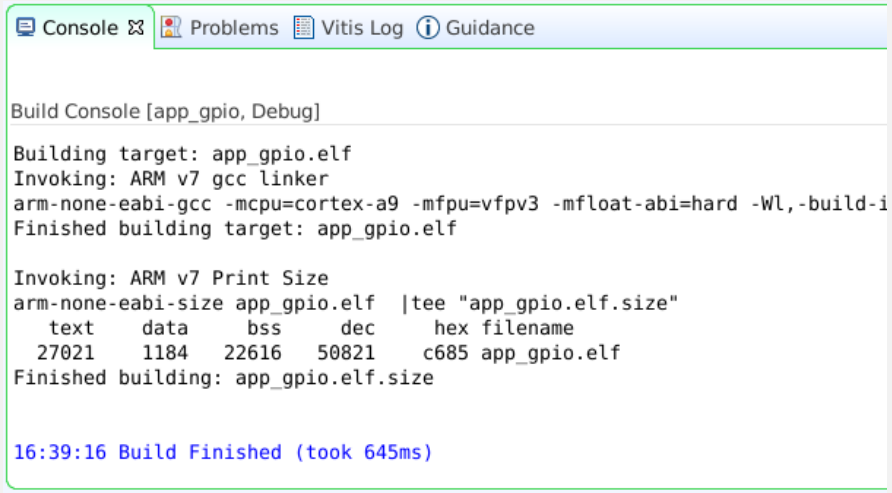

ps7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
PMOD_A_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
gpio_io_o[7:0]
AXI GPIO
PMOD_B_I
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
AXI GPIO

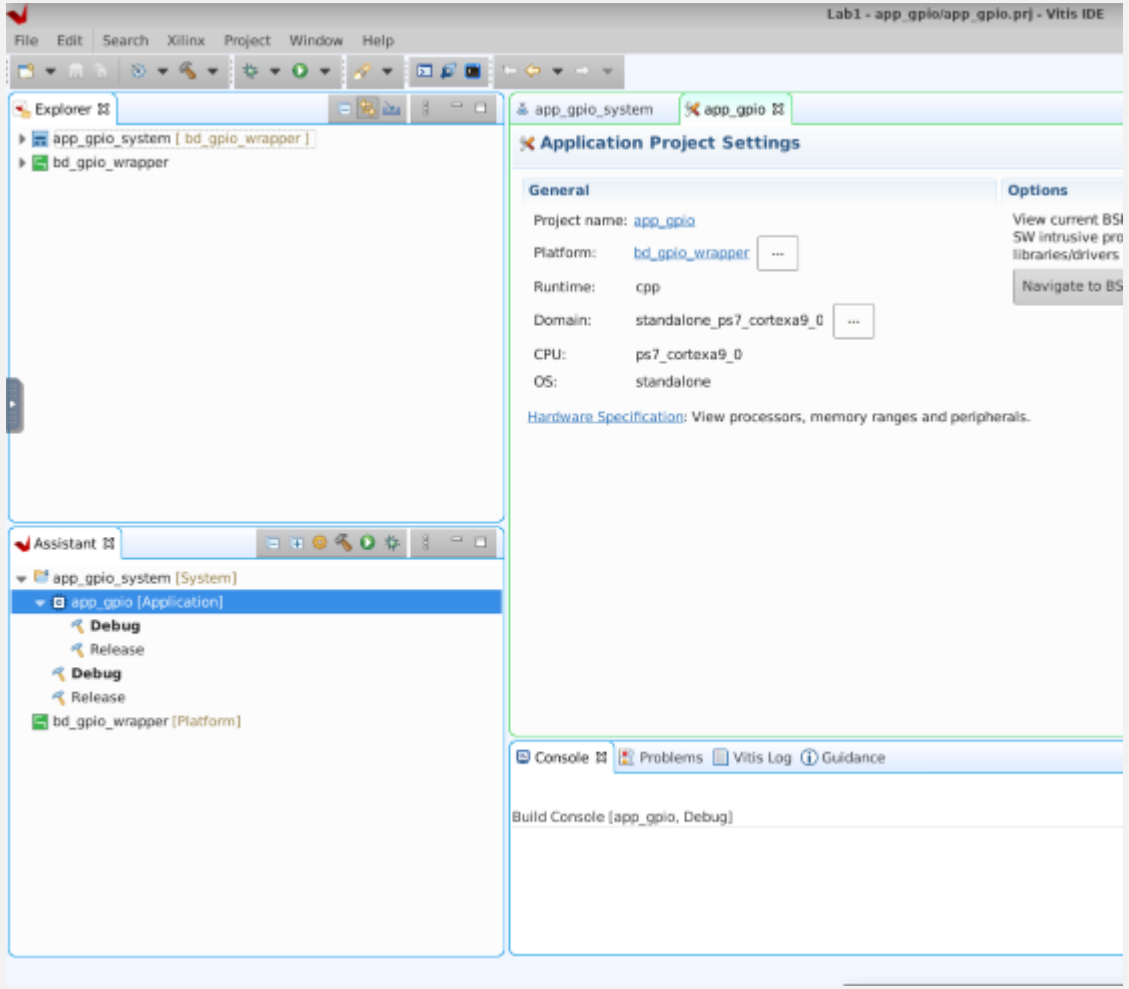
Labs 1: Final Block Design



Labs 1: Software

- Application project
- C program
- AXI Communication





Labs 1: Results

- PL Hardware
- PS program
- AXI Communication
- PMOD data transfer

Optional:

- Challenge

```
PMODA Output: 213, PMODB Receive: 213  PSGPIO Receive 13
PMODA Output: 214, PMODB Receive: 214  PSGPIO Receive 13
PMODA Output: 215, PMODB Receive: 215  PSGPIO Receive 13
PMODA Output: 216, PMODB Receive: 216  PSGPIO Receive 13
PMODA Output: 217, PMODB Receive: 217  PSGPIO Receive 13
PMODA Output: 218, PMODB Receive: 218  PSGPIO Receive 13
PMODA Output: 219, PMODB Receive: 219  PSGPIO Receive 13
PMODA Output: 220, PMODB Receive: 220  PSGPIO Receive 13
PMODA Output: 221, PMODB Receive: 221  PSGPIO Receive 13
PMODA Output: 222, PMODB Receive: 222  PSGPIO Receive 13
PMODA Output: 223, PMODB Receive: 223  PSGPIO Receive 13
PMODA Output: 224, PMODB Receive: 224  PSGPIO Receive 14
PMODA Output: 225, PMODB Receive: 225  PSGPIO Receive 14
PMODA Output: 226, PMODB Receive: 226  PSGPIO Receive 14
PMODA Output: 227, PMODB Receive: 227  PSGPIO Receive 14
PMODA Output: 228, PMODB Receive: 228  PSGPIO Receive 14
PMODA Output: 229, PMODB Receive: 229  PSGPIO Receive 14
PMODA Output: 230, PMODB Receive: 230  PSGPIO Receive 14
PMODA Output: 231, PMODB Receive: 231  PSGPIO Receive 14
PMODA Output: 232, PMODB Receive: 232  PSGPIO Receive 14
PMODA Output: 233, PMODB Receive: 233  PSGPIO Receive 14
PMODA Output: 234, PMODB Receive: 234  PSGPIO Receive 14
PMODA Output: 235, PMODB Receive: 235  PSGPIO Receive 14
PMODA Output: 236, PMODB Receive: 236  PSGPIO Receive 14
PMODA Output: 237, PMODB Receive: 237  PSGPIO Receive 14
PMODA Output: 238, PMODB Receive: 238  PSGPIO Receive 14
PMODA Output: 239, PMODB Receive: 239  PSGPIO Receive 14
```

User: smr3983
Password: 3983smr!CPT24

WARNING: Do not fail the password more than 3 times.
Feel free to raise your hand. Is better ask for help.

Links:

WhatsApp group

Google Fotos