

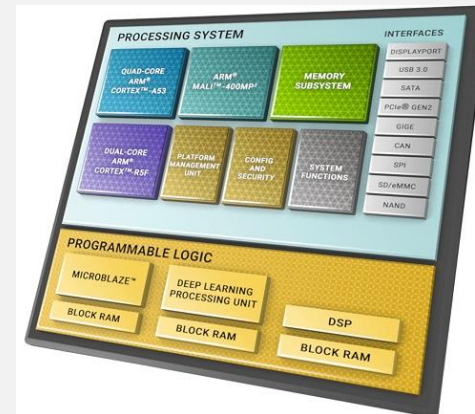
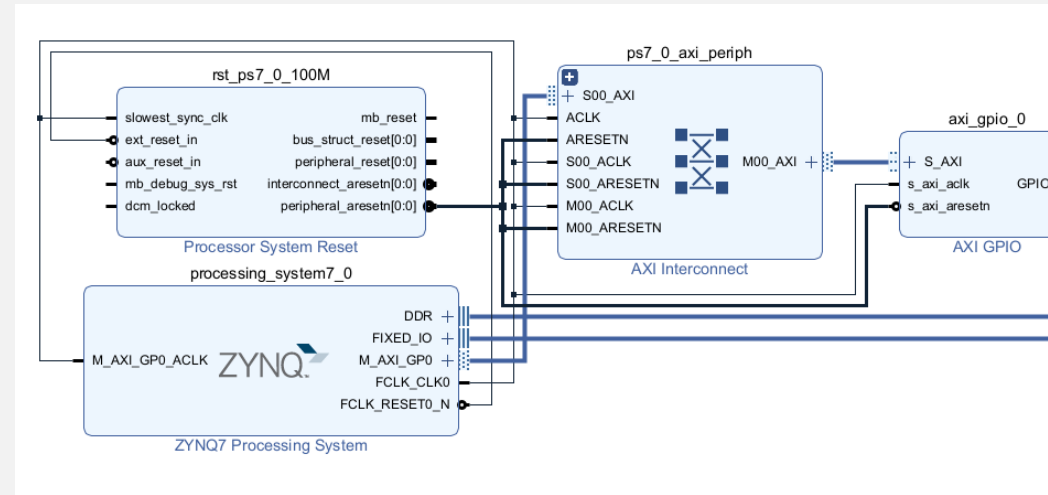
Workshop on Fully Programmable Systems-on-Chip for Scientific Applications

Lab 2: The RVI communication block: ComBlock

Maynor Ballina

Introduction

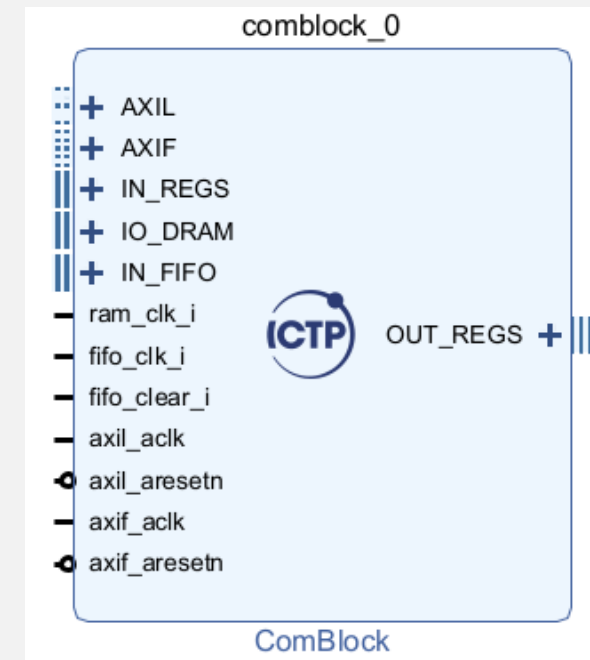
- Vendor specific interconnects (AXI, AVALON, Chiplink).
- What we learned yesterday?
 - ✓ AXI interconnect,
 - ✓ memory address,
 - ✓ data.
- Communication Block (ComBlock).



What is the ComBlock?

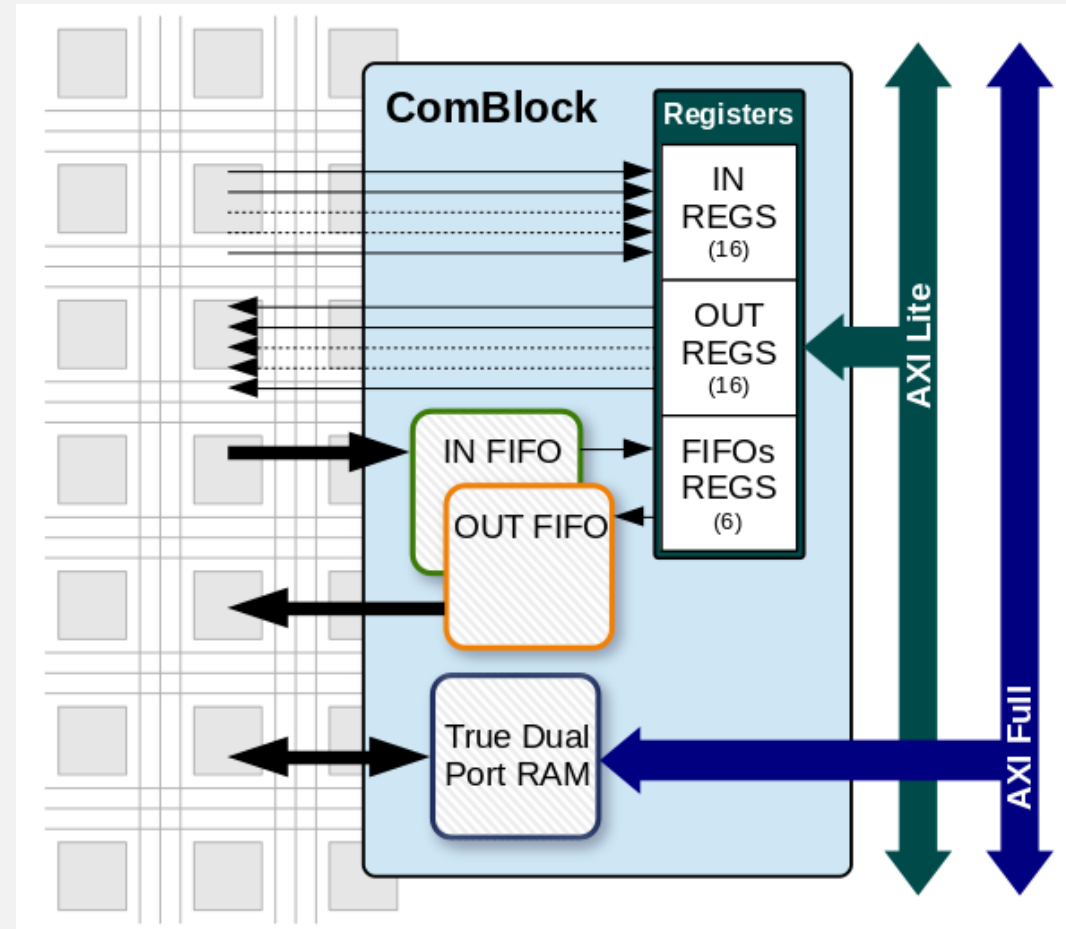
A communication block that abstracts you from the AXI protocol.

- Interconnect: AXI - Known interfaces (registers, RAM and FIFOs).
- Configurable resources, width, length, etc.
- Simple Clock-Domain-Crossing with FIFOs and TDPRAM.
- C driver for easy complete project integration.



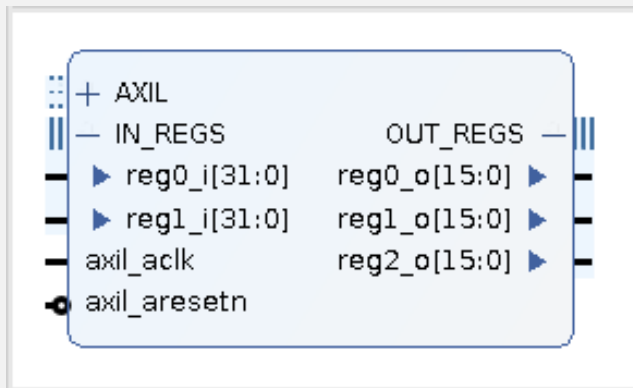
Features

- I/O Registers, I/O FIFOs, and TDPRAM.
- AXI Lite: Registers and FIFOs.
- AXI Full: TDPRAM.



Registers

- 16 input registers (FPGA to Processor).
- 16 output registers (Processor to FPGA).
- User configurable data width, 1-32 bits.
- Input and output independently enabled.

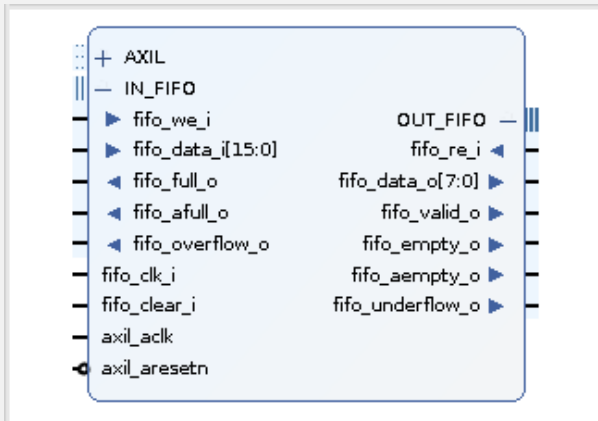


Registers

Input (FPGA to PROC)		Output (PROC to FPGA)	
<input checked="" type="checkbox"/> Enable		<input checked="" type="checkbox"/> Enable	
Data Width	<input type="text" value="32"/> [1 - 32]	Data Width	<input type="text" value="16"/> [1 - 32]
Quantity	<input type="text" value="2"/> [1 - 16]	Quantity	<input type="text" value="3"/> [1 - 16]

FIFOs

- Input and output FIFOs.
- Customizable width and depth.
- Asynchronous.
- Control registers on the Processor's side.

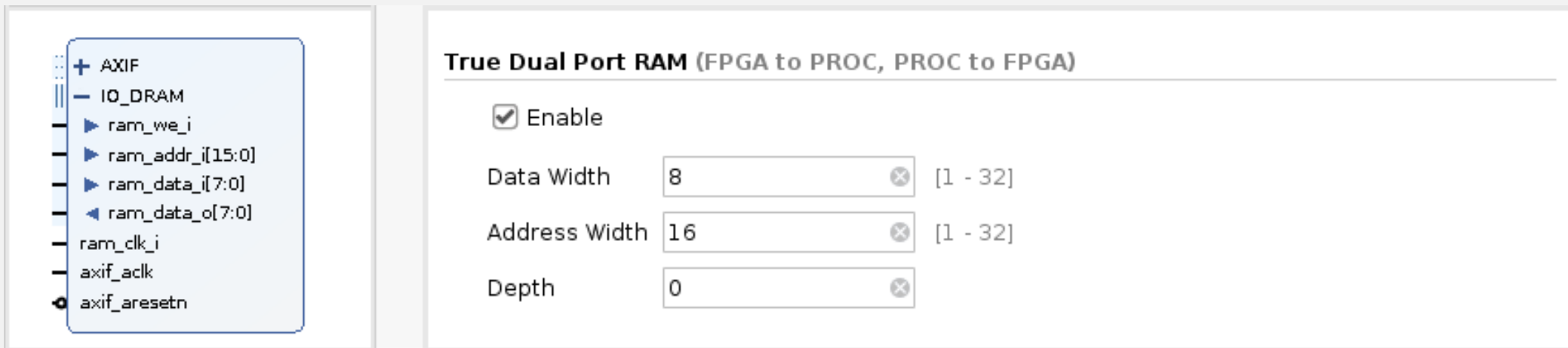


FIFOs

Input (FPGA to PROC)		Output (PROC to FPGA)	
<input checked="" type="checkbox"/> Enable		<input checked="" type="checkbox"/> Enable	
Data Width	16 [1 - 32]	Data Width	8 [1 - 32]
Depth	1024	Depth	256
Almost Full Offset	1	Almost Full Offset	1
Almost Empty Offset	1	Almost Empty Offset	1

TDPRAM

- Bidirectional.
- Clock-domain-crossing.
- Configurable depth, width and address width.

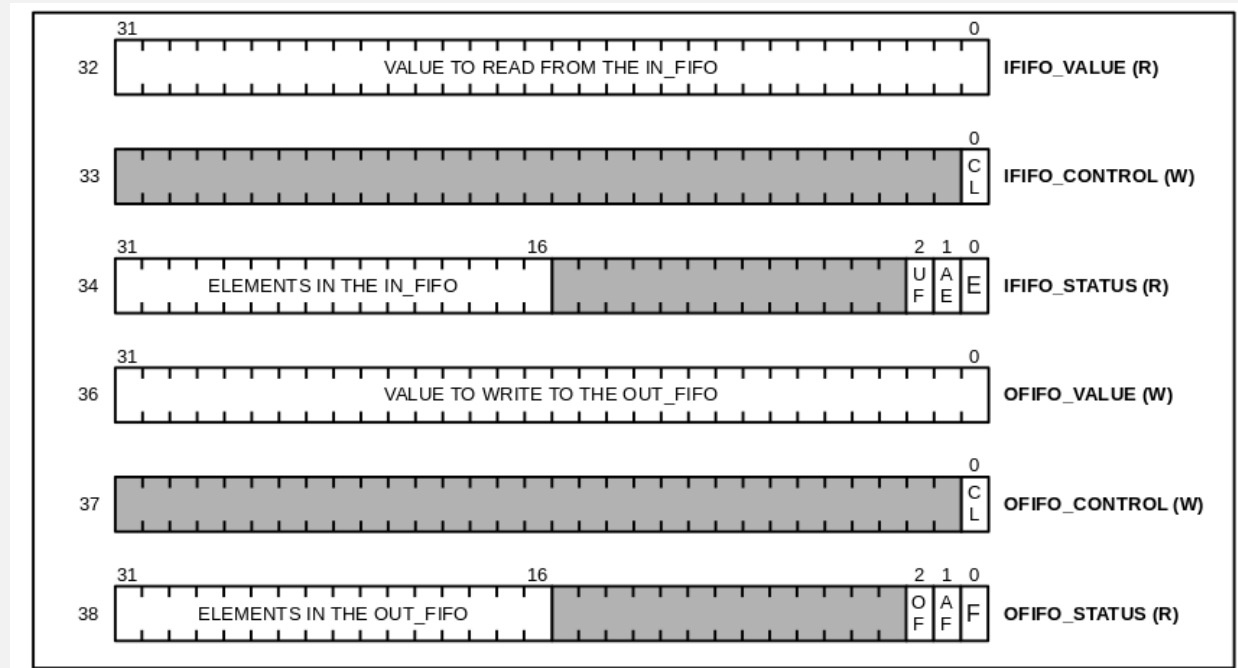


The image shows a configuration window for the True Dual Port RAM. On the left, a port list includes: + AXIF, - IO_DRAM, ram_we_i, ram_addr_i[15:0], ram_data_i[7:0], ram_data_o[7:0], ram_clk_i, axif_ack, and axif_aresetn. The main configuration area is titled "True Dual Port RAM (FPGA to PROC, PROC to FPGA)" and contains the following settings:

Parameter	Value	Range
Enable	<input checked="" type="checkbox"/>	
Data Width	8	[1 - 32]
Address Width	16	[1 - 32]
Depth	0	

Processor Interaction

- Device information in **xparameters.h**.
- Register mappings in **comblock.h**.
- CB_IREG, CB_OREG, ...
- Control registers.



C Drives

- Read and write functions **single memory position**:

```
void cbWrite(UINTPTR baseaddr, u32 reg, u32 value)
```

```
u32 cbRead(UINTPTR baseaddr, u32 reg)
```

- Read and write several **contiguous memory positions**:

```
void cbWriteBulk(UINTPTR baseaddr, int *buffer, u32 depth)
```

```
void cbReadBulk(int *buffer, UINTPTR baseaddr, u32 depth)
```

Where and how to get it?

- Hosted on GitLab (with continuous updates):

```
git clone https://gitlab.com/ictp-mlab/core-comblock.git
```

- Completely open source under BSD 3-clause license.
- Rodrigo Melo, collaboration between the Multidisciplinary Laboratory (MLAB) from The Abdus Salam International Centre for Theoretical Physics (ICTP, Italy). (not updated)

Workshop on Fully Programmable Systems-on-Chip for Scientific Applications

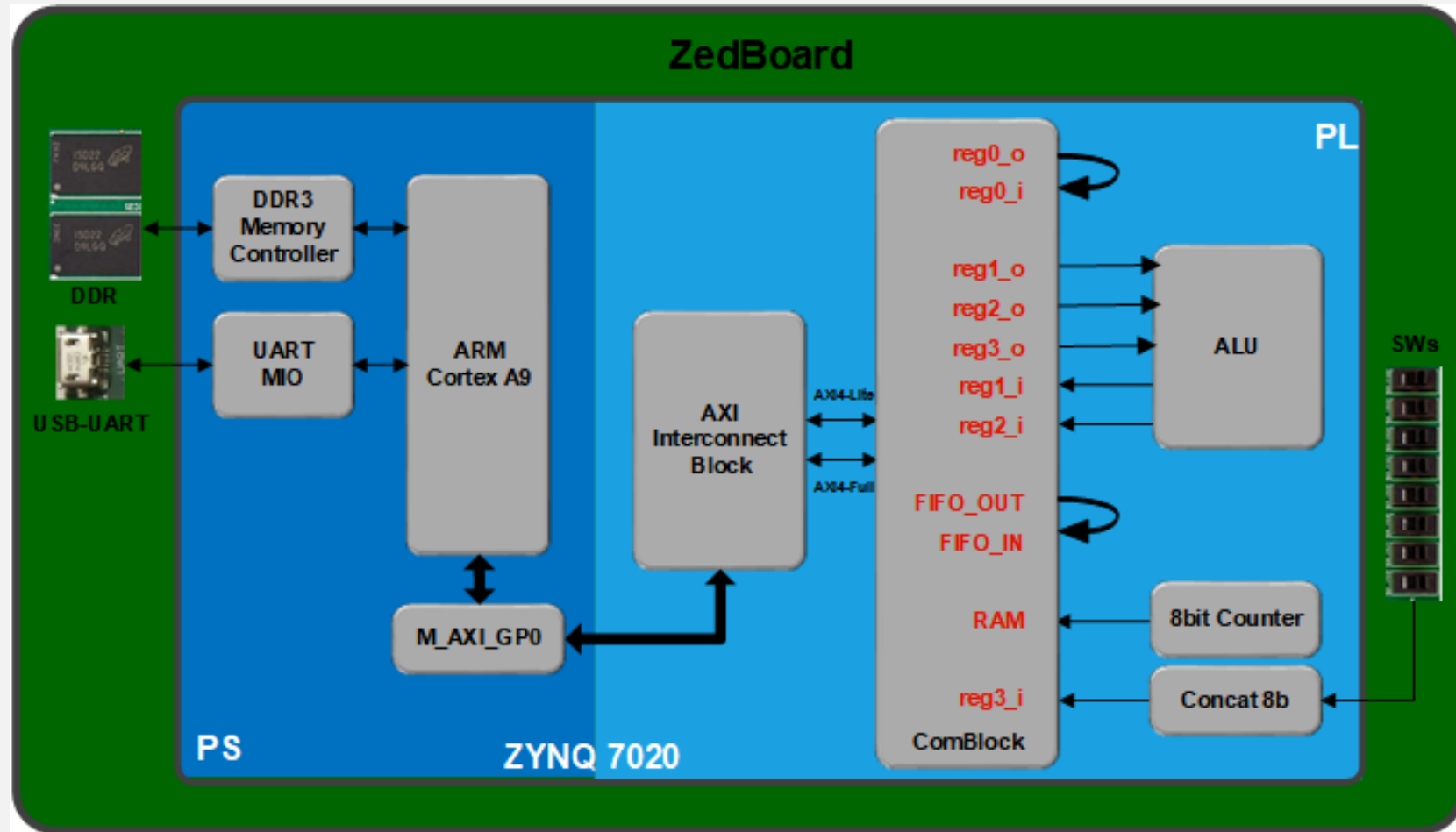
Lab 2: ComBlock and RTL instantiation

Maynor Ballina

Labs 2: Objectives

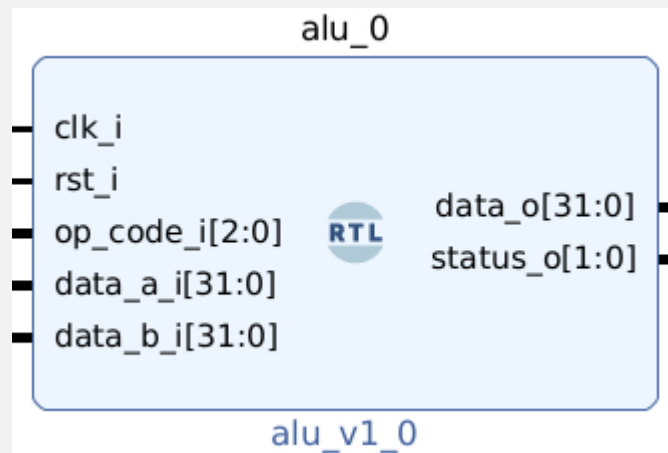
- Simulate a simple ALU and understand the VHDL code.
- Use and configuration of the ****ComBlock**** IP.
- Understand the data transfer between PL and PS using ****ComBlock**** IP.
- Instantiate RTL blocks and control them through the ****ComBlock**** registers.
- Perform unsigned integer arithmetic operations.

Labs 2: Design description



Labs 2: Hardware

RTL block, VHDL coded.
Unsigned integer data.
Customizable data width.



The screenshot shows the 'Re-customize IP' window for 'ComBlock (2.0)'. The window is divided into two main sections: a component list on the left and configuration options on the right.

Component List (Left):

- + AXIL
- + AXIF
- + IN_REGS
- + IO_DRAM
- + IN_FIFO
- ram_clk_i
- fifo_clk_i
- fifo_clear_i
- axil_ack
- axil_aresetn
- axif_ack
- axif_aresetn
- OUT_REGS
- OUT_FIFO

Configuration Options (Right):

Component Name: `comblock_0`

Registers

Input (FPGA to PROC)	Output (PROC to FPGA)
<input checked="" type="checkbox"/> Enable	<input checked="" type="checkbox"/> Enable
Data Width: 32 [1 - 32]	Data Width: 32 [1 - 32]
Quantity: 4 [1 - 16]	Quantity: 4 [1 - 16]

True Dual Port RAM (FPGA to PROC, PROC to FPGA)

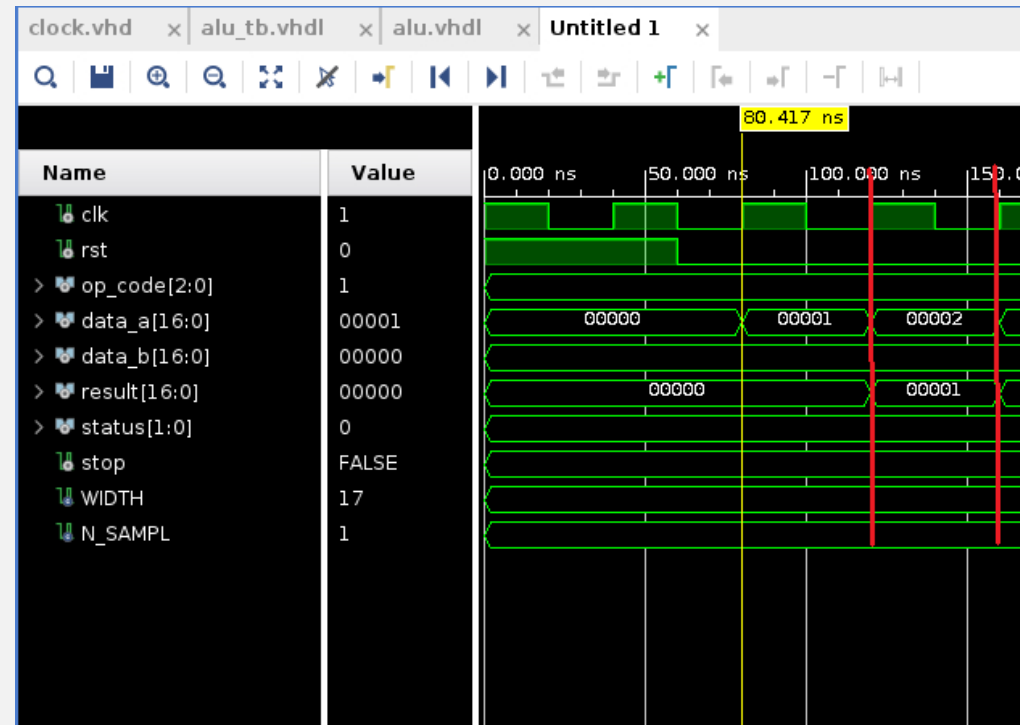
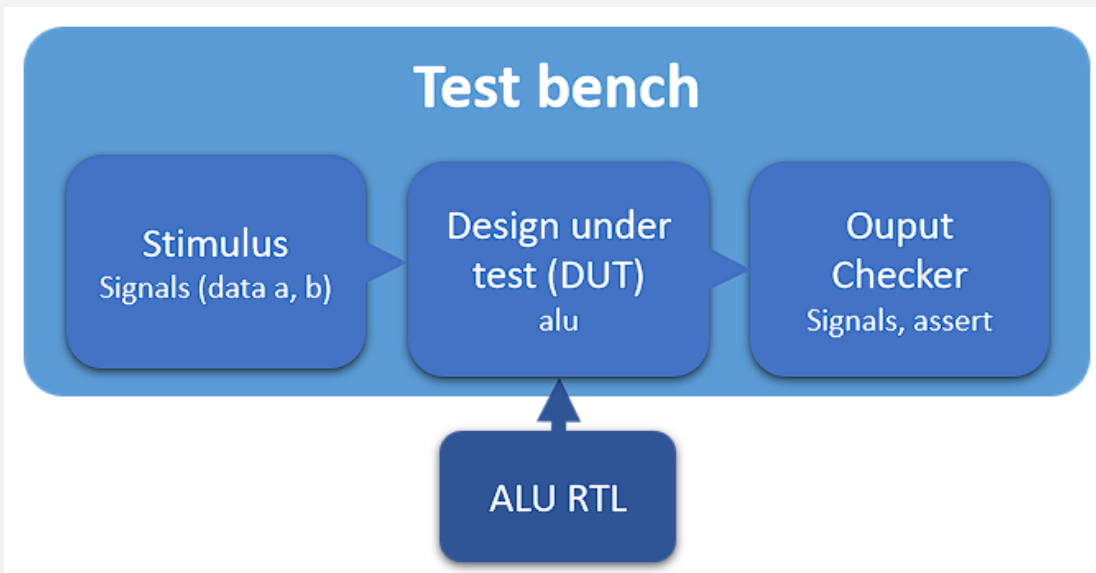
<input checked="" type="checkbox"/> Enable
Data Width: 16 [1 - 32]
Address Width: 16 [1 - 32]
Depth: 0 [0 - 67108863]

FIFOs

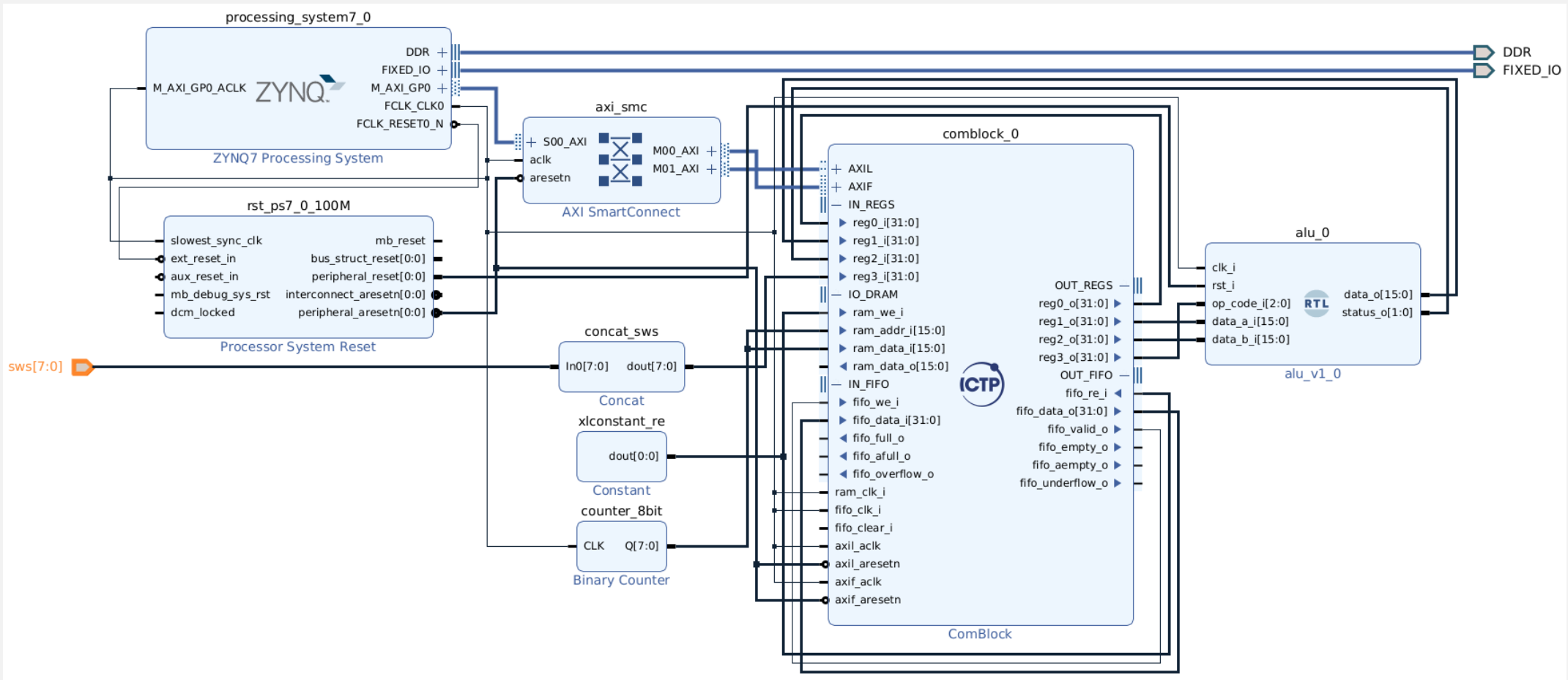
Input (FPGA to PROC)	Output (PROC to FPGA)
<input checked="" type="checkbox"/> Enable	<input checked="" type="checkbox"/> Enable
Data Width: 32 [1 - 32]	Data Width: 32 [1 - 32]
Depth: 1024	Depth: 1024
Almost Full Offset: 1	Almost Full Offset: 1
Almost Empty Offset: 1	Almost Empty Offset: 1

Buttons: OK, Cancel

Labs 2: Simulation

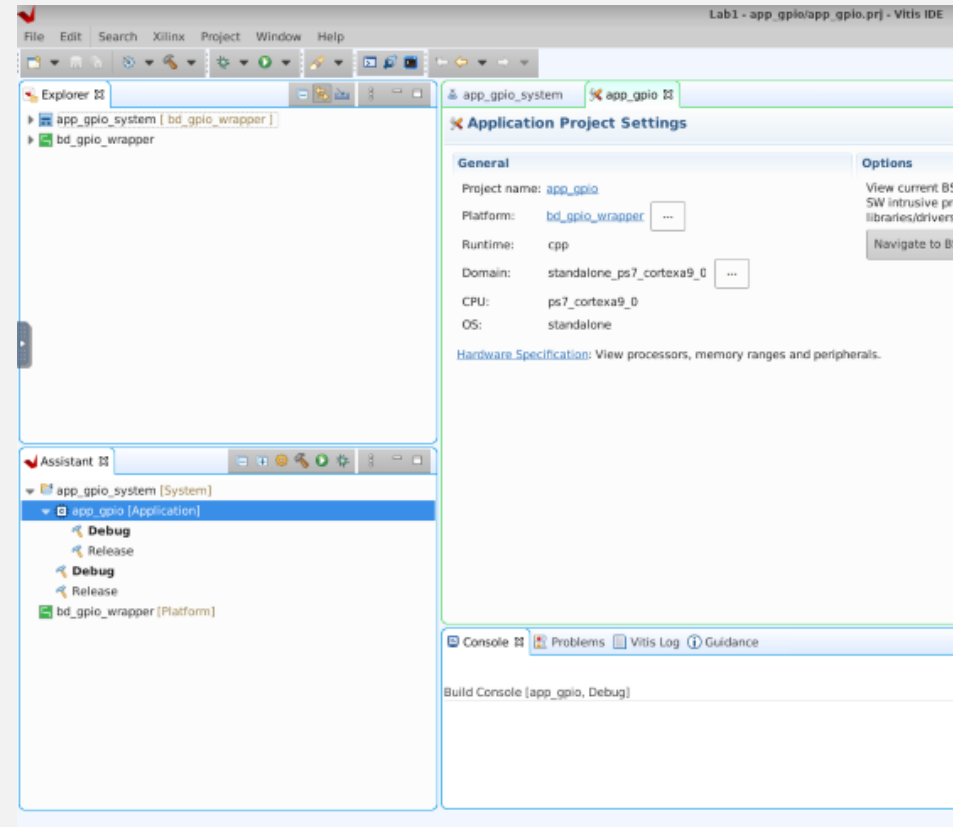


Labs 2: Final Block Design



Labs 2: Software

- C driver, use ComBlock instructions.
- Configuration and data exchange.
- Unsigned integer arithmetic operations.
- Select the operation with an SW.
- Identify and print status flag.

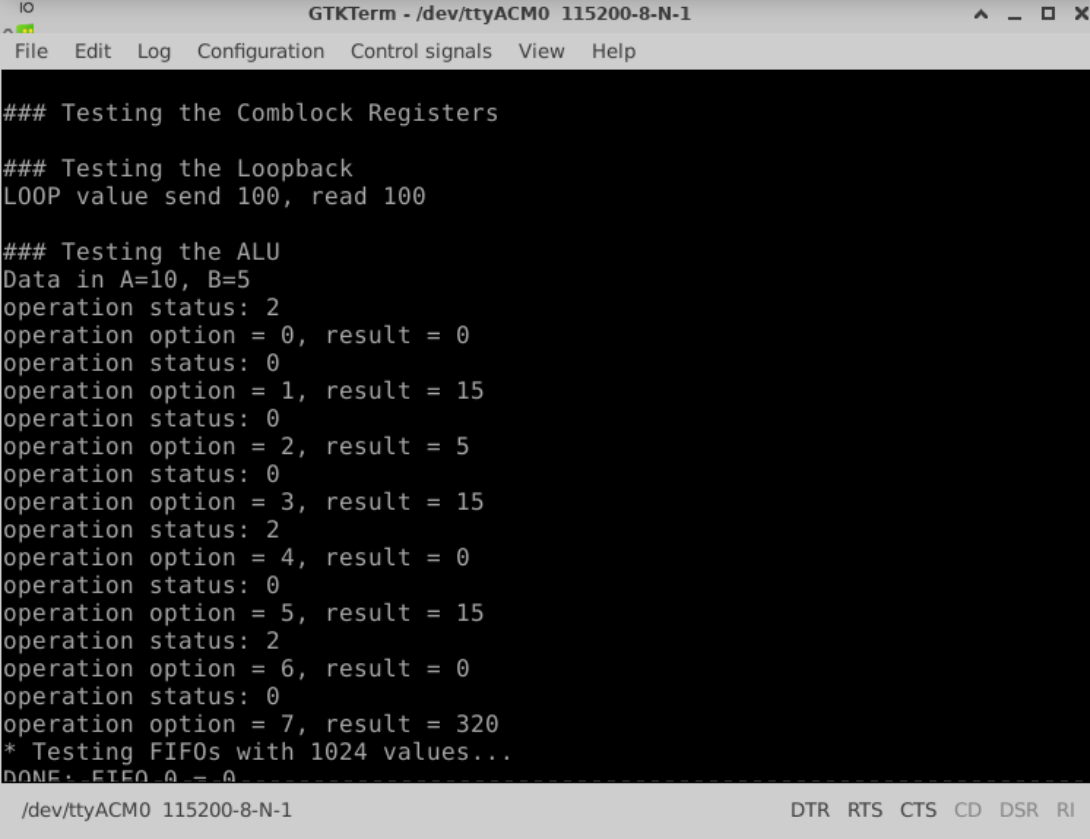


Labs 2: Results

- PL Hardware
- PS program
- Comblock Communication
- data transfer

Optional:

- Challenge



```
IO
GTKTerm - /dev/ttyACM0 115200-8-N-1
File Edit Log Configuration Control signals View Help

### Testing the Comblock Registers

### Testing the Loopback
LOOP value send 100, read 100

### Testing the ALU
Data in A=10, B=5
operation status: 2
operation option = 0, result = 0
operation status: 0
operation option = 1, result = 15
operation status: 0
operation option = 2, result = 5
operation status: 0
operation option = 3, result = 15
operation status: 2
operation option = 4, result = 0
operation status: 0
operation option = 5, result = 15
operation status: 2
operation option = 6, result = 0
operation status: 0
operation option = 7, result = 320
* Testing FIFOs with 1024 values...
DONE: FIFO @ = @

/dev/ttyACM0 115200-8-N-1 DTR RTS CTS CD DSR RI
```

User: smr3983

Password: 3983smr!CPT24

**WARNING: Do not fail the password more than 3 times.
Feel free to raise your hand. Is better ask for help.**

Links:

WhatsApp group



Google Fotos

