The Abdus Salam International Centre for Theoretical Physics

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Workshop on Fully Programmable Systems-on-Chip for Scientific Applications

Lab 2: The RVI communication block: ComBlock

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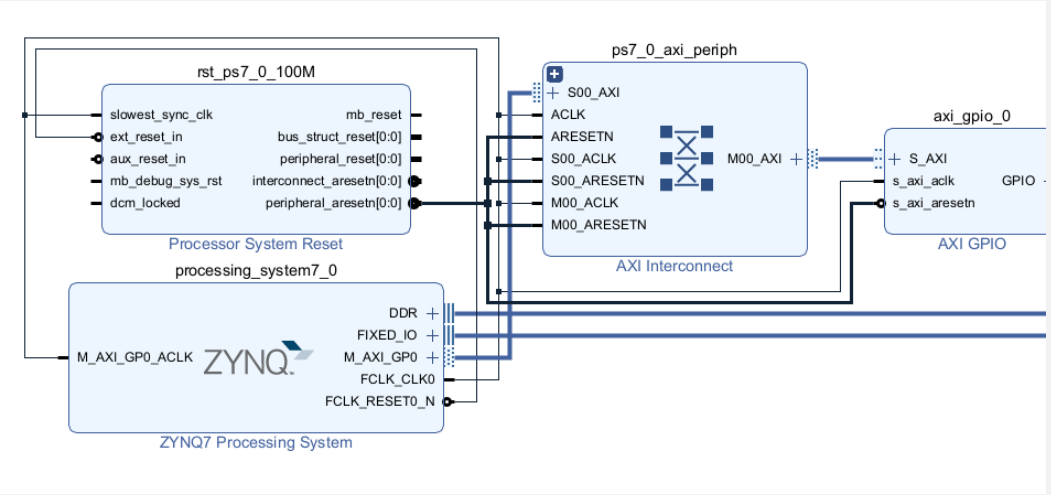
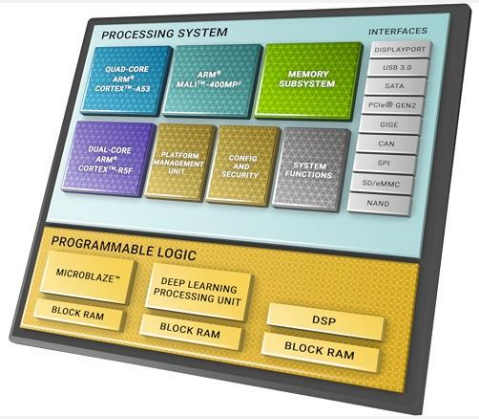
Introduction

- Vendor specific interconnects (AXI, AVALON, Chiplink).
- What we learned yesterday?
  - ✓ AXI interconnect,
  - ✓ memory address,
  - ✓ data.
- Communication Block (ComBlock).

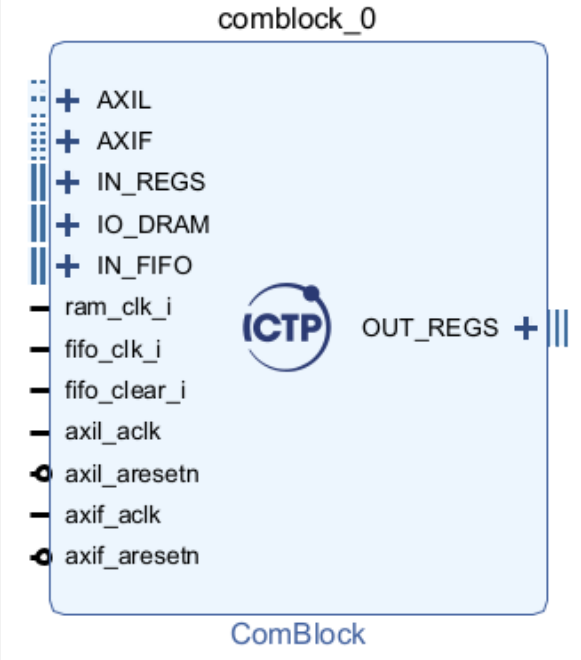




What is the ComBlock?

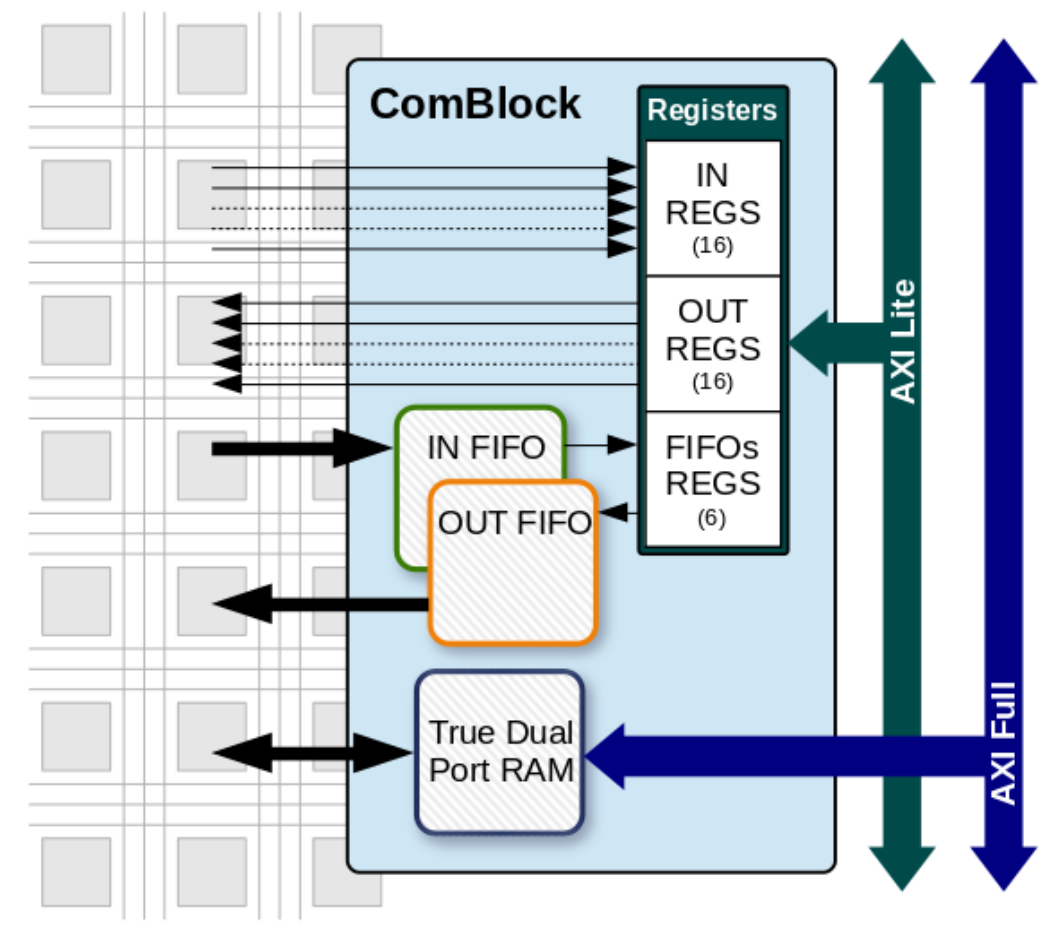
A communication block that abstracts you from the AXI protocol.

- Interconnect: AXI - Known interfaces (registers, RAM and FIFOs).
- Configurable resources, width, length, etc.
- Simple Clock-Domain-Crossing with FIFOs and TDPRAM.
- C driver for easy complete project integration.



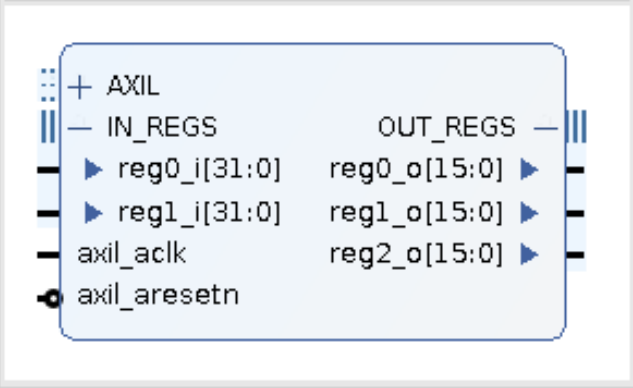
Features

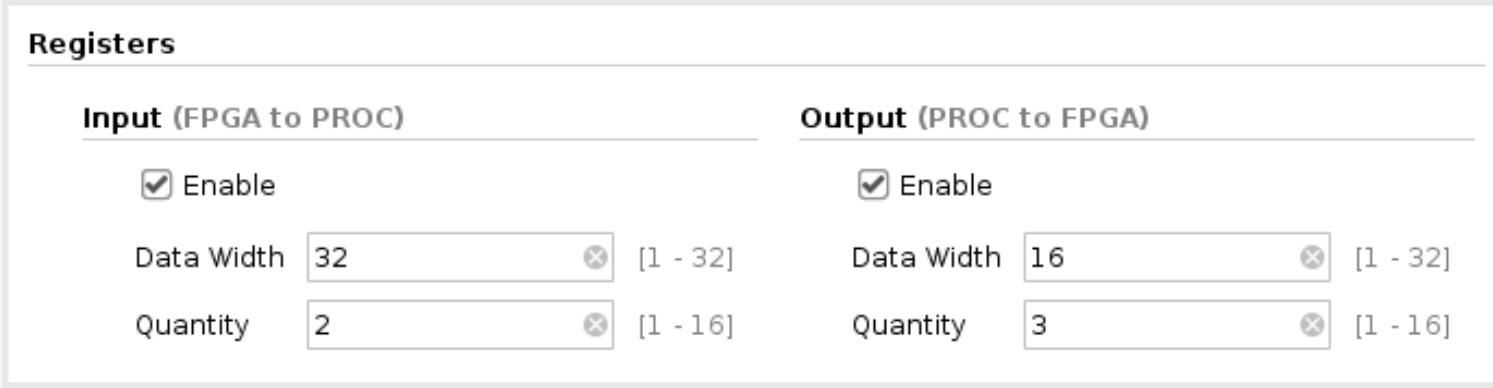
- I/O Registers, I/O FIFOS, and TDPRAM.
- AXI Lite: Registers and FIFOs.
- AXI Full: TDPRAM.



Registers

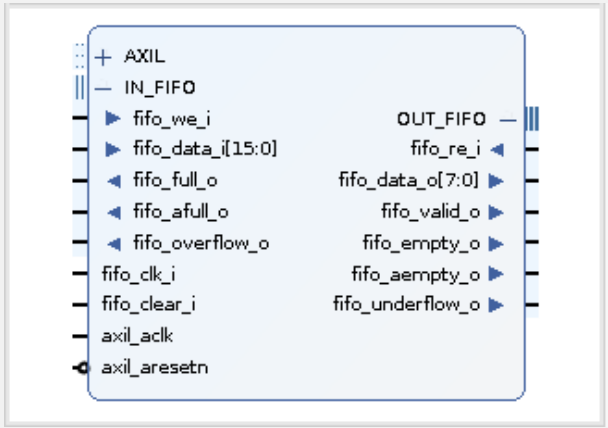
- 16 input registers (FPGA to Processor).
- 16 output registers (Processor to FPGA).
- User configurable data width, 1-32 bits.
- Input and output independently enabled.

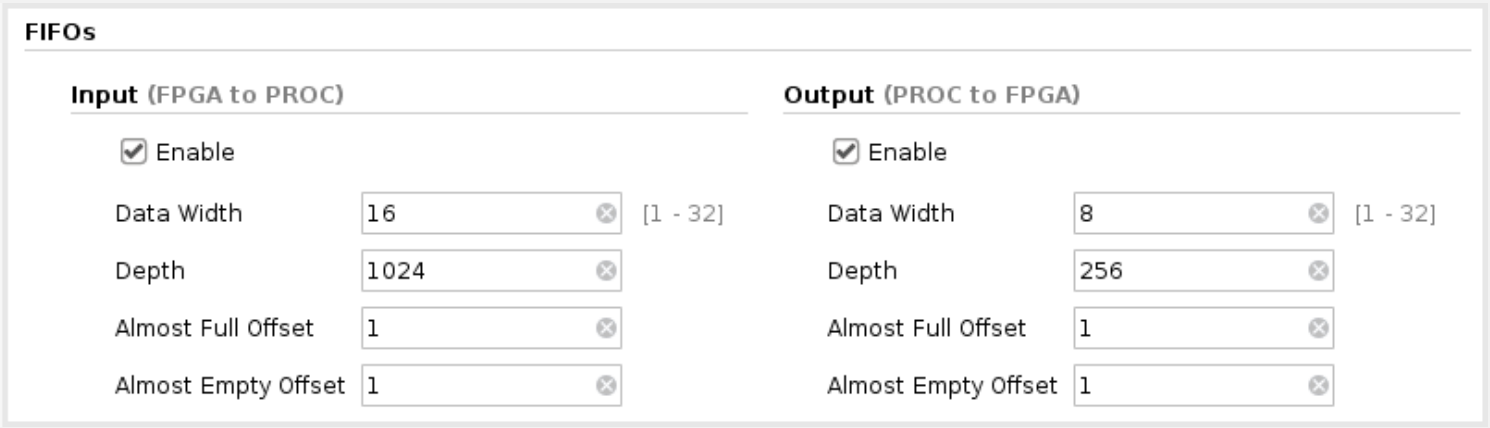




FIFOs

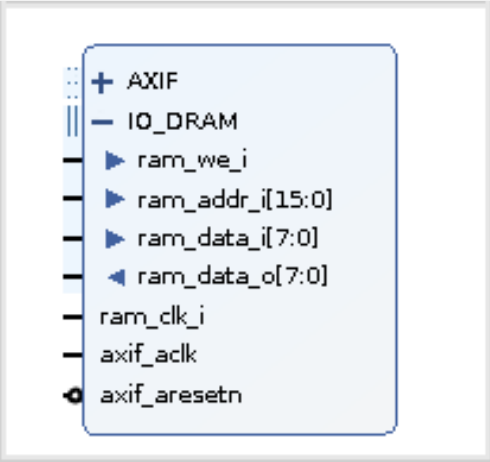
- Input and output FIFOs.
- Customizable width and depth.
- Asynchronous.
- Control registers on the Processor's side.

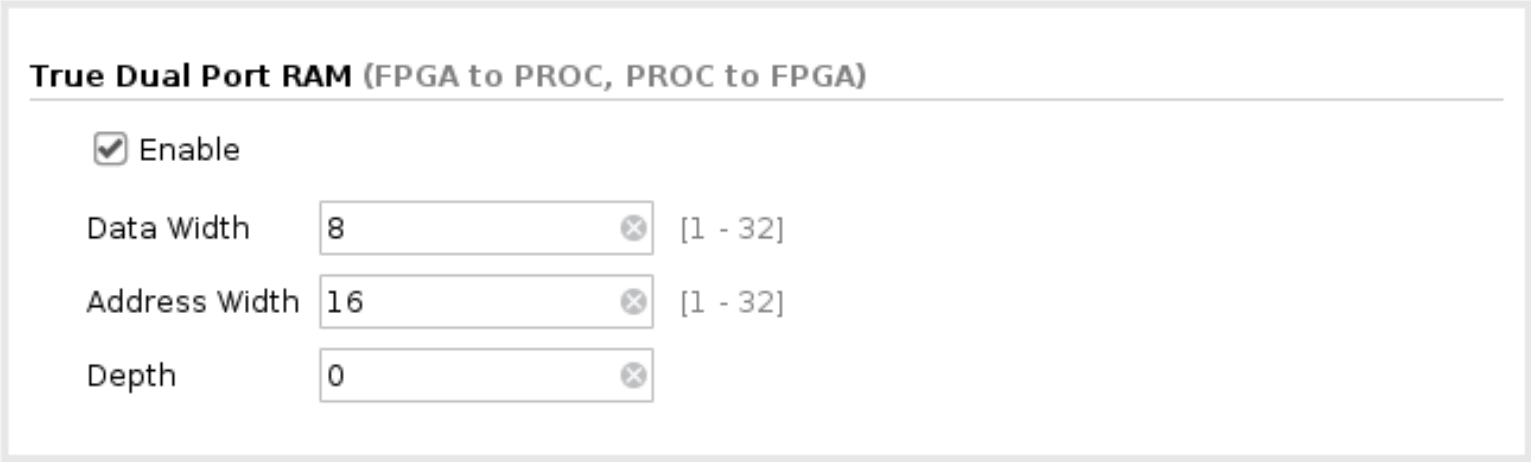




TDPRAM

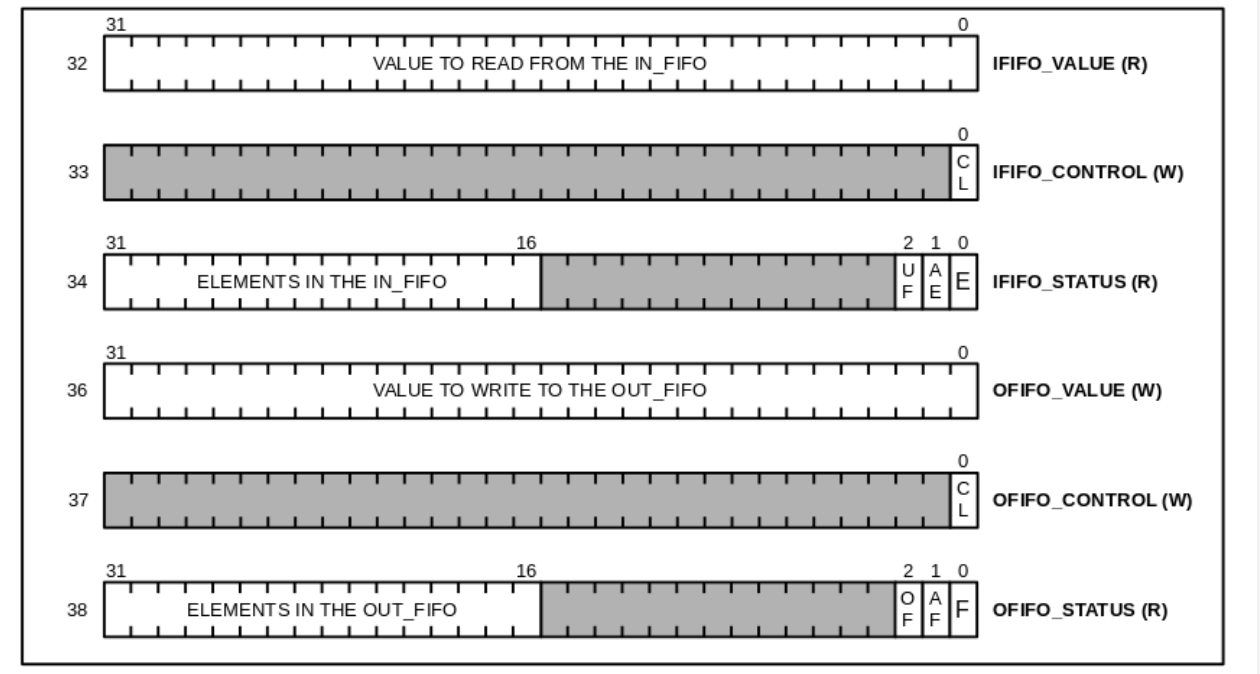
- Bidirectional.
- Clock-domain-crossing.
- Configurable depth, width and address width.





Processor Interaction

- Device information in **xparameters.h**.
- Register mappings in **comblock.h**.
- CB_IREG, CB_OREG, ...
- Control registers.



C Drives

- Read and write functions **single memory position**:

  void **cbWrite**(UINTPTR baseaddr, u32 reg, u32 value)

  u32 **cbRead**(UINTPTR baseaddr, u32 reg)

- Read and write several **contiguous memory positions**:

  void **cbWriteBulk**(UINTPTR baseaddr, int *buffer, u32 depth)

  void **cbReadBulk**(int *buffer, UINTPTR baseaddr, u32 depth)

Where and how to get it?

- Hosted on GitLab (with continuous updates):

  git clone https://gitlab.com/ictp-mlab/core-comblock.git

- Completely open source under BSD 3-clause license.

- Rodrigo Melo, collaboration between the Multidisciplinary Laboratory (MLAB) from The Abdus Salam International Centre for Theoretical Physics (ICTP, Italy). (not updated)

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Lab 2: ComBlock and RTL instantiation

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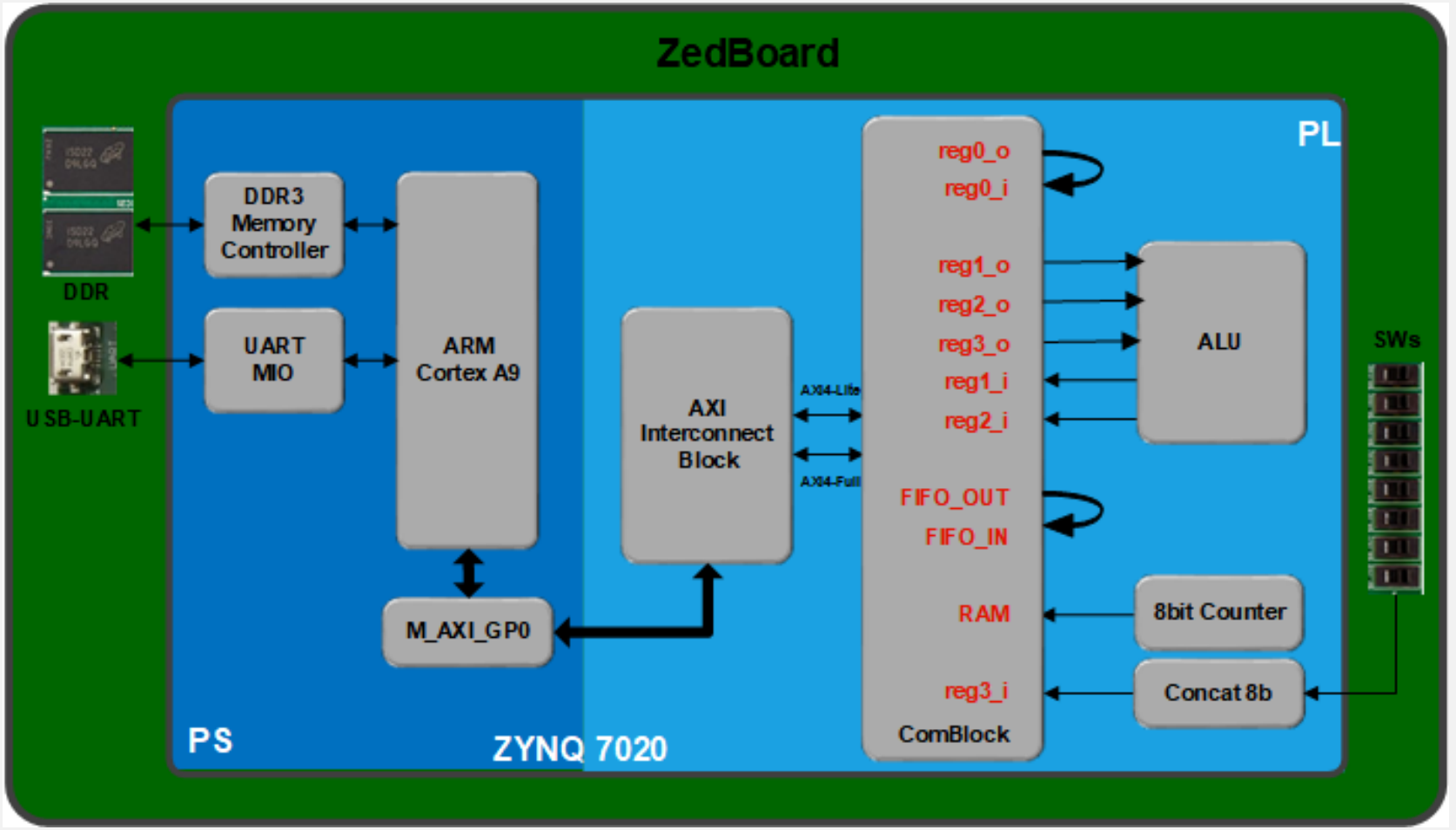
Labs 2: Objectives

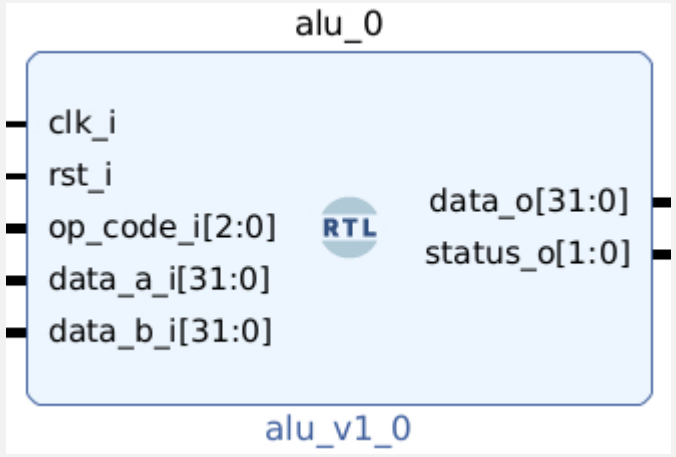
- Simulate a simple ALU and understand the VHDL code.
- Use and configuration of the **ComBlock** IP.
- Understand the data transfer between PL and PS using **ComBlock** IP.
- Instantiate RTL blocks and control them through the **ComBlock** registers.
- Perform unsigned integer arithmetic operations.

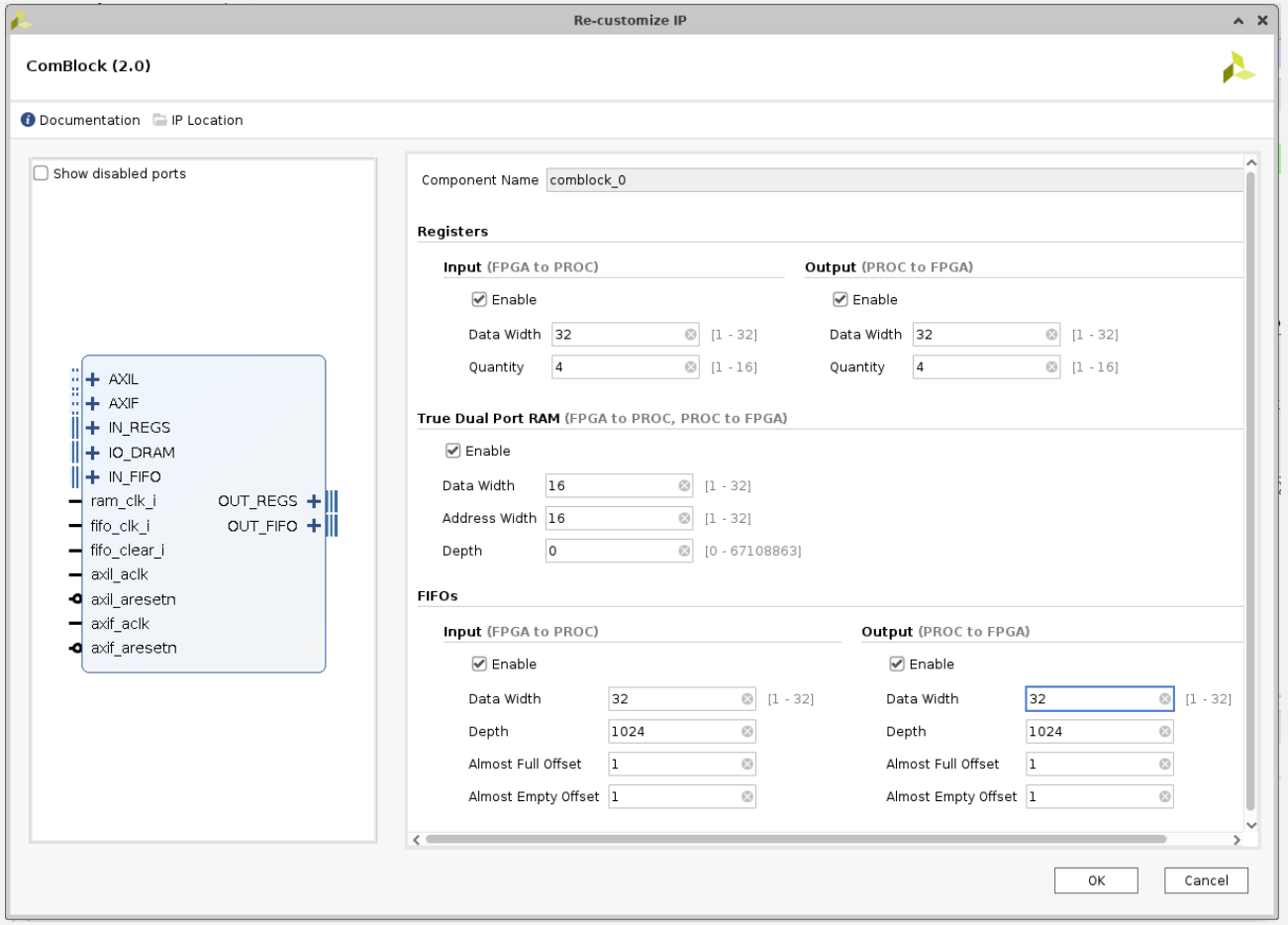
Labs 2: Design description



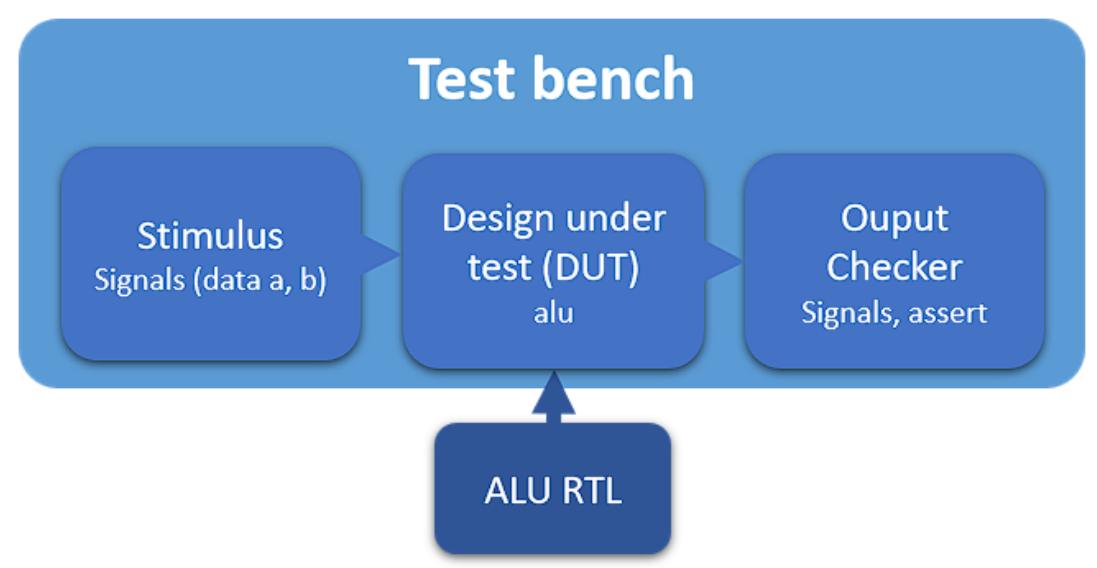
Labs 2: Hardware

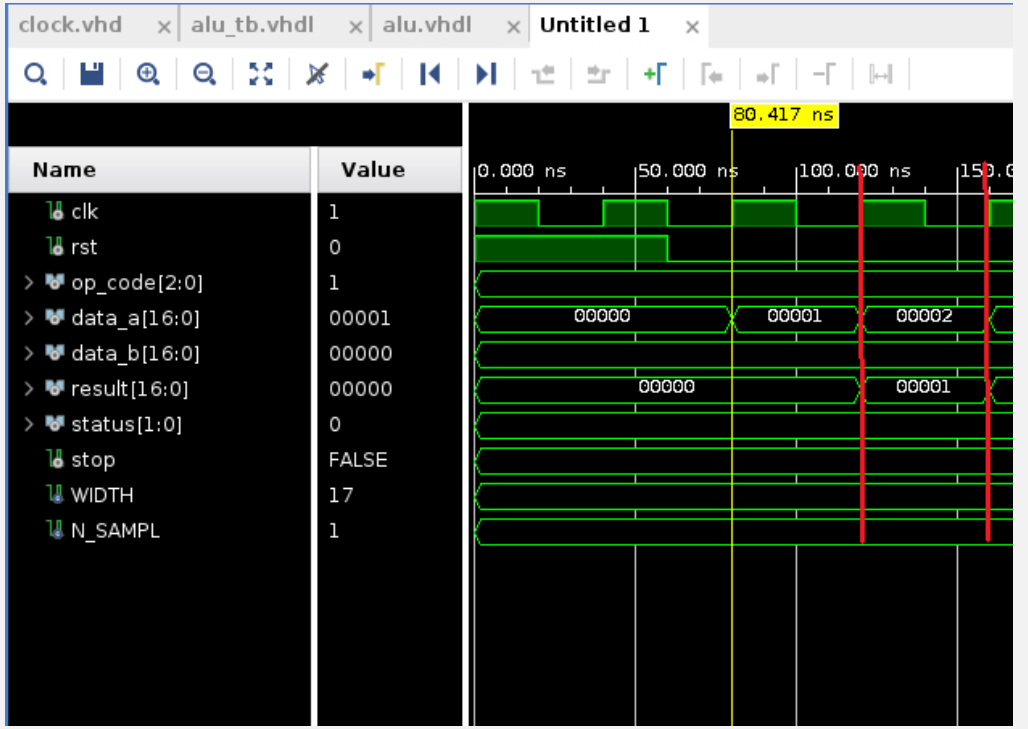
RTL block, VHDL coded.
Unsigned integer data.
Customizable data width.



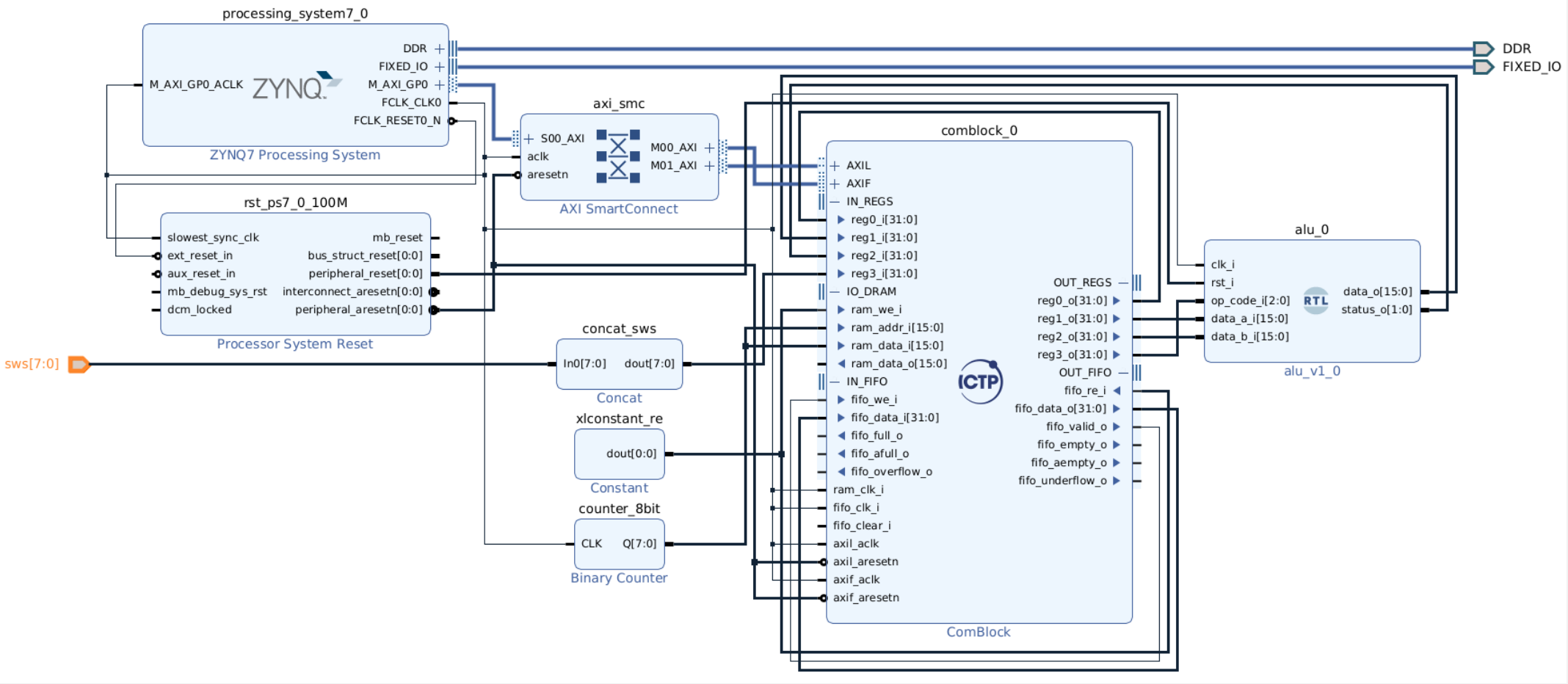


Labs 2: Simulation



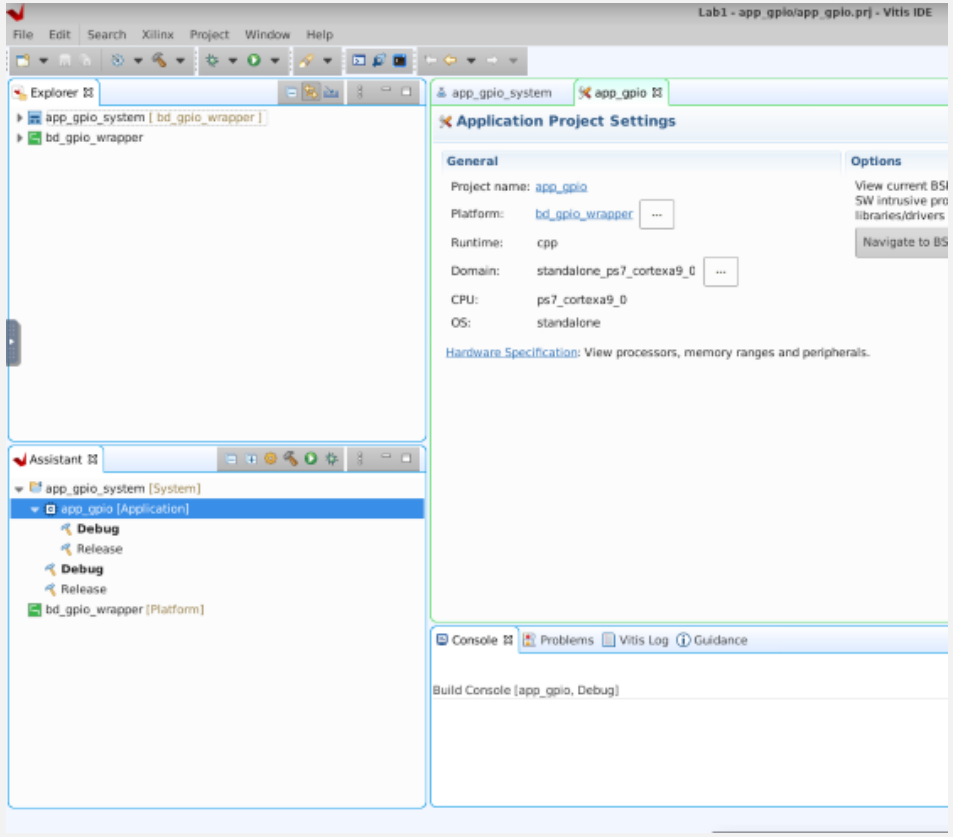


Labs 2: Final Block Design



Labs 2: Software

- C driver, use ComBlock instructions.
- Configuration and data exchange.
- Unsigned integer arithmetic operations.
- Select the operation with an SW.
- Identify and print status flag.

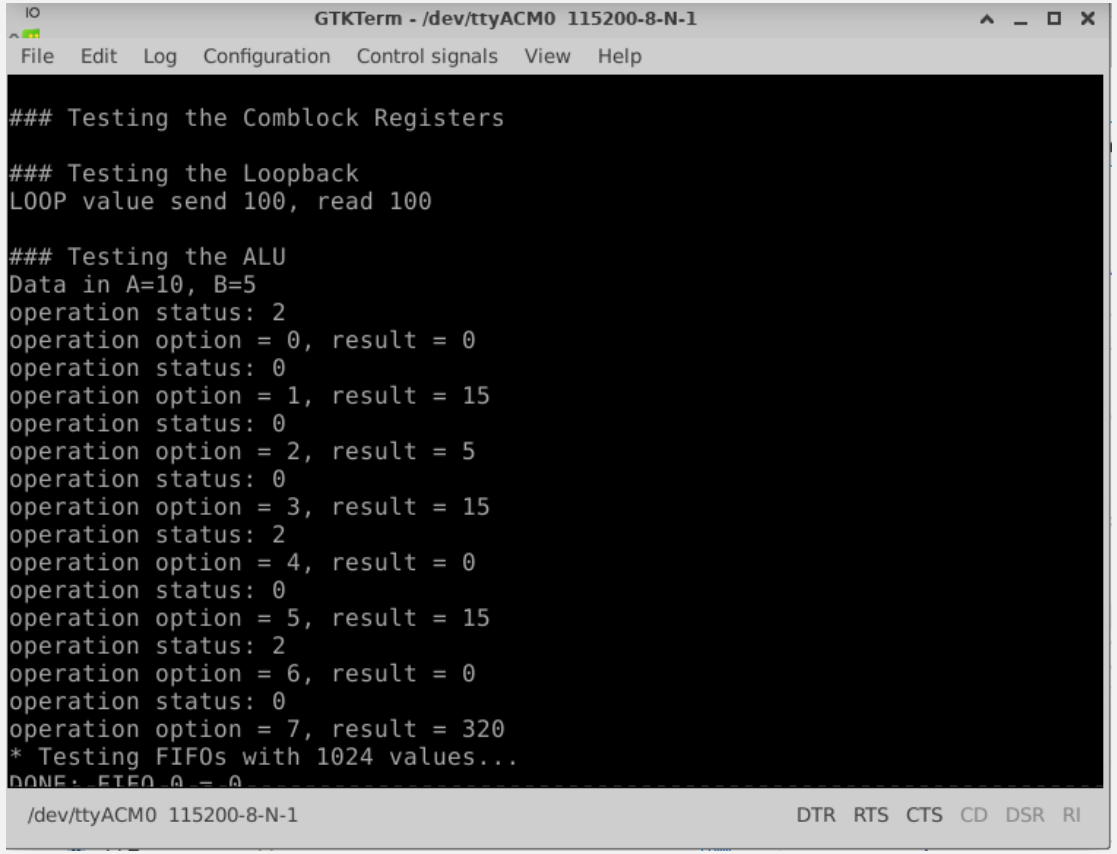


Labs 2: Results

- PL Hardware
- PS program
- Comblock Communication
- data transfer

Optional:

- Challenge



User: smr3983
Password: 3983smr!CPT24

WARNING: Do not fail the password more than 3 times.
Feel free to raise your hand. Is better ask for help.

Links:

WhatsApp group

Google Fotos