





Workshop on Fully Programmable Systems-on-Chip for Scientific Applications

Tool Command Language (TCL)









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TCL (Tool Command Language) or "*Tickle*" is a powerful, flexible scripting language initially developed in the late **1980**s by John Ousterhout. It's designed for command scripting and rapid prototyping.

- Key Characteristics:
 - Interpreted Language: TCL scripts are executed line-by-line, making it easy to test and modify in real-time.
 - Cross-Platform Compatibility: Runs on various operating systems, making it versatile across different development environments.
 - **Extensible**: TCL supports integration with other languages and tools, allowing it to adapt to various workflows.



Why TCL is relevant?

Widely Used in FPGA Tools: Major FPGA design tools, such as Xilinx Vivado, Intel Quartus, and Microsemi Libero, include TCL as their primary scripting language.

Automation and Control: TCL scripts can control FPGA design tools for tasks like synthesis, simulation, and implementation. It allows engineers to automate complex workflows that would be tedious and error-prone if done manually.

Adaptability: TCL provides a way to customize and streamline the FPGA design process, making it easier to adapt the workflow to specific project requirements and increase productivity.

TCL is both ingenious and frustrating

Tcl interpreters follow a basic set of rules, and that's what makes it a good tool command language in the first place.

Everything is a string:

```
1 % set listA [list 1 2 3]
2 1 2 3
3 % set listB "1 2 3"
4 1 2 3
5 % string match $listA $listB
6 1
7 %
```

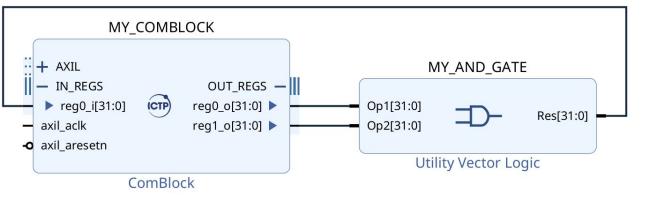
Everything can be redefined

```
% puts "Hello World!"
1
 2
    Hello World!
 3
    %
 4
    % # Let's redefine puts to do something more
5
    % rename puts puts_orig
6
7
    % proc puts {args} {puts_orig "BMAZED! $args"}
    %
8
    % puts "Hello World!"
9
    BMAZED! {Hello World!}
10
    %
```

TCL for FPGA Design

Role of TCL in FPGA Design Flow

- Automating Repetitive Tasks: SoC design involves many repetitive tasks, such as defining constraints, running synthesis, or generating reports. TCL scripts can be written to perform these tasks automatically. E.g. Synthesis, implementation, and generate a bitstream.
- **Configuration and Setup:**TCL scripts are frequently used to configure the design environment, including initializing settings and setting up design constraints, paths, and other variables. E.g. Board selection, Constraints (timing, placement, etc).
- Synthesis, Simulation, and Implementation
- **Batch Processing:** Multiple simulations, implementations, or tests need to be run on different configurations or parameters.



TCL Example



Instantiating Comblock

create_bd_cell -type ip -vlnv www.ictp.it:user:comblock:2.0 MY_COMBLOCK set_property -dict [list \ CONFIG.REGS_IN_DEPTH {1} \ CONFIG.REGS_OUT_DEPTH {2} \ CONFIG.DRAM_IO_ENA {false} \ CONFIG.FIFO_IN_ENA {false} \ [get_bd_cells MY_COMBLOCK] ### Instantiating Flopoco division module create_bd_cell -type ip -vlnv xilinx.com:ip:util_vector_logic:2.0 MY_AND_GATE set property CONFIG.C SIZE {32} [get bd cells MY_AND_GATE]

Block Diagarm Interconnection

Comblock to Logic Vector

connect_bd_net [get_bd_pins MY_COMBLOCK/reg0_o] [get_bd_pins MY_AND_GATE/Op1] connect_bd_net [get_bd_pins MY_COMBLOCK/reg1_o] [get_bd_pins MY_AND_GATE/Op2] # Logic Vector to Comblock

connect_bd_net [get_bd_pins MY_AND_GATE/Res] [get_bd_pins MY_COMBLOCK/reg0_i]

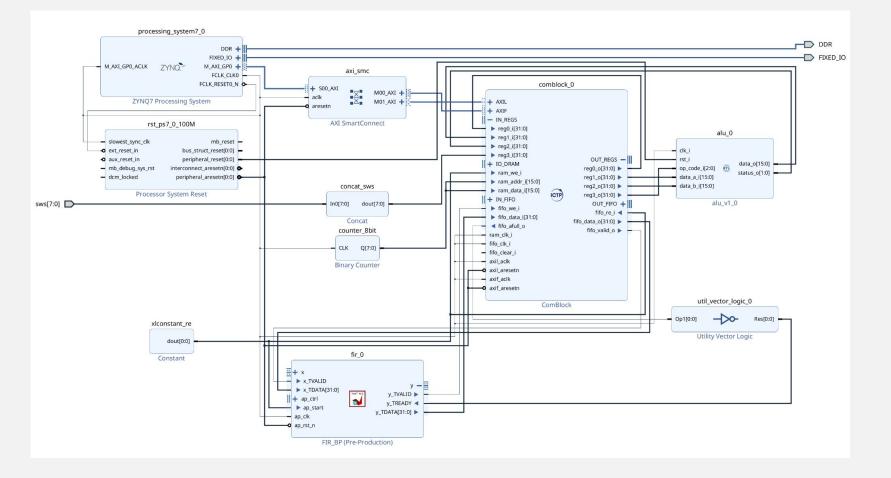
The Frustrating Part It can get very complicated very quickly.

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You haven't answered the question.... Why TCL?

Great for automation flow

source ./my_project.tcl

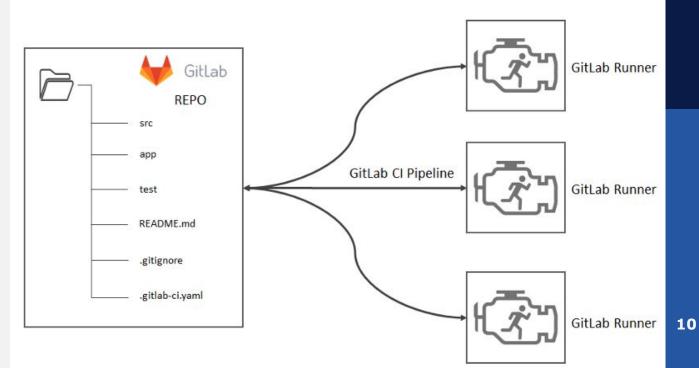


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We will continue in the lab.











International Centre for Theoretical Physics

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